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Data handbook

Electronic
components
and materials

Integrated circuits

Book IC11N 1985
New series

Linear LSI

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Signetics

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LINEAR LSI

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DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of four series of handbooks:

ELECTRON TUBES	BLUE
SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
COMPONENTS AND MATERIALS	GREEN

The contents of each series are listed on pages iv to viii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application information is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Electronic Components and Materials Division is given in our Preferred Type Range catalogue (issued annually).

Information on current Data Handbooks and on how to obtain a subscription for future issues is available from any of the Organizations listed on the back cover.
Product specialists are at your service and enquiries will be answered promptly.

ELECTRON TUBES (BLUE SERIES)

The blue series of data handbooks comprises:

T1	**Tubes for r.f. heating**	
T2a	**Transmitting tubes for communications, glass types**	
T2b	**Transmitting tubes for communications, ceramic types**	
T3	**Klystrons, travelling-wave tubes, microwave diodes**	
ET3	**Special Quality tubes, miscellaneous devices** (will not be reprinted)	
T4	**Magnetrons for microwave heating**	
T5	**Cathode-ray tubes** Instrument tubes, monitor and display tubes, C.R. tubes for special applications	
T6	**Geiger-Müller tubes**	
T7	**Gas-filled tubes** Segment indicator tubes, indicator tubes, dry reed contact units, thyratrons, industrial rectifying tubes, ignitrons, high-voltage rectifying tubes, associated accessories	
T8	**Picture tubes and components** Colour TV picture tubes, black and white TV picture tubes, colour monitor tubes for data graphic display, monochrome monitor tubes for data graphic display, components for colour television, components for black and white television and monochrome data graphic display	
T9	**Photo and electron multipliers** Photomultiplier tubes, phototubes, single channel electron multipliers, channel electron multiplier plates	
T10	**Camera tubes and accessories**	
T11	**Microwave semiconductors and components**	
T12	**Vidicons and Newvicons**	Data collations on these subjects are available now. Data Handbooks will be published in 1985.
T13	**Image intensifiers**	
T14	**Infrared detectors**	
T15	**Dry reed switches**	
T16	**Monochrome tubes and deflection units** Black and white TV picture tubes, monochrome data graphic display tubes, deflection units	

SEMICONDUCTORS (RED SERIES)

The red series of data handbooks comprises:

S1	**Diodes** Small-signal germanium diodes, small-signal silicon diodes, voltage regulator diodes (< 1,5 W), voltage reference diodes, tuner diodes, rectifier diodes
S2a	**Power diodes**
S2b	**Thyristors and triacs**
S3	**Small-signal transistors**
S4a	**Low-frequency power transistors and hybrid modules**
S4b	**High-voltage and switching power transistors**
S5	**Field-effect transistors**
S6	**R.F. power transistors and modules**
S7	**Surface mounted semiconductors**
S8	**Devices for optoelectronics** Photosensitive diodes and transistors, light-emitting diodes, displays, photocouplers, infrared sensitive devices, photoconductive devices.
S9	**Power MOS transistors**
S10	**Wideband transistors and wideband hybrid IC modules**
S11	**Microwave semiconductors** (to be published in this series in 1985) All present available in Handbook T11
S12	**Surface acoustic wave devices**

INTEGRATED CIRCUITS (PURPLE SERIES)

The purple series of data handbooks comprises:

EXISTING SERIES

IC1	**Bipolar ICs for radio and audio equipment**
IC2	**Bipolar ICs for video equipment**
IC3	**ICs for digital systems in radio, audio and video equipment**
IC4	**Digital integrated circuits** CMOS HE4000B family
IC5	**Digital integrated circuits — ECL** (superseded by IC08N) ECL10 000 (GX family), ECL100 000 (HX family), dedicated designs
IC6	**Professional analogue integrated circuits**
IC7	**Signetics bipolar memories**
IC8	**Signetics analogue circuits**
IC9	**Signetics TTL logic** (superseded by IC09N and IC15N)
IC10	**Signetics Integrated Fuse Logic (IFL)**
IC11	**Microprocessors, microcomputers and peripheral circuitry**

NEW SERIES

IC01N	**Radio, audio and associated systems** Bipolar, MOS	
IC02N	**Video and associated systems** Bipolar, MOS	
IC03N	**Integrated circuits for telephony** Bipolar, MOS	(published 1985)
IC04N	**HE4000B logic family** CMOS	
IC05N	**HE4000B logic family uncased integrated circuits** CMOS	(published 1984)
IC06N	**PC54/74HC/HCU/HCT logic families** HCMOS	
IC07N	**PC54/74HC/HCU/HCT uncased integrated circuits** HCMOS	
IC08N	**10K and 100K logic family** ECL	(published 1984)
IC09N	**Logic series** TTL	(published 1984)
IC10N	**Memories** MOS, TTL, ECL	
IC11N	**Linear LSI**	(published 1985)
IC12N	**Semi-custom gate arrays & cell libraries** ISL, ECL, CMOS	
IC13N	**Semi-custom integrated fuse logic** IFL series 20/24/28	
IC14N	**Microprocessors, microcontrollers & peripherals** Bipolar, MOS	
IC15N	**Logic series** FAST TTL	(published 1984)

Note

Books available in the new series are shown with their date of publication.

COMPONENTS AND MATERIALS (GREEN SERIES)

The green series of data handbooks comprises:

C1	**Programmable controller modules** PLC modules, PC20 modules
C2	**Television tuners, video modulators, surface acoustic wave filters**
C3	**Loudspeakers**
C4	**Ferroxcube potcores, square cores and cross cores**
C5	**Ferroxcube for power, audio/video and accelerators**
C6	**Synchronous motors and gearboxes**
C7	**Variable capacitors**
C8	**Variable mains transformers**
C9	**Piezoelectric quartz devices** Quartz crystal units, temperature compensated crystal oscillators, compact integrated oscillators, quartz crystal cuts for temperature measurements
C10	**Connectors**
C11	**Non-linear resistors** Voltage dependent resistors (VDR), light dependent resistors (LDR), negative temperature coefficient thermistors (NTC), positive temperature coefficient thermistors (PTC)
C12	**Variable resistors and test switches**
C13	**Fixed resistors**
C14	**Electrolytic and solid capacitors**
C15	**Ceramic capacitors***
C16	**Permanent magnet materials**
C17	**Stepping motors and associated electronics**
C18	**D.C. motors**
C19	**Piezoelectric ceramics**
C20	**Wire-wound components for TVs and monitors**
C21	**Assemblies for industrial use** HNIL FZ/30 series, NORbits 60-, 61-, 90-series, input devices

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* Film capacitors are included in Data Handbook C22 which will be published in 1985. The September 1982 edition of C15 should be retained until C22 is issued.

PREFACE

The Linear LSI Division, one of eight Signetics divisions, is a major supplier of a broad line of linear integrated circuits ranging from high-performance designs to many of the more popular industry standard devices and custom designs.

Employing Signetics' high quality processing and screening standards, the Linear LSI Division is dedicated to providing high quality Linear products to our worldwide customers. Our full product line addresses the needs of the EDP, Automotive, Military, Industrial, Consumer, and Communications markets.

The 1985 Linear LSI Data and Applications Manual provides complete technical data on our full line of interface, communications, amplifier, power conversion and control.

An applications section, selector guides, and cross reference guides are also included in this volume.

Although every attempt has been made to insure accuracy of information in this manual, Signetics assumes no liability for inadvertent errors.

Your suggestions for improvement in future editions are welcome.

Signetics Linear LSI Marketing

PRODUCT STATUS DEFINITIONS

DEFINITION OF TERMS

Data Sheet Identification	Product Status	Definition
Preview	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Advance Information	Sampling or Pre-Production	This data sheet contains advance information and specifications are subject to change without notice.
Preliminary	First Production	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification Noted	Full Production	This data sheet contains final specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

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Selection Guide

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CROSS REFERENCE BY PART NUMBER

PART NUMBER	COMPANY	SIGNETICS
DAC 08	PMI	DAC08E, N
DAC 0800LCN	NSC	MC1408-8N
AMDAC 08	AMD	DAC08C, E
LMDAC 08	NSC	DAC08
LM 1011/1111	NSC	NE645/646
LF 111	NSC	LM111
LM 111	AMD, MOTO, NSC, TI	LM111
µA 111	FSC	LM111
LM 119	AMD, NSC	LM119
LM 124	MOTO, NSC, TI	LM124
µA 124	FSC	LM124
LM 13600	NSC	LM13600
LM 13600A	NSC	LM13600A
LM 139	AMD, NSC, TI	LM139
µA 139	FSC	LM139
DAC 1408	PMI	MC1408
LM 1408	NSC	MC1408
SSS 1408A	AMD	MC1408-7
DAC 1408-7	PMI	MC1408-7
MC 1408-7	MOTO	MC1408-7
MC 1408-8	MOTO	MC1408-8
MC 1413	MOTO	ULN2003
MC 1416	MOTO	ULN2004
MC 1455	MOTO	NE555
AM 1458	AMD	MC1458
LM 1458	NSC	MC1458
MC 1458	MOTO, TI	MC1458
µA 1458	FSC	MC1458
µPC 1458	NEC	MC1458
DS 1488	NSC	MC1488
MC 1488	MOTO, TI	MC1488
µA 1488	FSC	MC1488
DS 1489/A	NSC	MC1489/A
MC 1489/A	MOTO	MC1489/A
µA 1489/A	FSC	MC1489/A
LM 1496	NSC	MC1496
MC 1496	MOTO	MC1496
SSS 1508A	AMD	MC1508
AM 1508-8	AMD	MC1508-8
LM 1508-8	NSC	MC1508-8
MC 1508-8	MOTO	MC1508-8
LM 1558	NSC	MC1558
MC 1558	MOTO, TI	MC1558
PM 1558	PMI	MC1558
µA 1558	FSC	MC1558
LM 158	MOTO, NSC, TI	LM158
LM 1596	NSC	MC1596
LM 161	NSC	SE529
MC 1596	MOTO	MC1596
MC 1723/C	MOTO	µA723/C
MC 1733	MOTO	µA733
MC 1747/C	MOTO	µA747/C
LM 1870	NSC	LM1870
LM 193	NSC, TI	LM193
µA 193	FSC	LM139

PART NUMBER	COMPANY	SIGNETICS
ULN 2003A	SPRAGUE, TI	ULN2003
ULN 2004A	SPRAGUE, TI	ULN2004
LM 211	AMD, MOTO, NSC, TI	LM211
µA 211	FSC	LM211
LM 219	AMD, NSC	LM219
LM 224	MOTO, NSC, TI	LM224
LM 239	TI	LM239
LM 239/A	MOTO, NSC	LM239/A
PM 239/A	PMI	LM239/A
LM 258	MOTO, NSC, TI	LM258
LM 2901	MOTO, NSC, TI	LM2901
µA 2901	FSC	LM2901
LM 2903	NSC, TI	LM2903
µA 2903	FSC	LM 2903
LM 2904	NSC	SA532
LM 293	NSC, TI	LM293
LM 3089	NSC	CA3089
TCA 3089	SPRAGUE	CA3089
LM 311	AMD, INTERSIL, MOTO, NSC, TI	LM311
TL 311	TI	LM311
µA 311	FSC	LM311
µPC 311	NEC	LM311
LM 319	AMD, NSC	LM319
LM 324	INTERSIL, MOTO, NSC, TI	LM324
µA 324	FSC	LM324
µP C324	NEC	LM324
MC 3302	MOTO	MC3302
MC 3303	MOTO, TI	MC3303
µA 3303	FSC	MC3303
ULN 3304	SPRAGUE	NE555
LM 339/A	MOTO, NSC, TI	LM339/A
µA 339/A	FSC	LM339/A
µP C339	NEC	LM339
MC 3403	MOTO	MC3403
MC 3410/C	MOTO	MC3410/C
MC 3456	MOTO	NE556
MC 3503	MOTO	MC3503
MC 3510	MOTO	MC3510
LM 3524	NSC	SG3524
SG 3524	TI	SG3524
LM 358	MOTO, NSC, TI	LM358
µPC 358	NEC	LM358
LM 361	NSC	NE529
LM 387	NSC	NE542
LM 393/A	NSC, TI	LM393/A
µPC 393	NEC	LM393
LF 398	AMD, NSC	LF398
µA 398	FSC	LF398
µPC 398	NEC	LF398
µPC 4558	NEC	NE4558
RC 4558	TI	NE4558
TL 494	MOTO, TI	NE5561
µA 494	FSC	NE5561
SN 5520	TI	NE5520
NE 5532/A	TI	NE5532/A

CROSS REFERENCE BY PART NUMBER Continued

PART NUMBER	COMPANY	SIGNETICS
SE/NE 5534/A	TI	SE/NE5534/A
NE 555	INTERSIL, MOTO, TI	NE555
LM 555/C	NSC	NE555
μA 555	FSC	NE555
LM 556	NSC	NE556
NE 556	INTERSIL, MOTO, TI	NE556
μA 556	FSC	NE556
μPC 558	NEC	NE558
LM 565	MOTO, NSC	NE565
LM 566	NSC	NE566
μPC 566	NEC	NE566
LM 567	NSC	NE567
NE 592	MOTO	NE592
TL 594	TI	NE594
AM 6012	AMD	AM6012
μPC 6012	NEC	AM6012
UDN 6116-2	SPRAGUE	SA594
UDN 6128	SPRAGUE	NE594
LM 723/C	MOTO, NSC	μA723/C
μA 723	INTERSIL, FSC, TI	μA723

PART NUMBER	COMPANY	SIGNETICS
LM 733	NSC	μA733
μA 733/C	INTERSIL, FSC, TI	μA733/C
ICL 741	INTERSIL	μA741C
LM 741	MOTO, NSC	μA741
PM 741/C	PMI	μA741/C
μPC 741	NEC	μA741
μA 741	FSC, TI	μA741
SSS 741	AMD	μA741
LM 747	NSC	μA747
PM 747/C	PMI	μA747C
SSS 747	AMD	μA747
μA 747	FSC, MOTO, TI	μA747
LM 748	NSC	μA748
μA 748	FSC, TI	μA748
μA 758	MOTO, NSC	μA758
ULN 8160	SPRAGUE	NE5560
ULN 8161	SPRAGUE	NE5561
SN 7588	TI	MC1488
SN 7589/A	TI	MC1489/A
SN 76689	TI	CA3089

CROSS REFERENCE BY COMPANY

AMD	SIGNETICS
AM 1508	MC 1508
AM 6012	AM 6012
AMDAC 08	DAC-08C,E
LF 398	NE 5537
LM 111	LM 111
LM 119	LM 119
LM 139	LM 139
LM 211	LM 211
LM 311	LM 311
LM 319	LM 319
SSS 1408A	MC 1408
SSS 1508A	MC 1508
SSS 741	μA 741
SSS 747	μA 747

FAIRCHILD	SIGNETICS
μA 111	LM 111
μA 124	LM 124
μA 139	LM 139
μA 1458	MC 1458
μA 1488	MC 1488
μA 1558	MC 1558
μA 193	LM 193
μA 2901	LM 2901
μA 2903	LM 2903
μA 301A	LM 301A
μA 311	LM 311
μA 324	LM 324
μA 3303	MC 3303
μA 339	LM 339
μA 398	LF 398
μA 494	NE 5561
μA 555	NE 555
μA 556	NE 556
μA 723	μA 723
μA 733	μA 733
μA 741	μA 741
μA 747	μA 747
μA 748	μA 748
μA 758	μA 758
μA F111	LM 111
μA F211	LM 211
μA F311	LM 311

INTERSIL	SIGNETICS
ICL 741	μA 741C
LM 311	LM 311
LM 324	LM 324
NE 555	NE 555
NE 556	NE 556

MOTOROLA	SIGNETICS
LM 111	LM 111
LM 124	LM 124
LM 139	LM 139
LM 158	LM 158
LM 211	LM 211
LM 224	LM 224
LM 239	LM 239
LM 258	LM 258
LM 2901	LM 2901
LM 311	LM 311
LM 324	LM 324
LM 339	LM 339
LM 358	LM 358
LM 565	NE 565
LM 723C	μA 723C
LM 741C	μA 741C
MC 1408	MC 1408
MC 1413	ULN 2003
MC 1416	ULN 2004
MC 1455	NE 555
MC 1458	MC 1458
MC 1488	MC 1488
MC 1489	MC 1489
MC 1489A	MC 1489A
MC 1508	MC 1508
MC 1558	MC 1558
MC 1596	MC 1596
MC 1723	μA 723
MC 1723C	μA 723C
MC 1733	μA 733
MC 1747	μA 747
MC 1747C	μA 747C
MC 3302	MC 3302
MC 3303	MC 3303
MC 3403	MC 3403
MC 3410	MC 3410
MC 3456	NE 556
MC 3503	MC 3503
MC 3510	MC 3510
NE 555	NE 555
NE 556	NE 556
NE 565	NE 565
NE 592	NE 592
SE 592	SE 592
TL 494	NE 5561
μA 723	μA 723
μA 741	μA 741
μA 747	μA 747C
μA 758	μA 758/A

NATIONAL	SIGNETICS
DAC 0800-LCN	DAC 08EN
DAC 0807	MC 1408-7
DAC 0808	MC 1408-8
DAC 0808CN	MC 1408-8N
DAC 0808LD	MC 1508
DS 1488	MC 1488
DS 1489	MC 1489
LF 111	LM 111
LF 211	LM 211
LF 311	LM 311
LF 398	LF 398/NE 5537
LM 1011/1111	NE 645/646
LM 111	LM 111
LM 119	LM 119
LM 124	LM 124
LM 13600	LM 13600
LM 13700	NE 5517
LM 139	LM 139
LM 1408	MC 1408
LM 1458	MC 1458
LM 1496	MC 1496
LM 1508	MC 1508
LM 1558	MC 1558
LM 158	LM 158
LM 1596	MC 1596
LM 161	SE 529
LM 1870	LM 1870
LM 193	LM 193
LM 211	LM 211
LM 219	LM 219
LM 224	LM 224
LM 239	LM 239
LM 258	LM 258
LM 2901	LM 2901
LM 2903	LM 2903
LM 2904	SA 532
LM 293	LM 293
LM 3089	CA 3089
LM 311	LM 311
LM 319	LM 319
LM 324	LM 324
LM 339	LM 339
LM 3524	SG 3524
LM 358	NE 532
LM 361	NE 529
LM 387	NE 542
LM 393	LM 393
MC 555	NE 555
LM 555C	NE 555
LM 556	NE 556
LM 565	NE 565
LM 566	NE 566
LM 567	NE 567
LM 723	μA 723
LM 733	μA 733
LM 741	μA 741
LM 747	μA 747
LM 748	μA 748
LMDAC 08	DAC 08
μA 758	μA 758/A

NEC	SIGNETICS
μPC 1458	MC 1458
μPC 1555	NE 555
μPC 311	LM 311
μPC 324	LM 324
μPC 339	LM 339
μPC 358	LM 358
μPC 393	LM 393
μPC 398	LF 398/NE 5537
μPC 4558	NE 4558
μPC 558	NE 558
μPC 566	NE 566
μPC 6012	AM 6012
μPC 624	DAC 08C,E
μPC 741	μA 741C

PMI	SIGNETICS
CMP 04FP	LM 339
DAC 08	DAC 08C,E
DAC 1408A	MC 1408
DAC 312	AM 6012
OP 220	LM 358
PM 1558	MC 1558
PM 239/A	LM 239/A
PM 741C	μA 741C
PM 747C	μA 747C

SPRAGUE	SIGNETICS
TCA 3089	CA 3089
UDN 6116-2	SA 594
ULN 6128	NE 594
ULN 2003	ULN 2003
ULN 2004	ULN 2004
ULN 2151	μA 741
ULN 3304	NE 555
ULN 8160	NE 5560
ULN 8161	NE 5561

TI	SIGNETICS
LF 398	LF 398
LM 111	LM 111
LM 124	LM 124
LM 139	LM 139
LM 1458	MC 1458
LM 158	LM 158
LM 193	LM 193
LM 211	LM 211
LM 224	LM 224
LM 239	LM 239
LM 258	LM 258
LM 2901	LM 2901
LM 2903	LM 2903
LM 293	LM 293
LM 311	LM 311
LM 324	LM 324
LM 339	LM 339
LM 358	LM 358
LM 393	LM 393
LM 1458	MC 1458
MC 1558	MC 1558
NE 5532	NE 5532
NE 5532A	NE 5532A
NE 5534	NE 5534
NE 5534A	NE 5534A
NE 555	NE 555
NE 556	NE 556
RC 4558	NE 4558
SE 5534	SE 5534
SE 5534A	SE 5534A
SE 555	SE 555
SE 556	SE 556
SG 3524	SG 3524
SN 5520	NE 5520
SN 7588	MC 1488
SN 7589	MC 1489
SN 7589A	MC 1489A
SN 76689	CA 3089
TL 311	LM 311
TL 494	NE 5561
TL 594	NE 594
μA 723	μA 723
μA 733	μA 733
μA 741	μA 741
μA 747	μA 747
μA 748	μA 748
ULN 2003A	ULN 2003
ULN 2004A	ULN 2004

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DAC 08	AN106: Using the DAC 08 without a Negative Supply
MC 1488/1489	AN113: Applications Using the MC1488/1489 Line Drivers and Receivers
MC 1496/1596	AN189: Balanced Modulator/Demodulator Applications Using the MC1496/MC1596
MC 3403	AN160: Applications for the MC3403
SG 3524	AN126: Applications Using the SG3524
NE 5080/5081	AN195: Applications Using the NE5080, NE5081
NE 521	AN116: Applications for the NE521/522/527/529
NE 522	AN116: Applications for the NE521/522/527/529
NE 527	AN116: Applications for the NE521/522/527/529
NE 529	AN116: Applications for the NE521/522/527/529
NE 531	AN151: Applications for the NE531
NE 538	AN150: Applications for the NE538
NE 542	AN190: Applications of Low Noise Stereo Amplifiers: NE542
NE 544	AN133: Applications Using the NE544 Servo Amplifier
NE 555	AN170: NE555 and NE556 Applications
NE 556	AN170: NE555 and NE556 Applications
NE 558	AN171: NE558 Applications
NE 564	AN179: Circuit Description of the NE564
	AN180: The NE564: Frequency Synthesis
	AN182: Clock Regenerator with Crystal Controlled Phase Locked VCO
	AN181: A 6MHz FSK Converter Design Example for the NE564
NE 565	AN183: Circuit Description of the NE565
	AN184: FSK Demodulator with NE565
NE 566	AN185: Circuit Description of the NE566
	AN186: Waveform Generators with the NE566
NE 567	AN187: Circuit Description of the NE567 Tone Decoder
	AN188: Selected Circuits Using the NE567
NE 570/571/SA571	AN174: Applications for Compandors: NE570/571/SA571
NE 572	AN175: Automatic Level Control: NE572
NE 587/589	AN112: LED Decoder Drivers: Using the NE587 and NE589
NE 592/5592	AN141: Using the NE592/5592 Video Amplifier
NE 5044	AN131: Applications Using the NE5044 Encoder
NE 5045	AN132: Applications Using the NE5045 Decoder
NE 5512/5514	AN144: Applications for the NE5512 and NE5514
NE 5517	AN145: NE5517: General Description and Applications for Use with the NE5517/A Transconductance Amplifier
NE 5520	AN118: LVDT Signal Conditioner: Applications Using the NE5520
NE 5532/33/34	AN142: Audio Circuits Using the NE5532/33/34
NE 5535	AN143: Applications Using the SE/NE5535
NE 5539	AN140: Compensation Techniques for Use with the SE/NE5539
NE 5560	AN121: Forward Converter Application Using the NE5560
	AN122: NE5560 Push-Pull Regulator Application
NE 5561	AN123: NE5561 Applications
	AN124: External Synchronization for the NE5561
μA 758	AN191: Stereo Decoder Applications Using the μA758

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AN106	Using the DAC-08 without a Negative Supply
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AN113	Applications Using the MC1488/1489 Line Drivers and Receivers

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AN180	The NE564: Frequency Synthesis
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AN150	Applications for the NE538
AN151	Applications for the NE531
AN160	Applications for the MC3403
AN144	Applications for the NE5512 and NE5514
AN145	NE5517: General Description and Applications for Use with the NE5517/A Transconductance Amplifier
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AN123	NE5561 Applications
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S O PACKAGE AVAILABILITY

LINEAR LSI DEVICES CURRENTLY AVAILABLE IN S.O. PACKAGE

For information regarding additional SO products released since the publication of this document, contact your local Signetics sales office.

[3]DAC-08E	SO-16
[3]LF398	SOL-14
LM1870D	SOL-20
LM311	SO-8
LM319	SO-14
LM324	SO-14
LM339	SO-14
LM358	SO-8
LM393	SO-8
[3]MC1408-8	SO-16
MC1458	SO-8
MC1488	SO-14
MC1489	SO-14
MC1489A	SO-14
MC3302	SO-14
MC3403	SO-14
NE4558	SO-8
[2]NE5018	SOL-24
[3]NE5036	SO-14
NE5037	SO-16
NE5044	SO-16
NE5045	SO-16
[1]NE5090	SOL-16
NE521	SO-14
NE522	SO-14
NE527	SO-14
NE529	SO-14
NE532	SO-8
[3]NE5512	SO-8
[2]NE5514	SOL-16
NE5517	SO-16
[1]NE5520	SOL-16
[1]NE5532	SOL-16
NE5534A	SO-8
NE5534	SO-8
[3]NE5537	SO-14
NE5539	SO-14
NE555	SO-8
NE556	SO-14
NE5560	SO-16
NE5561	SO-8
NE5568	SO-8
[1]NE558	SOL-16
NE5592	SO-14
NE564	SO-16
[3]NE565	SO-14
NE566	SO-8
NE567	SO-8
[1]NE571	SOL-16
NE572	SO-16
[2]NE587	SOL-20
[2]NE589	SOL-20
NE592	SO-8
NE592	SO-14
NE592H	SO-8
NE592H	SO-14
[1]NE594	SOL-20
NE602	SO-8
NE604	SO-16
[1]NE660	SOL-20
SA571	SO-16
SA572	SO-16
SA602	SO-8
SA604	SO-16
SG3524	SO-16
μA723C	SO-14
μA741C	SO-8
μA747C	SO-14
ULN2003	SO-16
ULN2004	SO-16

NOTES:

1. SOL released in large SO package only.
2. SOL and non-standard pinout.
3. SO and non-standard pinout.

ORDERING INFORMATION

For Prefixes AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA and ULN

ORDERING INFORMATION

Signetics' Linear LSI integrated circuit products may be ordered by contacting either the local Signetics sales office, Signetics representatives and/or Signetics authorized distributors. A complete listing is located in the back of this manual.

Minimum Factory Order:

Commercial Product:
$1000 per order
$250 per line item per order

Military Product:
$250 per line item per order

Table 1 provides part number information concerning Signetics originated products.

Table 2 is a cross reference of both the old and new package suffixes for all presently existing types, while Tables 3 and 4 provide appropriate explanations on the various prefixes employed in the part number descriptions.

As noted in Table 3, Signetics defines device operating temperature range by the appropriate prefix. It should be noted, however, that devices with a SE prefix (−55°C to +125°C) indicates only its operating temperature range and *not* its military qualification status. The military qualification status of any Linear LSI product can be determined by either looking in the Military Section in this manual and/or contacting your local sales office.

Table 1 PART NUMBER DESCRIPTION

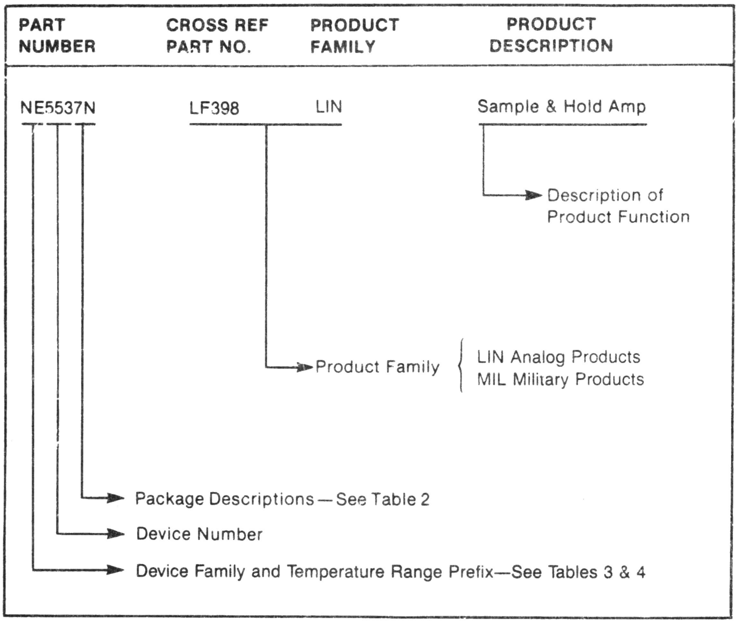

PART NUMBER
CROSS REF PART NO.
PRODUCT FAMILY
PRODUCT DESCRIPTION
NE5537N
LF398
LIN
Sample & Hold Amp
Description of Product Function
Product Family
LIN Analog Products
MIL Military Products
Package Descriptions—See Table 2
Device Number
Device Family and Temperature Range Prefix—See Tables 3 & 4

Table 2 PACKAGE DESCRIPTIONS

Old	New	PACKAGE DESCRIPTION
A,AA	N	14-lead plastic DIL
A	N-14	14-lead plastic DIL (Selected Analog products only)
B,BA	N	16-lead plastic DIL
-	D	Microminiature package (SO)
F	F	14, 16, 18, 22 and 24-lead ceramic (Cerdip) DIL
I,IK	I	14, 16, 18, 22, 28 and 4-lead ceramic DIL
K	H	10-lead TO-100
L	H	10-lead high-profile TO-100 can
NA,NX	N	24-lead plastic DIL
Q,R	Q	10, 14, 16 and 24-lead ceramic flat
T,TA	H	8-lead TO-99
U	U	SIL Plastic power
V	N	8-lead plastic DIL
XA	N	18-lead plastic DIL
XC	N	20-lead plastic DIL
XC	N	22-lead plastic DIL
XL,XF	N	28-lead plastic DIL

Table 3 SIGNETICS PREFIX AND DEVICE TEMPERATURE

PREFIX	DEVICE TEMPERATURE RANGE
N	0° to +70°C
S	−55° to +125°C
NE	0° to +70°C
SE	−55° to +125°C
SA	−40° to +85°C

Table 4 INDUSTRY STANDARD PREFIX

PREFIX	DEVICE FAMILY
AM	Linear Industry Standard
CA	Linear Industry Standard
DAC	Linear Industry Standard
JB	Mil Rel—Jan Qualified—Old Designator
JM	Mil Rel—Jan Qualified—New Designator
LF	Linear Industry Standard
LM	Linear Industry Standard
M	Mil Rel—Jan Processed
MC	Linear Industry Standard
NE	Linear Industry Standard
SA	Linear Industry Standard
SE	Linear Industry Standard
SG	Linear Industry Standard
μA	Linear Industry Standard
ULN	Linear Industry Standard

Section 2
Quality and Reliability

INDEX

SECTION 2 — QUALITY AND RELIABILITY

Quality and Reliability 2-1

QUALITY AND RELIABILITY

QUALITY AND RELIABILITY

Quality and reliability are two important measures of a product's merit. Quality is a measure of an integrated circuit's conformance to agreed-upon criteria at a given time, while Reliability is a measure of the circuit's ability to continue to conform over a period of time.

Quality

The quality of an integrated circuit is appraised by the user based on the ability of the circuit to meet the specified electrical criteria and external visual appearance. Linear LSI Division focuses on supplying to the user a product that has a high probability of meeting the user's needs through the sampling plans defined in MIL-STD-105D and the quality levels (AQL's) stated in Table II. Many of the inspection methods at critical process steps are now based on MIL-STD-883 criteria in order to build, rather than test, quality into the product.

Reliability

System performance over a period of time is the user's measure of an integrated circuit's reliability. The SUPR II Program improves system reliability by building quality into the product via additional manufacturing inspections and the offering of a burn-in screen. In addition to the SUPR II Program, Signetics performs periodic reliability testing via the SUREIII/883A Program to assure continuing uniformity and long-term reliability of all product lines. This data base is updated quarterly and is available upon request from the Linear LSI QR manager.

How Do Integrated Circuit Failures Occur?

Results from the Signetics Failure Analysis Lab over a three-year period on product returned from board checkout, system checkout, field usage and accelerated life testing are graphically presented in Figure 1. Under typical system operating conditions, random manufacturing defects, as outlined in Table 1, are the primary cause of true device failure. Also shown in Table 1 are the process controls that have been added via the SUPR II Program to minimize these defects prior to shipment to the customer. The device failure models are categorized as:

Half of the devices analyzed were found to be electrically good. They are attributed to being "false pulls" that occur during normal troubleshooting at the board and system levels.

Devices damaged by electrical over-stress account for 25% of the failures. Typical causes for electrical over-stress are incorrect board insertion, board shorts between device pins, power supply transients, and poor handling techniques.

The remaining 25% were verified to be true failures which occurred as a result of an in-process manufacturing defect or test escape.

Improved Quality Benefits

From the user's point of view, improved integrated circuit quality from the supplier means a lower cost of ownership. This cost saving can be effected through the reduction or elimination of involved incoming inspection testing, reduced PC board rework, simplified system checkout, reduced in-line inventories, and less complicated part tracking by Purchasing Management.

The SUPR II Program is Corporate in scope and covers Logic (Standard TTL, Schottky TTL, Low Power Schottky TTL, ECL, 8T Interface), Analog (Industrial, Consumer, Interface), Bipolar Memories (RAMs, ROMs, PROMs), and MOS Memories (RAMs, ROMs, Shift Registers). All package options are also available.

The SUPR II flow is detailed in Figure 5, including the test methods and Quality acceptance levels (Table 2 provides the electrical/mechanical finished product AQLs). Highlights of the flow are visual inspections, hermeticity, and burn-in, all based on MIL-STD-883 criteria.

A good example of the savings which can be achieved by purchasing tighter inspection levels is given in Figure 2. Here we are comparing the various levels of inspection (AQLs) available for device functionality and its impact on the number of PC boards which must be reworked during system manufacturing.

FAILURE ANALYSIS DATA SUMMARY

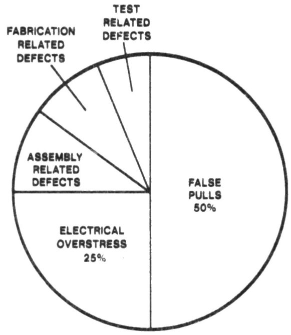


Figure 1

AQL LEVELS ON FUNCTIONALITY VERSUS BOARD REWORK RATES

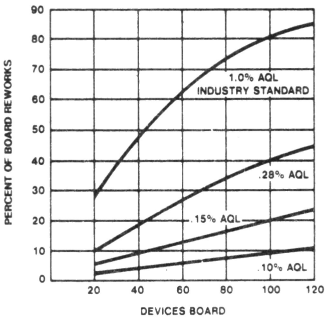


Figure 2

FAILURE MECHANISMS	CAUSES	PROCESS CONTROLS
Die Fabrication Related	Metalization Oxide Defects Mechanical Scratches Contamination	SEM Monitor Visual Stabilization Brake Burn-In
Assembly Related	Bonding, Wire, Package and Seal Defects	Preseal Visual Stabilization Bake Hermeticity
Test Related	Test Escapes	Tightened AQL Guarantees High Temperature Testing Product Characterization

QUALITY AND RELIABILITY

LEVEL B
Removal of Infant Mortality Failures

Failure rates are most severe during the first few months of operating life. This is known as the "infant mortality" phase. A system manufacturer has various options to solve problems arising from infant failures. He can ship his system to the end customer and repair field failures as they occur. He can operate the system in-house for this period and repair failures. Or he can purchase devices which have already been preconditioned to eliminate the early failures. Each customer must choose the most cost-effective method for his particular business. A considerable number of the reliabilty defects which cause early failures are eliminated by the manufacturing control and preconditioning steps of SUPR II Level A processing. More persistent defects can be removed by the use of "burn-in" techniques. The "burn-in" processing of SUPR II Level B effectively allows the system manufacturer to ship his equipment at Point 3 on the failure rate curve in Figure 3.

RELATIVE FAILURE RATE VERSUS TIME

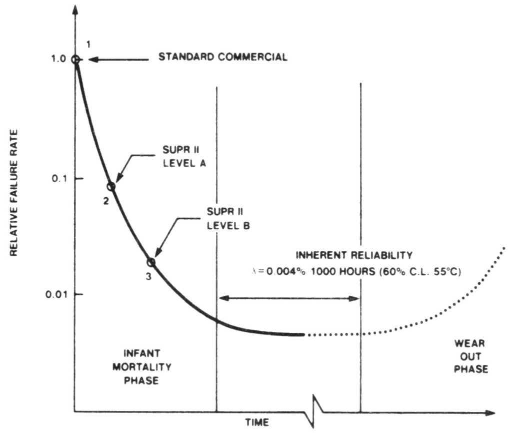


Figure 3

Burn-In Conditions

MIL-STD-883A, Method 1015 describes a number of different conditions for integrated circuit burn-in. For SUPR II Level B, Signetics has selected Condition F. This is the accelerated burn-in method derived from MIL-STD-883A, utilizing a high temperature reversed bias condition. This bias scheme is preferred for infant mortality screening, while operating conditions are generally utilized for internal reliability programs oriented toward generating MTBF data for the system designer.

Integrated Burn-In Flow

Signetics SUPR II Level B burn-in is performed to provide reliability assurance equivalent to a 168-hour/125°C screen. This process has been integrated into the standard manufacturing flow to provide the customer with the most cost effective screen and significantly reduced delivery times.

		LINEAR LSI QUALITY	
		AQL Guarantees	Process Average (PPM)
DC PARAMETRIC/FUNCTIONAL **AC PARAMETRIC**	MIN/MAX RATED OVER TEMP 25°C (Combined)	0.1	150
MECHANICAL	MAJOR/ MINOR (Combined)	0.4	150
SEAL TESTS (CERAMIC/METAL CANS ONLY)	FINE LEAK 5×8^{-8}cc/s GROSS LEAK (Combined)	0.4	1000

Table 2 SUPR II AQL GUARANTEE

BURN-IN FLOW

ASSEMBLY

The flow from SEM control through package seal is common to Levels A and B.

TEST

The pre-burn-in electrical screen is designed to remove assembly rejects and increase equipment efficiency.

BURN-IN

The 24-hour/155°C accelerated burn-in is well controlled to provide maximum screening effectiveness without damaging good devices.

TEST

The post-burn-in electrical is a 100% production DC/function electrical test.

Figure 4

SURE III/883B RELIABILITY PROGRAM

Definition

Signetics is recognized as a manufacturer of reliable integrated circuits. Signetics realized long ago the need for a comprehensive reliability program to provide timely data representative of the entire

QUALITY AND RELIABILITY

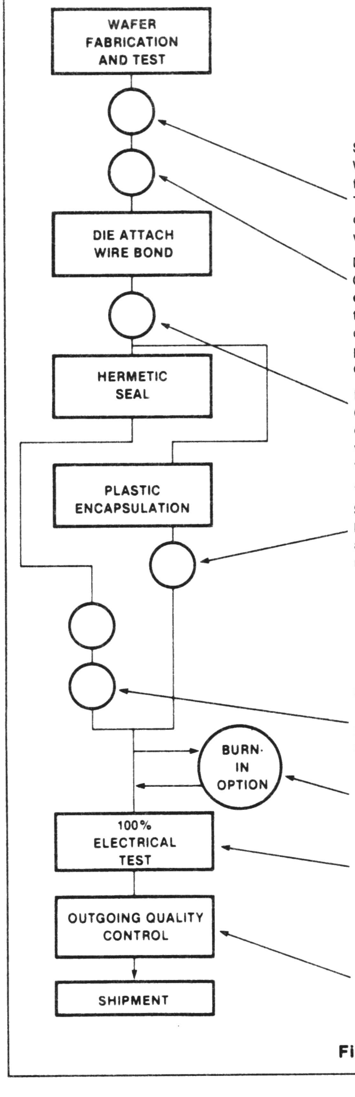
Signetics product line. Thus the establishment of a Systematic and Uniform Reliability Evaluation program, known as SURE, which provides this data in a manner unique to the industry. Furthermore, this program is provided at no cost to customers.

The SURE Program is a Signetics in-house Qualification Test Program which has been in existence since 1963. The SURE Program is designed to monitor the continuing uniformity of all Signetics products and to demonstrate via periodic qualifications that Signetics products meet or exceed the stringent long-term reliability requirements of their intended applications.

The SURE Program is reviewed and modified annually to incorporate appropriate changes in military microelectronic test programs, products and demonstrated product capabilities, and market requirements. The 1978 SUREIII/883B Reliability Program contains minor changes to the 1975 SUREII/883A Program, most significant of which is the inclusion of recent changes in military microelectronic test programs (i.e., inclusion of MIL-STD-883B, Method 5005.4 and MIL-M-38510D). The SUREIII/883B Program continues to incorporate additional environmental tests to fulfill the need for special reliability assurance of plastic products.

Data generated from this program is updated quarterly and is available from the Linear LSI Division QRA manager. Both quality and reliability have recently received major corporate focus at Signetics through the application—in all departments—of the Signetics 14-step Quality Improvement Program.

SUPR II PROCESS FLOW



SCANNING ELETRON MICROSCOPE CONTROL (SEM)
Wafers are sampled daily by the Quality Control Laboratory from each fabrication area and subjected to SEM analysis. This process control reveals manufacturing defects such as contact and oxide step coverage in the metalization process which may result in early failures.

DIE SORT VISUAL ACCEPTANCE
Criteria based on MIL-STD-883, Method 2010, Condition B, are employed to detect defects caused during fabrication, wafer testing, or the mechanical scribe and break operation. Critical defects such as scratches, smears, and glassivated bonding pads are inspected to a 1% AQL. Lot acceptance for noncritical defects is to a 4% AQL.

PRE-SEAL VISUAL ACCEPTANCE
Criteria based on MIL-STD-883, Method 2010, Condition B, are employed to detect any damage incurred at the die attach and wire bonding stations. Critical defects such as scratches, contamination and smeared ball bonds are inspected to a 0.65% AQL. Lot acceptance is to 2.5% AQL.

STABILIZATION BAKE PRECONDITIONING
Plastic molded devices are baked to stress wire and die bonds and help eliminate marginal devices. It also ensures an optimum plastic seal to enhance moisture resistance.

SEAL TESTS
Package seal integrity is ensured by 100% gross leak testing per MIL-STD-883, Method 1014, Condition C and fine leak sampling per Condition A or B.

BURN-IN (LEVEL B OPTION)
Devices are burned in for the equivalent of 168 hours at 125°C in accordance with MIL-STD-883A, Method 1015, Condition F.

100% PRODUCTION ELECTRICAL TESTING
Every device is tested for functional and DC parameters at 25°C, room ambient.

QA GUARANTEES
A final QA inspection step guarantees the mechanical and electrical AQL's of Table II. Every shipment is sealed and identified by QA personnel.

Figure 5

Section 3
Military

INDEX

SECTION 3 — MILITARY

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MILITARY PRODUCTS/PROCESS LEVELS

MILITARY PRODUCTS/ PROCESS LEVELS

The Signetics MIL 38510/883 Program is organized to provide a broad selection of processing options, structured around the most commonly requested customer flows. The program is designed to provide our customers:

- Fully compliant 883B flows on all products.
- Standard processing flows to help minimize the need for custom specs.
- Cost savings realized by using standard processing flows in lieu of custom flows.
- Better delivery lead times by minimizing spec negotiation time, plus allow customers to buy product off-the-shelf or in various stages of production rather than waiting for devices started specifically to custom specs.

The following explains the different processing options available to you. Special device marking clearly distinguishes the type of screening performed.

JAN CASE OUTLINE AND LEAD FINISH	SIGNETICS MILITARY PACKAGE TYPES					
	CERAMIC					
	8-PIN	14-PIN	16-PIN	18-PIN	20-PIN	24-PIN
PB	FE	—	—	—	—	—
CB	—	F	—	—	—	—
EB	—	—	F	—	—	—
JB	—	—	—	—	—	F
DB	—	W	—	—	—	—
FB	—	—	W	—	—	—
RB	—	—	—	—	F	—
VB	—	—	—	F	—	—

All products listed are also available in Die form.

Table 1 MILITARY PACKAGE AVAILABILITY

	JS	JB	RB
	JAN Qualified		883B
54	X	X	X
54LS	X	X	X
54S	X	X	X
82	—	—	X
8T	—	—	X
93XX	—	X	X
96XX	—	—	X
Analog	—	X	X
Bipolar Memory	—	X	X
Microprocessor	—	—	X

Table 2 MILITARY SUMMARY

JAN QUALIFIED (JS and JB)

JAN Qualified product is designed to give you the optimum in quality and reliability. The JAN processing level is offered as the result of the government's product standardization programs, and is monitored by the Defense Electronic Supply Center (DESC), through the use of industry-wide procedures and specifications.

JAN Qualified products are manufactured, processed and tested in a government certified facility to Mil-M-38510, and appropriate device slash sheet specifications. Design documentation, lot sampling plans, electrical test data and qualification data for each specific part type has been approved by the Defense Electronic Supply Center (DESC) and products appear on the DESC Qualified Products List (QPL 38510).

Quality conformance inspection testing, per MIL-STD-883, Method 5005, is performed according to Mil-M-38510 as follows:

- Group A; each sublot.
- Group B; one sublot for each package type every week.
- Group C; one sublot for each microcircuit group every 13 weeks.
- Group D; one sublot for each package type every 26 weeks.

NOTE: This category of part conforms to Quality Level B ($\pi Q = 1.0$) of MIL-HDBK-217D.

In addition to the common specs used throughout the industry for processing and testing, JAN Qualified products also possess a requirement for a standard marking used throughout the IC industry.

By implementing this space-oriented government standardization program, Signetics complies with the trend of reducing the numerous similar Source Control Drawings (SCD's). This standardized trend results in a *single* complete and comprehensive specification, a *single* product flow, and a *single* administrative effort—for both the aerospace community and for Signetics. This effort will also result in a *single* lower price. Because the list of Signetics' qualified products will change periodically, you may wish to contact your nearest Signetics' Sales Office or refer to the *Products Qualified* under Military Specification from DESC for our current update.

JAN Class S orders will be quoted with unit price only (similar to present Class B programs). There will be no lot charges for SEM inspection, electrical testing, or Group B or D qualification. All additional charges are amortized in the unit price.

Package types currently qualified are:
1) Cerdip—ceramic dual-in-line
2) Cerpac—ceramic flat pack

Government Source Inspection (GSI) is a required portion of the JAN 38510 Class S specification. No alterations to this specification may be instituted. Therefore, the only customer source inspection option is at pre-ship (verification only).

Additional program data options (such as wafer lot acceptance, attributes, Group B, D, and others) are available upon request for a nominal fee.

MIL-STD-883, LEVEL B

Processing to this option is ideal when no JAN slash sheets are released on devices required. Product is processed to MIL-STD-883 Method 5004, and is 100% electrically tested to Signetics data sheets.

Quality conformance inspection per MIL-STD-883, Method 5005, Group A, is performed on each sublot. Group A subgroup electrical parameters are those included in the detailed Signetics data book. Contact the factory for parametric subgroup assignments.

Generic quality conformance data per method 5005, Groups B, C and D, is generally available on popular device types and packages, but availability is not guaranteed. The factory must be consulted prior to ordering generic data. When available, generic data is defined as follows:

- Group B; Performed once per package type every six weeks of seal.
- Group C; Performed once per microcircuit group every 52 weeks of seal.

MILITARY PRODUCTS/PROCESS LEVELS

- Group D; Performed once per package type every 52 weeks of seal.

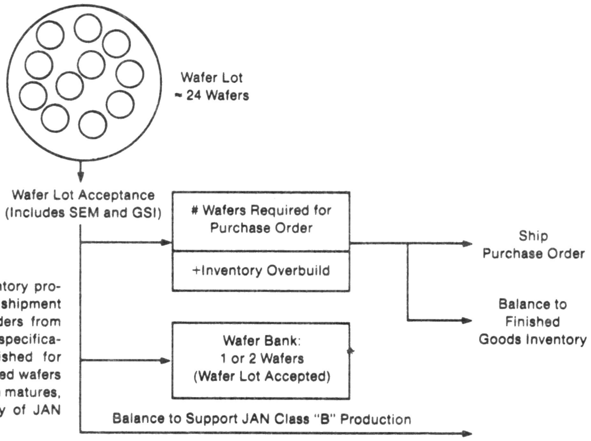
Quality conformance endpoint electrical parameters for Groups C and D are the Group A subgroups 1, 2, and 3.

Copies of generic data, Groups A, B, C and D, may be ordered by customers at a nominal charge.

NOTE: This category of part conforms to Quality Level B-2 (π_Q = 6.5 of MIL-HDBK-217D.

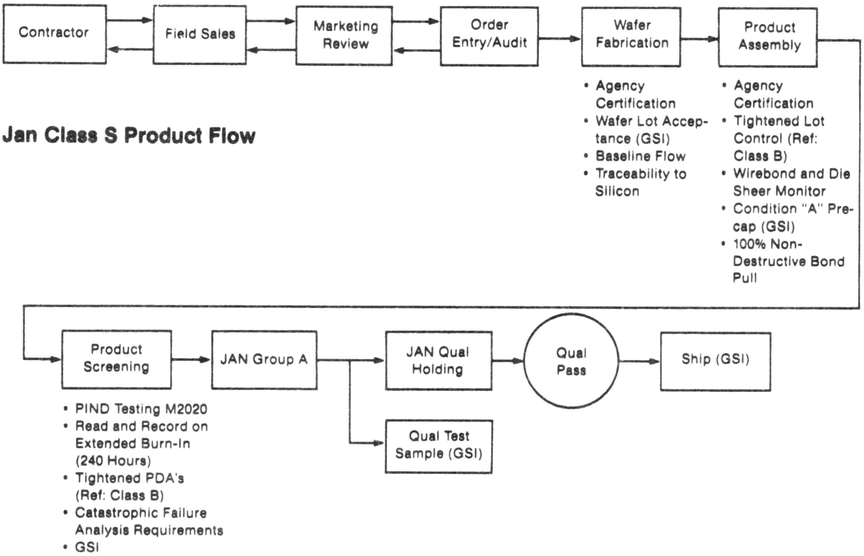
PROCESS LEVEL AND MARKING	PRE-CAP VISUAL	BURN IN	FUNCTIONAL TEST	DC/AC @ 25° C	DC @ TEMP	QPL	OFFSHORE
JS/JB JM38510XXXXX	2010, Cond. B	Yes	100%	100%	100%	Yes	No
RB SXXXX883B	2010, Cond. B	Yes	100%	100%	100%	No	Yes

JAN Class S Product Inventory


Wafer Lot
~ 24 Wafers
Wafer Lot Acceptance
(Includes SEM and GSI)
# Wafers Required for Purchase Order
+Inventory Overbuild
Ship
Purchase Order
Balance to
Finished
Goods Inventory
Wafer Bank:
1 or 2 Wafers
(Wafer Lot Accepted)
Balance to Support JAN Class "B" Production

The Signetics' JAN Class S inventory program will reduce delivery time and shipment delinquencies. As continuing orders from customers are processed to this specification, inventories will be established for products in the form of pre-qualified wafers and finished parts. As the program matures, this will allow immediate delivery of JAN Class S parts.

Jan Class S Product Flow


Contractor
Field Sales
Marketing Review
Order Entry/Audit
Wafer Fabrication
Product Assembly
• Agency Certification
• Wafer Lot Acceptance (GSI)
• Baseline Flow
• Traceability to Silicon
• Agency Certification
• Tightened Lot Control (Ref: Class B)
• Wirebond and Die Sheer Monitor
• Condition "A" Precap (GSI)
• 100% Non-Destructive Bond Pull
Product Screening
JAN Group A
JAN Qual Holding
Qual Pass
Ship (GSI)
Qual Test Sample (GSI)
• PIND Testing M2020
• Read and Record on Extended Burn-In (240 Hours)
• Tightened PDA's (Ref: Class B)
• Catastrophic Failure Analysis Requirements
• GSI

MILITARY PRODUCTS/PROCESS LEVELS

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 AND MIL-STD-883 REQUIREMENTS, METHODS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS		
			CLASS S	JAN QUALIFIED (JB)	883B (RB)
General Mil-M-38510 1. Pre-Certification A. Product Assurance Program B. Manufacturer's Certification	The Manufacturer shall establish and implement a Products Assurance Program Plan and provide for a manufacturer survey by the qualifying activity, Para. 3.4.1.1	—	X	X	N/A
2. Certification	Received after manufacturer has completed a successful survey, Para. 3.4.1.2	—	X	X	N/A
3. Device Qualification	Device qualification shall consist of subjecting the desired device to groups A, B, C & D of method 5005, Para. 3.4.1.2	—	X	X	N/A
4. Traceability	Traceability maintained back to a production lot Para. 3.4.6	—	X	X	X
5. Country of Origin	Devices must be manufactured, assembled, and tested within the U.S. or its territories, Para. 3.2.1	—	X	X	N/A
Screening Per Method 5004 of Mil-Std-883					
6. Non-Destructive Bond Pull	2023	100%	×	N/A	N/A
7. Internal Visual (Precap)	2010, Cond. A or B	100%	A	B	B
8. Stabilization Bake	1008, Cond. C Min	100%	×	×	×
9. Temperature Cycling	1010, cond. C; (10 cycles, –65°C to +150°C)	100%	×	×	×
10. Constant Acceleration	2001, Cond. E; (30kg in YI Plane)	100%	×	×	×
11. Visual Inspection	There is no test method for this screen; it is intended only for the removal of "Catastrophic Failures" defined as "Missing Leads, Broken Packages or Lids Off."	100%	×	×	×
12. Seal (Hermeticity) A. Fine	Cond. A or B (5.0 × 10^{-8}CC/Sec)	100%	×	×	×
B. Gross	Cond. C Min.	100%	×	×	×
13. Marking	Fungus inhibiting ink	100%	X	×	×
14. Particle Impart Noise Test	2020, Cond. A; per Paragraph 4.6.3 of MIL-M-38510	100%	×	N/A	N/A
15. Radiographic	2012; two views	100%	×	N/A	N/A
16. Interim Electricals (Pre Burn-In)	Per applicable Device Specification	100%	×	Optional	Optional
17. Burn-In	1015, Cond. as specified (160 hrs. Min at 125°C)	100%	240 hrs.	×	×

MILITARY PRODUCTS/PROCESS LEVELS

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 AND MIL-STD-883 REQUIREMENTS, METHODS AND TEST CONDITIONS	REQUIRE-MENT	PROCESSING LEVELS		
			CLASS S	**JAN QUALIFIED (JB)**	**883B (RB)**
18. Final Electricals	Per applicable Device Specification	100%	100% Read & Record	Slash Sheet	Data Sheet
a. Static Tests @25°C	Sub Group 1		×	×	×
b. Static Tests @ + 125°C	Sub Group 2		×	×	×
c. Static Tests @ − 55°C	Sub Group 3		×	×	×
d. Dynamic Test @25°C	Sub Group 4 (for Linear Products mainly)		×	×	×
e. Functional Test @25°C	Sub Group 7		×	×	×
f. Switching Test @25°C	Sub Group 9		×	×	×
g. Switching Test Temperature	Sub Groups 10, 11 (as applicable)		×	N/A	N/A
19. Percent Defective Allowable (PDA)	A PDA of 10% is a normal requirement applied against the static tests @25°C (A-1). This is controlled by the slash sheets for JAN products. For RB 10% is standard.	10%	5% 3% Functional	×	×
20. External Visual	2009	100%	×	×	×
Quality Conformance Inspection per Method 5005 of Mil-Std 883	**ATTRIBUTE DATA ONLY**				
21. Group A	Electrical Tests—Final Electricals (#14 above) repeated on a sample basis (Sub Groups 1 thru 12 as specified) performed in line with final electricals.	Each sublot	×	×	×
22. Group B	Package functional and constructional related test (package dimensions, resistance to solvents, internal visual & mechanical, bond strength & solderability).	Each pkg. type	Each sublot	Each week of seal	Generic
23. Group C	Die related tests (1,000 hr. operating life, temperature cycling, & constant acceleration).	Each μcircuit group	N/A	Each 13 weeks of seal	Generic
24. Group D.	Package related tests (physical dimensions, lead fatigue, thermal shock, temperature cycle, moisture resistance, mechanical shock, vibration, variable frequency, constant acceleration & salt atmosphere).	Each pkg. type	Each 26 weeks of seal	Each 26 weeks of seal	Generic

Table 5 REQUIREMENTS AND SCREENING FLOWS FOR STANDARD PRODUCTS (Cont'd)

MILITARY PRODUCTS/PROCESS LEVELS

LINEAR DEVICES

DEVICE	DESCRIPTION	PACKAGE DIP
	OPERATIONAL AMPLIFIERS	
LH2101A	Dual Op Amp	F
LM101A	Hi Perf Op Amp	F,FE
LM124	Quad Op Amp	F
SE5532	Dual Op Amp	FE
SE5532A	Dual Op Amp	FE
SE5534	Low Noise Op Amp	FE
SE5534A	Low Noise Op Amp	FE
SE5537	Sample and Hold Amp	FE
SE5539	High Freq Op Amp	F
	COMPARATORS	
SE521	Dual Differential Comparator	F
SE527	Voltage Comparator	F
SE529	Voltage Comparator	F
LM139/A	Quad Voltage Comparator	F
	DIFFERENTIAL AMPLIFIERS	
SE592	Video Amplifier	F
μA733	Video Amplifier	F
	PHASE LOCKED LOOPS	
SE567	Tone Decoder PLL	F
	TIMERS	
SE555	Timer	F, FE
SE556	Dual Timer	F
	D to A CONVERTERS	
SE5018	8-Bit μP-Comp DAC	F
	SMPS CONTROL CIRCUITS	
SE5560	SMPS Controller	F

JAN M—38510			
DEVICE	**SLASH SHEET**	**PKG**	**QUAL STATUS**
SE555	10903BCB	F	QPL 1
SE555	10903BPB	FE	QPL 1
SE556-1	10902BCB	F	QPL 1
LH2101A	10105BEB	F	QPL 1
LM101A	10103BCB	F	QPL 1
LM101A	10103BPB	FE	QPL 1

Section 4
Interface Data Conversion Products

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SECTION 4 — INTERFACE/DATA CONVERSION PRODUCTS

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D/A AND A/D CONVERTER—SYMBOLS AND DEFINITIONS

Absolute Accuracy Error

Absolute Accuracy Error is the difference between the theoretical analog input required to produce a given output code and the actual analog input required to produce the same code. The actual input is a range and the error is the midpoint of the measured band and the theoretical band.

Absolute Maximum Ratings

The Absolute Maximum Ratings are the operating safe zones. Exceeding these limits could cause permanent damage to the device. The device is NOT guaranteed to operate at these limits.

Conversion Speed

Conversion Speed is the speed at which a converter can make repetitive conversions.

Conversion Time

Conversion time is the time required for a complete conversion cycle of an ADC. Conversion time is a function of the number of bits and the clock frequency.

Differential Non-Linearity (DNL)

Differential Non-Linearity of a DAC is the deviation of the measured output step size from the ideal step size. In an ADC it is the deviation in the range of inputs from 1 LSB that causes the output to change from one given code to the next code. Excessive DNL gives rise to non-monotonic behavior in a DAC and missing codes in an ADC.

Differential Non-Linearity Tempco

Differential Non-Linearity Tempco is the temperature coefficient of DNL and specifies how DNL changes with temperature.

Full Scale Tempco

Full Scale Tempco in a DAC is the change of full scale output with a change of temperature. In an ADC it is the change in the input required to cause full scale transistion. Expressed in ppm/degree C.

Gain Error

Gain Error is the error of the slope of the line drawn through the midpoints of the steps of the transfer function as compared to the ideal slope. It is usually measured by determining the error of the analog input voltage to cause a full scale output word with the ideal value that should cause this full scale output. This gain error is usually expressed in LSB or in percent of full scale range.

Hysteresis Error

Hysteresis Error is the code transition voltage dependence relative to the direction from which the transistion is approached.

Integral Non-Linearity

Integral Non-Linearity is the difference between the ideal transfer characteristic and the actual characteristic.

Least Significant Bit (LSB)

The Least Significant Bit is the lowest order bit, or the bit with the least weight.

Missing Code

A Missing Code is a code combination that does not appear in the ADC's output range.

Monotonicity

A DAC is monotonic if its output either increases or remains the same when the input code is incremented from any code to the next higher code.

Most Significant Bit (MSB)

The Most Significant Bit is the highest order bit, or the one with the most weight.

Offset Error

Offset error is the constant error or shift from the ideal transfer characteristic of a converter. In a DAC it is the output obtained when that output should be zero. In an ADC it is the difference between the input level that causes the first code transistion and what that input level should be.

Output Voltage Compliance

Output Voltage Compliance of a current output DAC is the range of acceptable voltages at the DAC output for the DAC output current to remain within its specified limits.

Power Supply Sensitivity

Power Supply Sensitivity of a DAC is the change of output current or voltage with changes in the power supply voltage. In an ADC, it is the change in the transistion points from code to code with changes in the power supply voltage.

Quantizing Error

In an A/D converter there is an infinite number of possible input levels, but only 2^n output codes (n = number of bits). There will, therefore, be an error in the output code that could be as great as ½ LSB because of this quantizing effect. The greatest error occurs at the transistion point where the output state changes.

Relative Accuracy

Relative Accuracy is a measure of the difference of the theoretical output value with a given input after any offset and gain errors have been nulled out.

Resolution

Resolution is the number of bits at the input or output of an ADC or DAC. It is the number of discrete steps or states at the output and is equal to 2^n where in is the resolution of the converter. However, n bits of resolution does not guarantee n bits of accuracy.

Setting Time

Setting Time is the delay in a DAC from the 50 percent point on the change in the input digital code to the effected change in the output signal. It is expressed in terms of how long it takes the output to settle to and remain within a certain error band around the final value and is usually specific for full scale range changes.

Transfer Characteristic

The Transfer Characteristic is the relationship of the output to the input.

NOTE:
Refer to Section 9 (Interface Circuits) for an in-depth explanation of data converters and their applications.

CONVERTER SELECTOR GUIDES

D/A CONVERTERS

DEVICE	BITS	ACC. %	CONV. SPEED (μs)	OUTPUT V	OUTPUT I	INT. REF.	INT. LATCH	PACKAGE N	PACKAGE D	PACKAGE F	TEMPERATURE RANGE Com'l.	TEMPERATURE RANGE Mil	COMMENTS
MC1408-7	8	0.39	0.07		X			X		X			
MC1408-8	8	0.19	0.07		X			X	X	X	X		
MC1508-8	8	0.19	0.07		X					X		X	
DAC08	8	0.19	0.07		X					X		X	
DAC08A	8	0.10	0.07		X					X		X	
DAC08C	8	0.39	0.07		X			X		X	X		
DAC08E	8	0.19	0.07		X			X	X	X	X		
DAC08H	8	0.10	0.07		X			X		X	X		
NE5018	8	0.19	0.2	X		X	X	X		X	X		
SE5018	8	0.19	0.2	X		X	X			X		X	
NE5019	8	0.10	0.2	X		X	X	X		X	X		
SE5019	8	0.10	0.2	X		X	X			X			
NE5118	8	0.19	2.3		X	X	X	X		X	X		
SE5118	8	0.19	2.3		X	X	X			X		X	
NE5119	8	0.10	2.3		X	X	X	X		X	X		
SE5119	8	0.10	2.3		X	X	X			X		X	
NE5020	10	0.10	5.0	X		X	X	X		X	X		
NE5410	10	0.05	0.25		X					X	X		±¼ LSB DNL
SE5410	10	0.05	0.25		X					X		X	±¼ LSB DNL
MC3410	10	0.05	0.25		X					X	X		±½ LSB DNL
MC3510	10	0.05	0.25		X					X		X	±½ LSB DNL
AM6012	12	0.05	0.25		X					X	X		±1 LSB DNL
TDA1540D	14	0.012	0.5		X	X	X			X	X		Serial Input ±½ LSB DNL

A/D CONVERTERS

DEVICE	BITS	ACC.%	CONV. SPEED (μs)	INPUT V	INPUT I	THREE-STATE OUTPUT	INT. REF.	INT. CLOCK	PACKAGE N	PACKAGE F	PACKAGE FE	TEMPERATURE RANGE Com'l.	TEMPERATURE RANGE Mil
NE5034	8	0.19	17		X	X		X		X		X	
NE5036	6	0.78	23	X		X			X		X	X	
NE5037	6	0.78	9	X		X			X	X		X	
TDA1534	14	0.012	8.5		X		X	X	X			X	
ADC0801-1	8	0.10	73	X		X		X		X		X[1]	
ADC0802-1	8	0.19	73	X		X		X		X		X[1]	
ADC0803-1	8	0.19	73	X		X		X		X		X[1]	
ADC0804-1	8	0.39	73	X		X		X		X		X[1]	
ADC0805-1	8	0.39	73	X		X	X	X		X		X[1]	

Note:

1. Automotive temperature range: −40 to +85°C

CMOS 8-BIT A/D CONVERTERS

ADC0801/2/3/4/5-1

Preliminary

DESCRIPTION

The ADC0801 family is a series of five CMOS 8-bit successive approximation A/D converters using a resistive ladder and capacitive array together with an auto-zero comparator. These converters are designed to operate with microprocessor controlled buses using a minimum of external circuitry. The three-state output data lines can be connected directly to the data bus.

The differential analog voltage input allows for increased common-mode rejection and provides a means to adjust the zero scale offset. Additionally, the voltage reference input provides a means of encoding small analog voltages to the full 8 bits of resolution.

FEATURES

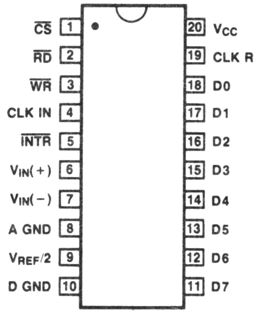
- **Compatible with most microprocessors**
- **Differential inputs**
- **Three-state outputs**
- **Logic levels TTL and MOS compatible**
- **Can be used with internal or external clock**
- **Analog input range 0V to V_{CC}**
- **Single 5V supply**
- **Guaranteed specification with 1MHz clock**

APPLICATIONS

- **Transducer to microprocessor interface**
- **Digital thermometer**
- **Digitally-controlled thermostat**
- **Microprocessor-based monitoring and control systems**

PIN CONFIGURATION

F,N PACKAGE



TOP VIEW

ORDER NUMBERS

ADC0801/02-1F
ADC0801/02/03-1 LCF
ADC081/02/03/04/05-1 LCN
ADC0804-1 CN

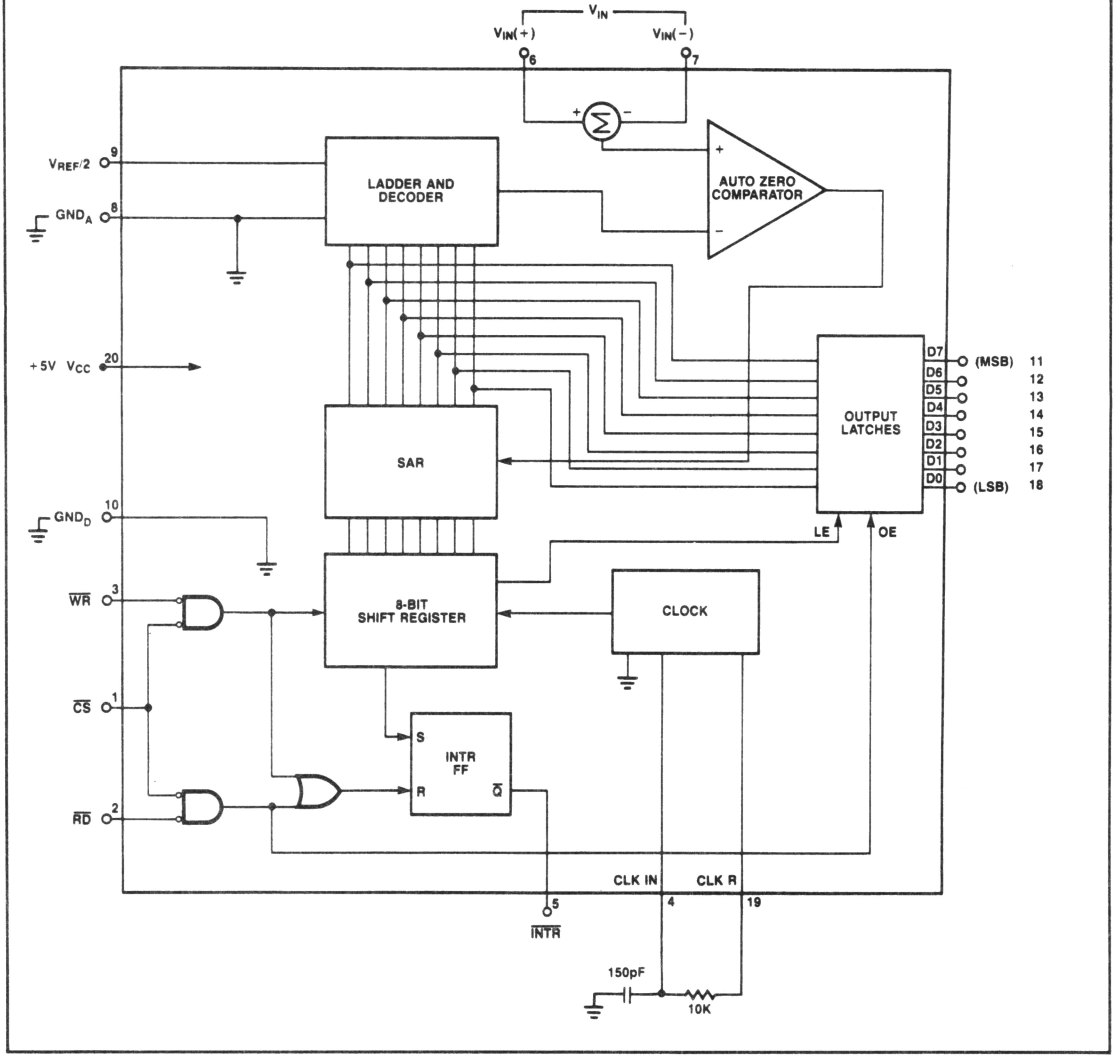
ABSOLUTE MAXIMUM RATINGS

SYMBOL & PARAMETER		RATING	UNIT
V_{CC}	Supply Voltage	6.5	V
	Logic Control Input Voltages	−0.3 to +16	V
	All Other Input Voltages	−0.3 to (V_{CC} +0.3)	V
T_A	Operating Temperature Range ADC0801/02-1 F	−55 to +125	°C
	ADC0801/02/03-1 LCF	−40 to +85	°C
	ADC0801/02/03/04/05-1 LCN	−40 to +85	°C
	ADC0804-1 CN	0 to +70	°C
T_{STG}	Storage Temperature	−65 to +150	°C
T_{SOLD}	Lead Soldering Temperature (10 seconds)	300	°C
P_D	Package Power Dissipation at T_A = 25°C	875	mW

CMOS 8-BIT A/D CONVERTERS ADC0801/2/3/4/5-1

Preliminary

BLOCK DIAGRAMS


V_{IN}
$V_{IN}(+)$
$V_{IN}(-)$
6
7
+
−
$V_{REF}/2$
9
GND_A
8
LADDER AND DECODER
AUTO ZERO COMPARATOR
+5V V_{CC}
20
OUTPUT LATCHES
D7
D6
D5
D4
D3
D2
D1
D0
(MSB) 11
12
13
14
15
16
17
(LSB) 18
SAR
GND_D
10
LE
OE
$\overline{WR}$
3
8-BIT SHIFT REGISTER
CLOCK
$\overline{CS}$
1
INTR FF
S
R
$\overline{Q}$
$\overline{RD}$
2
CLK IN
CLK R
5
4
19
$\overline{INTR}$
150pF
10K

CMOS 8-BIT A/D CONVERTERS

ADC0801/2/3/4/5-1

Preliminary

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 5.0V$, $f_{CLK} = 1MHz$, $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified.

SYMBOL & PARAMETER	TEST CONDITIONS	ADC0801/2/3/4/5			UNIT
		Min	Typ	Max	
ADC0801 Relative Accuracy Error (Adjusted)	Full Scale Adjusted			0.25	LSB
ADC0802 Relative Accuracy Error (Unadjusted)	$\frac{V_{REF}}{2} = 2.500\ V_{DC}$			0.50	LSB
ADC0803 Relative Accuracy Error (Adjusted)	Full Scale Adjusted			0.50	LSB
ADC0804 Relative Accuracy Error (Unadjusted)	$\frac{V_{REF}}{2} = 2.500\ V_{DC}$			1	LSB
ADC0805 Relative Accuracy Error (Unadjusted)	$\frac{V_{REF}}{2}$ = has no connection			1	LSB
$\frac{V_{REF}}{2}$ Input Resistance		400	640		Ω
Analog Input Voltage Range		−0.05		V_{CC} +0.05	V
DC Common Mode Error	Over Analog Input Voltage Range		1/16	1/8	LSB
Power Supply Sensitivity	$V_{CC} = 5V \pm 10\%$[1]				
CONTROL INPUTS					
V_{IH} Logical "1" Input Voltage	$V_{CC} = 5.25V_{DC}$	2.0		15	V_{DC}
V_{IL} Logical "0" Input Voltage	$V_{CC} = 4.75V_{DC}$			0.8	V_{DC}
I_{IH} Logical "1" Input Current	$V_{IN} = 5V_{DC}$		0.005	1	μA_{DC}
I_{IL} Logical "0" Input Current	$V_{IN} = 0V_{DC}$	−1	−0.005		μA_{DC}
CLOCK IN AND CLOCK R					
V_T+ Clk In Positive-Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T- Clk In Negative-Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H Clk In Hysteresis $(V_{T+}) - (V_{T-})$		0.6	1.3	2.0	V_{DC}
V_{OL} Logical "0" Clk R Output Voltage	$I_{OL} = 360\mu A$, $V_{CC} = 4.75\ V_{DC}$			0.4	V_{DC}
V_{OH} Logical "1" Clk R Output Voltage	$I_{OH} = -360\mu A$, $V_{CC} = 4.75\ V_{DC}$	2.4			V_{DC}
DATA OUTPUT AND $\overline{INTR}$					
V_{OL} Logical "0" Output Voltage					
Data Outputs	$I_{OL} = 1.6mA$, $V_{CC} = 4.75\ V_{DC}$			0.4	V_{DC}
$\overline{INTR}$ Outputs	$I_{OL} = 1.0mA$, $V_{CC} = 4.75\ V_{DC}$			0.4	V_{DC}
V_{OH} Logical "1" Output Voltage	$I_{OH} = -360\mu A$, $V_{CC} = 4.75\ V_{DC}$	2.4			V_{DC}
	$I_{OH} = -10\mu A$, $V_{CC} = 4.75\ V_{DC}$	4.5			V_{DC}
I_{OZL} 3-State Output Leakage	$V_{OUT} = 0V_{DC}$, $\overline{CS}$ = Logical "1"	−3			μA_{DC}
I_{OZH} 3-State Output Leakage	$V_{OUT} = 5V_{DC}$, $\overline{CS}$= Logical "1"			3	μA_{DC}
I_{SC} + Output Short Circuit Current	$V_{OUT} = O_V$, $T_A = 25°C$	4.5	6		mA_{DC}
I_{SC} − Output Short Circuit Current	$V_{OUT} = V_{CC}$, $T_A = 25°C$	9.0	16		mA_{DC}
I_{CC} Power Supply Current	$f_{CLK} = 1MHz$, $V_{REF/2}$ = Open $\overline{CS}$ = Logical "1", $T_A = 25°C$		3.0	3.5	mA

NOTE:

1. Analog inputs must remain within the range: $-0.05 \leq V_{IN} \leq V_{CC} + 0.05V$.

CMOS 8-BIT A/D CONVERTERS ADC0801/2/3/4/5-1

Preliminary

AC ELECTRICAL CHARACTERISTICS

SYMBOL & PARAMETER		TO	FROM	TEST CONDITIONS	ADC0801/2/3/4/5			UNIT
					Min	Typ	Max	
Conversion Time				f_{CLK} = 1MHz[1]	66		73	μs
f_{CLK}	Clock Frequency			See Note 1.	0.1	1.0	3.0	MHz
	Clock Duty Cycle			See Note 1.	40		60	%
CR	Free-Running Conversion Rate			$\overline{CS}$ = 0, f_{CLK} = 1MHz $\overline{INTR}$ Tied To $\overline{WR}$			13690	conv/s
$t_{W(\overline{WR})L}$	Start Pulse Width			$\overline{CS}$ = 0	30			ns
t_{ACC}	Access Time	Output	$\overline{RD}$	$\overline{CS}$ = 0, C_L = 100 pF		75	100	ns
t_{1H}, t_{OH}	Three-State Control	Output	$\overline{RD}$	CL = 10 pF, RL = 10K See Three-State Test Circuit		70	100	ns
t_{W1}, t_{R1}	$\overline{INTR}$ Delay	$\overline{INTR}$	$\overline{WD}$ or $\overline{RD}$			100	150	ns
C_{IN}	Logic Input =Capacitance					5	7.5	pF
C_{OUT}	Three-State Output Capacitance					5	7.5	pF

NOTE:
1. Accuracy is guaranteed at f_{CLK} =1MHz. Accuracy may degrade at higher clock frequencies.

FUNCTIONAL DESCRIPTION

The ADC0801 through ADC0805 series of A/D converters are successive approximation devices with 8-bit resolution and no missing codes. The most significant bit is tested first and after 64 clock cycles a digital 8-bit binary word is transferred to an output latch and the $\overline{\text{INTR}}$ pin goes low, indicating that conversion is complete. A conversion in progress can be interrupted by issuing another start command. The device may be operated in a continuous conversion mode by connecting the $\overline{\text{INTR}}$ and $\overline{\text{WR}}$ pins together and holding the $\overline{\text{CS}}$ pin low. To insure start-up when connected this way, an external $\overline{\text{WR}}$ pulse is required at power-up.

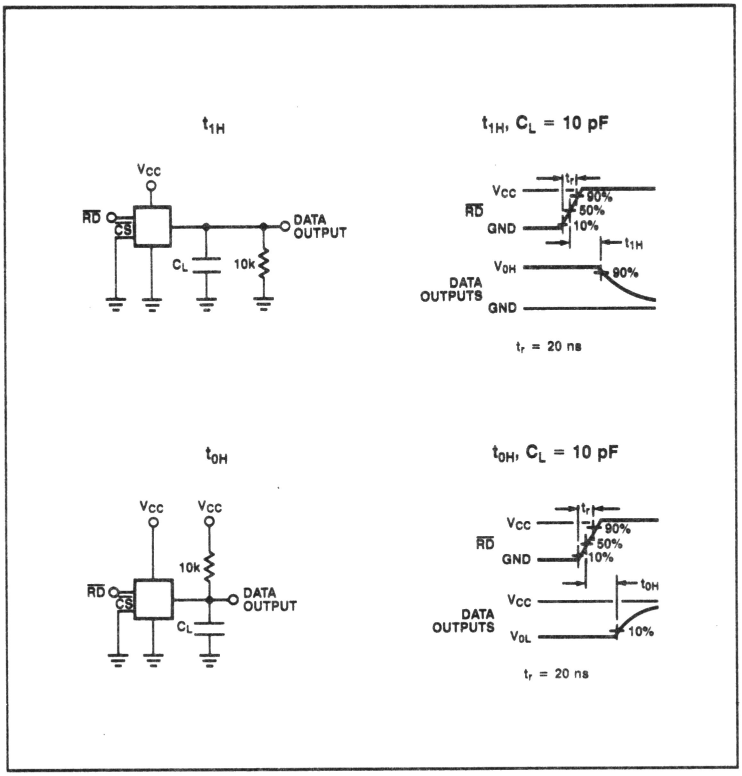
As the $\overline{\text{WR}}$ input goes low, when $\overline{\text{CS}}$ is low, the SAR is cleared and remains so as long as these two inputs are low. Conversion begins between 1 and 8 clock periods after at least one of these inputs goes high. As the conversion begins, the $\overline{\text{INTR}}$ line goes high. Note that the $\overline{\text{INTR}}$ line will remain low until 1 to 8 clock cycles after either the $\overline{\text{WR}}$ or the $\overline{\text{CS}}$ input (or both) goes high.

When the $\overline{\text{CS}}$ and $\overline{\text{RD}}$ inputs are both brought low to read the data, the $\overline{\text{INTR}}$ line will go low and the three-state output latches are enabled.

The digital control lines ($\overline{\text{CS}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$) operate with standard TTL levels and have been renamed when compared with standard A/D Start and Output Enable labels. For non-microprocessor based applications, the $\overline{\text{CS}}$ pin can be grounded, the $\overline{\text{WR}}$ pin can be interpreted as a $\overline{\text{START}}$ pulse pin, and the $\overline{\text{RD}}$ pin performs the OE (Output Enable) function.

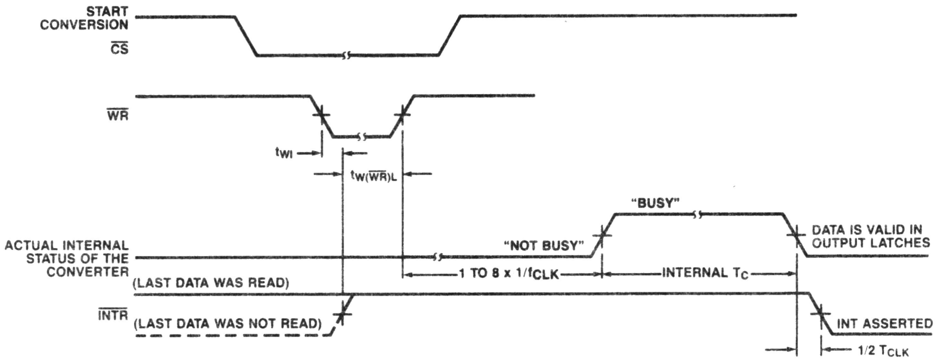
The $V_{IN}(-)$ input can be used to subtract a fixed voltage from the input voltage. Because there is a time interval between sampling the $V_{IN}(+)$ and the $V(-)$ inputs, it is important that these inputs remain constant, during the entire conversion cycle.

THREE-STATE TEST CIRCUITS AND WAVEFORMS

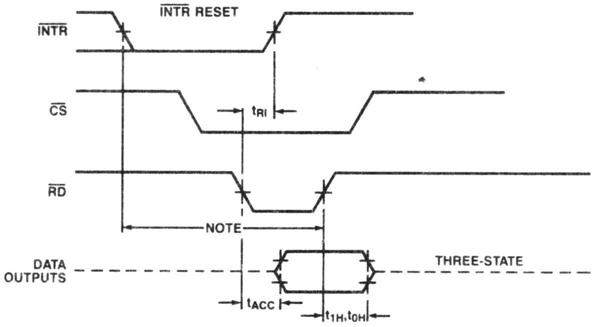

t_{1H}
V_{CC}
$\overline{\text{RD}}$
$\overline{\text{CS}}$
DATA OUTPUT
C_L
10k
t_{1H}, C_L = 10 pF
V_{CC}
$\overline{\text{RD}}$
GND
t_r
90%
50%
10%
t_{1H}
V_{OH}
90%
DATA OUTPUTS
GND
t_r = 20 ns
t_{0H}
V_{CC}
V_{CC}
10k
$\overline{\text{RD}}$
$\overline{\text{CS}}$
DATA OUTPUT
C_L
t_{0H}, C_L = 10 pF
V_{CC}
$\overline{\text{RD}}$
GND
t_r
90%
50%
10%
t_{0H}
V_{CC}
DATA OUTPUTS
V_{OL}
10%
t_r = 20 ns

Preliminary

TIMING DIAGRAMS (All timing is measured from the 50% voltage points)


START CONVERSION
$\overline{\text{CS}}$
$\overline{\text{WR}}$
t_{WI}
$t_{W(\overline{WR})L}$
"BUSY"
"NOT BUSY"
DATA IS VALID IN OUTPUT LATCHES
ACTUAL INTERNAL STATUS OF THE CONVERTER
1 TO 8 x 1/f_{CLK}
INTERNAL T_C
(LAST DATA WAS READ)
$\overline{\text{INTR}}$
(LAST DATA WAS NOT READ)
INT ASSERTED
1/2 T_{CLK}

OUTPUT ENABLE AND RESET $\overline{\text{INTR}}$


$\overline{\text{INTR}}$ RESET
$\overline{\text{INTR}}$
$\overline{\text{CS}}$
t_{RI}
$\overline{\text{RD}}$
NOTE
DATA OUTPUTS
THREE-STATE
t_{ACC}
t_{1H}, t_{0H}

Note: Read strobe must occur 8 clock periods ($8/f_{CLK}$) after assertion of interrupt to guarantee reset of $\overline{\text{INTR}}$.

8-BIT HI-SPEED A/D CONVERTER

NE5034

DESCRIPTION

The NE5034 is a high-speed microprocessor-compatible 8-bit Analog-to-Digital converter. It uses the successive approximation conversion technique, and includes the comparator, reference DAC, SAR, an internal clock and three-state buffers all on the same chip.

The converter can accommodate a wide analog input voltage range, bipolar or unipolar, selectable through external input resistors. An external capacitor controls the internal clock frequency, providing conversion times down to 17μs. Faster conversion times are possible using an external clock.

Microprocessor interfacing requirements are simple, allowing analog-to-digital conversion with a minimum of external components.

FEATURES

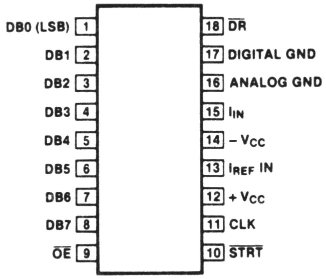
- **8-bit resolution and accuracy**
- **Accepts unipolar or bipolar inputs**
- **Three-state output buffers for easy microprocessor interface**
- **Choice of internal or external clocking**
- **Short conversion time, 17μs typical using internal clock**

APPLICATIONS

- **All microprocessor-based monitoring and control systems requiring analog signal inputs.**
- **Typical applications include: Automated process control, machine tools, robots, test and measurement instruments, environmental controls**
- **Other applications include: Ratiometric A/D conversion, very high resolution A/D conversion systems requiring high speed 8-bit building blocks**

PIN CONFIGURATION

F PACKAGE


DB0 (LSB) 1
DB1 2
DB2 3
DB3 4
DB4 5
DB5 6
DB6 7
DB7 8
OE 9
18 DR
17 DIGITAL GND
16 ANALOG GND
15 IIN
14 −VCC
13 IREF IN
12 +VCC
11 CLK
10 STRT

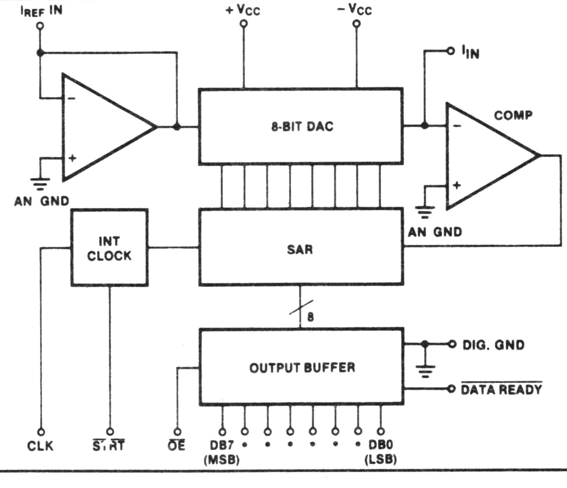
TOP VIEW

ORDER NUMBERS
NE5034F

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
$V_{CC}+$	Positive supply voltage	0 to +6	V
$V_{CC}-$	Negative supply voltage	0 to −15	V
I_{REF}	Reference current	1.5	mA
I_{IN}	Analog input current	5.0	mA
V_O	Data output voltage	6.0	V
Analog GND to Digital GND		1.0	V
V_L	Logic input voltage	−1 to $V_{CC}+$	V
P_D	Power dissipation		
	F package	1000	mW
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

BLOCK DIAGRAM


IREF IN
+VCC
−VCC
IIN
COMP
8-BIT DAC
AN GND
AN GND
INT CLOCK
SAR
8
OUTPUT BUFFER
DIG. GND
DATA READY
CLK
STRT
OE
DB7 (MSB)
DB0 (LSB)

DC ELECTRICAL CHARACTERISTICS $+V_{CC} = 5.0V$, $-V_{CC} = -12V$, $0°C \leq T_A \leq 70°C$ unless otherwise specified

SYMBOL AND PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution		8	8	8	Bits
	Relative accuracy error[1, 2]				± 1/2	LSB
$V_{CC}+$	Positive supply range		4.75	5.0	5.25	V
$V_{CC}-$	Negative supply range		−11.4	−12	−12.6	V
E_{FS}	Full scale gain error	$I_{REF} = 1.0mA$, $T_A = 25°C$		± 2	± 5	LSB
E_{ZS}	Zero scale offset error	$I_{REF} = 1.0mA$, $T_A = 25°C$		± 0.5	± 1	LSB
Psr	Power supply rejection[3]	$I_{REF} = 1.0$ mA, V_{CC} +4.75 to +5.25V, V_{CC} −11.4 to −12.6V			± 1/2	LSB
V_{IH}	Logic 1 input voltage ($\overline{\text{STRT}}$ and $\overline{\text{OE}}$)		2.0			V
V_{IH}	Logic 1 input voltage ext. clock		2.4			V
V_{IL}	Logic 0 input voltage ($\overline{\text{STRT}}$ and $\overline{\text{OE}}$)				0.8	V
V_{IL}	Logic 0 input voltage ext clock				0.7	V
I_{IH}	Logic 1 input current ($\overline{\text{STRT}}$ and $\overline{\text{OE}}$)	$V_{IN} = 2.4V$			20	μA
I_{IH}	Logic 1 input current ext clock	$V_{IN} = 2.4V$		100		μA
I_{IL}	Logic 0 input current ($\overline{\text{STRT}}$ and $\overline{\text{OE}}$)	$V_{IN} = 0.4V$		−20	−100	μA
I_{IL}	Logic 0 input current ext. clock	$V_{IN} = 0.7V$		−100		μA
V_{OL}	Logic 0 output voltage	$I_{OL} = 1.6mA$, $\overline{\text{OE}} = 0.8V$			0.4	V
V_{OH}	Logic 1 output voltage	$I_{OH} = 400\mu A$, $\overline{\text{OE}} = 0.8V$	2.4			V
I_{OZ}	Three-state leakage	$\overline{\text{OE}} = 2.0V$, $V_{OL} = 0V$ or $5V$		± 10		μA
I_{CC+}	Positive supply current	$V_{CC} + 5V$, $V_{CC} - 12V$		18	36	mA
I_{CC}	Negative supply current	$V_{CC} + 5V$, $V_{CC} - 12V$		−11	−22	mA

NOTES

1. Relative accuracy is defined as the deviation of the code transition points from the ideal code transition points on a straight line drawn from zero scale to full scale of the device.
2. Specifications given in LSBs refer to the weight of the least significant bit at the 8-bit level which is 0.39% of the full scale voltage.
3. MAX change in full scale.

AC ELECTRICAL CHARACTERISTICS $V+ = +5V$, $V- = -12V$, $T_A = 25°C$

SYMBOL & PARAMETER	TO	FROM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Internal clock frequency			$C_L = 60pF$ (See Figure 1)		500		KHz
External clock frequency						700	KHz
Tw $\overline{\text{STRT}}$ pulse width			Clock freq. = 500KHz	400			ns
External clock pulse width positive/negative				600			ns
Set up time[1]			See Figure 3	300			ns
tp (out data) propagation delay	data out	$\overline{\text{OE}}$	See Figure 2		50	200	ns
tp (out $\overline{\text{DR}}$) propagation delay	data ready out	8th clock	See Figure 3		700		ns
tp (3-state) propagation delay 3-state	high impedance o/p	$\overline{\text{OE}}$	See Figure 2		60	200	ns
tp (DB0) propagation delay	DB0	$\overline{\text{DR}}$	See Figure 3			500	ns
tp (SDR) $\overline{\text{STRT}}$ low to $\overline{\text{DR}}$ high	data ready high	$\overline{\text{STRT}}$ low	See Figure 3		700		ns

NOTE

1. See description of "Set up time".

TYPICAL PERFORMANCE CHARACTERISTICS

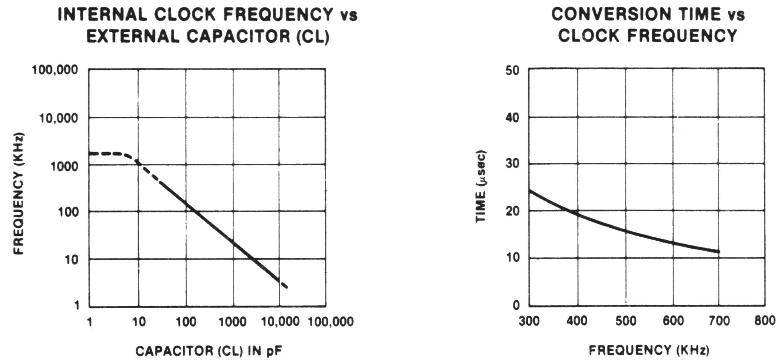
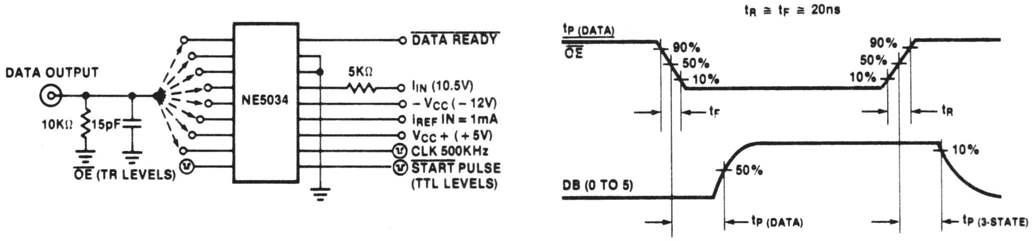


FIGURE 1

TEST LOAD CIRCUITS

DATA OUTPUT HIGH


DATA OUTPUT
10KΩ
15pF
$\overline{OE}$ (TR LEVELS)
NE5034
5KΩ
$\overline{DATA\ READY}$
I_{IN} (10.5V)
$-V_{CC}$ (−12V)
I_{REF} IN = 1mA
$V_{CC}+$ (+5V)
CLK 500KHz
$\overline{START}$ PULSE
(TTL LEVELS)
$t_R \cong t_F \cong 20ns$
$t_{P(DATA)}$
$\overline{OE}$
90%
50%
10%
t_F
90%
50%
10%
t_R
10%
50%
DB (0 TO 5)
$t_{P(DATA)}$
$t_{P(3\text{-}STATE)}$

DATA OUTPUT LOW

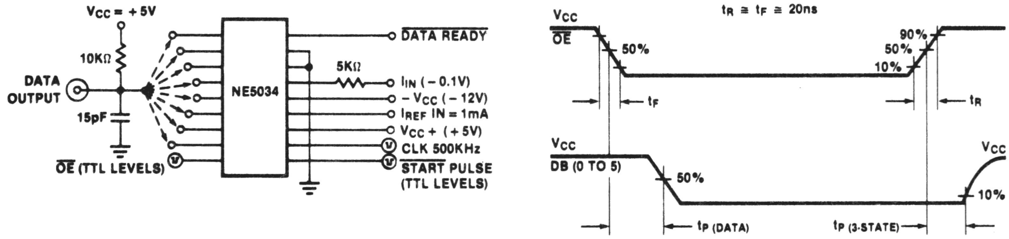

V_{CC} = +5V
10KΩ
DATA OUTPUT
15pF
$\overline{OE}$ (TTL LEVELS)
NE5034
5KΩ
$\overline{DATA\ READY}$
I_{IN} (−0.1V)
$-V_{CC}$ (−12V)
I_{REF} IN = 1mA
$V_{CC}+$ (+5V)
CLK 500KHz
$\overline{START}$ PULSE
(TTL LEVELS)
$t_R \cong t_F \cong 20ns$
V_{CC}
$\overline{OE}$
50%
t_F
90%
50%
10%
t_R
V_{CC}
DB (0 TO 5)
50%
V_{CC}
10%
$t_{P(DATA)}$
$t_{P(3\text{-}STATE)}$

FIGURE 2

8-BIT HI-SPEED A/D CONVERTER NE5034

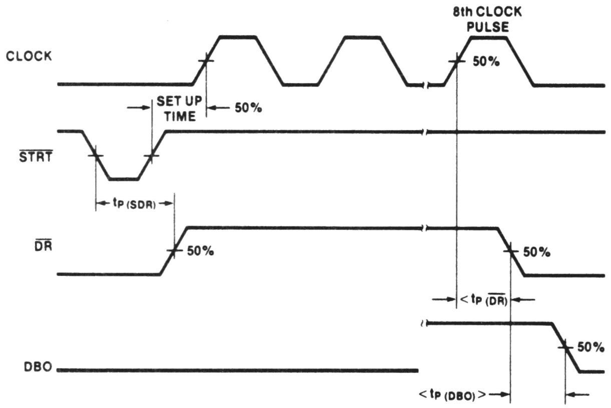


FIGURE 3

FUNCTIONAL PIN DEFINITIONS

$\overline{\text{DATA}}$ $\overline{\text{READY}}$ ($\overline{\text{DR}}$)

This is an output pin used to indicate that a conversion is in progress. $\overline{\text{DR}}$ goes to a logic "1" when $\overline{\text{STRT}}$ is at a logic "0". At the completion of a conversion $\overline{\text{DR}}$ returns to a logic "0". There is a delay (MAX 0.5μs) from the time $\overline{\text{DR}}$ goes to "0" to the time DB0 data is valid.

DB0-DB7

Eight three-state data outputs each with a drive capability of one TTL load. DB0 is the LSB and DB7 is the MSB.

$\overline{\text{OE}}$

Output enable input. When $\overline{\text{OE}}$ is at a logic "1" the data outputs assume a high impedance state. With $\overline{\text{OE}}$ at a logic "0", data is placed on the outputs. Data appearing on the outputs is only valid if both $\overline{\text{OE}}$ and $\overline{\text{DR}}$ are at logic "0" (see note on $\overline{\text{DR}}$ timing).

$\overline{\text{STRT}}$

This pin is used to reset the converter and start a new conversion. A logic "0" applied to this pin for a minimum of 400ns will reset the converter to a condition with DB7 at a logic "1" and all other Data outputs at logic "0". It will also cause $\overline{\text{DR}}$ to go to a logic "1" (see timing diagrams for delay times). Conversion will start with the 1st clock pulse after $\overline{\text{STRT}}$ returns to a logic "1" (see notes on set up time required). A $\overline{\text{STRT}}$ pulse while a conversion is taking place will cause the conversion to be aborted and the converter will reset. (See notes on short-cycle operation.)

CLK IN

An external capacitor between this pin and ground generates the internal clock pulses. (See diagram for clock frequency vs capacitor value). In order to synchronize the internal clock, to the start pulse a diode (small signal type e.g., 1N914) should be connected between $\overline{\text{STRT}}$ and CLK IN (see Figures 4 and 5). Without this diode the start pulse could occur at a time which could cause one of the conditions described in the Note on "set up" time. Applying an external TTL-or MOS-compatible clock to this pin slaves the NE5034 to external clock frequency. In this case, the diode is not required but the "set up" time requirements should be noted.

BASIC CIRCUIT DESCRIPTION

The NE5034 is an 8-bit A/D converter which incorporates the successive-approximation conversion method. Upon receipt of the $\overline{\text{STRT}}$ pulse, successive bits, beginning with the MSB (DB7), are applied to the input of the internal 8-bit current output DAC by the I^2L successive-approximation register (SAR) (see Block Diagram).

The comparator determines whether the output current of the DAC is greater or less than the input current converted from the unknown analog input voltage through an external input resistor. If the DAC output current is greater, the data latch for the trial bit is reset to a '0'; if it is less, the trial data bit stays at '1'. After all the bits from DB7 to DB0 have been tried, the SAR contains a valid 8-bit binary output code which accurately represents the unknown analog input to within ± 1/2 LSB (± 0.2%). This binary output will now remain in the SAR until another $\overline{\text{STRT}}$ pulse is applied.

During the successive-approximation sequence, the $\overline{\text{DATA}}$ $\overline{\text{READY}}$ signal remains at '1'. Upon completion of the conversion, the signal goes to a '0', indicating that data is valid and ready. If the $\overline{\text{OE}}$ input is left at a '0' during the conversion, the DATA OUTPUT shows the conversion sequence (see short cycle section). When the $\overline{\text{OE}}$ line is made a logic '1', the output buffers will go to a high impedance state and will remain so until the $\overline{\text{OE}}$ is returned to a '0' state.

TIMING DESCRIPTION

The timing diagram shown in Figure 7 shows the successive trial and decisions for each data bit.

With $\overline{\text{STRT}}$ at a logic "0" the converter is reset to a condition with DB7 at a logic "1", DR at a logic "1" and DB0-DB6 at logic "0".

Conversion starts after $\overline{\text{STRT}}$ returns to a logic "1". Starting with DB7 each bit is tried in turn, with the decision point being at the time of the positive going edge of the clock. Starting with the first positive edge after $\overline{\text{STRT}}$ returns to logic "1" (see note on "set up" time). The 8th positive going edge makes the decision on DB0 (LSB) and also causes $\overline{\text{DR}}$ to return to a logic "0" to indicate the conversion is complete. (See note on $\overline{\text{DR}}$ timing.)

SHORT-CYCLE OPERATION

In applications where less than 8 bits of resolution are required the NE5034 can be operated to achieve shorter conversion times. No hard wire changes are required to perform "short-cycling".

Conversion to X number of bits is completed at the end of X + 0.5 clock cycles (after a start pulse) $\overline{\text{DR}}$ will still be at a logic "1" state.

$\overline{\text{OE}}$ can be used to 3-state the outputs even during short-cycle operation.

BASIC SET-UP DIAGRAM
UNIPOLAR INPUT VALUES (0 – 10V)

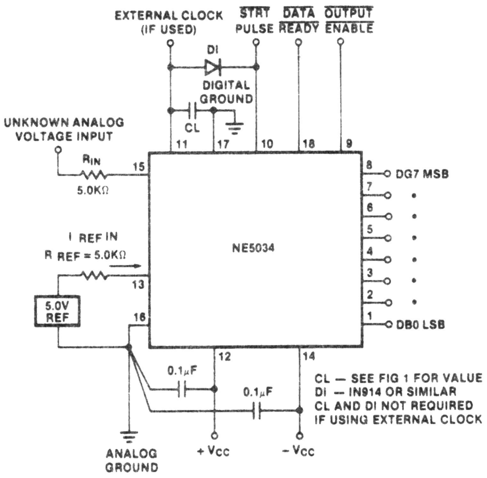

EXTERNAL CLOCK (IF USED)
STRT PULSE
DATA READY
OUTPUT ENABLE
DI
DIGITAL GROUND
CL
UNKNOWN ANALOG VOLTAGE INPUT
RIN
5.0KΩ
I REF IN
R REF = 5.0KΩ
5.0V REF
NE5034
11
17
10
18
9
15
13
16
8
7
6
5
4
3
2
1
12
14
DG7 MSB
DB0 LSB
0.1μF
0.1μF
ANALOG GROUND
+Vcc
–Vcc
CL — SEE FIG 1 FOR VALUE
DI — IN914 OR SIMILAR
CL AND DI NOT REQUIRED IF USING EXTERNAL CLOCK

FIGURE 4.

BASIC SET-UP DIAGRAM
BIPOLAR INPUT VALUES (± 10V RANGE)

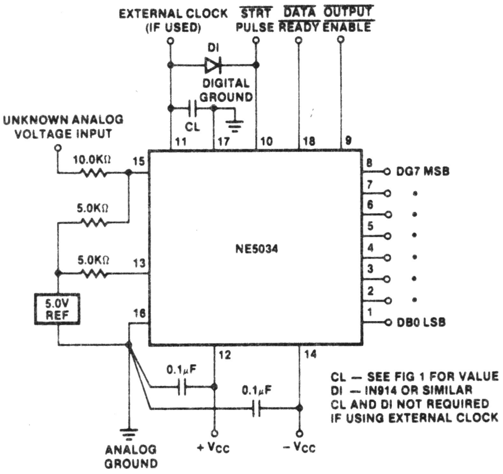

EXTERNAL CLOCK (IF USED)
STRT PULSE
DATA READY
OUTPUT ENABLE
DI
DIGITAL GROUND
CL
UNKNOWN ANALOG VOLTAGE INPUT
10.0KΩ
5.0KΩ
5.0KΩ
5.0V REF
NE5034
11
17
10
18
9
15
13
16
8
7
6
5
4
3
2
1
12
14
DG7 MSB
DB0 LSB
0.1μF
0.1μF
ANALOG GROUND
+Vcc
–Vcc
CL — SEE FIG 1 FOR VALUE
DI — IN914 OR SIMILAR
CL AND DI NOT REQUIRED IF USING EXTERNAL CLOCK

FIGURE 5.

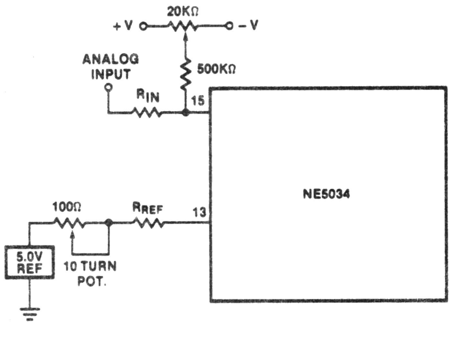

20KΩ
+V
–V
ANALOG INPUT
500KΩ
RIN
15
NE5034
100Ω
RREF
13
5.0V REF
10 TURN POT.

FIGURE 6. SUGGESTED ZERO/FULL SCALE ADJUST CIRCUIT

SET UP TIME

When using an external clock, the positive going edge of the start pulse must be synchronized to the clock pulse. There is a "set up" time of 300ns required between the time of the start pulse returning to a logic "1" and the next positive going edge of the clock.

If the positive edge of the start pulse occurs less than 300ns prior to the positive clock edge, one of the following conditions will occur:

a) The converter recognizes the clock pulse and converts as normal.
b) The conversion starts one clock pulse later.
c) The conversion never starts, this will be indicated by the fact that $\overline{\text{DR}}$ does not return to logic "0". In this case a new start pulse will be required.

DATA READY ($\overline{\text{DR}}$) TIMING

After $\overline{\text{DR}}$ returns to a logic "0" indicating a conversion is complete there is a time delay of 500ns before the data at DB0 output (the Least Significant Bit) is valid.

ZERO OFFSET (NEGATIVE FULL SCALE) CALIBRATION PROCEDURES

1. Apply continuous start pulses to the $\overline{\text{STRT}}$ input.
2. Apply 1/2 LSB in the case of unipolar operation, or 1/2 LSB above – FS in the case of bipolar operation to the analog input.
3. Observe all data outputs after each conversion is completed.
4. Adjust the potentiometer connected to I_{IN} (see Figure 6) until the LSB flickers between '0' and '1', and all other data outputs remain '0' following each conversion.

FULL SCALE (POSITIVE FULL SCALE) CALIBRATION:

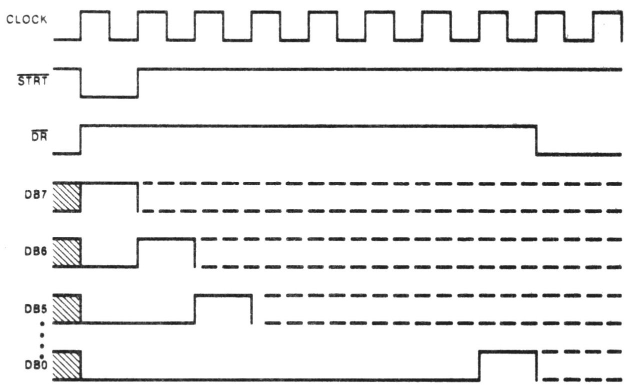
1. Apply continuous start pulses to the $\overline{\text{STRT}}$ input.
2. Apply full scale minus 1 1/2 LSB to the analog input.
3. Observe all data outputs after each conversion is completed.
4. Adjust the voltage applied to $V_{REF\ IN}$ (Figure 4) until the LSB varies between '0' and '1', and all other data outputs stay '1' after each conversion.

NOTE:

1. Where an input of 1/2 LSB is called for, the voltage is equal to $\frac{FS}{256}$.
2. The sequence of calibration should be:
   a. Zero offset
   b. Full scale adjust
   c. Zero offset
   d. Full scale adjust

OPERATING PRECAUTIONS:

Analog and digital grounds should have separate returns. Noise and jitter on digital ground will degrade accuracy unless the input is referenced to a 'clean' analog ground.



NOTE
1. $\overline{\text{OE}}$ = Logic "0"
2. See "Short-Cycle" section

FIGURE 7. NE5034 TIMING DIAGRAM

UNIPOLAR BINARY OPERATION:

A standard connection for a 0 to 10V unipolar binary operation, with $V_{REF\ IN}$ equal to +5 volts, is shown in Figure 4. The NE5034 can quantize full scale ranges of 1V to 10V. It should be noted, however, that for smaller full scale ranges, the accuracy and speed will degrade.

The input voltage versus output code relationship for unipolar operation is shown in Table 1. The full scale range is 2 times $I_{REF\ IN}$.

Table 1. Unipolar—Binary

ANALOG INPUT	DIGITAL OUTPUT CODE
NOTES 1, 2, 3	MSB LSB
FS—1 LSB	1 1 1 1 1 1 1 1
FS—2 LSB	1 1 1 1 1 1 1 0
3/4 FS	1 1 0 0 0 0 0 0
1/2 FS + 1 LSB	1 0 0 0 0 0 0 1
1/2 FS	1 0 0 0 0 0 0 0
1/2 FS – 1 LSB	0 1 1 1 1 1 1 1
1/4 FS	0 1 0 0 0 0 0 0
1 LSB	0 0 0 0 0 0 0 1
0	0 0 0 0 0 0 0 0

Table 2. Bipolar—Offset Binary

ANALOG INPUT	DIGITAL OUTPUT CODE
NOTES 1, 3, 4	MSB LSB
+ (FS – 1 LSB)	1 1 1 1 1 1 1 1
+ (FS – 2 LSB)	1 1 1 1 1 1 1 0
+ (1/2 FS)	1 1 0 0 0 0 0 0
+ (1 LSB)	1 0 0 0 0 0 0 1
0	1 0 0 0 0 0 0
– (1 LSB)	0 1 1 1 1 1 1 1
– (1/2 FS)	0 1 0 0 0 0 0 0
– (FS – 1 LSB)	0 0 0 0 0 0 0 1
– FS	0 0 0 0 0 0 0 0

BIPOLAR (OFFSET BINARY) OPERATION:

A standard connection for a – 5 to + 5V or – 10 to + 10V bipolar operation is shown in Figure 5.

NOTES:
1. Analog inputs shown are nominal center values of code.
2. "FS" is full scale; i.e., $2I_{REF\ IN}$ (Unipolar mode).
3. 1 LSB equals (2^{-8}) (FS).
4. "FS" is full scale; i.e., $I_{REF\ IN}$ (Bipolar mode).

6-BIT A/D CONVERTER (SERIAL OUTPUT) NE5036

DESCRIPTION

The NE5036 is an easy to use, low cost, successive approximation Analog to Digital converter, fabricated in Bipolar/I^2L technology, and packaged in a convenient 8-pin mini dip package.

With an external reference voltage, the NE5036 will accept input voltages between 0V and V_{REF}. Holding the $\overline{START}$ pin low for at least 8 clock pulses in duration will provide the 6-bit result of the conversion in a serial format.

FEATURES

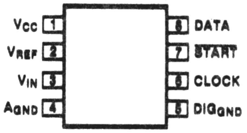
- **Three-state output buffer for easy μProcessor interfacing**
- **Fast successive approximation converter, 23μsec**
- **T^2L compatible inputs and outputs**
- **Easy interface to CMOS μProcessors**
- **Guaranteed no missing codes over full operating range**
- **Single supply operation, +5V**
- **High impedance analog inputs**
- **Positive true binary serial output**

APPLICATIONS

- **Temperature control**
- **μP-based appliances**
- **Light level monitor**
- **Electronic toys**
- **Joystick interface**
- **μP/Transducer interface**

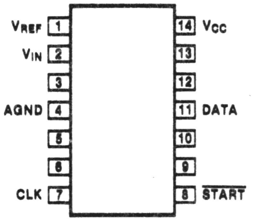
PIN CONFIGURATION

FE, N PACKAGE


VCC 1
VREF 2
VIN 3
AGND 4
8 DATA
7 START
6 CLOCK
5 DIGGND

TOP VIEW
ORDER NUMBERS
NE5036FE, NE5036N

D³ PACKAGE


VREF 1
VIN 2
3
AGND 4
5
6
CLK 7
14 VCC
13
12
11 DATA
10
9
8 START

TOP VIEW
ORDER NUMBER
NE5036D

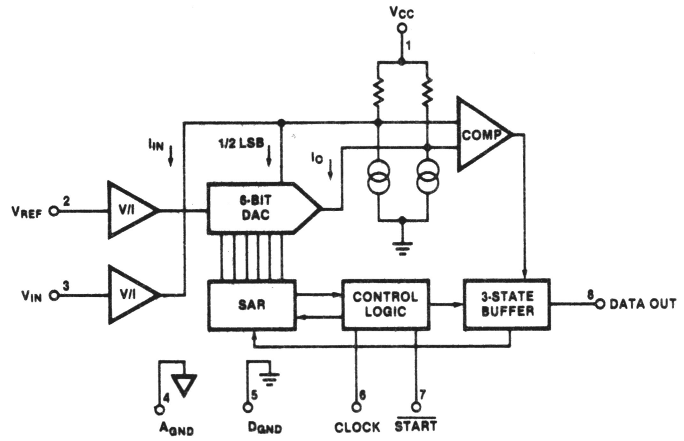
NOTES:

1. SOL–Released in large SO package only
2. SOL and non-standard pinout.
3. SO and non-standard pinouts.

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage	7	V
V_{REF}	Reference voltage	7	V
$V_{IN\,(Analog)}$	Analog input voltage	7	V
$V_{IN\,(Digital)}$	Digital input voltage ($\overline{START}$ & CLOCK)	7	V
D_{OUT}	Data output pin		
	Three-state mode	7	V
	Enabled mode	20	mA
Δ_{GND}	Analog GND to digital GND	±1	V
T_A	Operating temperature range	0 to 70	°C
T_{Stg}	Storage temperature range	−65 to 150	°C
t_{Sold}	Lead soldering temperature	300	°C
P_D	Power dissipation		
	FE package	220	mW
	N package	220	mW

BLOCK DIAGRAM


VCC
1
IIN
1/2 LSB
IO
COMP
VREF 2
V/I
6-BIT DAC
VIN 3
V/I
SAR
CONTROL LOGIC
3-STATE BUFFER
8 DATA OUT
4 AGND
5 DGND
6 CLOCK
7 START

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 5.0V$; $V_{REF} = 2.0V$; Clock = 350kHz; $0°C \leq T_A \leq 70°C$ unless otherwise specified. Typical values are specified at 25°C.

SYMBOL AND PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution		6	6	6	Bits
	Relative accuracy[1,2]			1/4	1/2	LSB
V_{CC}	Positive supply voltage		+4.75	+5.0	+5.50	V
ϵ_{FS}	Full scale gain error[2,3,4]	$V_{REF} = 2.0V$, $T_A = 25°C$		±1	±2	LSB
ϵ_{ZS}	Zero scale offset error[2]	$V_{REF} = 2.0V$, $T_A = 25°C$		±1/2	−1/2, +2	LSB
P_{SR}	Power supply rejection Max change in full scale[2]	$V_{REF} = 2.0V$ $4.75V \leq V_{CC} \leq 5.5V$		±1/2	±1	LSB
I_{IN}	Analog input bias current	$0 \leq V_{IN} \leq 2.5V$		1	10	µA
I_{REF}	Reference bias current	$0 \leq V_{REF} \leq 2.5V$		1	10	µA
R_{IN}	Analog input resistance		3	30		MΩ
V_{IH}	Logic '1' input voltage		2.0			V
V_{IL}	Logic '0' input voltage				0.8	V
I_{IH}	Logic '1' input current				10	µA
I_{IL}	Logic '0' input current			1	10	µA
I_{OH}	Logic '1' output current	$2.4V \leq V_{OH}$	300			µA
I_{OL}	Logic '0' output current	$V_{OL} \leq 0.4V$	1.6			mA
I_{OZ}	Three-state leakage current			±0.1	±40	µA
I_{CC}	Positive supply current			14	24	mA

AC ELECTRICAL CHARACTERISTICS

$V_{CC} = 5.0V$; $V_{REF} = 2.0V$; Clock = 350kHz; $0°C \leq T_A \leq 70°C$ unless otherwise specified. Typical values are specified at 25°C. (Refer to test figures.)

SYMBOL AND PARAMETER		TO	FROM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{MAX}	Max clock frequency				350			kHz
T_{CONV}	Conversion time						8	Clock cycles
t_W	Clock pulse width				1.3			µs
t_S	Setup time, $\overline{\text{START}}$ to clock[6]	Clock	$\overline{\text{START}}$		500			ns
$t_{P\,(OUT)}$	Propagation delay[5]	Data out	Clock	$T_A = 25°C$, $t_r = t_f < 20ns$			600	ns
$t_{P\,(3\text{-}STATE)}$	Propagation delay[5]	Data (3-State)	$\overline{\text{START}}$	$T_A = 25°C$, $t_r = t_f < 20ns$			600	ns

NOTES

1. Relative accuracy is defined as the deviation of the code transition points from the ideal code transition points on the straight line drawn from zero scale to full scale of the device.
2. Specifications given in LSB's refer to the weight of the least significant bit at the bit level which is 1.56% of the full scale voltage.
3. Full scale gain error is the deviation of the code transition point (111110 to 111111) from its ideal value (accounting for offset error at 000000).
4. The analog input voltage (V_{IN}) range is from 0V to V_{REF} nominally, with the output remaining at 111111 even though the input may increase from V_{REF} to V_{CC}. (For optimum performance V_{REF} can be any value from 1.5V to 2.5V.)
5. The time between the specified reference points on the clock and the output waveforms with the output changing (low to high or high to low).
6. The high to low transition of the $\overline{\text{START}}$ pulse should occur at least 500ns prior to the negative edge of the clock pulse to insure its recognition. The $\overline{\text{START}}$ pulse should stay high for at least 500ns between conversions to guarantee proper recognition.

6-BIT A/D CONVERTER (SERIAL OUTPUT) NE5036

CIRCUIT DESCRIPTION

NE5036 is a complete 6-bit, serial output, A/D converter which incorporates the successive approximation method. The chip includes the internal control logic, the successive approximation register (SAR), 6-bit DAC, comparator and the output buffer. An externally generated clock source (max freq = 350 kHz) must be provided to pin 6. An external reference voltage supplied to pin 2 sets the full scale range of the A/D converter as shown in the Block Diagram.

Upon the $\overline{\text{START}}$ pin going low, successive approximation conversion commences after the first low going edge of the clock pulse. Successive bits, beginning with the MSB (D5) are applied to the input of the internal 6-bit current output DAC by the I^2L successive approximation register.

The comparator determines whether the output current of the DAC is greater or less than the input current, converted from the unknown analog input voltage through the V/I converter. If the DAC output is greater, that bit of the DAC is set to 0 and simultaneously the output buffer goes to 0. If it is less, that bit stays at 1 and the output buffer goes to 1. After the second high to low transition of the clock pulse, the MSB (D5) data is valid. On successive clock pulses, successive bits are tried and the output buffer represents that bit. $\overline{\text{START}}$ has to stay low for at least 8 clock pulses for the conversion to be completed and to access the 6-bit result of the conversion. A conversion in process can be interrupted by issuing another $\overline{\text{START}}$ pulse.

When $\overline{\text{START}}$ is in a high state, the output buffer is in a high impedance state.

The timing diagram for the device is shown in Figure 1.

TRANSFER CHARACTERISTICS

The NE5036 is designed to have a nominal 1/2 LSB offset, so that the code transition points are located 1/2 LSB on either side of the exact analog input for a given code. Thus the first transition (000000 to 000001) will occur at an input of 1/2 LSB (15.63mV with a V_{REF} of 2.0V), plus any offset. Subsequent transition (to full scale — 111111) will occur at 62.5 LSB (1.953V at V_{REF} of 2.0V).

The ideal transfer characteristic of NE5036 is shown in Figure 2.

LAYOUT PRECAUTIONS

Analog ground (pin 4) and Digital ground (pin 5) are not connected internally and should be connected together as close to the device as possible for optimum performance. The leads to the analog inputs should be kept as short as possible to minimize input noise pickup. Input bypass capacitors from the analog inputs to ground will eliminate noise pickup. Power supplies should be decoupled with at least 1μF and should be located close to the device to minimize the effects of noise spikes on V_{CC}.

The reference input and the analog voltage input must both remain stable during conversion to insure accuracy and proper operation. This can be done by adequately bypassing these inputs and/or keeping the impedance at these inputs at or below 2K-ohms.

TIMING DIAGRAM

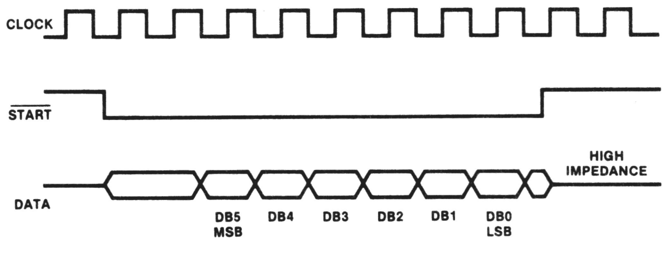


Figure 1

IDEAL TRANSFER CHARACTERISTICS

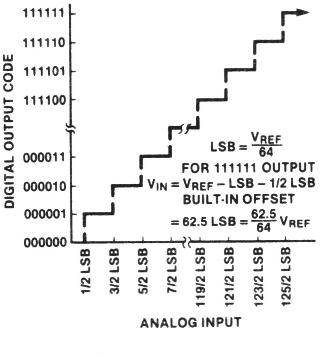
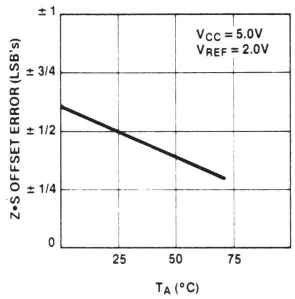


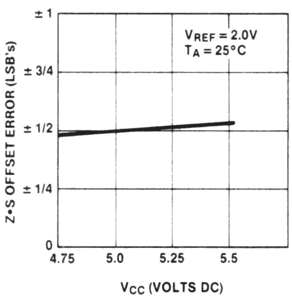
Figure 2

TYPICAL PERFORMANCE CHARACTERISTICS

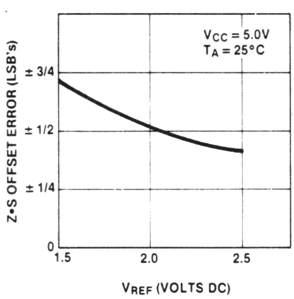
ZERO SCALE OFFSET ERROR vs TEMPERATURE



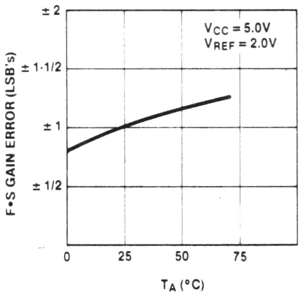
ZERO SCALE OFFSET ERROR vs V_{CC}



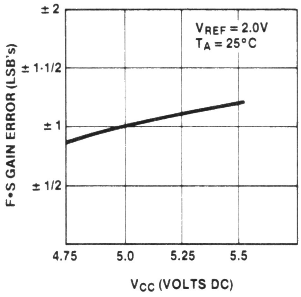
ZERO SCALE OFFSET ERROR vs V_{REF}



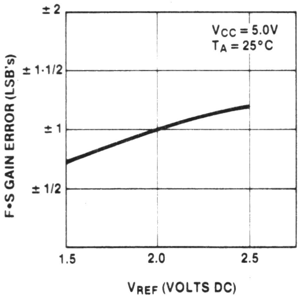
FULL SCALE GAIN ERROR vs TEMPERATURE



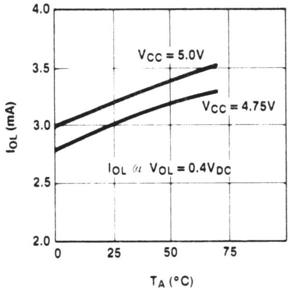
FULL SCALE GAIN ERROR vs V_{CC}



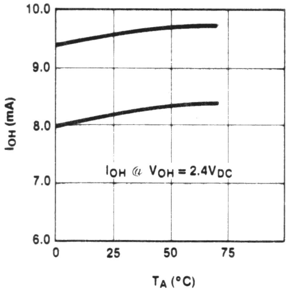
FULL SCALE GAIN ERROR vs R_{REF}



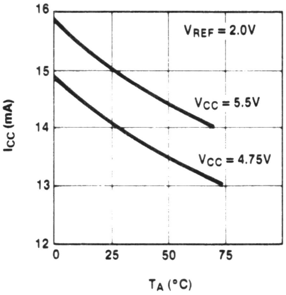
I_{OL} vs TEMPERATURE (DATA OUTPUT)



I_{OH} vs TEMPERATURE (DATA OUTPUT)



I_{CC} vs TEMPERATURE

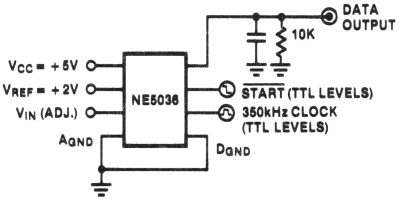


6-BIT A/D CONVERTER (SERIAL OUTPUT) NE5036

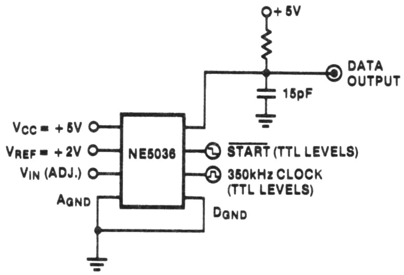
AC TEST CIRCUITS AND WAVEFORMS

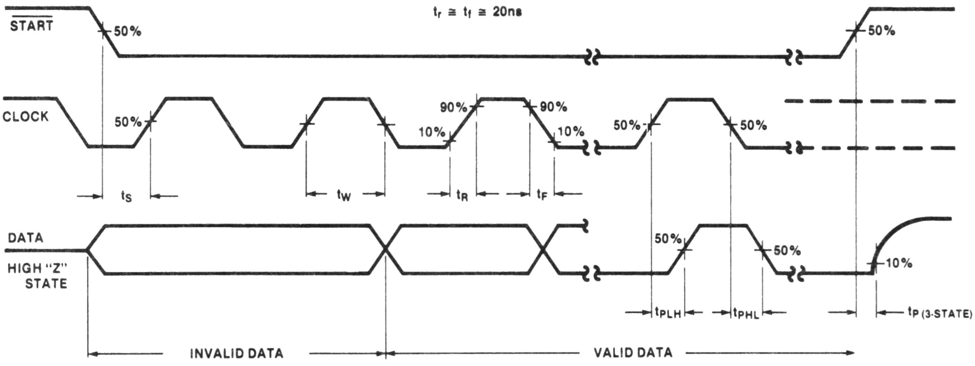
PROPAGATION DELAY TIME $t_{p\,(DATA)}$

DATA OUTPUT (LOW TO HIGH)


DATA OUTPUT
10K
Vcc = +5V
VREF = +2V
VIN (ADJ.)
NE5036
START (TTL LEVELS)
350kHz CLOCK (TTL LEVELS)
AGND
DGND

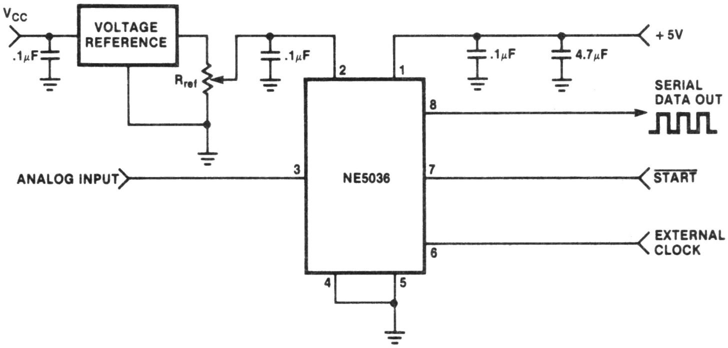
DATA OUTPUT (HIGH TO LOW)


+5V
DATA OUTPUT
15pF
Vcc = +5V
VREF = +2V
VIN (ADJ.)
NE5036
START (TTL LEVELS)
350kHz CLOCK (TTL LEVELS)
AGND
DGND

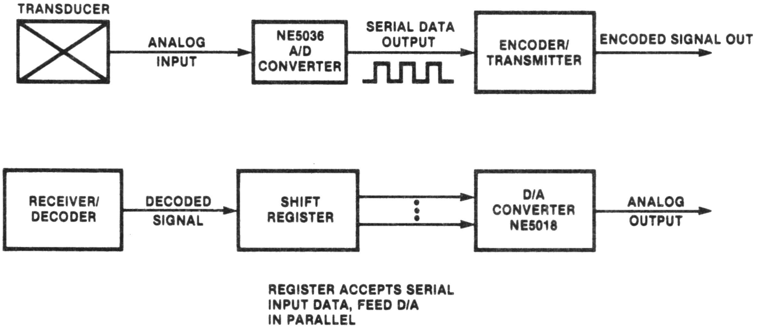

tr ≅ tf ≅ 20ns
START
50%
50%
CLOCK
50%
90%
90%
10%
10%
50%
50%
tS
tW
tR
tF
DATA
HIGH "Z" STATE
50%
50%
10%
tPLH
tPHL
tP (3-STATE)
INVALID DATA
VALID DATA

TYPICAL APPLICATION

1. BASIC NE5036 CONFIGURATION


V_{CC}
.1µF
VOLTAGE REFERENCE
R_{ref}
.1µF
2
1
.1µF
4.7µF
+5V
8
SERIAL DATA OUT
ANALOG INPUT
3
NE5036
7
$\overline{START}$
6
EXTERNAL CLOCK
4
5

2. DIGITAL COMMUNICATIONS USING NE5036


TRANSDUCER
ANALOG INPUT
NE5036 A/D CONVERTER
SERIAL DATA OUTPUT
ENCODER/ TRANSMITTER
ENCODED SIGNAL OUT
RECEIVER/ DECODER
DECODED SIGNAL
SHIFT REGISTER
D/A CONVERTER NE5018
ANALOG OUTPUT
REGISTER ACCEPTS SERIAL INPUT DATA, FEED D/A IN PARALLEL

6-BIT A/D CONVERTER (PARALLEL OUTPUTS) NE5037

DESCRIPTION

The NE5037 is a low cost, complete successive approximation analog to digital (A/D) converter, fabricated in Bipolar/I^{2}L technology. With an external reference voltage, the NE5037 will accept input voltages between 0V and V_{REF}. An external $\overline{START}$ pulse of at least 300ns in duration will provide the 6-bit result of the conversion in parallel format. Full conversion with no missing codes occurs in 9μs.

FEATURES

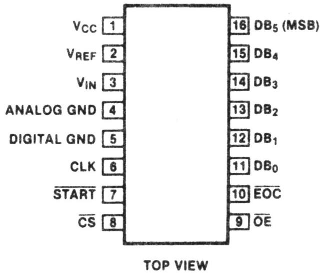
- **T^{2}L compatible inputs and outputs**
- **Three state output buffer**
- **Easy interface to CMOS μProcessors**
- **Fast conversion—9μs**
- **Guaranteed no missing codes over full temp range**
- **Single supply operation, +5V**
- **Positive true binary outputs**
- **High impedance analog inputs**

APPLICATIONS

- **Temperature control**
- **μP-based appliances**
- **Light level monitors**
- **Head position sensing**
- **Electronic toys**
- **Joystick interface**

PIN CONFIGURATION

D, F, N PACKAGE

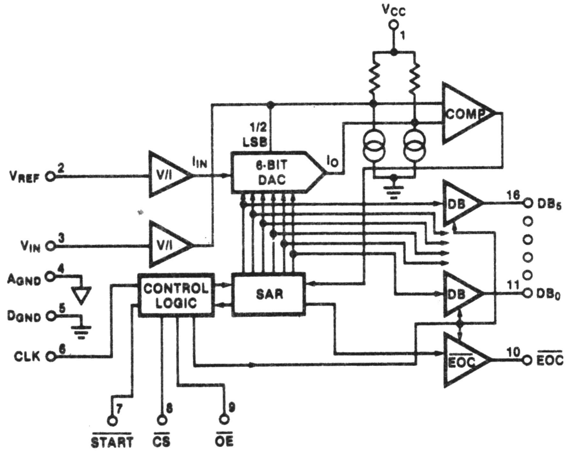

V_{CC} 1
V_{REF} 2
V_{IN} 3
ANALOG GND 4
DIGITAL GND 5
CLK 6
$\overline{START}$ 7
$\overline{CS}$ 8
16 DB_5 (MSB)
15 DB_4
14 DB_3
13 DB_2
12 DB_1
11 DB_0
10 $\overline{EOC}$
9 $\overline{OE}$
TOP VIEW

ORDER NUMBERS
NE5037F, NE5037N
NE5037D

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Power supply voltage	7	V
V_{REF}	Reference voltage	7	V
$V_{IN\ (Analog)}$	Analog input voltage	7	V
$V_{IN\ (Digital)}$	Digital input voltage ($\overline{CS}$, $\overline{OE}$, $\overline{START}$, CLK)	7	V
D_{OUT}	Data outputs (DB0 to DB5)		
	Three-state mode	7	V
	Enabled mode (each output)	5	mA
$\overline{EOC}$	End of conversion	V_{CC}	
Δ_{GND}	Analog GND to digital GND	±1	V
T_A	Operating temperature range	0 to 70	°C
T_{STG}	Storage temperature range	−65 to 150	°C
t_{SOLD}	Lead soldering temperature (10 seconds)	300	°C
P_D	Power dissipation		
	F package	220	mW
	N package	220	mW

BLOCK DIAGRAM


V_{CC}
1
COMP
1/2 LSB
I_{IN}
6-BIT DAC
I_O
V_{REF} 2
V/I
V_{IN} 3
V/I
A_{GND} 4
D_{GND} 5
CLK 6
CONTROL LOGIC
SAR
DB
16 DB_5
DB
11 DB_0
EOC
10 $\overline{EOC}$
7 $\overline{START}$
8 $\overline{CS}$
9 $\overline{OE}$

6-BIT A/D CONVERTER (PARALLEL OUTPUTS) NE5037

DC ELECTRICAL CHARACTERISTICS

$V_{CC}=5.0V$; $V_{REF}=2.0V$; Clock = 1MHz; $0°C \le T_A \le 70°C$ unless otherwise specified. Typical values are specified at 25°C.

SYMBOL AND PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution		6	6	6	Bits
	Relative accuracy[1,2]			1/4	1/2	LSB
V_{CC}	Positive supply voltage		+4.75	+5.0	+5.50	V
ϵ_{FS}	Full scale gain error[2,3,4]	$V_{REF}=2.0V$, $T_A=25°C$		±1	±2	LSB
ϵ_{ZS}	Zero scale offset error[2]	$V_{REF}=2.0V$, $T_A=25°C$		±1/2	−1/2, +2	LSB
P_{SR}	Power supply rejection Max change in full scale[2]	$V_{REF}=2.0V$ $4.75V \le V_{CC} \le 5.5V$		±1/2	±1	LSB
I_{IN}	Analog input bias current	$0 \le V_{IN} \le 2.5V$		1	10	μA
I_{REF}	Reference bias current	$0 \le V_{REF} \le 2.5V$		1	10	μA
R_{IN}	Analog input resistance		3	30		MΩ
V_{IH}	Logic '1' input voltage		2.0			V
V_{IL}	Logic '0' input voltage				0.8	V
I_{IH}	Logic '1' input current				10	μA
I_{IL}	Logic '0' input current			1	10	μA
I_{OH}	Logic '1' output current[5]	$2.4V \le V_{OH}$	300			μA
I_{OL}	Logic '0' output current[5]	$V_{OL} \le 0.4V$	1.6			mA
I_{OZ}	Three-state leakage current			±0.1	±40	μA
I_{CC}	Positive supply current			18	24	mA

AC ELECTRICAL CHARACTERISTICS

$V_{CC}=5.0V$; $V_{REF}=2.0V$; Clock = 1MHz; $0°C \le T_A \le 70°C$ unless otherwise specified. Typical values are specified at 25°C. (Refer to AC test figures.)

SYMBOL AND PARAMETER		TO	FROM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{MAX}	Maximum clock frequency				1			MHz
t_W	Start pulse width				300			ns
	Minimum positive/negative clock pulse width				300			ns
T_{CONV}	Conversion time						9	Clock cycles
$t_{P\,(OUT\,DATA)}$	Propagation delay[6]	Data out	$\overline{OE}$	$T_A=25°C$, $t_r=t_f \le 20ns$			500	ns
$t_{P\,(OUT\,EOC)}$	Propagation delay[7]	$\overline{EOC}$	Clock	$T_A=25°C$, $t_r=t_f \le 20ns$			800	ns
$t_{P\,(3\text{-}STATE)}$	Propagation delay, 3-state	3-State Data	$\overline{OE}$	$T_A=25°C$, $t_r=t_f \le 20ns$			500	ns

NOTES

1. Relative accuracy is defined as the deviation of the code transition points from the ideal code transition points on a straight line drawn from zero scale to full scale of the device.
2. Specifications given in LSB's refer to the weight of the least significant bit at the 6 bit level which is 1.56% of the full scale voltage.
3. Full scale gain error is the deviation of the full scale code transition point (111110 to 111111) from its ideal value.
4. The analog input voltage (V_{IN}) range is 0V to V_{REF} nominally, with the output remaining at 111111 even though the input may increase from V_{REF} to V_{CC}. (For optimum performance, V_{REF} can be any value from 1.5V to 2.5V.)
5. The data outputs have active pull-ups. The $\overline{EOC}$ line is open collector with a nominal 5kΩ internal pull-up resistor
6. Propagation delay of data outputs is defined as the delay in the data outputs reading their final value after the low going edge of $\overline{OE}$.
7. Propagation delay of $\overline{EOC}$ is defined as the delay in $\overline{EOC}$ going low, following the low going edge of the 9th clock pulse after the start pulse.

CIRCUIT DESCRIPTION

NE5037 is a complete 6-bit, parallel output, microprocessor compatible, A/D converter which incorporates the successive approximation method. The chip includes the internal control logic, the successive approximation register (SAR), 6-bit DAC, comparator and output buffers. An externally generated clock source (max frequency = 1MHz) must be provided to pin 6.

An external reference voltage supplied to pin 2 sets the full scale range of the A/D converter.

The $\overline{CS}$ pin must be at a low level prior to the start of the conversion process. Upon receipt of a $\overline{START}$ pulse the internal control logic resets the SAR. On the first low going edge of the clock pulse, successive approximation conversion commences. Successive bits beginning with the MSB (D5) are supplied to the input of the internal 6-bit current output DAC by the I^2L successive approximation register.

The comparator determines whether the output current of the DAC is greater or less than the input current, converted from the unknown analog input voltage through the V/I converter. If the DAC output is greater, that bit of the DAC is set to '0' and simultaneously the corresponding output buffer goes to '0'. If it is less, that bit stays at '1' and the output buffer also stays at '1'. On successive clock pulses, successive bits of the DAC are tried and the corresponding output buffer represents the bits of the DAC. On the eighth low going edge of the clock pulse (after the receipt of the start pulse). The $\overline{\text{EOC}}$ pin goes low, thereby indicating that the conversion is complete. The output data is now valid. In order to access the result of the conversion, the $\overline{\text{OE}}$ pin must be set to a low level. $\overline{\text{EOC}}$ is reset to a high state when $\overline{\text{OE}}$ is low. When $\overline{\text{OE}}$ is in a '1' state, the output buffers are in a high impedance state.

Refer to Figure 1 for the timing diagram.

TRANSFER CHARACTERISTICS

The ideal transfer characteristic of the NE5037 is shown in Figure 2.

The NE5037 is designed to have a nominal ½ LSB offset so that the code transition points are located ½ LSB on either side of the exact analog inputs for a given code.

Thus the first transition (000000 to 000001) will occur at an input of ½ LSB (15.63mV with a V_{REF} of 2.0V). Subsequent transitions will occur at nominal increments of 1 LSB. The last transition (to full scale—111111) will occur at 62.5 LSB (1.953V at V_{REF} of 2.0V).

LAYOUT PRECAUTIONS

Analog ground (pin 4) and Digital ground (pin 5) are not connected internally and should be connected together as close to the device as possible, for optimum performance. The circuit will operate with as much as ±200mV between the two grounds but some degradation will occur. The leads to the analog inputs should be kept as short as possible to minimize noise pickup. Input bypass capacitors from the analog inputs to ground will eliminate noise pickup. Power supplies should be decoupled with at least 1μF located close to the device to minimize the effects of noise spikes.

The reference input and the analog voltage input must both remain stable during conversion to insure accuracy and proper operation. This can be done by adequately bypassing these inputs and/or keeping the impedance of these inputs at or below 2K-ohms.

TIMING DIAGRAM

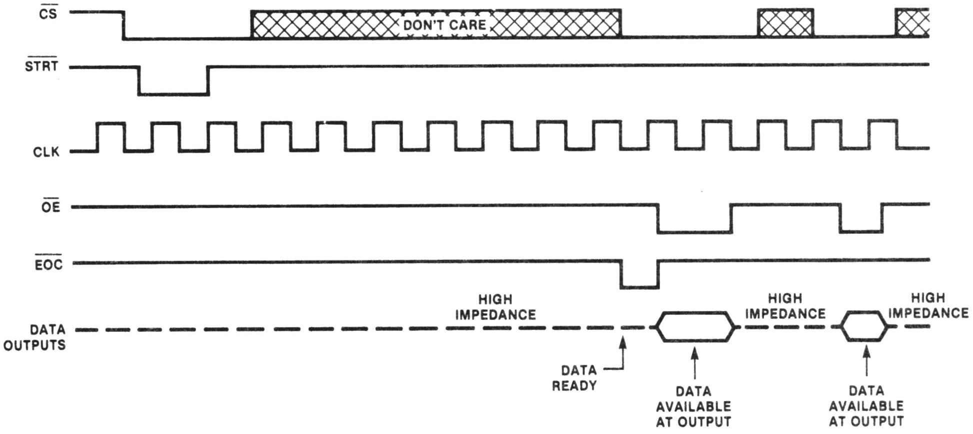


Figure 1

IDEAL TRANSFER CHARACTERISTICS

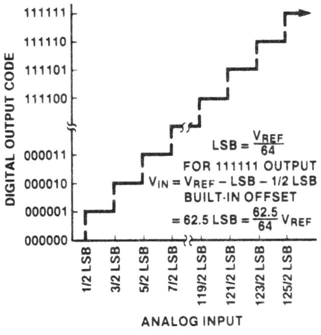
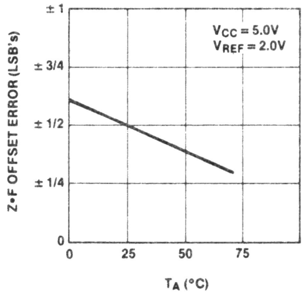


Figure 2

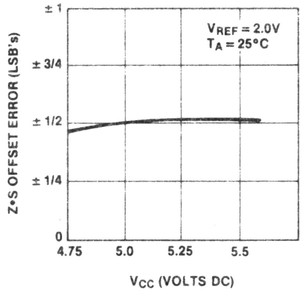
6-BIT A/D CONVERTER (PARALLEL OUTPUTS) NE5037

TYPICAL PERFORMANCE CHARACTERISTICS

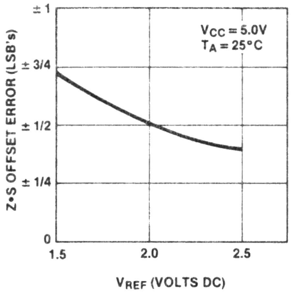
ZERO SCALE OFFSET ERROR vs TEMP



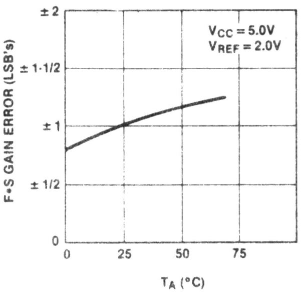
ZERO SCALE OFFSET ERROR vs V_{CC}



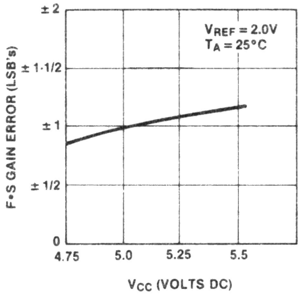
ZERO SCALE OFFSET ERROR vs V_{REF}



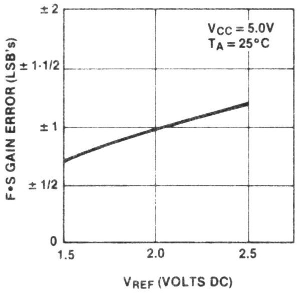
FULL SCALE GAIN ERROR vs TEMP



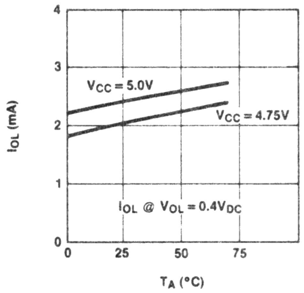
FULL SCALE GAIN ERROR vs V_{CC}



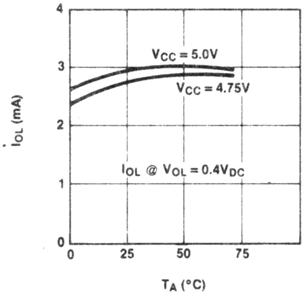
FULL SCALE GAIN ERROR vs V_{REF}



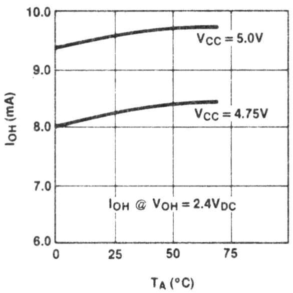
I_{OL} vs TEMP (DATA OUTPUTS)



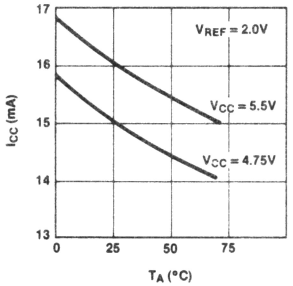
I_{OL} vs TEMP ($\overline{EOC}$)



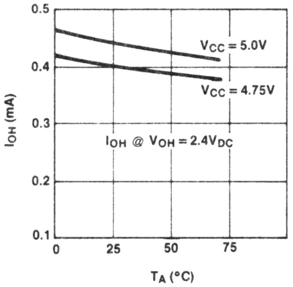
I_{OH} vs TEMP (DATA OUTPUTS)



I_{CC} vs TEMP



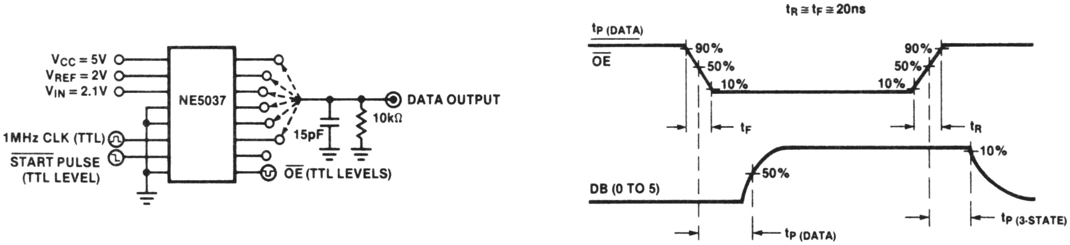
I_{OH} vs TEMP ($\overline{EOC}$)



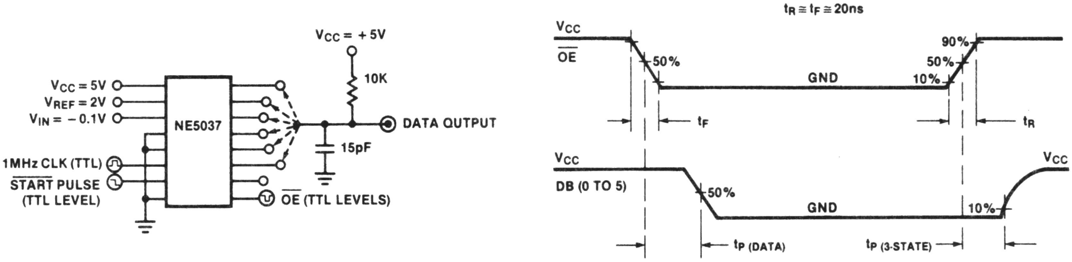
6-BIT A/D CONVERTER (PARALLEL OUTPUTS) NE5037

AC TEST CIRCUITS AND WAVEFORMS

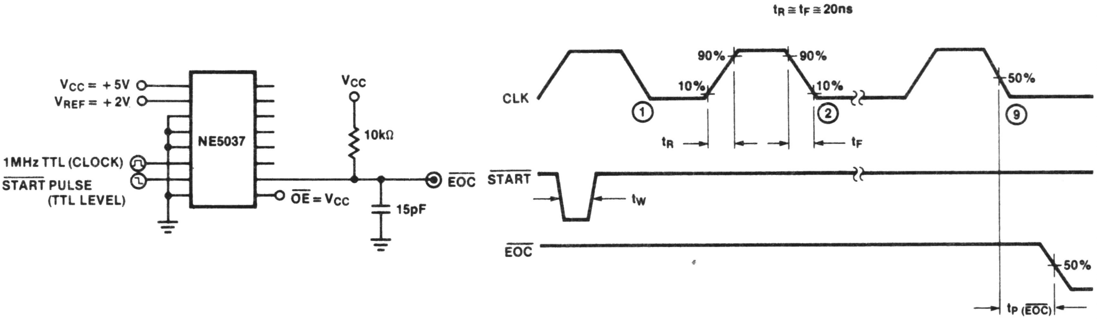
PROPAGATION DELAY TIME $t_{P\,(DATA)}$ AND $t_{P\,(3\text{-}STATE)}$


Vcc = 5V
VREF = 2V
VIN = 2.1V
NE5037
1MHz CLK (TTL)
START PULSE
(TTL LEVEL)
15pF
10kΩ
DATA OUTPUT
OE (TTL LEVELS)
tR ≅ tF ≅ 20ns
tP (DATA)
OE
90%
50%
10%
tF
tR
DB (0 TO 5)
50%
10%
tP (DATA)
tP (3-STATE)

DATA OUTPUT HIGH


Vcc = +5V
10K
Vcc = 5V
VREF = 2V
VIN = −0.1V
NE5037
DATA OUTPUT
15pF
1MHz CLK (TTL)
START PULSE
(TTL LEVEL)
OE (TTL LEVELS)
tR ≅ tF ≅ 20ns
Vcc
OE
50%
GND
90%
50%
10%
tF
tR
Vcc
DB (0 TO 5)
50%
GND
10%
Vcc
tP (DATA)
tP (3-STATE)

PROPAGATION DELAY TIME EOC $t_{P\,(EOC)}$


Vcc = +5V
VREF = +2V
NE5037
1MHz TTL (CLOCK)
START PULSE
(TTL LEVEL)
Vcc
10kΩ
OE = Vcc
15pF
EOC
tR ≅ tF ≅ 20ns
CLK
90%
10%
90%
10%
50%
①
②
⑨
tR
tF
START
tW
EOC
50%
tP (EOC)

APPLICATION

- **0 to 63°C Temperature Sensor**

CIRCUIT DESCRIPTION

The temperature sensor of Figure 3A provides an input to Pin 3 of the NE5037 of 32 millivolts per degree Celsius. This 32mV is the value of one LSB for the NE5037. The LM334 is a three-terminal temperature sensor and provides a current of 1 microamp for each degree Kelvin. The 32K-ohm resistor provides the 32 millivolts for each microamp through it, while the transistor bleeds off 273 microamps of the temperature sensor (LM334) current, lowering the reading by 273 degrees Kelvin, thus converting from Kelvin to Celsius.

To read temperature, conversion is started by sending a momentary low signal to Pin 7 of the NE5037. When Pin 10 of the NE5037 goes low, conversion is complete and a low is applied to Pin 9 of the NE5037 to read data on Pins 11 through 16. Note that this temperature data is in straight binary format.

The controller can be a microprocessor in a temperature control application, or discrete circuitry in a simple temperature reporting application. A temperature reporting (digital thermometer) circuit is shown in Figure 3B. The ROMs or PROMs

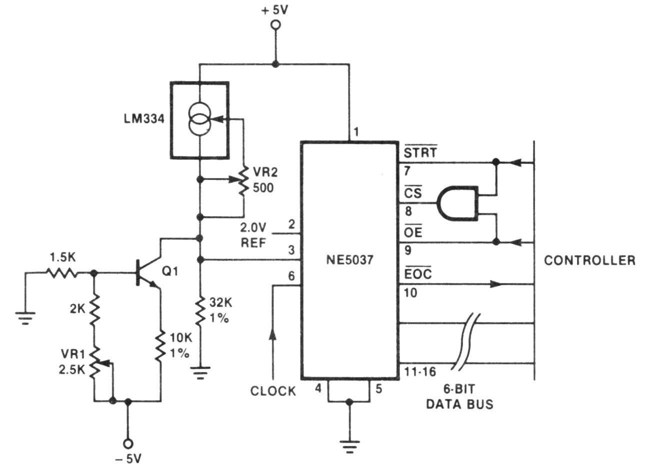

+5V
LM334
VR2
500
1
STRT
7
CS
8
OE
9
EOC
10
2.0V
REF
2
3
6
NE5037
CONTROLLER
1.5K
Q1
2K
VR1
2.5K
10K
1%
32K
1%
CLOCK
4
5
11-16
6-BIT
DATA BUS
-5V

Figure 3A. Temperature Sensor

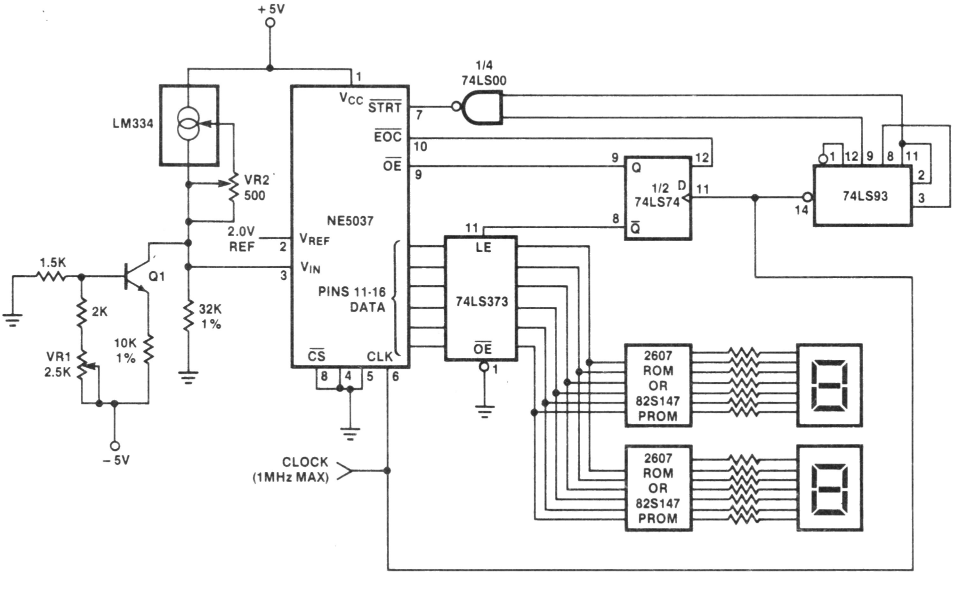

+5V
1
1/4
74LS00
LM334
VCC
STRT
7
EOC
10
OE
9
VR2
500
NE5037
2.0V
REF
2
VREF
3
VIN
PINS 11-16
DATA
CS
CLK
8
4
5
6
1.5K
Q1
2K
10K
1%
VR1
2.5K
32K
1%
-5V
CLOCK
(1MHz MAX)
9
Q
12
1/2
74LS74
D
11
8
Q̄
11
LE
74LS373
OE
1
1
12
9
8
11
2
3
14
74LS93
2607
ROM
OR
82S147
PROM
2607
ROM
OR
82S147
PROM

Figure 3B. Digital Thermometer

must have the correct code for converting the data from the NE5037 (used as address for the ROMs or PROMs) to the appropriate segment driver codes.

The displayed output could easily be converted to degrees Fahrenheit by the controller of Figure 3A or through the (P)ROMs of Figure 3B. When doing this, a third (hundreds) digit (P)ROM and display will, of course, be needed for displaying temperatures above 99°F.

An inexpensive clock can be made from NAND gates or inverters, as shown in Figure 3C.

CIRCUIT ADJUSTMENT

Adjust VR2 for about 1/4 of maximum resistance. With the sensor (LM334) stable at a known temperature near the lower end of the expected range of temperature readings, adjust VR1 for a drop of 2.73 volts across the (10K) emitter resistor of Q1. Set reference voltage at Pin 2 of the NE5037 for 2 volts and adjust VR2 for a digital reading corresponding to the known temperature.

Because high accuracy is not necessary in many applications, this is often all the adjustment necessary and yields an indicated temperature that is within 3 degrees Celsius of actual temperature. Should higher accuracy be required, adjustment of the NE5037 reference voltage at Pin 2 is needed. After performing the above adjustments, bring the sensor temperature to a value near the maximum expected reading (but not above 63 degrees Celsius) and adjust the reference voltage at Pin 2 of the NE5037 for a digital output indication of the known temperature. Then stabilize the sensor again at a temperature near the low end of the expected range of readings and adjust VR1 for a digital indication of that known temperature. This procedure will provide an accuracy of ± 1 degree Celsius.

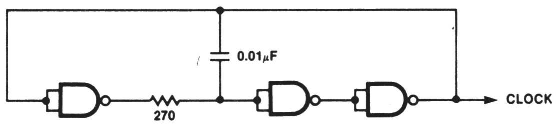


Figure 3C. Simple Clock Circuit

12-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER Am6012

DESCRIPTION

The Am6012 12-Bit multiplying Digital-to-Analog converter provides high speed and 0.025% differential nonlinearity over its full commercial temperature range.

The D/A converter uses a 3-bit segment generator for the MSBs in conjunction with a 9-bit R-2R diffused resistor ladder to provide 12-bit resolution without costly trimming processes. This technique guarantees a very uniform step size (up to ± ½ LSB from the ideal), monotonicity to 12 bits and integral nonlinearity to 0.05% at its differential current outputs.

The dual complementary outputs of the Am6012 increase its versatility, and effectively double the peak-to-peak output swing. Digital inputs, in addition, can be configured to accept all popular logic families.

While the device requires a reference input of 1mA for a 4mA full scale current, operation is nearly independent of power supply voltage shifts. The power supply rejection ratio is ± 0.001%FS/% ΔV. The devices will work from + 5, − 12V to ± 18V rails, with as low as 230mW power consumption typical.

FEATURES

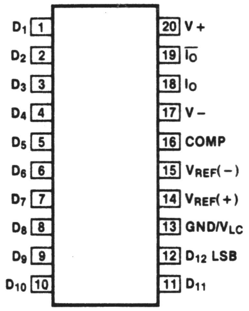
- **12-bit resolution**
- **Accurate to within ± 0.05%**
- **Monotonic over temperature**
- **Fast settling time, 250ns typical**
- **Trimless design for low cost**
- **Differential current outputs**
- **High-speed multiplying capability**
- **Full scale current, 4mA (with 1mA reference)**
- **High output compliance voltage, − 5 to + 10V**
- **Low power consumption, 230mW**

APPLICATIONS

- **CRT displays, computer graphics**
- **Robotics, and machine tools**
- **Automatic test equipment**
- **Programmable power supplies**
- **CAD/CAM systems**
- **Data acquisition and control systems**
- **Analog-to-Digital converter systems**

PIN CONFIGURATION

F PACKAGE



D1 1
D2 2
D3 3
D4 4
D5 5
D6 6
D7 7
D8 8
D9 9
D10 10
20 V+
19 $\overline{I_O}$
18 I_O
17 V−
16 COMP
15 $V_{REF}(-)$
14 $V_{REF}(+)$
13 GND/V_{LC}
12 D_{12} LSB
11 D_{11}

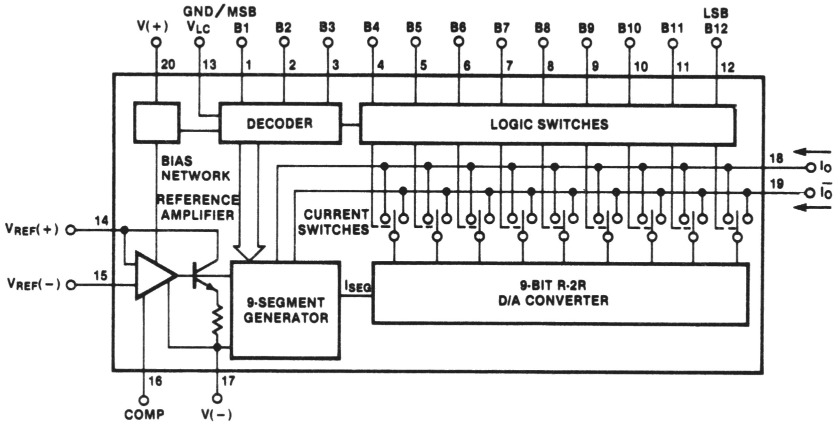
TOP VIEW

ORDER NUMBER
AM6012F

ABSOLUTE MAXIMUM RATINGS

Operating Temperature	
Am6012F	0°C to + 70°C
Storage Temperature	− 65°C to + 150°C
Lead Temperature (Soldering, 60 sec)	300°C
Power Supply Voltage	± 18V
Logic Inputs	− 5V to + 18V
Voltage Across Current Outputs	− 8V to + 12V
Reference Inputs V_{14}, V_{15}	V− to V+
Reference Input Differential Voltage (V_{14} to V_{15})	± 18V
Reference Input Current (I_{14})	1.25mA

BLOCK DIAGRAM



GND/MSB
V(+)
V_{LC}
B1
B2
B3
B4
B5
B6
B7
B8
B9
B10
B11
LSB
B12
20
13
1
2
3
4
5
6
7
8
9
10
11
12
DECODER
LOGIC SWITCHES
BIAS NETWORK
REFERENCE AMPLIFIER
CURRENT SWITCHES
18
I_O
19
$\overline{I_O}$
$V_{REF}(+)$
14
$V_{REF}(-)$
15
9-SEGMENT GENERATOR
I_{SEG}
9-BIT R-2R D/A CONVERTER
16
17
COMP
V(−)

ELECTRICAL CHARACTERISTICS: $V+ = +15V$, $V- = -15V$, $I_{REF} = 1.0mA$, $0°C \leq T_A \leq 70°C$

Parameter	Description	Test Conditions	Am6012F			Units
			Min.	Typ.	Max.	
	Resolution		12			Bits
	Monotonicity		12			Bits
D.N.L.	Differential Nonlinearity	Deviation from ideal step size	—	—	±.025	%FS
			12	—	—	Bits
N.L.	Nonlinearity	Deviation from ideal straight line	—	—	±.05	%FS
I_{FS}	Full Scale Current	$V_{REF} = 10.000V$ $R_{14} - R_{15} = 10.000k\Omega$ $T_A = 25°C$	3.935	3.999	4.063	mA
TCI_{FS}	Full Scale Tempco		—	±10	±40	ppm/°C
				±.001	±.004	%FS/°C
V_{OC}	Output Voltage Compliance	D.N.L. Specification guaranteed over compliance range $R_{OUT} > 10$ megohms typ.	−5	—	+10	Volts
I_{FSS}	Symmetry	$I_{FS} - I_{\overline{FS}}$	—	±0.4	±2.0	µA
I_{ZS}	Zero Scale Current		—	—	0.10	µA
t_S	Settling Time	To ±1/2 LSB, all bits ON or OFF, $T_A = 25°C$	—	.250	500	nsec
t_{PLH} t_{PHL}	Propagation Delay — all bits	50% to 50%	—	25	50	nsec
C_{OUT}	Output Capacitance		—	20	—	pF
V_{IL}	Logic Input Levels Logic "0"		—	—	0.8	Volts
V_{IH}	Logic "1"		2.0	—	—	
I_{IN}	Logic Input Current	$V_{IN} = -5$ to $+18V$	—	—	40	µA
V_{IS}	Logic Input Swing	$V- = -15V$	−5	—	+18	Volts
I_{REF}	Reference Current Range		0.2	1.0	1.1	mA
I_{15}	Reference Bias Current		0	−0.5	−2.0	µA
dI/dt	Reference Input Slew Rate	$R_{14(eq)} = 800\Omega$ CC = 0pF	4.0	8.0	—	mA/µs
$PSSI_{FS+}$	Power Supply Sensitivity	$V+ = +13.5V$ to $+16.5V$, $V- = -15V$	—	±0.0005	±.001	%FS/%
$PSSI_{FS-}$		$V- = -13.5V$ to $-16.5V$, $V+ = +15V$	—	±.00025	±.001	
V+	Power Supply Range	$V_{OUT} = 0V$	4.5	—	18	Volts
V−			−18	—	−10.8	
I+	Power Supply Current	$V+ = +5V$, $V- = -15V$	—	5.7	8.5	mA
I−			—	−13.7	−18.0	
I+		$V+ = +15V$, $V- = -15V$	—	5.7	8.5	
I−			—	−13.7	−18.0	
P_D	Power Dissipation	$V+ = +5V$, $V- = -15V$	—	234	312	mW
		$V+ = +15V$, $V- = -15V$	—	291	397	

12-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER Am6012

CIRCUIT DESCRIPTION

The Am6012 is a 12-bit DAC which uses diffused resistors and requires no trimming to guarantee monotonicity over the temperature range. A segmented DAC design guarantees a more uniform step size over the temperature range than is normally available with trimmed 12-bit converters. The converter features differential high compliance current outputs, wide supply range, and a multiplying reference input.

In many converter applications, uniform step size is more important than conformance to an ideal straight line. Many 12-bit converters are used for high resolution rather than high linearity, since few transducers are more linear than ±0.1%. All classic binarily weighted converters require ±1/2 LSB (±.012%) linearity in order to guarantee monotonicity, which requires very tight resistor matching and tracking. The Am6012 uses conventional bipolar processing to achieve high differential linearity and monotonicity without requiring correspondingly high linearity, or conformance to an ideal straight line.

One design approach which provides monotonicity without requiring high linearity is the MOS switch-resistor string. This circuit is actually a full complement to a current switched R-2R DAC since it is slower, has a voltage output, and if implemented at the 12-bit level would use 4096 low tolerance resistors rather than a minimum number of high tolerance resistors as in the R-2R network. Its lack of speed and density for 12 bits are its drawbacks.

With the segmented DAC approach, the 4096 required output levels are composed of 8 groups of 512 steps each. Each step group is generated by a 9-bit DAC, and each of the segment slopes is determined by one of 8 equal current sources. The resistors which determine monotonicity are in the 9-bit DAC. The major carry of the 9-bit DAC is repeated in each of the 8 segments, and requires eight times lower initial resistor accuracy and tracking to maintain a given differential nonlinearity over temperature.

The operation of the segmented DAC may be visualized by assuming an input code of all zeroes. The first segment current I_O is divided into 512 levels by the 9-bit multiplying DAC and fed to the output, I_{OUT}. As the input code increases, a new segment current is selected for each 512 counts. The previous segment is fed to output I_{OUT} where the new step group is added to it, thus ensuring monotonicity independent of segment resistor values. All higher order segments feed $\overline{I_{OUT}}$.

With the segmented DAC approach, the precision of the 8 main resistors determines linearity only. The influence of each of these resistors on linearity is four times lower than that of the MSB resistor in an R-2R DAC. Hence, assuming the same resistor tolerances for both, the linearity of the segmented approach would actually be higher than that of an R-2R design.

The step generator or 9-bit DAC is composed of a master and a slave ladder. The slave ladder generates the four least significant bits from the remainder of the master ladder by active current splitting utilizing scaled emitters. This saves ladder resistors and greatly reduces the range of emitter scaling required in the 9-bit DAC. All current switches in the step generator are high speed fully differential switches which are capable of switching low currents at high speed. This allows the use of a binary scaled network all the way to the least significant bit which saves power and simplifies the circuitry.

Diffused resistors have advantages over thin film resistors beyond simple economy and bipolar process compatibility. The resistors are fabricated in single crystal rather than amorphous material which gives them better long term stability and tracking and much higher moisture resistance. They are diffused at 1000°C and so are resistant to changes in value due to thermal and chemical causes. Also, no burn-in is required for stability. The contact resistance between aluminum and silicon is more predictable than between aluminum and an amorphous thin film, and no sandwich metals are required to enhance or protect the contact or limit alloying. The initial match between two diffused resistors is similar to that of thin film since both are defined by photomasks and chemical etching. Since the resistors are not trimmed or altered after fabrication, their tracking and long term characteristics are not degraded.

DIFFERENTIAL vs INTEGRAL NONLINEARITY

Integral nonlinearity, for the purposes of the discussion, refers to the "straightness" of the line drawn through the individual response points of a data converter. Differential nonlinearity, on the other hand, refers to the deviation of the spacing of the adjacent points from a 1 LSB ideal spacing. Both may be expressed as either a percentage of full scale output or as fractional LSBs or both. The graphs in Figure 1 define the manner in which these parameters are specified. The left graph shows a portion of the transfer curve of a DAC with 1/2 LSB INL and the (implied) DNL spec of 1LSB. Below this is a graphic representation of the way this would appear on a CRT screen where the Am6012 is used as a display driver. On the right is a portion of the transfer curve of a DAC specified for 2LSB INL with 1/2 LSB DNL specified and the graphic display below it.

One of the characteristics of an R-2R DAC in standard form is that any transition which causes a zero LSB change (i.e. the same output for two different codes) will exhibit the same output each time that transition occurs. The same holds true for transitions causing a 2LSB change. These two problem transitions are allowable for the standard definition of monotonicity and also allow the device to be specified very tightly for INL. The major problem arising from this error type is in A/D converter implementations. Inputs producing the same output are now represented by ambiguous output codes for an identical input. Also, 2LSB gaps can cause large errors at those input levels (assuming 1/2 LSB quantizing levels). It can be seen from the two figures that the DNL specified D/A converter will yield much finer grained data than the INL specified part, thus improving the ability of the A/D to resolve changes in the analog input.

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O + \overline{I_O} = I_{FR}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 18 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 18 and turned on at pin 19. A decreasing logic count increases $\overline{I_O}$ as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FR}; do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 25V above V− and is independent of the positive supply. Negative compliance is +10V above V−.

12-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER Am6012

DIFFERENTIAL LINEARITY COMPARISON

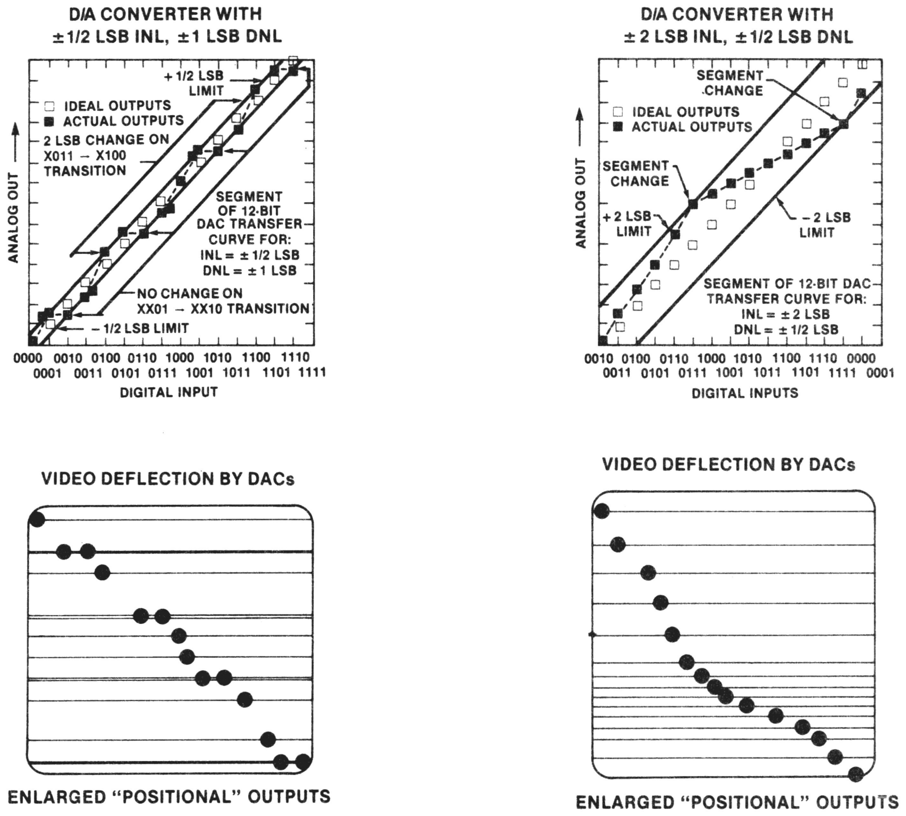


Figure 1

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The Am6012 operates over a wide range of power supply voltages from a total supply of 20V to 36V. When operating with V− supplies of −10V or less, $I_{REF} \leq 1mA$ is recommended. Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at −9V with $I_{REF} = 1mA$ is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be applied to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the Am6012 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be used to insure logic swings, etc. remain between acceptable limits.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the Am6012 are guaranteed to apply over the entire rated operating temperature range. Full scale output current drift is tight, typically ±10ppm/°C, with zero scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R14 should match and track that of the output resistor for minimum overall full scale drift.

SETTLING TIME

The Am6012 is capable of extremely fast settling times, typically 250ns at

$I_{REF} = 1.0mA$. Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 25ns for each of the 12 bits. Settling time to within 1/2 LSB of the LSB is therefore 25ns, with each progressively larger bit taking successively longer. The MSB settles in 250ns, thus determining the overall settling time of 250ns. Settling to 10-bit accuracy requires about 90 to 130ns. The output capacitance of the Am6012 including the package is approximately 20pF; therefore, the output RC time constant dominates settling time if $R_L > 500\Omega$.

Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times, due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 0.5mA, with gradual increases for lower I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve ±2μA, therefore a 2.5kΩ load is needed to provide adequate drive for most oscilloscopes. At I_{REF} values of less than 0.5mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 011111111111 to 100000000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.1% of the final value, and thus settling times may be observed at lower values of I_{REF}.

Am6012 switching transients or "glitches" are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference, and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is independent of input logic states; 0.1μF capacitors at the supply pins provide full transient protection.

APPLICATIONS INFORMATION

REFERENCE AMPLIFIER SETUP

The Am6012 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +1.0mA. The full range output current is a linear function of the reference current and is given by:

$$I_{FR} = \frac{4095}{4096} \times 4 \times (I_{REF}) = 3.999\ I_{REF},$$

where $I_{REF} = I_{14}$

In positive reference applications, an external positive reference voltage forces current through R14 into the $V_{REF(+)}$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 15. Reference current flows from ground through R14 into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R15 (nominally equal to R14) is used to cancel bias current errors. (Figure 2a)

Bipolar references may be accommodated by offsetting V_{REF} or pin 15. The negative common-mode range of the reference amplifier is given by: $V_{CM-} = V-$ *plus $(I_{REF} \times 3k\Omega)$ plus 1.8V. The positive common-mode range is V+ less 1.23V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R14 should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full scale trimming may be accomplished by adjusting the value of R14, or by using a potentiometer for R14.

MULTIPLYING OPERATION

The Am6012 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 1mA to 1μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 1.0mA.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V−. The value of this capacitor depends on the impedance presented to pin 14. For R14 values of 1.0, 2.5 and 5.0kΩ; minimum values of C_C are 5, 12 and 25pF. Larger values of R14 require proportionately increased values of C_C for proper phase margin. (See Figure 2b)

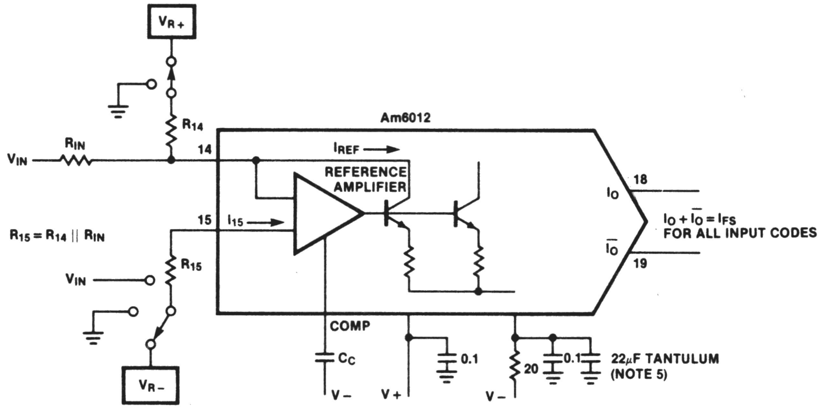
For fastest response to a pulse, low values of R14 enabling small C_C values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For $R14 = 1k\Omega$ and $C_C = 5pF$, the reference amplifier slews at 4mA/ms enabling a transition from $I_{REF} = 0$ to $I_{REF} = 1mA$ in 250ns.

Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme. This technique provides lowest full scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff $(I_{REF} = 0)$ condition. Full scale transition (0 to 1mA) occurs in 62.5ns when the equivalent impedance at pin 14 is 800Ω and $C_C = 0$. This yields a reference slew rate of 8mA/μs which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

The Am6012 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 40μA logic input current, and completely adjustable logic threshold voltage. For V− = −15V, the logic inputs may swing between −5 and +10V. This enables direct interface with +15V CMOS logic, even when the Am6012 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by: V− plus $(I_{REF} \times 3k\Omega)$ plus 1.8V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 13, V_{LC}). For TTL interface, simply ground pin 13. When interfacing ECL, an $I_{REF} \leq 1mA$ is recommended. For interfacing other logic families, see block titled "Interfacing With Various Logic Families." For general setup of the logic control circuit, it should be noted that pin 13 will sink 1.1mA typical, external circuitry should be designed to accommodate this current (Figure 3).

REFERENCE AMPLIFIER BIASING


V_{R+}
R_{14}
Am6012
R_{IN}
V_{IN}
14
I_{REF}
REFERENCE AMPLIFIER
18
I_O
$I_O + \overline{I_O} = I_{FS}$
FOR ALL INPUT CODES
15
I_{15}
$R_{15} = R_{14} \parallel R_{IN}$
R_{15}
V_{IN}
$\overline{I_O}$
19
V_{R-}
COMP
C_C
V−
V+
0.1
20
0.1
22µF TANTULUM
(NOTE 5)

Reference Configuration	R_{14}	R_{15}	R_{IN}	C_C	I_{REF}
Positive Reference	V_{R+}	0V	N/C	.01µF	V_{R+}/R_{14}
Negative Reference	0V	V_{R-}	N/C	.01µF	$-V_{R-}/R_{14}$
Lo Impedance Bipolar Reference	V_{R+}	0V	V_{IN}	(Note 1)	$(V_{R+}/R_{14}) + (V_{IN}/R_{IN})$ (Note 2)
Hi Impedance Bipolar Reference	V_{R+}	V_{IN}	N/C	(Note 1)	$(V_{R+} - V_{IN})/R_{14}$ (Note 3)
Pulsed Reference (Note 4)	V_{R+}	0V	V_{IN}	No Cap	$(V_{R+}/R_{14}) + (V_{IN}/R_{IN})$

Notes:

1. The compensation capacitor is a function of the impedance seen at the $+V_{REF}$ input and must be at least 5pF × $R_{14(eq)}$ in kΩ. For $R_{14} < 800\Omega$ no capacitor is necessary.
2. For negative values of V_{IN}, V_{R+}/R_{14} must be greater than $-V_{IN}$ Max/R_{IN} so that the amplifier is not turned off.
3. For positive values of V_{IN}, V_{R+} must be greater than V_{IN} Max so the amplifier is not turned off.
4. For pulsed operation, V_{R+} provides a DC offset and may be set to zero in some cases. The impedance at pin 14 should be 800Ω or less.
5. For optimum settling time, decouple V− with 20Ω and bypass with 22µF tantulum capacitor.
6. Reference current and reference resistor — there is a 1 to 4 scale factor between the reference current (I_{REF}) and the full scale output current (I_{FS}). If $V_{REF} = +10V$ and $I_{FS} = 4mA$, the value of the R_{14} is:

$$R_{14} = \frac{4 \times 10 \text{ Volt}}{4\text{mA}} = 10\text{k}\Omega \qquad R_{14} = R_{15}$$

Figure 2a

MINIMUM SIZE COMPENSATION CAPACITOR ($I_{FS} = 4mA$, $I_{REF} = 1.0mA$)

$R_{14(EQ)}$(kΩ)	C_C(pF)
10	50
5	25
2	10
1	5
.5	0

Note: A 0.01µF capacitor is recommended for fixed reference operation.

REFERENCE AMPLIFIER FREQUENCY RESPONSE

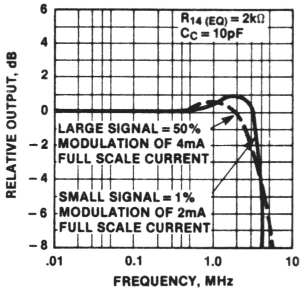
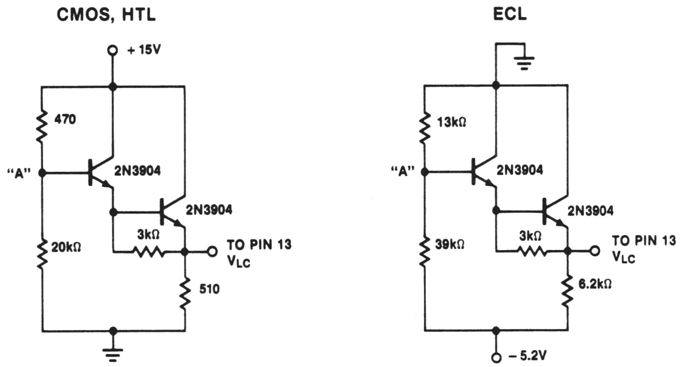


Figure 2b

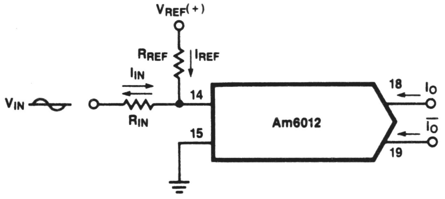
INTERFACING CIRCUITS FOR ECL, CMOS, HTL LOGIC INPUTS


CMOS, HTL
+15V
470
"A"
2N3904
2N3904
3kΩ
20kΩ
TO PIN 13
V_{LC}
510
ECL
13kΩ
"A"
2N3904
2N3904
3kΩ
39kΩ
TO PIN 13
V_{LC}
6.2kΩ
−5.2V

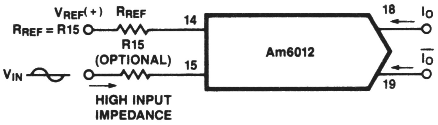
NOTES:
1. Set the voltage "A" to the desired logic input switching threshold.
2. Allowable range of logic threshold is typically −5V to +13.5V when operating the DAC on ± 15V supplies.

Figure 3

ACCOMMODATING BIPOLAR REFERENCE

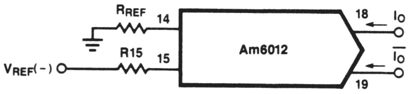

$V_{REF}(+)$
R_{REF}
I_{REF}
I_{IN}
V_{IN}
R_{IN}
14
15
Am6012
18
I_O
$\overline{I_O}$
19

I_{REF} > PEAK NEGATIVE SWING OF I_{IN}


$V_{REF}(+)$
R_{REF}
R_{REF} = R15
R15
(OPTIONAL)
V_{IN}
HIGH INPUT IMPEDANCE
14
15
Am6012
18
I_O
$\overline{I_O}$
19

$V_{REF}(+)$ MUST BE ABOVE PEAK POSITIVE SWING OF V_{IN}

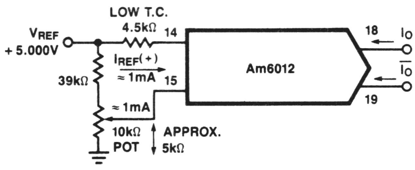
BASIC NEGATIVE REFERENCE OPERATION


R_{REF}
14
R15
15
$V_{REF}(-)$
Am6012
18
I_O
$\overline{I_O}$
19

$$I_{FS} \approx \frac{V_{REF}(-)}{R_{REF}} \times 4$$

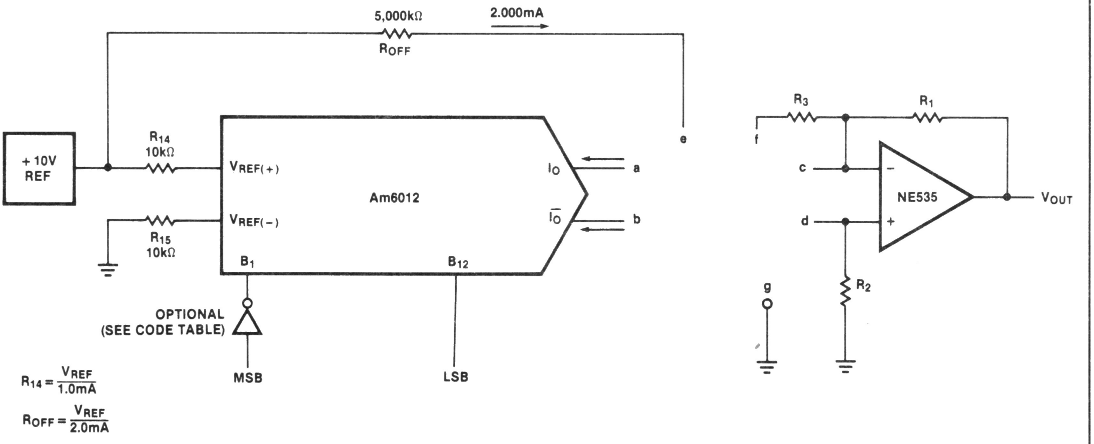
NOTE:
R_{REF} SETS I_{FS}; R15 IS FOR A BIAS CURRENT CANCELLATION.

RECOMMENDED FULL-SCALE ADJUSTMENT CIRCUIT


LOW T.C.
4.5kΩ
V_{REF}
+5.000V
14
$I_{REF}(+)$
≈ 1mA
15
39kΩ
≈ 1mA
10kΩ POT
APPROX. 5kΩ
Am6012
18
I_O
$\overline{I_O}$
19

APPLICATION CIRCUITS

Am6012 LOGIC INPUTS



$R_{14} = \frac{V_{REF}}{1.0mA}$

$R_{OFF} = \frac{V_{REF}}{2.0mA}$

	Code Format	Connections	Output Scale	MSB											LSB	I_0 (mA)	$\overline{I_0}$ (mA)	V_{OUT}
				B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12			
Unipolar	Straight binary; one polarity with true input code, true zero output.	a-c	Positive full scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9976
		b-g	Positive full scale — LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9951
		R1 = R2 = 2.5K	Zero scale	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	.0000
	Complementary binary; one polarity with complementary input code, true zero output.	a-g	Positive full scale	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	9.9976
		b-c	Positive full scale — LSB	0	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	9.9951
		R1 = R2 = 2.5K	Zero scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	.0000
Symmetrical Offset	Straight offset binary; offset half scale, symmetrical about zero, no true zero output.	a-c	Positive full scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9976
		b-d	Positive full scale — LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9927
		f-g	(+) Zero scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.0024
		R1 = R3 = 2.5K	(−) Zero scale	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−.0024
		R2 = 1.25K	Negative full scale — LSB	0	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	−9.9927
			Negative full scale	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	−9.9976
	1's complement; offset half scale, symmetrical about zero, no true zero output, MSB complemented (need inverter at B1).	a-c	Positive full scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9976
		b-d	Positive full scale — LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9927
		f-g	(+) Zero scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.0024
		R1 = R3 = 2.5K	(−) Zero scale	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−.0024
		R2 = 1.25K	Negative full scale — LSB	1	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	−9.9927
			Negative full scale	1	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	−9.9976
Offset with True Zero	Offset binary; offset half scale, true zero output.	e-a-c	Positive full scale	1	1	1	1	1	1	1	1	1	1	1	1	3.999	.000	9.9951
		b-g	Positive full scale — LSB	1	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9902
		R1 = R2 = 5K	+LSB	1	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	.0049
			Zero Scale	1	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.000
			−LSB	0	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−.0049
			Negative full scale + LSB	0	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	−9.9951
			Negative full scale	0	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	−10.000
	2's complement; offset half scale, true zero output, MSB complemented (need inverter at B1).	e-a-c	Positive full scale	0	1	1	1	1	1	1	1	1	1	1	1	3.999	.006	9.9951
		b-g	Positive full scale — LSB	0	1	1	1	1	1	1	1	1	1	1	0	3.998	.001	9.9902
		R1 = R2 = 5K	+1 LSB	0	0	0	0	0	0	0	0	0	0	0	1	2.001	1.998	.0049
			Zero scale	0	0	0	0	0	0	0	0	0	0	0	0	2.000	1.999	.000
			−1 LSB	1	1	1	1	1	1	1	1	1	1	1	1	1.999	2.000	−0.049
			Negative full scale + LSB	1	0	0	0	0	0	0	0	0	0	0	1	.001	3.998	−9.9951
			Negative full scale	1	0	0	0	0	0	0	0	0	0	0	0	.000	3.999	−10.000

Figure 4

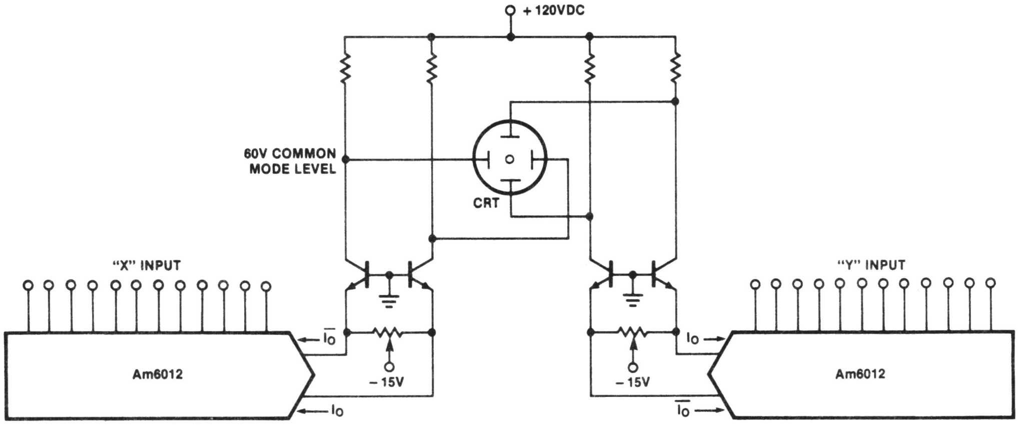
ADDITIONAL CODE MODIFICATIONS

1. Any of the offset binary codes may be complemented by reversing the output terminal pair.

12-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER Am6012

APPLICATION CIRCUITS

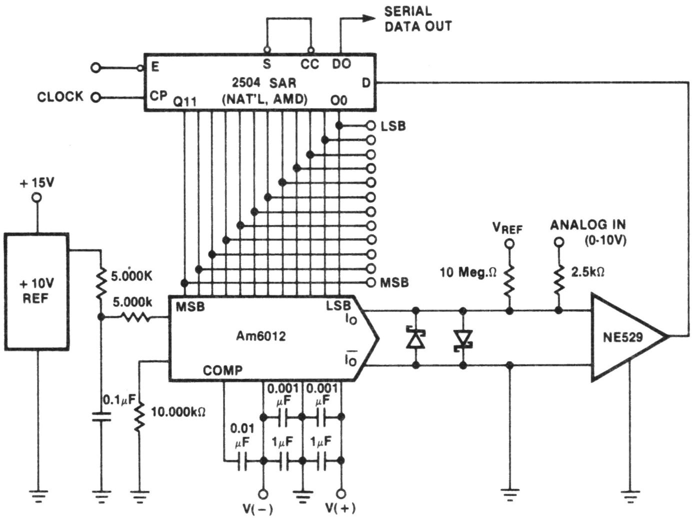
CRT DISPLAY DRIVER

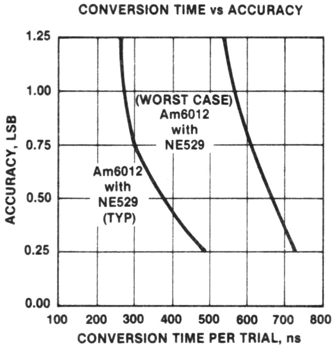

+120VDC
60V COMMON MODE LEVEL
CRT
"X" INPUT
"Y" INPUT
Am6012
Am6012
Io
Io
Io
Io
−15V
−15V

NOTES: 1. FULL DIFFERENTIAL DRIVE LOWERS POWER SUPPLY VOLTAGE.
2. ELIMINATES INVERTING AMPLIFIERS AND TRANSFORMERS.
3. INDEPENDENT BEAM CENTERING CONTROLS.

Figure 5

12-BIT HIGH-SPEED A/D CONVERTER


SERIAL DATA OUT
E
S
CC
DO
2504 SAR (NAT'L, AMD)
CP
Q11
O0
D
CLOCK
LSB
MSB
+15V
+10V REF
5.000K
5.000k
MSB
LSB
Am6012
Io
Io
COMP
0.1μF
10.000kΩ
0.001 μF
0.001 μF
0.01 μF
1μF
1μF
V(−)
V(+)
VREF
ANALOG IN (0-10V)
10 Meg.Ω
2.5kΩ
NE529

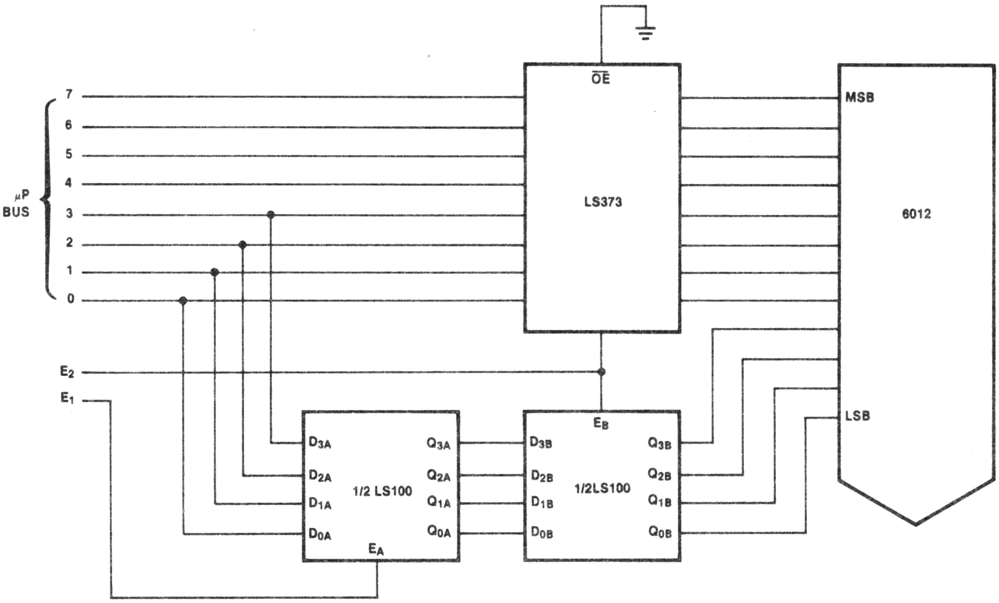


CONVERSION TIME (ns)	TYP	WORST CASE
SAR	33	55
NE529	100	150
TOTAL	383ns	705ns
× 13	5.0μs	9.1μs

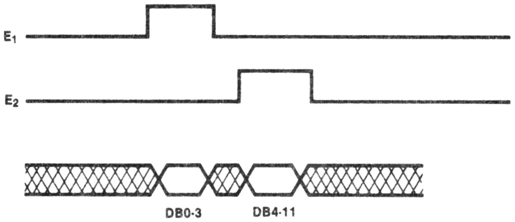
Figure 6

APPLICATION CIRCUITS

INTERFACE WITH 8-BIT MICROPROCESSOR BUS


$\overline{OE}$
μP BUS
7
6
5
4
3
2
1
0
LS373
MSB
6012
LSB
E2
E1
D3A
D2A
D1A
D0A
1/2 LS100
Q3A
Q2A
Q1A
Q0A
EA
EB
D3B
D2B
D1B
D0B
1/2LS100
Q3B
Q2B
Q1B
Q0B

TIMING SEQUENCE


E1
E2
DB0-3
DB4-11

DATA REMAINS ON INPUTS OF DAC UNTIL UPDATED BY E2 PULSE. TIMING WILL DEPEND ON PROCESSOR USED.

Figure 7

8-BIT HIGH SPEED MULTIPLYING D/A CONVERTER

DAC-08 SERIES

FORMERLY: NE5007/5008-F,N
SE5008-F

DESCRIPTION

The DAC-08 series of 8-bit monolithic multiplying Digital-to-Analog Converters provide very high speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 70ns settling times with very low glitch and at low power consumption. Monotonic multiplying performance is attained over a wide 20 to 1 reference current range. Matching to within 1 LSB between reference and full scale currents eliminates the need for full scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

Dual complementary outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. True high voltage compliance outputs allow direct output voltage conversion and eliminate output op amps in many applications.

All DAC-08 series models guarantee full 8-bit monotonicity and linearities as tight as 0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±4.5V to ±18V power supply range, with 37mW power consumption attainable at ±5V supplies.

The compact size and low power consumption make the DAC-08 attractive for portable and military aerospace applications.

FEATURES

- **Fast settling output current—70ns**
- **Full scale current prematched to ±1 LSB**
- **Direct interface to TTL, CMOS, ECL, HTL, PMOS**
- **Relative accuracy to 0.1% maximum over temperature range**
- **High output compliance −10V to +18V**
- **True and complemented outputs**
- **Wide range multiplying capability**
- **Low FS current drift—±10ppm/°C**
- **Wide power supply range—±4.5V to ±18V**
- **Low power consumption—37mW at ±5V**

APPLICATIONS

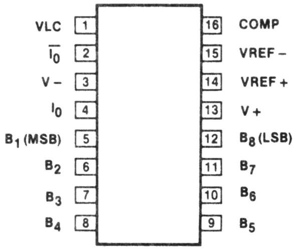
- **8-bit, 1μs A-to-D converters**
- **Servo-motor and pen drivers**
- **Waveform generators**
- **Audio encoders and attenuators**
- **Analog meter drivers**
- **Programmable power supplies**
- **CRT display drivers**
- **High speed modems**
- **Other applications where low cost, high speed and complete input/output versatility are required**
- **Programmable gain and attentuation**
- **Analog-Digital Multiplication**
- **Stepping motor drive**

ORDERING INFORMATION

RELATIVE ACCURACY	0 to 70°C	−55 to 125°C
0.39% FS	DAC-08CN	
	DAC-08CF	
0.19% FS	DAC-08EN	
	DAC-08EF	DAC-08F
	DAC-08ED	
0.1% FS	DAC-08HF	DAC-08AF
	DAC-08HN	

PIN CONFIGURATION

F,N PACKAGE

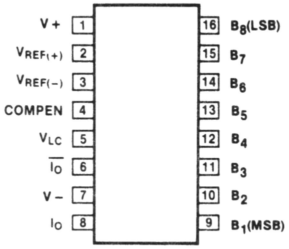


TOP VIEW

ORDER NUMBER

DAC-08AF	SE5009F
DAC-08F	SE5008F
DAC-08HF,N	NE5009F,N
DAC-08CF,N	NE5007F,N

D³ PACKAGE



TOP VIEW

ORDER NUMBER

DAC-08ED

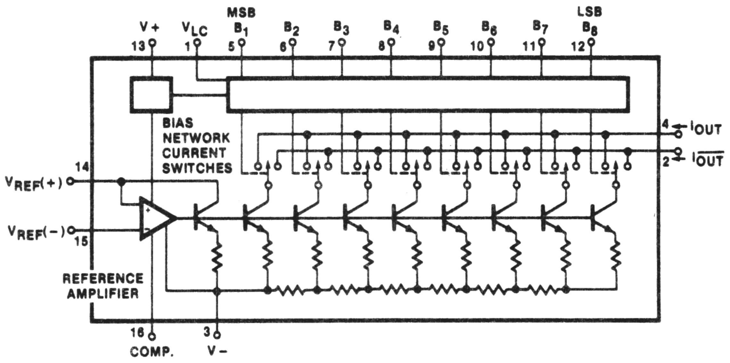
DAC-08 ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
	Power Supply Voltage, V+ to V−	36	V
V_5-V_{12}	Digital Input Voltage	V− to V− plus 36V	
V_{LC}	Logic Threshold Control	V− to V+	
V_0	Applied Output Voltage	V− to +18	V
I_{14}	Reference Current	5.0	mA
V_{14}, V_{15}	Reference Amplifier Inputs	V_{EE} to V_{CC}	
P_D	Power Dissipation (Package Limitation)		
	Ceramic Package	1000	mW
	Plastic Package	800	mW
	Lead Soldering Temperature (60 sec)	300	°C
T_A	Operating Temperature Range		
	DAC-08, DAC-08A	−55 to +125	°C
	DAC-08C, E, H	0 to +75	°C
T_{STG}	Storage Temperature Range	−65 to +150	°C

NOTES:
1. SOL - Released in Large SO package only.
2. SOL and non-standard pinout.
3. SO and non-standard pinouts.

8-BIT HIGH SPEED MULTIPLYING D/A CONVERTER DAC-08 SERIES

BLOCK DIAGRAM


MSB
LSB
V+
VLC
B1
B2
B3
B4
B5
B6
B7
B8
13
1
5
6
7
8
9
10
11
12
BIAS
NETWORK
CURRENT
SWITCHES
4
IOUT
2
$\overline{\text{IOUT}}$
14
VREF(+)
VREF(−)
15
REFERENCE
AMPLIFIER
16
COMP.
3
V−

TEST CIRCUIT

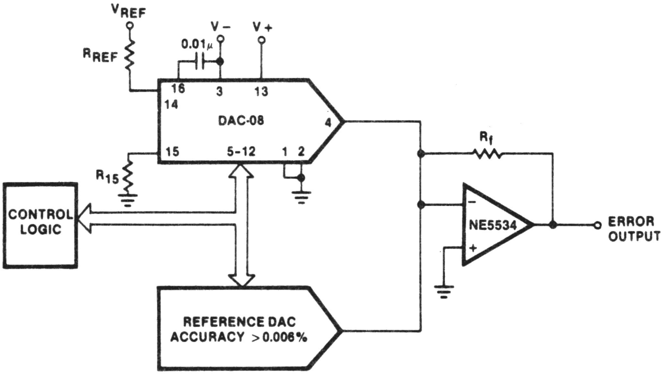

VREF
RREF
V−
V+
0.01µ
16
3
13
14
DAC-08
4
15
5-12
1 2
R15
Rf
NE5534
ERROR
OUTPUT
CONTROL
LOGIC
REFERENCE DAC
ACCURACY >0.006%

Figure 1. Relative Accuracy Test Circuit

TEST CIRCUITS (Cont'd)

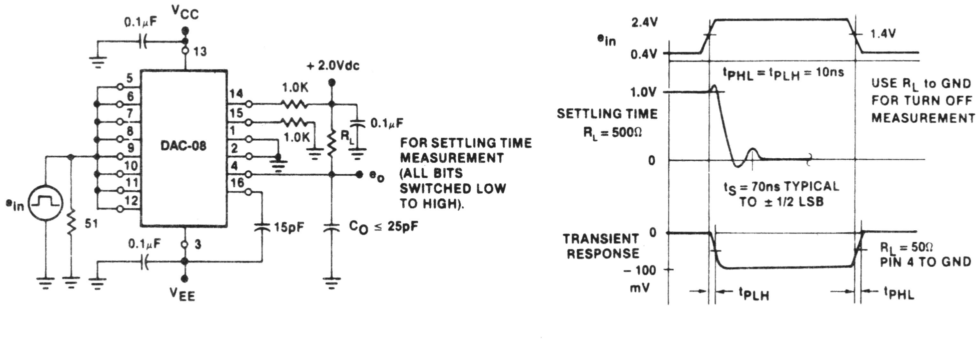

0.1μF
VCC
13
5
6
7
8
9
10
11
12
DAC-08
14
15
1
2
4
16
+2.0Vdc
1.0K
1.0K
0.1μF
RL
FOR SETTLING TIME MEASUREMENT (ALL BITS SWITCHED LOW TO HIGH).
eo
ein
51
0.1μF
3
15pF
CO ≤ 25pF
VEE
2.4V
ein
0.4V
1.4V
tPHL = tPLH = 10ns
USE RL to GND FOR TURN OFF MEASUREMENT
1.0V
SETTLING TIME
RL = 500Ω
0
tS = 70ns TYPICAL TO ± 1/2 LSB
TRANSIENT RESPONSE
0
−100 mV
RL = 50Ω PIN 4 TO GND
tPLH
tPHL

Figure 2. Transient Response and Settling Time

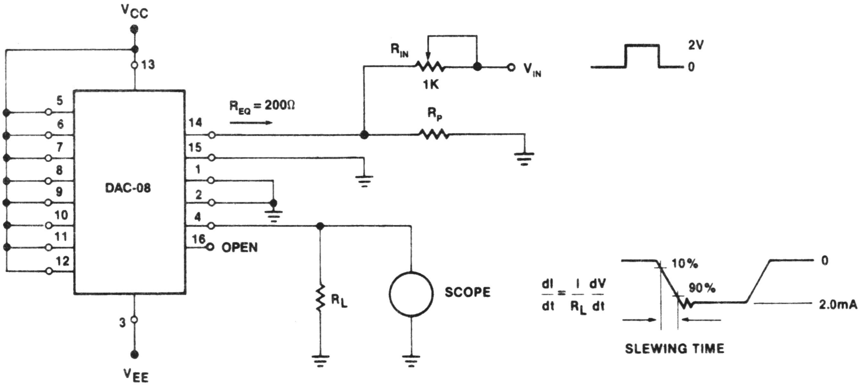
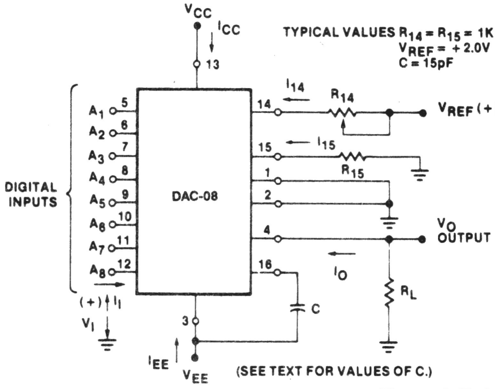

VCC
13
5
6
7
8
9
10
11
12
DAC-08
14
15
1
2
4
16 OPEN
3
VEE
REQ = 200Ω
RIN
1K
VIN
RP
RL
SCOPE
2V
0
dI/dt = 1/RL dV/dt
10%
90%
0
2.0mA
SLEWING TIME

Figure 3. Reference Current Slew Rate Measurement


VCC
ICC
13
TYPICAL VALUES R14 = R15 = 1K
VREF = +2.0V
C = 15pF
DIGITAL INPUTS
A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
A8 12
DAC-08
I14
R14
14
VREF (+)
15
I15
R15
1
2
4
16
VO OUTPUT
IO
RL
C
(+) II
VI
3
IEE
VEE
(SEE TEXT FOR VALUES OF C.)

V_I AND I_I APPLY TO INPUTS A_1 THROUGH A_8

THE RESISTOR TIED TO PIN 15 IS TO TEMPERATURE COMPENSATE THE BIAS CURRENT AND MAY NOT BE NECESSARY FOR ALL APPLICATIONS.

$$I_O = K\left\{\frac{A_1}{2}+\frac{A_2}{4}+\frac{A_3}{8}+\frac{A_4}{16}+\frac{A_5}{32}+\frac{A_6}{64}+\frac{A_7}{128}+\frac{A_8}{256}\right\}$$

where $K \cong \frac{V_{REF}}{R_{14}}$

and A_N = "1" IF A_N IS AT HIGH LEVEL
A_N = "0" IF A_N IS AT LOW LEVEL

Figure 4. Notation Definitions

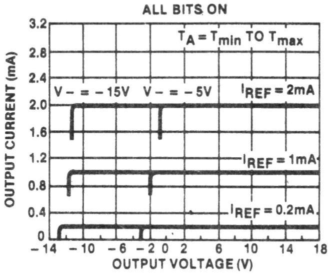
8-BIT HIGH SPEED MULTIPLYING D/A CONVERTER DAC-08 SERIES

ELECTRICAL CHARACTERISTICS Pin 3 must be at least 3V more negative than the potential to which R_{15} is returned. $V_{CC} = \pm 15V$, $I_{REF} = 2.0mA$, Output characteristics refer to both IOUT and IOUT unless otherwise noted. DAC-08C, E, H: $T_A = 0°C$ to $70°C$. DAC-08/08A: $T_A = -55°C$ to $125°C$.

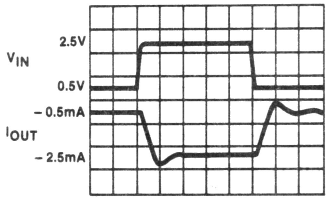
PARAMETER		TEST CONDITIONS	DAC-08C			DAC-08E DAC-08			DAC-08H DAC-08A			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	8	8	8	Bits
	Monotonicity*		8	8	8	8	8	8	8	8	8	Bits
	Relative accuracy	Over temperature range			±0.39			±0.19			± 0.1	.%FS
	Differential nonlinearity				±0.39			±0.19			±0.19	%FS
t_s	Settling time	To ±1/2 LSB, all bits switched on or off, $T_A = 0°C$		70	135		70	135		70	135	ns
t_{PLH} t_{PHL}	Propagation delay Low-to-high High-to-low	T_A=25°C, each bit. All bits switched		35	60		35	60		35	60	ns
TCI_{FS}	Full scale tempco			±10			±10			±10	± 50	ppm/°C
V_{OC}	Output voltage compliance	Full scale current change <½ LSB	-10		+18	-10		+18	-10		+18	V
I_{FS4}	Full scale current	V_{REF}=10.000V, R_{14}, R_{15}=5.000kΩ,	1.94	1.99	2.04	1.94	1.99	2.04	1.984	1.992	2.000	mA
I_{FSS}	Full scale symmetry	$I_{FS4}-I_{FS2}$		±2.0	±16		±1.0	±8.0		±1.0	± 4.0	μA
I_{ZS}	Zero scale current			0.2	4.0		0.2	2.0		0.2	1.0	μA
I_{FSR}	Full scale output current range	R_{14} R_{15} = 5.000kΩ V_{REF} = + 15.0V, V– = – 10V V_{REF} = + 25.0V, V– = –12V	2.1 4.2			2.1 4.2			2.1 4.2			mA
	Logic input levels											V
V_{IL}	Low	V_{LC}=0V			0.8			0.8			0.8	
V_{IH}	High		2.0			2.0			2.0			
	Logic input current	V_{LC}=0V										μA
I_{IL}	Low	V_{IN}=-10V to +0.8V		-2.0	-10		-2.0	-10		-2.0	-10	
I_{IH}	High	V_{IN}=2.0V to 18V		0.002	10		0.002	10		0.002	10	
V_{IS}	Logic input swing	V–=-15V	-10		+18	-10		+18	-10		+18	V
V_{THR}	Logic threshold range	V_S=±15V	-10		+13.5	-10		+13.5	-10		+13.5	V
I_{15}	Reference bias current			-1.0	-3.0		-1.0	-3.0		-1.0	-3.0	μA
dI/dt	Reference input slew rate		4.0	8.0		4.0	8.0		4.0	8.0		mA/μs
	Power supply sensitivity	I_{REF}=1mA										%FS/%VS
$PSSI_{FS+}$	Positive	V+=4.5 to 5.5V, V–=-15V; V+=13.5 to 16.5V, V–=-15V		0.0003	0.01		0.0003	0.01		0.0003	0.01	
$PSSI_{FS-}$	Negative	V–=-4.5 to -5.5V, V+=+15V; V–=-13.5 to -16.5, V+=+15V		0.002	0.01		0.002	0.01		0.002	0.01	
	Power supply current											mA
I+	Positive	V_S=±5V, IREF=1.0mA		3.1	3.8		3.1	3.8		3.1	3.8	
I-	Negative			-4.3	-5.8		-4.3	-5.8		-4.3	-5.8	
I+	Positive	V_S=+5V, -15V, I_{REF}=2.0mA		3.1	3.8		3.1	3.8		3.1	3.8	
I-	Negative			– 7.1	-7.8		– 7.1	-7.8		– 7.1	-7.8	
I+	Positive	V_S=±15V, I_{REF}=2.0mA		3.2	3.8		3.2	3.8		3.2	3.8	
I-	Negative			– 7.2	-7.8		– 7.2	-7.8		– 7.2	-7.8	
P_D	Power dissipation	±5V, I_{REF}=1.0mA		37	48		37	48		37	48	mW
		+5V, -15V, I_{REF}=2.0mA		122	136		122	136		122	136	
		±15V, I_{REF}=2.0mA		156	174		156	174		156	174	

TYPICAL PERFORMANCE CHARACTERISTICS

OUTPUT CURRENT vs OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)



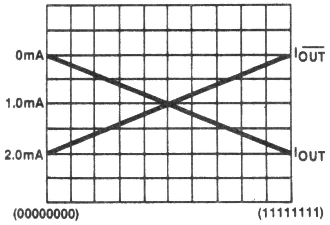
FAST PULSED REFERENCE OPERATION



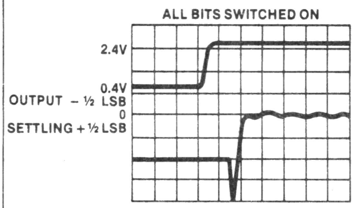
200ns/division

R_{EQ} = 200Ω, R_L = 100Ω, CC = 0

TRUE AND COMPLEMENTARY OUTPUT OPERATION



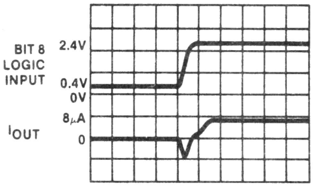
FULL SCALE SETTLING TIME



50ns/DIVISION

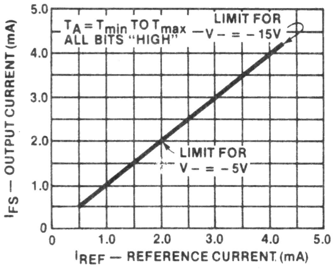
I_{FS} = 2mA, R_L = 1kΩ ½ LSB = 4μA

LSB SWITCHING

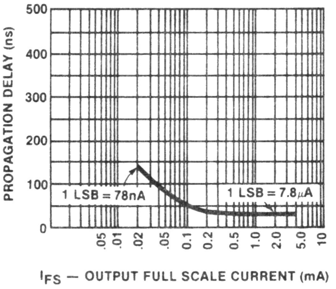


50ns/division

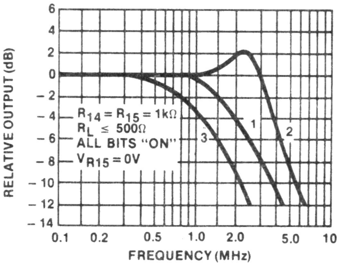
FULL SCALE CURRENT vs REFERENCE CURRENT



LSB PROPAGATION DELAY vs IFS



REFERENCE INPUT FREQUENCY RESPONSE



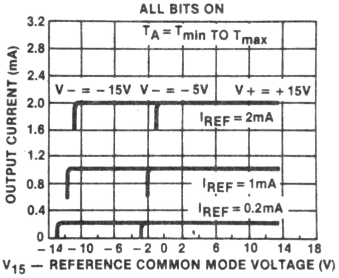
Curve 1: CC = 15pF, V_{IN} = 2.0V p-p centered at + 1.0V.

Curve 2: CC = 15pF, V_{IN} = 50mV p-p centered at + 200mV.

Curve 3: CC = 0pF, V_{IN} = 100mV p-p centered at 0V and applied thru 50Ω connected to pin 14. + 2.0V applied to R_{14}.

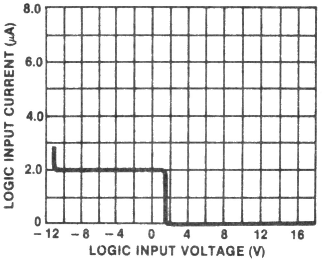
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

REFERENCE AMP COMMON MODE RANGE

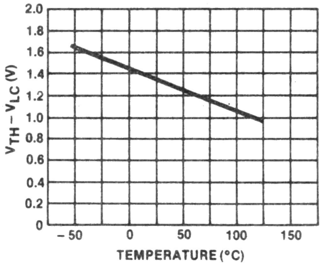


Positive common mode range is always (V+) − 1.5V

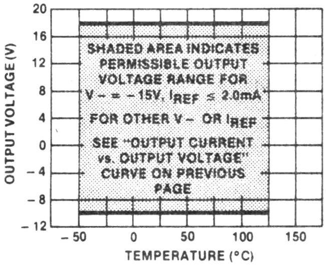
LOGIC INPUT CURRENT vs INPUT VOLTAGE



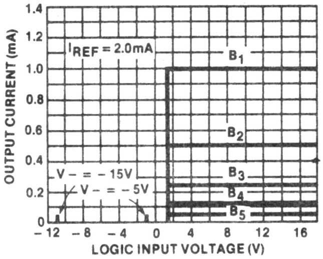
$V_{TH} - V_{LC}$ vs TEMPERATURE



OUTPUT VOLTAGE COMPLIANCE vs TEMPERATURE



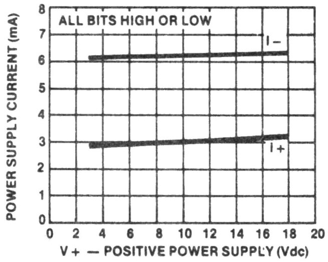
BIT TRANSFER CHARACTERISTICS



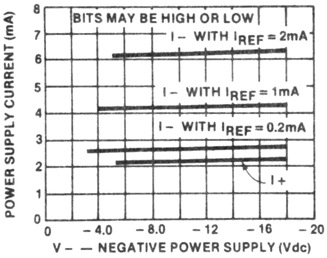
NOTE

B_1 through B_8 have identical transfer characteristics. Bits are fully switched, with less than ½ LSB error, at less than ±100mV from actual threshold. These switching points are guaranteed to lie between 0.8 and 2.0 volts over the operating temperature range (VLC = 0.0V).

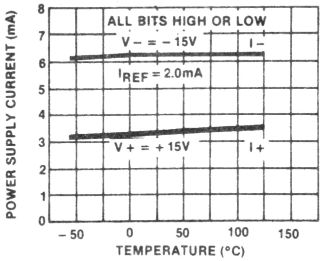
POWER SUPPLY CURRENT vs V+



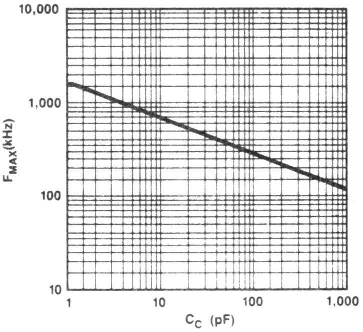
POWER SUPPLY CURRENT vs V−



POWER SUPPLY CURRENT vs TEMPERATURE

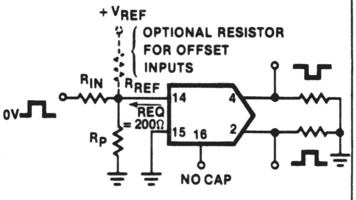


MAXIMUM REFERENCE INPUT FREQUENCY VS. COMPENSATION CAPACITOR VALUE



TYPICAL APPLICATION

PULSED REFERENCE OPERATION



$REQ = R_{IN} \parallel R_P$

TYPICAL VALUES

$R_{IN} = 5K$
$+V_{IN} = 10V$

FUNCTIONAL DESCRIPTION

Reference Amplifier Drive and Compensation

The reference amplifier input current must always flow into pin 14 regardless of the setup method or reference supply voltage polarity.

Connections for a positive reference voltage are shown in Figure 1. The reference voltage source supplies the full reference current. For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. R15 may be eliminated with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased as R14 value is increased. This is in order to maintain proper phase margin. For R14 values of 1.0, 2.5, and 5.0K ohms, minimum capacitor values are 15, 37, and 75pF, respectively. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection. (Fluctuations in the negative supply have more effect on accuracy than do any changes in the positive supply.)

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15, as shown. A high input impedance is the main advantage of this method. The negative reference votage must be at least 3.0V above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When using a DC reference voltage, capacitive bypass to ground is recommended. The 5.0V logic supply is not recommended as a reference voltage, but if a well regulated 5.0V supply which drives logic is to be used as the reference, R14 should be formed of two series resistors with the junction of the two resistors bypassed with 0.1μF to ground. For reference voltages greater than 5.0V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

Output Voltage Range

The voltage at pin 4 must always be at least 4.5 volts more positive than the voltage of the negative supply (pin 3) when the reference current is 2mA or less, and at least 8 volts more positive than the negative supply when the reference current is between 2mA and 4mA. This is necessary to avoid saturation of the output transistors, which would cause serious accuracy degradation.

Output Current Range

Any time the full scale current exceeds 2mA, the negative supply must be at least 8 volts more negative than the output voltage. This is due to the increased internal voltage drops between the negative supply and the outputs with higher reference currents.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy, full scale accuracy and full scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full scale current after zero scale current has been nulled out. The relative accuracy of the DAC08 series is essentially constant over the operating temperature range due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the DAC08 series has a very low full scale current drift over the operating temperature range.

The DAC08 series is guaranteed accurate to within ± 1/2 LSB at +25°C at a full scale output current of 1.992mA. The relative accuracy test circuit is shown in Figure 1. The 12-bit converter is calibrated to a full scale output current of 1.99219mA, then the DAC08 full scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on the oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accurate D-to-A converter. Sixteen-bit accuracy implies a total of ±1/2 part in 65,536, or ±0.00076%, which is much more accurate than the ±0.19% specification of the DAC08 series.

Monotonicity

A monotonic converter is one which always provides analog output greater than or equal to the preceding value for a corresponding increment in the digital input code. The DAC08 series is monotonic for all values of reference current above 0.5mA. The recommended range for operation is a DC reference current between 0.5mA and 4.0mA.

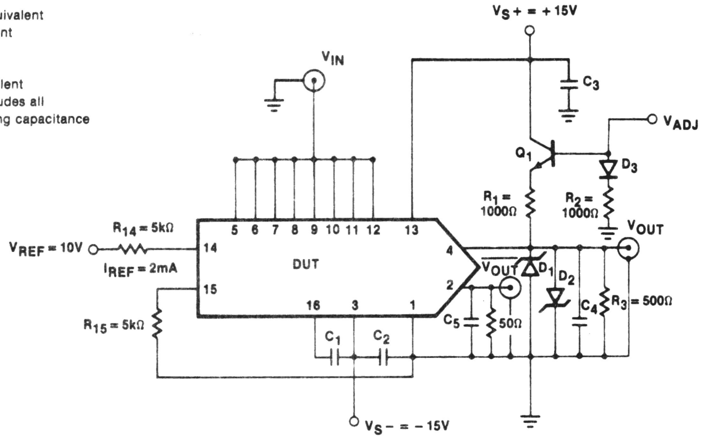
Settling Time

The worst case switching condition occurs when all bits are switched on, which corresponds to a low-to-high transition for all input bits. This time is typically 70ns for settling to within 1/2 LSB for 8-bit accuracy. This time applies when $R_L < 500$ ohms and $C_O < 25$pF. The slowest single switch is the least significant bit, which typically turns on and settles in 65ns. In applications where the DAC functions in a positive going ramp mode, the worst case condition does not occur and settling times less than 70ns may be realized.

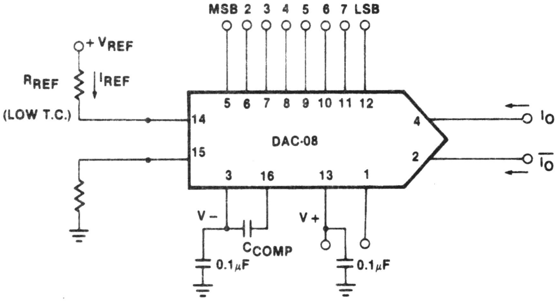
Extra care must be taken in board layout since this usually is the dominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing for low frequencies, minimum scope lead length, and avoidance of ground loops are all mandatory.

SETTLING TIME AND PROPAGATION DELAY

D₁, D₂ = IN6263 or equivalent
D₃ = IN914 or equivalent
C₁ = 0.01μf
C₂, C₃ = 0.1μf
Q₁ = 2N3904 or equivalent
C₄, C₅ = 15pf and includes all
probe and fixturing capacitance

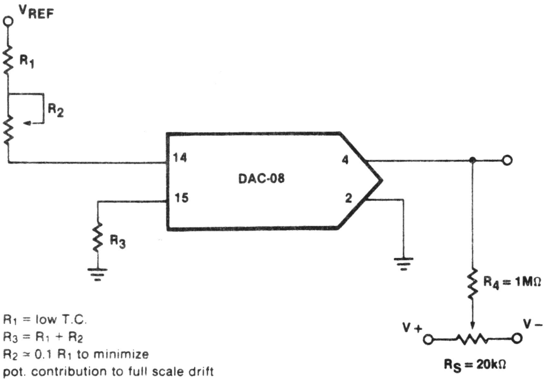

$V_S+ = +15V$
V_{IN}
C_3
V_{ADJ}
Q_1
D_3
$R_1 = 1000Ω$
$R_2 = 1000Ω$
V_{OUT}
$R_{14} = 5kΩ$
$V_{REF} = 10V$
$I_{REF} = 2mA$
5 6 7 8 9 10 11 12 13
14
15
DUT
4
2
16 3 1
$\overline{V_{OUT}}$
D_1
D_2
C_4
$R_3 = 500Ω$
$R_{15} = 5kΩ$
C_5
50Ω
C_1
C_2
$V_S- = -15V$

BASIC DAC-08 CONFIGURATION


MSB 2 3 4 5 6 7 LSB
$+V_{REF}$
R_{REF}
(LOW T.C.)
I_{REF}
5 6 7 8 9 10 11 12
14
15
DAC-08
4
2
3 16 13 1
I_O
$\overline{I_O}$
V−
V+
C_{COMP}
0.1μF
0.1μF

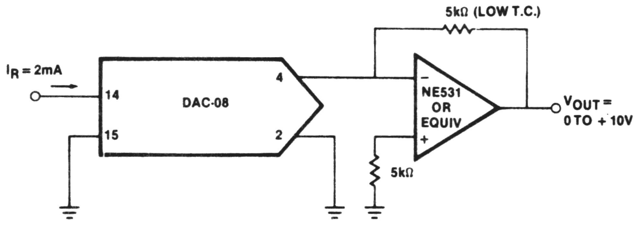
$I_{FS} \approx \frac{+V_{Ref}}{R_{Ref}} \times \frac{255}{256}$; $I_O + \overline{I_O} = I_{FS}$ for all logic states

RECOMMENDED FULL SCALE AND ZERO SCALE ADJUST


V_{REF}
R_1
R_2
14
15
DAC-08
4
2
R_3
$R_4 = 1MΩ$
V+
V−
$R_S = 20kΩ$

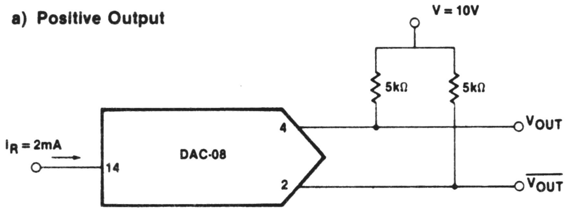
R_1 = low T.C.
$R_3 = R_1 + R_2$
$R_2 \simeq 0.1\ R_1$ to minimize
pot. contribution to full scale drift

UNIPOLAR VOLTAGE OUTPUT FOR LOW IMPEDANCE OUTPUT

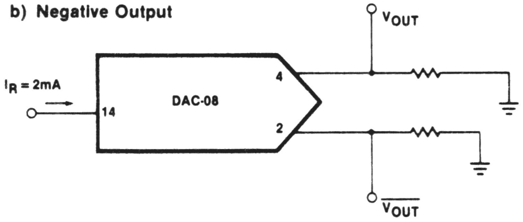

5kΩ (LOW T.C.)
I_R = 2mA
14
15
DAC-08
4
2
NE531
OR
EQUIV
−
+
5kΩ
V_{OUT} =
0 TO + 10V

UNIPOLAR VOLT OUTPUT FOR HIGH IMPEDANCE OUTPUT

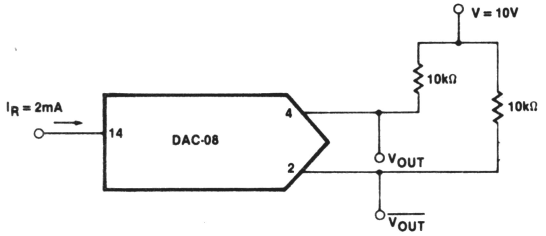
a) Positive Output


V = 10V
5kΩ
5kΩ
I_R = 2mA
14
DAC-08
4
2
V_{OUT}
$\overline{V_{OUT}}$

b) Negative Output


V_{OUT}
I_R = 2mA
14
DAC-08
4
2
$\overline{V_{OUT}}$

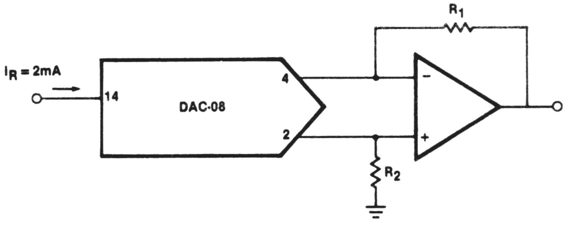
BASIC BIPOLAR OUTPUT OPERATION (OFFSET BINARY)


V = 10V
10kΩ
10kΩ
I_R = 2mA
14
DAC-08
4
2
V_{OUT}
$\overline{V_{OUT}}$

CODE CHART

	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	V_{OUT}	$\overline{V_{OUT}}$
POS full scale	1	1	1	1	1	1	1	1	- 9.920V	+10.000
POS f.s. - 1LSB	1	1	1	1	1	1	1	0	- 9.840V	+9.920
+ Zero scale + 1LSB	1	0	0	0	0	0	0	1	- 0.080V	+0.160
Zero scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero scale - 1LSB	0	1	1	1	1	1	1	1	0.080	0.000
Neg full scale - 1LSB	0	0	0	0	0	0	0	1	+ 9.920	- 9.840
Neg full scale	0	0	0	0	0	0	0	0	+10.000	- 9.920

SYMMETRICAL OFFSET BINARY (BIPOLAR)


R_1
I_R = 2mA
14
DAC-08
4
2
−
+
R_2

V_{OUT} = 0 to ±V*

±V *Range:
±5V for $R_1 = R_2$ = 2.5K
±10V for $R_1 = R_2$ = 5.0K

3 DIGIT BCD CONVERTER

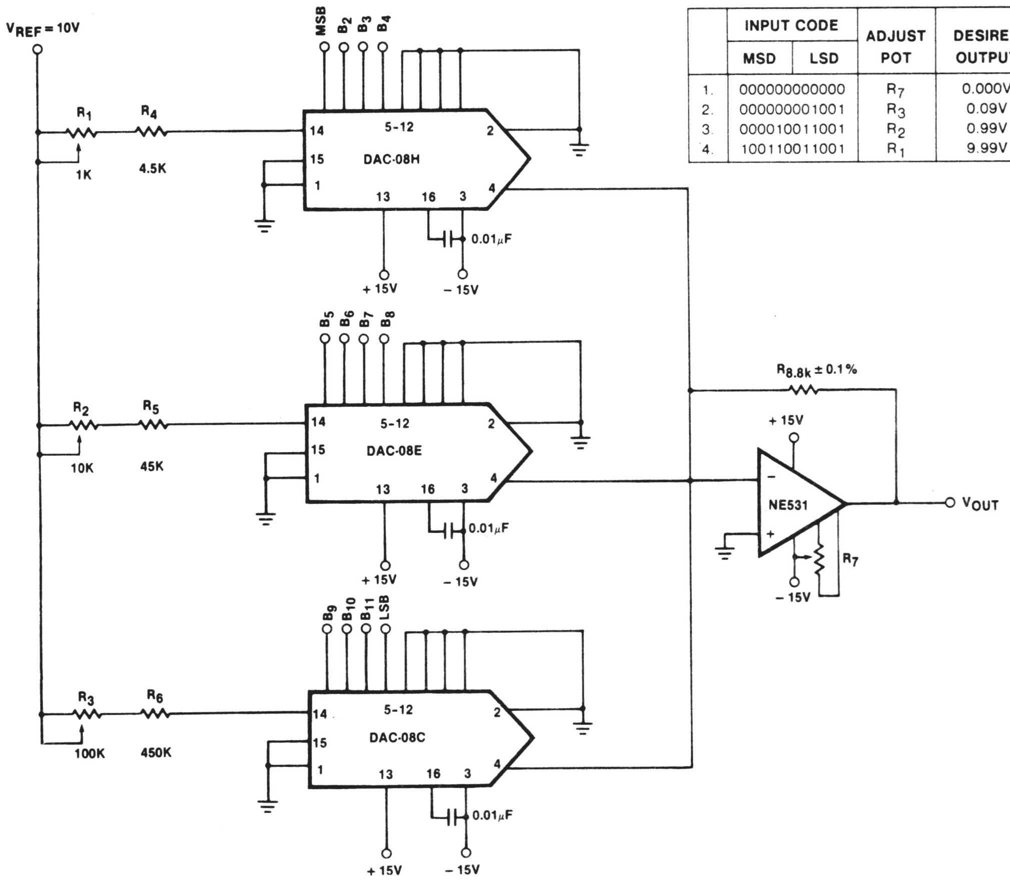
A 3 digit BCD converter, using inexpensive 8-bit binary DACs, can achieve ±0.1% accuracy. The circuit shown in Figure 20 utilizes three DACs, one for each decade, to provide 0 to 999 output steps. DAC 1 contains the first four significant digits controlling the hundreds digit; DAC 2 controls the tens digit and DAC 3 steps 0 to 9. The feedback resistor (R_7) sets the zero scale at 0.00V.

The input coding is the popular 8-4-2-1 coding; i.e. the weighting ratios are 8, 4, 2 and 1. The full scale (999) BCD code is input code 100110011001.

Full scale adjustment procedure.

In the sequence below, switch on the following code combinations and adjust the indicated potentiometer for the proper output.

3 DIGIT BCD CONVERTER WITH ±0.1% ACCURACY


V_{REF} = 10V
MSB
B_2
B_3
B_4
R_1
R_4
1K
4.5K
14
15
1
5-12
DAC-08H
2
4
13
16
3
0.01μF
+15V
−15V
B_5
B_6
B_7
B_8
R_2
R_5
10K
45K
14
15
1
5-12
DAC-08E
2
4
13
16
3
0.01μF
+15V
−15V
B_9
B_{10}
B_{11}
LSB
R_3
R_6
100K
450K
14
15
1
5-12
DAC-08C
2
4
13
16
3
0.01μF
+15V
−15V
$R_{8.8k}$ ± 0.1%
+15V
−
+
NE531
R_7
−15V
V_{OUT}

	INPUT CODE		ADJUST POT	DESIRED OUTPUT
	MSD	LSD		
1.	000000000000		R_7	0.000V
2.	000000001001		R_3	0.09V
3.	000010011001		R_2	0.99V
4.	100110011001		R_1	9.99V

8-BIT MULTIPLYING D/A CONVERTER MC1508-8/1408-8/1408-7

DESCRIPTION

The MC1508/MC1408 series of 8-bit monolithic digital-to-analog converters provide high speed performance with low cost. They are designed for use where the output current is a linear product of an 8-bit digital word and an analog reference voltage.

FEATURES

- **Fast settling time—70ns (typ)**
- **Relative accuracy ±0.19% (max error)**
- **Non-inverting digital inputs are TTL and CMOS compatible**
- **High speed multiplying rate 4.0mA/µs (input slew)**
- **Output voltage swing +.5V to -5.0V**
- **Standard supply voltages + 5.0V and -5.0V to -15V**
- **Military qualifications pending**

APPLICATIONS

- **Tracking A-to-D converters**
- **2½-digit panel meters and DVM's**
- **Waveform synthesis**
- **Sample and hold**
- **Peak detector**
- **Programmable gain and attenuation**
- **CRT character generation**
- **Audio digitizing and decoding**
- **Programmable power supplies**
- **Analog-digital multiplication**
- **Digital-digital multiplication**
- **Analog-digital division**
- **Digital addition and subtraction**
- **Speech compression and expansion**
- **Stepping motor drive**
- **Modems**
- **Servo motor and pen drivers**

CIRCUIT DESCRIPTION

The MC1508/MC1408 consists of a reference current amplifier, an R-2R ladder, and 8 high speed current switches. For many applications, only a reference resistor and reference voltage need be added.

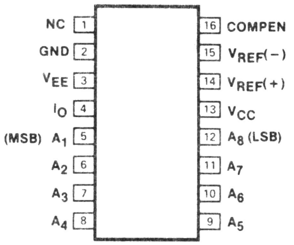
The switches are non-inverting in operation; therefore, a high state on the input turns on the specified output current component.

The switch uses current steering for high speed, and a termination amplifier consisting of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching, and provides a low impedance termination of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binarily-related components, which are fed to the switches. Note that there is always a remainder current which is equal to the least significant bit. This current is shunted to ground, and the maximum output current is 255/256 of the reference amplifier current, or 1.992mA for a 2.0mA reference amplifier current if the NPN current source pair is perfectly matched.

PIN CONFIGURATION

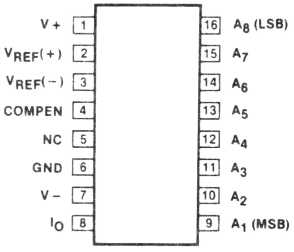
F,N PACKAGE


NC 1
GND 2
V_{EE} 3
I_O 4
(MSB) A_1 5
A_2 6
A_3 7
A_4 8
16 COMPEN
15 $V_{REF}(-)$
14 $V_{REF}(+)$
13 V_{CC}
12 A_8 (LSB)
11 A_7
10 A_6
9 A_5

TOP VIEW

ORDER NUMBERS
MC1508-8F MC1408-7N
MC1408-7F

D[3] PACKAGE


V+ 1
$V_{REF}(+)$ 2
$V_{REF}(-)$ 3
COMPEN 4
NC 5
GND 6
V- 7
I_O 8
16 A_8 (LSB)
15 A_7
14 A_6
13 A_5
12 A_4
11 A_3
10 A_2
9 A_1 (MSB)

TOP VIEW

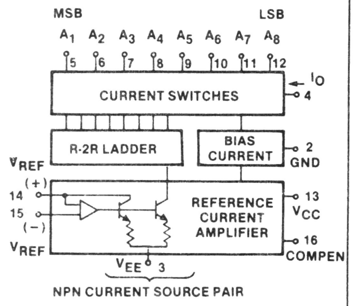
ORDER NUMBER
MC 1408-8D

NOTES:
1. SOL Released in Large SO package only.
2. SOL and non-standard pinout.
3. SO and non-standard pinouts.

ABSOLUTE MAXIMUM RATINGS T_A = +25°C unless otherwise specified

	PARAMETER	RATING	UNIT
	Power Supply Voltage		
V_{CC}	Positive	+5.5	V
V_{EE}	Negative	−16.5	V
V_5-V_{12}	Digital Input Voltage	0 to V_{CC}	V
V_0	Applied Output Voltage	−5.2 to +18	V
I_{14}	Reference Current	5.0	mA
V_{14}, V_{15}	Reference Amplifier Inputs	V_{EE} to V_{CC}	
P_D	Power Dissipation (Package Limitation)		
	Ceramic Package	1000	mW
	Plastic Package	800	mW
	Lead Soldering Temperature (60 sec)	300	°C
T_A	Operating Temperature Range		
	MC1508	−55 to +125	°C
	MC1408	0 to +75	°C
T_{STG}	Storage Temperature Range	−65 to +150	°C

BLOCK DIAGRAM


MSB
LSB
A_1 A_2 A_3 A_4 A_5 A_6 A_7 A_8
5 6 7 8 9 10 11 12
CURRENT SWITCHES
I_O
4
R-2R LADDER
BIAS CURRENT
2
GND
V_{REF} (+)
14
15
(−) V_{REF}
REFERENCE CURRENT AMPLIFIER
13
V_{CC}
16
COMPEN
V_{EE} 3
NPN CURRENT SOURCE PAIR

8-BIT MULTIPLYING D/A CONVERTER MC1508-8/1408-8/1408-7

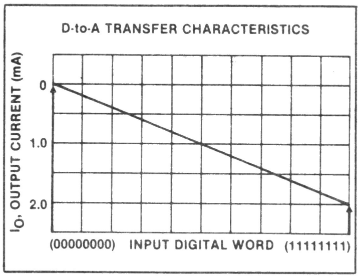
DC ELECTRICAL CHARACTERISTICS[1]

Pin 3 must be 3V more negative than the potential to which R_{15} is returned.
V_{CC} = +5.0Vdc, V_{EE} = −15Vdc, $\frac{V_{ref}}{R_{14}}$ = 2.0mA
unless otherwise specified.
MC1508: T_A = −55°C to 125°C. MC1408: T_A = 0°C to 75°C
unless otherwise noted.

PARAMETER	TEST CONDITIONS	MC1508-8			MC1408-8			MC1408-7			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
E_r Relative accuracy	Error relative to full scale I_O, Figure 3			±0.19			±0.19			±0.39	%
t_s Setting time[1]	To within 1/2 LSB, includes t'PLH, T'A = +25°C, Figure 4		70			70			70		ns
Propagation delay time t_{PLH} Low-to-high t_{PHL} High-to-low	T_A = +25°C, Figure 4		35	100		35	100		35	100	ns
TCI_O Output full scale current drift			−20			−20			−20		PPM/°C
Digital input logic level (MSB)											Vdc
V_{IH} High	Figure 5	2.0			2.0			2.0			
V_{IL} Low				0.8			0.8			0.8	
Digital input current (MSB)	Figure 5										mA
I_{IH} High	V_{IH} = 5.0V		0	0.04		0	0.04		0	0.04	
I_{IL} Low	V_{IL} = 0.8V		−0.4	−0.8		−0.4	−0.8		−0.4	−0.8	
I_{15} Reference input bias current	Pin 15, Figure 5		−1.0	−5.0		−1.0	−5.0		−1.0	−5.0	μA
I_{OR} Output current range	Figure 5										mA
	V_{EE} = −5.0V	0	2.0	2.1	0	2.0	2.1	0	2.0	2.1	
	V_{EE} = −7.0V to −15V	0	2.0	4.2	0	2.0	4.2	0	2.0	4.2	
I_O Output current	Figure 5 V_{ref} = 2.000V, R14 = 1000Ω	1.9	1.99	2.1	1.9	1.99	2.1	1.9	1.99	2.1	mA
$I_{O(min)}$ Off-state	All bits low		0	4.0		0	4.0		0	4.0	μA
V_O Output voltage compliance	E_r≤0.19% at T_A = +25°C, Figure 5										Vdc
	V_{EE} = −5V		−0.6, +10	−0.55, +0.5		−0.6, +10	−0.55, +0.5		−0.6, +10	−0.55, +0.5	
	V_{EE} below −10V		−5.5, +10	−5.0, +0.5		−5.5, +10	−5.0, +0.5		−5.5, +10	−5.0, +0.5	
SRI_{ref} Reference current slew rate	Figure 6		8.0			8.0			8.0		mA/μs
$PSRR_{(-)}$ Output current power supply sensitivity	I_{ref} = 1mA		0.5	2.7		0.5	2.7		0.5	2.7	μA/V
Power supply current											mA
I_{CC} Positive	All bits low,		+2.5	+22		+2.5	+22		+2.5	+22	
I_{EE} Negative	Figure 5		−6.5	−13		−6.5	−13		−6.5	−13	
Power supply voltage range											Vdc
V_{CCR} Positive	T_A = +25°C,	+4.5	+5.0	+5.5	+4.5	+5.0	+5.5	+4.5	+5.0	+5.5	
V_{EER} Negative	Figure 5	−4.5	−15	−16.5	−4.5	−15	−16.5	−4.5	−15	−16.5	
P_D Power dissipation	All bits low, Figure 5										mW
	V_{EE} = −5.0Vdc		34	170		34	170		34	170	
	V_{EE} = −15Vdc		110	305		110	305		110	305	

NOTES:
1. All bits switched.

TYPICAL PERFORMANCE CHARACTERISTICS



FUNCTIONAL DESCRIPTION

Reference Amplifier Drive and Compensation

The reference amplifier input current must always flow into pin 14 regardless of the setup method or reference supply voltage polarity.

Connections for a positive reference voltage are shown in Figure 1. The reference voltage source supplies the full reference current. For bipolar reference signals, as in the multiplying mode, R_{15} can be tied to a negative voltage corresponding to the minimum input level. R_{15} may be eliminated and pin 15 grounded, with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increasing values of R_{14} to maintain proper phase margin. For R_{14} values of 1.0, 2.5, and 5.0K ohms, minimum capacitor values are 15, 37, and 75pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection. (Fluctuations in the negative supply have more effect on accuracy than do any changes in the positive supply).

A negative reference voltage may be used if R_{14} is grounded and the reference voltage is applied to R_{15}, as shown in Figure 2. A high input impedance is the main advantage of this method. The negative reference voltage must be at least 3.0V above the V_{EE} supply. Bipolar input signals may be handled by connecting R_{14} to a positive reference voltage equal to the peak positive input level at pin 15.

Capacitive bypass to ground is recommended when a DC reference voltage is used. The 5.0V logic supply is not recommended as a reference voltage, but if a well regulated 5.0V supply which drives logic is to be used as the reference, R_{14} should be formed of two series resistors and the junction of the two resistors bypassed with 0.1μF to ground. For reference voltages greater than 5.0V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

Output Voltage Range

The voltage at pin 4 must always be at least 4.5 volts more positive than the voltage of the negative supply (pin 3) when the reference current is 2mA or less, and at least 8 volts more positive than the negative supply when the reference current is between 2mA and 4mA. This is necessary to avoid saturation of the output transistors, which would cause serious degradation of accuracy.

Signetics' MC1508/MC1408 does not need a range control because the design extends the compliance range down to 4.5 volts (or 8 volts—see above) above the negative supply voltage without significant degradation of accuracy. Signetics' MC1508/MC1408 can be used in sockets designed for other manufacturers' MC1508/MC1408 without circuit modification.

Output Current Range

Any time the full scale current exceeds 2mA, the negative supply must be at least 8 volts more negative than the output voltage. This is due to the increased internal voltage drops between the negative supply and the outputs with higher reference currents.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy, full scale accuracy and full scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full scale current after zero scale current has been nulled out. The relative accuracy of the MC1508/MC1408 is essentially constant over the operating temperature range because of the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current; however, the MC1508/MC1408 has a very low full scale current drift over the operating temperature range.

The MC1508/MC1408 series is guaranteed accurate to within ±1/2 LSB at +25°C at a full scale output current of 1.99mA. The relative accuracy test circuit is shown in Figure 3. The 12-bit converter is calibrated to a full scale output current of 1.99219mA; then the MC1508/MC1408's full scale current is trimmed to the same value with R_{14} so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on the oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accurate D-to-A converter. Sixteen-bit accuracy implies a total of ±1/2 part in 65,536, or ±0.00076%, which is much more accurate than the ±0.19% specification of the MC1508/MC1408.

Monotonicity

A monotonic converter is one which always provides an analog output greater than or equal to the preceding value for a corresponding increment in the digital input code. The MC1508/MC1408 is monotonic for all values of reference current above 0.5mA. The recommended range for operation is a DC reference current between 0.5mA and 4.0mA.

Settling Time

The worst case switching condition occurs when all bits are switched on, which corresponds to a low-to-high transition for all input bits. This time is typically 70ns for settling to within 1/2 LSB for 8-bit accuracy. This time applies when RL <500 ohms and C_O <25pF. The slowest single switch is the least significant bit, which typically turns on and settles in 65ns. In applications where the D-to-A converter functions in a positive going ramp mode, the worst case condition does not occur and settling times less than 70ns may be realized.

Extra care must be taken in board layout since this usually is the dominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing for low frequencies, minimum scope lead length, good ground planes, and avoidance of ground loops are all mandatory.

TEST CIRCUITS

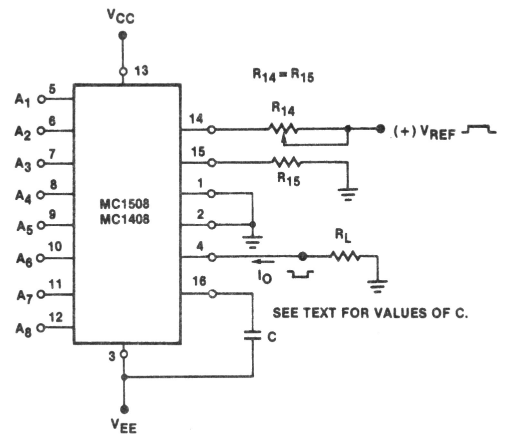

VCC
13
R14 = R15
A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
A8 12
MC1508
MC1408
14
R14
(+) VREF
15
R15
1
2
RL
4
IO
16
SEE TEXT FOR VALUES OF C.
C
3
VEE

Figure 1. Positive V_{REF}

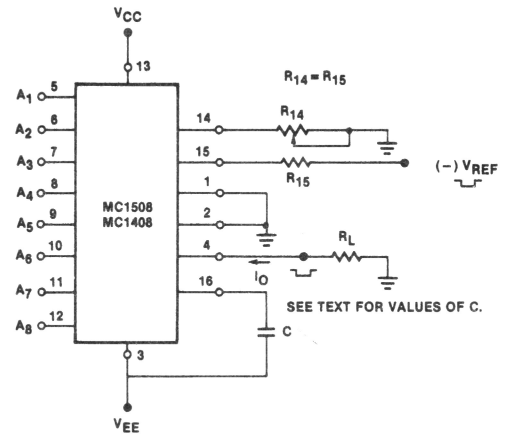

VCC
13
R14 = R15
A1 5
A2 6
A3 7
A4 8
A5 9
A6 10
A7 11
A8 12
MC1508
MC1408
14
R14
15
R15
(−) VREF
1
2
RL
4
IO
16
SEE TEXT FOR VALUES OF C.
C
3
VEE

Figure 2. Negative V_{REF}

TEST CIRCUITS (Cont'd)

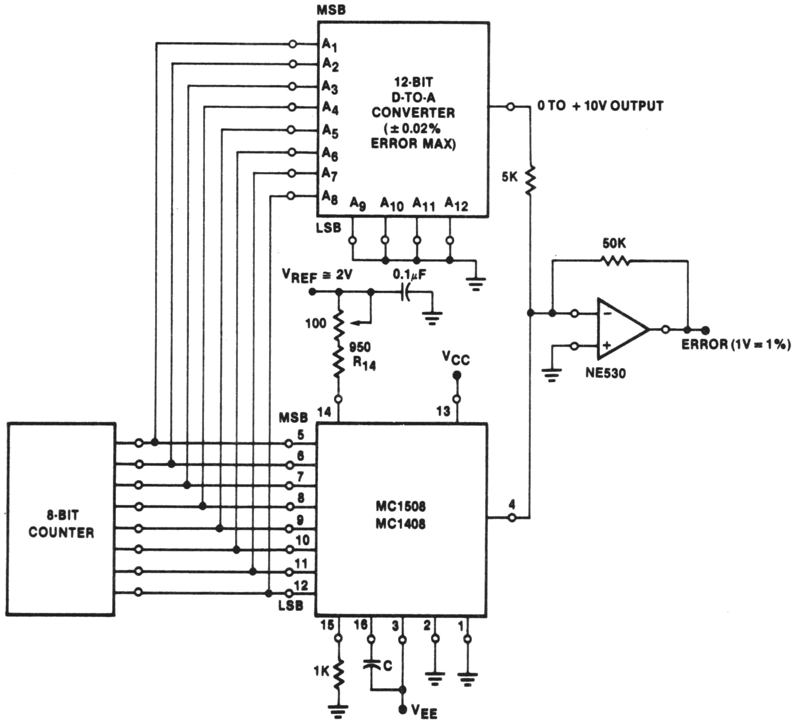

MSB
A_1
A_2
A_3
A_4
A_5
A_6
A_7
A_8
A_9
A_{10}
A_{11}
A_{12}
LSB
12-BIT D-TO-A CONVERTER (±0.02% ERROR MAX)
0 TO +10V OUTPUT
5K
50K
V_{REF} ≅ 2V
0.1µF
100
950 R_{14}
V_{CC}
ERROR (1V = 1%)
NE530
MSB
14
13
5
6
7
8
9
10
11
12
LSB
8-BIT COUNTER
MC1508 MC1408
4
15
16
3
2
1
1K
C
V_{EE}

Figure 3. Relative Accuracy

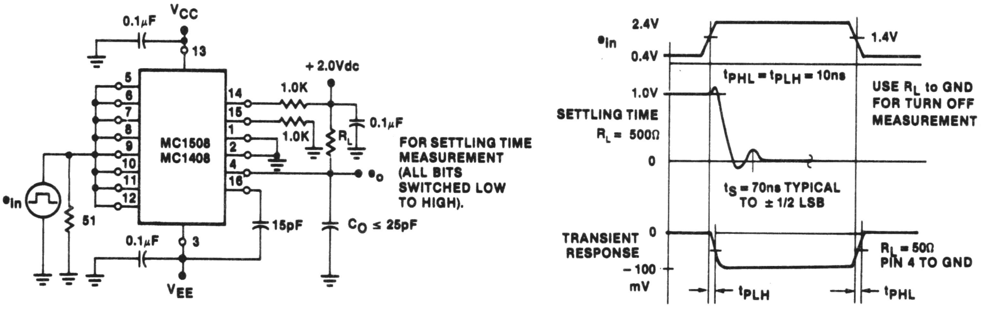
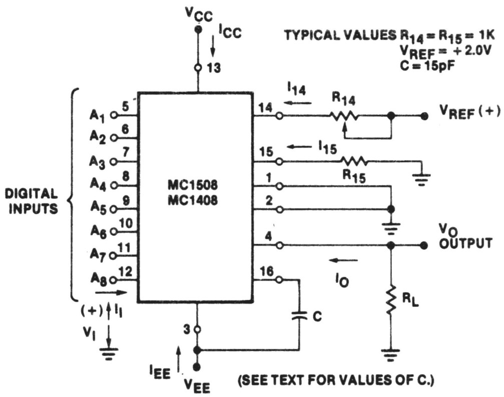

0.1µF
V_{CC}
13
5
6
7
8
9
10
11
12
MC1508 MC1408
14
15
1
2
4
16
+2.0Vdc
1.0K
1.0K
R_L
0.1µF
FOR SETTLING TIME MEASUREMENT (ALL BITS SWITCHED LOW TO HIGH).
e_o
e_{in}
51
0.1µF
3
V_{EE}
15pF
$C_O \leq 25pF$
e_{in}
2.4V
0.4V
1.4V
$t_{PHL} = t_{PLH}$ = 10ns
USE R_L to GND FOR TURN OFF MEASUREMENT
1.0V
SETTLING TIME
R_L = 500Ω
0
t_S = 70ns TYPICAL TO ±1/2 LSB
TRANSIENT RESPONSE
0
−100
mV
R_L = 50Ω PIN 4 TO GND
t_{PLH}
t_{PHL}

Figure 4. Transient Response and Settling Time

8-BIT MULTIPLYING D/A CONVERTER

MC1508-8/1408-8/1408-7

TEST CIRCUITS (Cont'd)


V_{CC}
I_{CC}
13
TYPICAL VALUES $R_{14} = R_{15} = 1K$
$V_{REF} = +2.0V$
$C = 15pF$
I_{14}
R_{14}
14
$V_{REF}(+)$
15
I_{15}
R_{15}
1
2
4
16
V_O
OUTPUT
I_O
R_L
C
DIGITAL INPUTS
A_1 5
A_2 6
A_3 7
A_4 8
A_5 9
A_6 10
A_7 11
A_8 12
MC1508
MC1408
$(+)$ I_I
V_I
3
I_{EE}
V_{EE}
(SEE TEXT FOR VALUES OF C.)

V_I AND I_I APPLY TO INPUTS A_1 THROUGH A_8

THE RESISTOR TIED TO PIN 15 IS TO TEMPERATURE COMPENSATE THE BIAS CURRENT AND MAY NOT BE NECESSARY FOR ALL APPLICATIONS.

$$I_O = K \left\{ \frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{128} + \frac{A_8}{256} \right\}$$

where $K \cong \frac{V_{REF}}{R_{14}}$

and A_N = "1" IF A_N IS AT HIGH LEVEL
A_N = "0" IF A_N IS AT LOW LEVEL

Figure 5. Notation Definitions

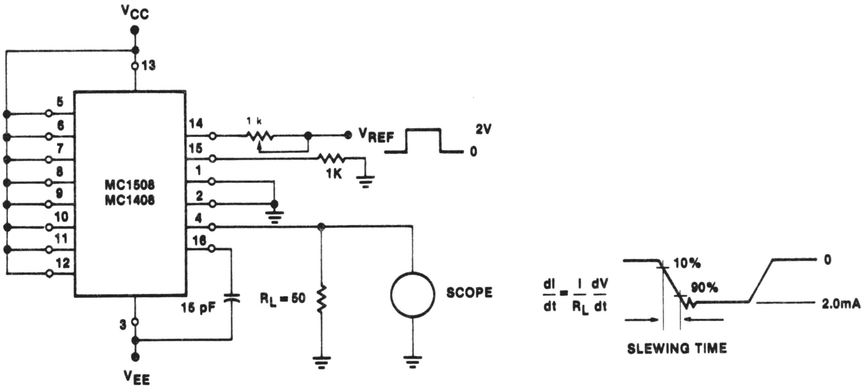

V_{CC}
13
5
6
7
8
9
10
11
12
MC1508
MC1408
14
15
1
2
4
16
1 k
V_{REF}
2V
0
1K
15 pF
$R_L = 50$
SCOPE
3
V_{EE}
$\frac{dI}{dt} = \frac{1}{R_L}\frac{dV}{dt}$
10%
90%
0
2.0mA
SLEWING TIME

Figure 6. Reference Current Slew Rate Measurement

10-BIT HIGH-SPEED MULTIPLYING D/A CONVERTER MC3410, MC3510, MC3410C

DESCRIPTION

The MC3410 series are 10-Bit Multiplying Digital-to-Analog Converters. They are capable of high-speed performance, and are used as general-purpose building blocks in cost-effective D/A systems.

The Signetics' design provides complete 10-bit accuracy without laser trimming, and guaranteed monotonicity over temperature. Segmented current sources, in conjunction with an R/2R DAC provides the binary weighted currents. The output buffer amplifier and voltage reference have been omitted to allow greater speed, lower cost, and maximum user flexibility.

FEATURES

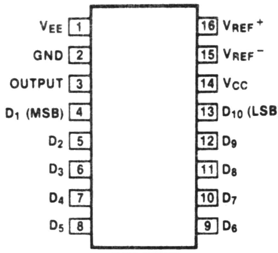
- **10-bit resolution and accuracy (±0.05%)**
- **Guaranteed monotonicity over temperature**
- **Fast settling time—250ns typical**
- **Digital inputs are TTL and CMOS compatible**
- **Wide output voltage compliance range**
- **High-speed multiplying input slew rate —20mA/μs**
- **Reference amplifier internally compensated**
- **Standard supply voltages +5V and −15V**

APPLICATIONS

- **Successive approximation A/D converters**
- **High-speed, automatic test equipment**
- **High-speed modems**
- **Waveform generators**
- **CRT displays**
- **Strip CHART and X-Y plotters**
- **Programmable power supplies**
- **Programmable gain and attenuation**

PIN CONFIGURATION

F PACKAGES


V_EE 1
GND 2
OUTPUT 3
D₁ (MSB) 4
D₂ 5
D₃ 6
D₄ 7
D₅ 8
16 V_REF+
15 V_REF−
14 V_CC
13 D₁₀ (LSB)
12 D₉
11 D₈
10 D₇
9 D₆

TOP VIEW

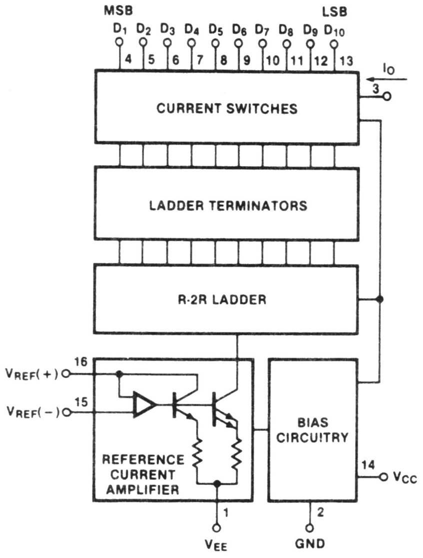
ORDER NUMBERS

MC3410F MC3410CF MC3510F

ABSOLUTE MAXIMUM RATINGS $T_A = +25°C$ unless otherwise noted

SYMBOL AND PARAMETER		RATING	UNIT
V_{CC}	Power Supply	+7.0	Vdc
V_{EE}		−18	Vdc
V_I	Digital Input Voltage	+15	Vdc
V_O	Applied Output Voltage	0.5, −5.0	Vdc
$I_{REF(16)}$	Reference Current	2.5	mA
V_{REF}	Reference Amplifier Inputs	V_{CC}, V_{EE}	Vdc
$V_{REF(D)}$	Reference Amplifier Differential Inputs	0.7	Vdc
T_A	Operating Temperature Range		
	MC3510	−55 to +125	°C
	MC3410, 3410C	0 to +70	°C
T_J	Junction Temperature		
	Ceramic Package	+175	°C
	Plastic Package	+150	°C

BLOCK DIAGRAM


MSB
LSB
D₁ D₂ D₃ D₄ D₅ D₆ D₇ D₈ D₉ D₁₀
4 5 6 7 8 9 10 11 12 13
I_O
3
CURRENT SWITCHES
LADDER TERMINATORS
R-2R LADDER
V_REF(+)
16
V_REF(−)
15
REFERENCE CURRENT AMPLIFIER
BIAS CIRCUITRY
14
V_CC
1
V_EE
2
GND

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = +5.0Vdc$, $V_{EE} = -15Vdc$, $\frac{V_{REF}}{R16} = 2.0mA$, all digital inputs at high logic level.
MC3510: $T_A = -55°C$ to $+125°C$, MC3410 Series: $T_A = 0°$ to $+70°C$
unless otherwise noted.

SYMBOL AND PARAMETER		TEST CONDITIONS	MC3510, MC3410			MC3410C			UNIT
			Min	Typ	Max	Min	Typ	Max	
E_r	Relative accuracy (Error relative to full scale I_O)	$T_A = 25°C$			± 0.05			± 0.1	%
					1/4			1/2	LSB
TCE_r	Relative accuracy drift (Relative to full scale I_O)			2.5			2.5		ppm/°C
	Monotonicity	Over temperature	10			10			Bits
t_s	Settling time to within ± ½ LSB (all bits low to high)	$T_A = 25°C$		250			250		ns
t_{PLH} t_{PHL}	Propagation delay time	$T_A = 25°C$		35 20			35 20		ns
TCI_O	Output full scale current drift				60			70	ppm/°C
V_{IH}	Digital Input Logic Levels (All bits) High Level, Logic "1" Low Level, Logic "0"		2.0		0.8	2.0		0.8	Vdc
I_{IH} I_{IL}	Digital Input Current (All bits) High Level, $V_{IH} = 5.5V$ Low Level, $V_{IL} = 0.8V$			-0.05	+.04 -0.4		-0.05	+.04 -0.4	mA
$I_{REF(15)}$	Reference Input Bias Current (Pin 15)			-1.0	-5.0		-1.0	-5.0	μA
I_{OR}	Output Current Range			4.0*	5.0		4.0	5.0	mA
I_{OH}	Output Current (All bits high)	$V_{REF} = 2.000V$, $R_{16} = 1000Ω$	3.8	3.996	4.2	3.8	3.996	4.2	mA
I_{OL}	Output Current (All bits low)	$T_A = 25°C$		0	2.0		0	4.0	μA
V_O	Output Voltage Compliance	$T_A = 25°C$			-2.5 +0.2			-2.5 +0.2	Vdc
SR I_{REF}	Reference Amplifier Slew Rate			20			20		mA/μs
ST I_{REF}	Reference Amplifier Settling Time	0 to 4.0mA, ±0.1%		2.0			2.0		μs
PSRR(−)	Output Current Power Supply Sensitivity			0.003	0.01		0.003	0.02	%/%
C_O	Output Capacitance	$V_O = 0$		25			25		pF
C_I	Digital Input Capacitance (All bits high)			4.0			4.0		pF
I_{CC} I_{EE}	Power Supply Current (All bits low)			-11.4	+18 -20		-11.4	+18 -20	mA
V_{CC} V_{EE}	Power Supply Voltage Range	$T_A = 25°C$	+4.75 -14.25	+5.0 -15	+5.25 -15.75	+4.75 -14.25	+5.0 -15	+5.25 -15.75	Vdc
	Power Consumption (All bits low) (All bits high)			220 200	380		220 200	380	mW

TYPICAL PERFORMANCE CHARACTERISTICS

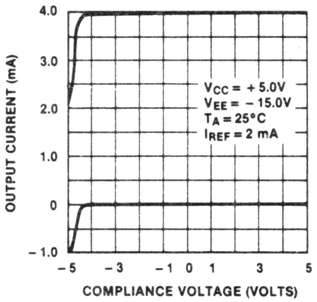


Figure 1. Output Current vs. Output Compliance Voltage

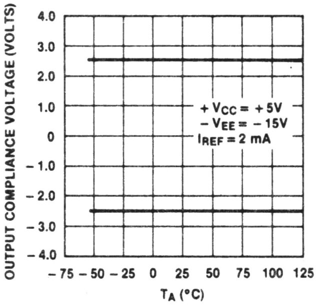


Figure 2. Maximum Output Compliance Voltage vs. Temperature

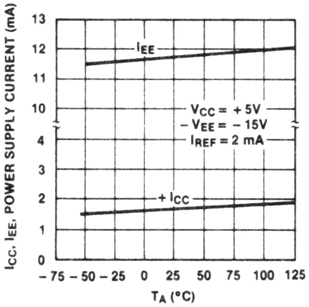


Figure 3. Power Supply Currents vs. Temperature

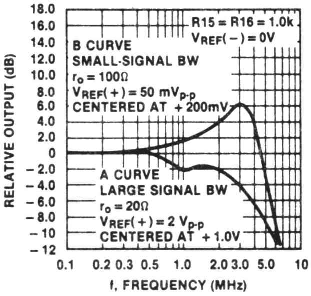


Figure 4. Reference Amplifier Frequency Response

CIRCUIT DESCRIPTION

The MC3410 consists of four segment current sources which generate the 2 Most Significant Bits (MSBs), and an R/2R DAC implemented with ion implanted resistors for scaling the remaining 8 Least Significant Bits (LSBs). (See Figure 5.) This approach provides complete 10-bit accuracy without trimming.

The individual bit currents are switched ON or OFF by fully differential current switches. The switches use current steering for speed.

An on-chip high-slew reference current amplifier drives the R/2R ladder and segment decoder. The currents are scaled in such a way that, with all bits on, the maximum output current is two times 1023/1024 of the reference amplifier current, or nominally 3.996mA for a 2.000mA reference input current. The reference amplifier allows the user to provide a voltage input. Out-board resistor R16 (see Figure 6) converts this voltage to a usable current. A current mirror doubles this reference current and feeds it to the segment decoder and resistor ladder. Thus, for a reference voltage of 2.0 Volts and a 1kΩ resistor tied to Pin 16, the full scale current is approximately 4.0mA. This relationship will remain regardless of the reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 6a. For negative reference voltage inputs, or for bipolar reference voltage inputs in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. For a negative reference input, R16 should be grounded (Figure 6b). In addition, the negative voltage reference must be at least 3V above the V_{EE} supply voltage for best operation. Bipolar input signals may be handled by connecting R16 to a positive voltage equal to the peak positive input level at Pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5.0V supply, which drives logic, is to be used as the reference, R16 should be decoupled by connecting it to the +5.0V logic supply through another resistor and bypassing the junction of the two resistors with a 0.1μF capacitor to ground.

The reference amplifier is internally compensated with a 10pF feed-forward capacitor, which gives it its high slew rate and fast settling time. Proper phase margin is maintained with all possible values of R16 and reference voltages which supply

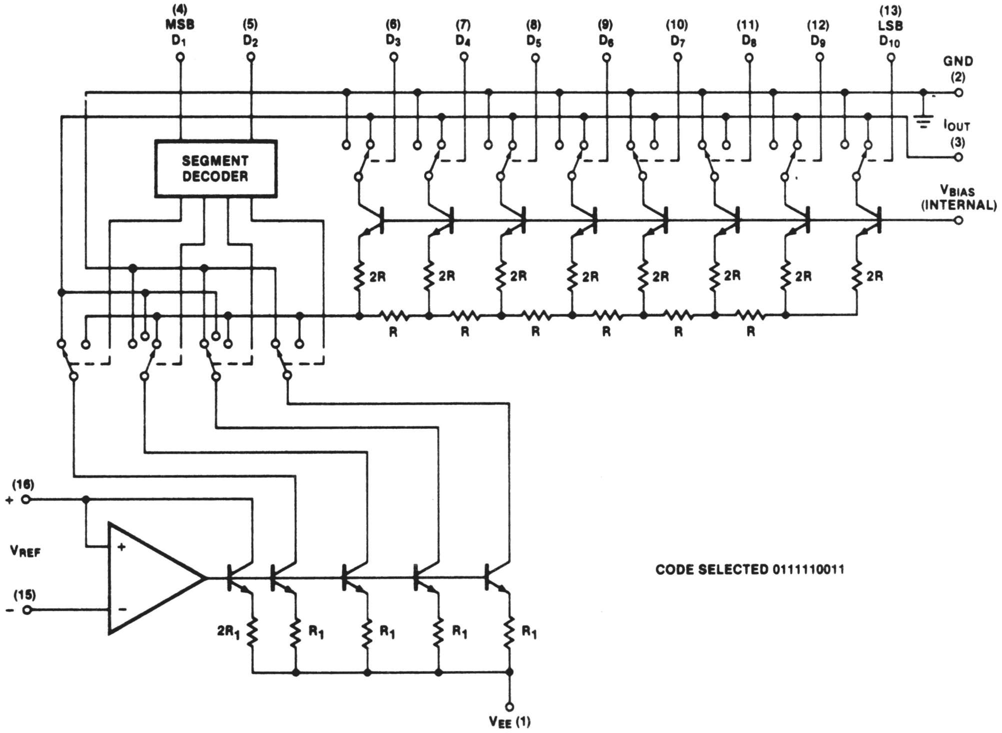
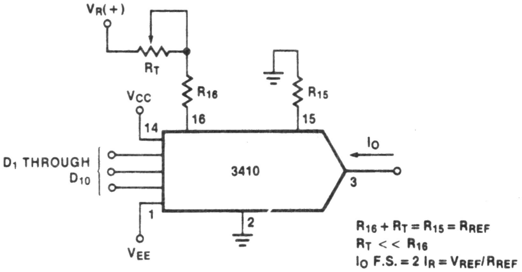
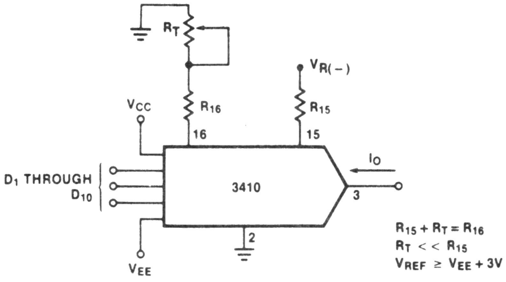


Figure 5. MC3410 Equivalent Circuit



$R_{16} + R_T = R_{15} = R_{REF}$
$R_T << R_{16}$
I_O F.S. $= 2\ I_R = V_{REF}/R_{REF}$

a) POSITIVE REFERENCE VOLTAGE



$R_{15} + R_T = R_{16}$
$R_T << R_{15}$
$V_{REF} \geq V_{EE} + 3V$

b) NEGATIVE REFERENCE VOLTAGE

Figure 6. Basic Connections

2.0mA reference current into Pin 16. The reference current can also be supplied by a high impedance current source of 2.0mA. As R16 increases, the bandwidth of the amplifier decreases slightly and settling time increases. For a current source with a dynamic output impedance of 1.0MΩ, the bandwidth of the reference amplifier is approximately half what it is in the case of R16 = 1.0kΩ, and settling time is ≈10μs. The reference amplifier phase margin decreases as the current source value decreases in the case of a current source reference, so that the minimum reference current supplied from a current source is 0.5mA for stability.

OUTPUT VOLTAGE COMPLIANCE

The output voltage compliance ranges from −2.5 to +0.2V. As shown in Figure 2, this compliance range is nearly constant over temperature. At the temperature extremes, however, the compliance voltage may be reduced if $V_{EE} > -15V$.

ACCURACY

Absolute accuracy is a measure of each output current level with respect to its intended value. It is dependent upon relative accuracy and full scale current drift. Relative accuracy, or linearity, is the measure of each output current with respect to its intended fraction of the full scale current. The relative accuracy of the MC3410 is fairly constant over temperature due to the excellent temperature tracking, of the implanted resistors. The full scale current from the reference amplifier may drift with temperature causing a change in the absolute accuracy. However, the MC3410 has a low full scale current drift with temperature.

The MC3510 and the MC3410 are accurate to within ±.05% at 25°C with a reference current of 2.0mA on Pin 16.

MONOTONICITY

The MC3410, MC3510 and MC3410C are guaranteed monotonic over temperature. This means that for every increase in the input digital code, the output current either remains the same or increases but never decreases. In the multiplying mode, where reference input current will vary, monotonicity can be assured if the reference input current remains above 0.5mA.

SETTLING TIME

The worst case switching condition occurs when all bits are switched "on," which corresponds to a low-to-high transition for all bits. This time is typically 250ns for the output to settle to within ± 1/2 LSB for 10-bit accuracy, and 200ns for 8-bit accuracy. The turn-off time is typically 120ns. These times apply when the output swing is limited to a small (<0.7 Volt) swing and the external output capacitance is under 25pF.

The major carry (MSB off-to-on, all others on-to-off) settles in approximately the same time as when all bits are switched off-to-on.

If a load resistor of 625 Ohms is connected to ground, allowing the output to swing to −2.5 Volts, the settling time increases to 1.5μs.

Extra care must be taken in board layout as this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing, and minimum scope lead length are all necessary.

A typical test set-up for measuring settling time is shown in Figure 7. The same set-up for the most part can be used to measure the slew rate of the reference amplifier (Figure 9) by tying all data bits high, pulsing the voltage reference input between 0 and 2V, and using a 500Ω load resistor R_L.

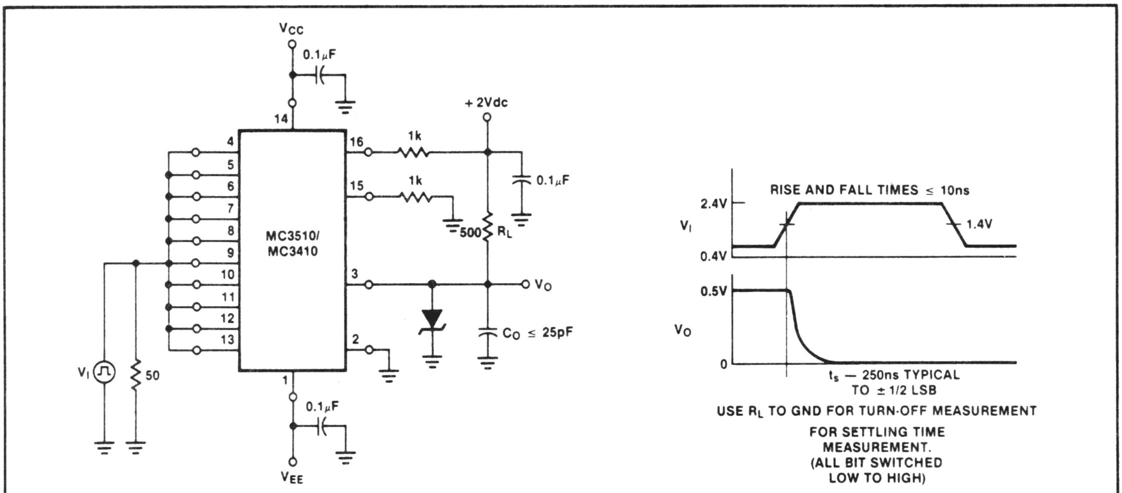

V_CC
0.1μF
14
4
5
6
7
8
9
10
11
12
13
MC3510/
MC3410
16
15
1k
1k
+2Vdc
0.1μF
500
R_L
3
V_O
2
C_O ≤ 25pF
1
0.1μF
V_EE
V_I
50
RISE AND FALL TIMES ≤ 10ns
2.4V
0.4V
1.4V
V_I
0.5V
V_O
0
t_s — 250ns TYPICAL
TO ± 1/2 LSB
USE R_L TO GND FOR TURN-OFF MEASUREMENT
FOR SETTLING TIME
MEASUREMENT.
(ALL BIT SWITCHED
LOW TO HIGH)

Figure 7. Settling Time

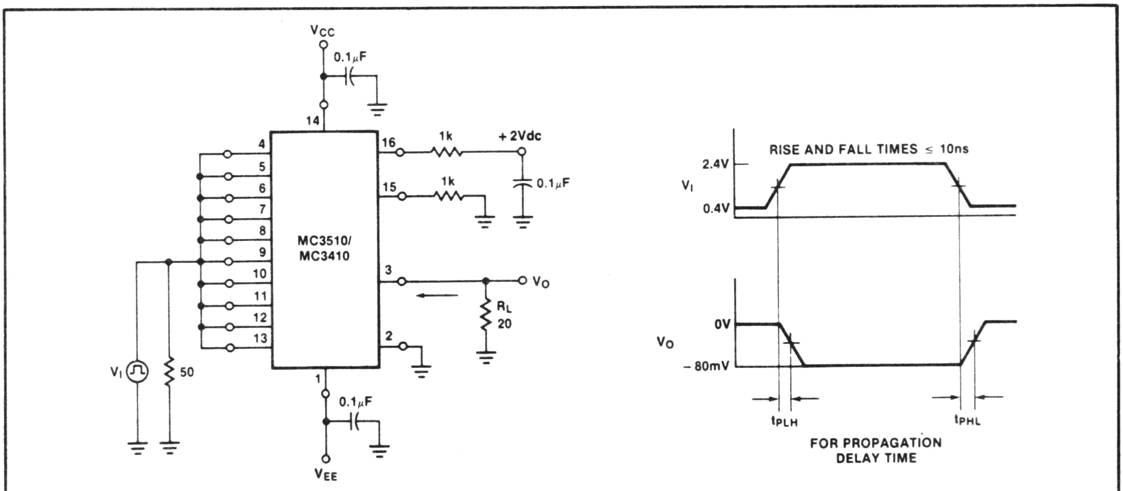

V_CC
0.1μF
14
4
5
6
7
8
9
10
11
12
13
MC3510/
MC3410
16
15
1k
1k
+2Vdc
0.1μF
3
V_O
R_L
20
2
1
0.1μF
V_EE
V_I
50
RISE AND FALL TIMES ≤ 10ns
2.4V
0.4V
V_I
0V
−80mV
V_O
t_PLH
t_PHL
FOR PROPAGATION
DELAY TIME

Figure 8. Propagation Delay Time

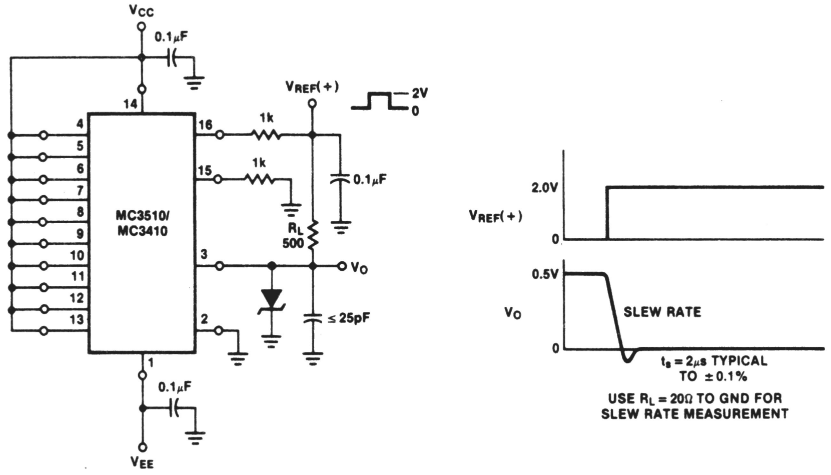
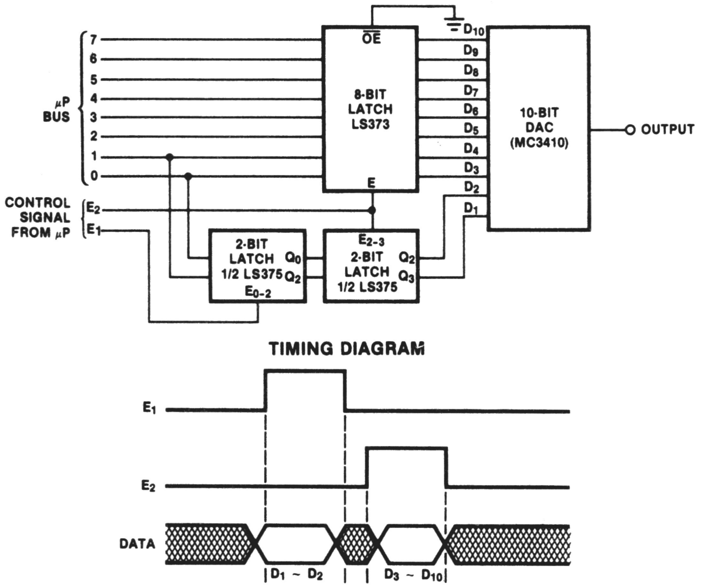

VCC
0.1µF
14
4
5
6
7
8
9
10
11
12
13
MC3510/
MC3410
16
1k
15
1k
VREF(+)
2V
0
0.1µF
RL
500
3
VO
2
≤ 25pF
1
0.1µF
VEE
VREF(+)
2.0V
0
VO
0.5V
0
SLEW RATE
ts = 2µs TYPICAL
TO ±0.1%
USE RL = 20Ω TO GND FOR
SLEW RATE MEASUREMENT

Figure 9. Reference Amplifier Settling Time and Slew Rate

TYPICAL APPLICATIONS


µP
BUS
7
6
5
4
3
2
1
0
CONTROL
SIGNAL
FROM µP
E2
E1
OE
8-BIT
LATCH
LS373
E
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
10-BIT
DAC
(MC3410)
OUTPUT
2-BIT
LATCH
1/2 LS375
Q0
Q2
E0-2
E2-3
2-BIT
LATCH
1/2 LS375
Q2
Q3
TIMING DIAGRAM
E1
E2
DATA
D1 ~ D2
D3 ~ D10

THE VALID DATA WILL BE LATCHED TO THE DAC UNTIL UPDATED WITH E_2 PULSE.
TIMING WILL DEPEND ON THE PROCESSOR USED.

Figure 10. Interfacing 10-Bit DAC with 8-Bit Microprocessor

8-BIT μP-COMPATIBLE D/A CONVERTER

SE/NE5018

DESCRIPTION

The NE5018 is a complete 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most micro-processors.

The chip also comprises a stable voltage reference (5V nominal) and a high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

FEATURES

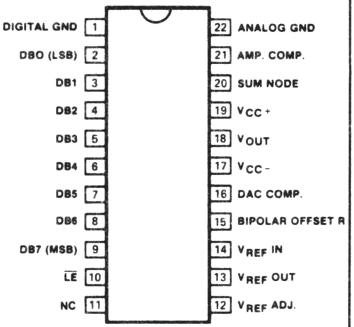
- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Output buffer amplifier**
- **Accurate to ± 1/2 LSB (.19%)**
- **Monotonic to 8 bits**
- **Amplifier and reference both short-circuit protected**
- **Compatible with 8085, 6800 and many other μP's**

APPLICATIONS

- **Precision 8-bit D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- **Measuring instruments**
- **Analog-digital multiplication**

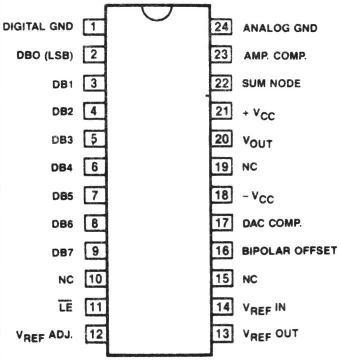
PIN CONFIGURATION

F,N PACKAGE


DIGITAL GND 1
DB0 (LSB) 2
DB1 3
DB2 4
DB3 5
DB4 6
DB5 7
DB6 8
DB7 (MSB) 9
$\overline{LE}$ 10
NC 11
22 ANALOG GND
21 AMP. COMP.
20 SUM NODE
19 $V_{CC}+$
18 V_{OUT}
17 $V_{CC}-$
16 DAC COMP.
15 BIPOLAR OFFSET R
14 V_{REF} IN
13 V_{REF} OUT
12 V_{REF} ADJ.

ORDER NUMBERS
SE/NE5018F,N

D² PACKAGE


DIGITAL GND 1
DBO (LSB) 2
DB1 3
DB2 4
DB3 5
DB4 6
DB5 7
DB6 8
DB7 9
NC 10
$\overline{LE}$ 11
V_{REF} ADJ. 12
24 ANALOG GND
23 AMP. COMP.
22 SUM NODE
21 $+V_{CC}$
20 V_{OUT}
19 NC
18 $-V_{CC}$
17 DAC COMP.
16 BIPOLAR OFFSET
15 NC
14 V_{REF} IN
13 V_{REF} OUT

TOP VIEW
ORDER NUMBER
NE5018D²

NOTES:
1. SOL-Released in Large SO package only.
2. SOL and non-standard pinout.
3. SO and non-standard pinouts.

BLOCK DIAGRAM

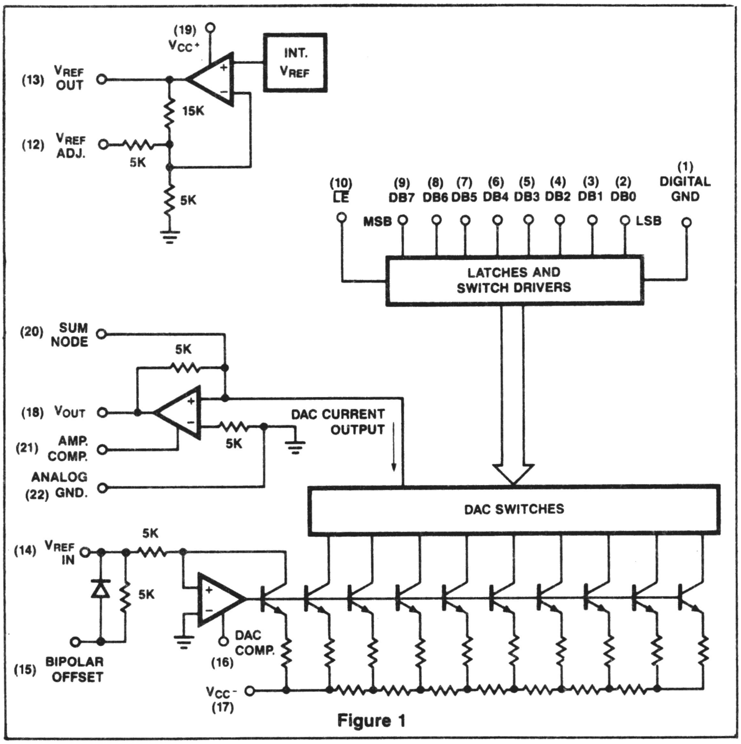

(19) $V_{CC}+$
INT. V_{REF}
(13) V_{REF} OUT
15K
(12) V_{REF} ADJ.
5K
5K
(10) $\overline{LE}$
(9) DB7
(8) DB6
(7) DB5
(6) DB4
(5) DB3
(4) DB2
(3) DB1
(2) DB0
(1) DIGITAL GND
MSB
LSB
LATCHES AND SWITCH DRIVERS
(20) SUM NODE
5K
(18) V_{OUT}
5K
DAC CURRENT OUTPUT
(21) AMP. COMP.
ANALOG (22) GND.
DAC SWITCHES
(14) V_{REF} IN
5K
5K
DAC COMP. (16)
(15) BIPOLAR OFFSET
$V_{CC}-$ (17)

Figure 1

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF}IN$	Voltage at V_{REF} input	12	V
$V_{REF}ADJ$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at V_{REF} OUT	Continuous	
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	
P_D	Power dissipation*		
	-N package	800	mW
	-F package	1000	mW
T_A	Operating temperature range		
	SE5018	−55 to +125	°C
	NE5018	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES

For N package, derate at 120°C/W above 35°C

For F package, derate at 75°C/W above 75°C

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5018. $-55°C \leq T_A \leq 125°C$, NE5018. $0°C \leq T_A \leq 70°C$ unless otherwise specified.[1] Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	SE5018			NE5018			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy				±0.19			±0.19	%FS
$V_{CC}+$	Positive supply voltage		11.4	15		11.4	15		V
$V_{CC}-$	Negative supply voltage		−11.4	−15		−11.4	−15		V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, $2V < V_{IN} < 18V$		0.1	10		0.1	10	μA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, $-5V < V_{IN} < 0.8V$		−2.0	−10		−2.0	−10	μA
V_{FS}	Full scale output voltage	Unipolar operation $V_{REF\ IN} = 5.000V$, $T_A = 25°C$	9.50	9.961	10.50	9.50	9.961	10.50	V
V_{FS}	Full scale output voltage	Bipolar operation $V_{REF\ IN} = 5.000V$, $T_A = 25°C$	4.5 -5.04	+4.961 −5.000	5.5 -4.960	4.5 5.04	+4.961 −5.000	5.5 4.960	V
V_{ZS}	Zero scale voltage		-30	5	+30	-30	5	+30	mV
I_{OS}	Output short circuit current	$T_A = 25°C$ $V_{OUT} = 0V$		15	40		15	40	mA
PSR+(out)	Output power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01		.001	.01	%FS/%VS
PSR−(out)	Output power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq -16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01		.001	.01	%FS/%VS
TC_{FS}	Full scale temperature coefficient	$V_{REF\ IN} = 5.000V$		20			20		ppm/°C
TC_{ZS}	Zero scale temperature coefficient			5			5		ppm/°C

8-BIT µP-COMPATIBLE D/A CONVERTER **SE/NE5018**

DC ELECTRICAL CHARACTERISTICS (Cont'd) $V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5018. $-55°C \leq T_A \leq 125°C$, NE5018. $0°C \leq T_A \leq 70°C$ unless otherwise specified.[1] Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	SE/5018			NE5018			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{REF}	Reference output current	Note 8			3			3	mA
I_{REFSC}	Reference short circuit current	$T_A = 25°C$ $V_{REF\ OUT} = 0V$		15	30		15	30	mA
$PSR+_{(REF)}$	Reference power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, $I_{REF} = 1.0mA$		.003	.01		.003	.01	%VR/%VS
$PSR-_{(REF)}$	Reference power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq 16.5V$,		.003	.01		.003	.01	%VR/%VS
V_{REF}	Reference voltage	$I_{REF} = 1.0mA$ $T_A = 25°C$	4.9	5.0	5.25	4.9	5.0	5.25	V
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$		60			60		ppm/°C
Z_{IN}	DAC V_{REF} IN input impedance	$I_{REF} = 1.0mA$ $T_A = 25°C$	4.15	5.0	5.85	4.15	5.0	5.85	KΩ
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		7	14		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		−10	−15		−10	−15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$		255	435		255	435	mW

NOTE

1. Refer to Figure 2.

AC ELECTRICAL CHARACTERISTICS[2] $V_{CC} = \pm 15V$, $T_A = 25°C$

PARAMETER		TO	FROM	TEST CONDITIONS	SE/NE5018			UNIT
					Min	Typ	Max	
T_{SLH}	Settling time	±½ LSB	Input	All bits low to high[3]		1.8		µs
T_{SHL}	Settling time	±½ LSB	Input	All bits high to low[4]		2.3		µs
t_{plh}	Propagation delay	Output	Input	All bits switched low to high[3]		300		ns
t_{phl}	Propagation delay	Output	Input	All bits switched high to low[4]		150		ns
t_{plsb}	Propagation delay	Output	Input	1 LSB change[3,4]		150		ns
t_{plh}	Propagation delay	Output	$\overline{LE}$	low to high transition[5]		300		ns
t_{phl}	Propagation delay	Output	$\overline{LE}$	high to low transition[6]		150		ns
t_s	Set-up time	$\overline{LE}$	Input	2, 7	100			ns
t_h	Hold time	Input	$\overline{LE}$	2, 7	50			ns
t_{pw}	Latch enable pulse width			2, 7	150			ns

NOTES

2. Refer to Figure 3.
3. See Figure 6.
4. See Figure 7.
5. See Figure 8.
6. See Figure 9.
7. See Figure 10.
8. For reference currents > 3mA, use of an external buffer is required.

DC PARAMETRIC TEST CONFIGURATION

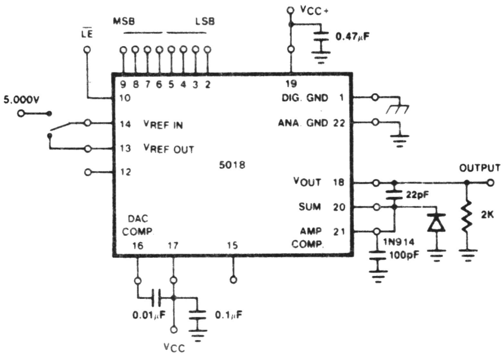

MSB
LSB
LE
VCC+
0.47μF
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
ANA. GND 22
5.000V
14 VREF IN
13 VREF OUT
12
5018
VOUT 18
SUM 20
AMP COMP. 21
OUTPUT
22pF
2K
1N914
100pF
DAC COMP
16
17
15
0.01μF
0.1μF
VCC

Figure 2

AC PARAMETRIC TEST CONFIGUTATION

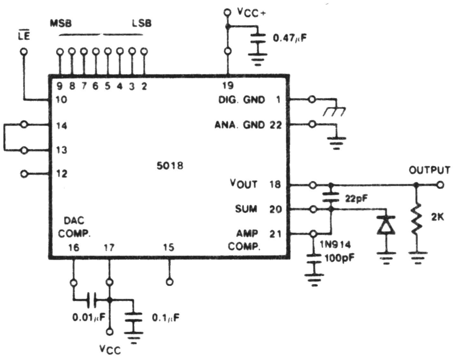

MSB
LSB
LE
VCC+
0.47μF
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
ANA. GND 22
14
13
12
5018
VOUT 18
SUM 20
AMP COMP. 21
OUTPUT
22pF
2K
1N914
100pF
DAC COMP.
16
17
15
0.01μF
0.1μF
VCC

Figure 3

FULL/ZERO SCALE ADJUST—UNIPOLAR OUTPUT (0-10V)

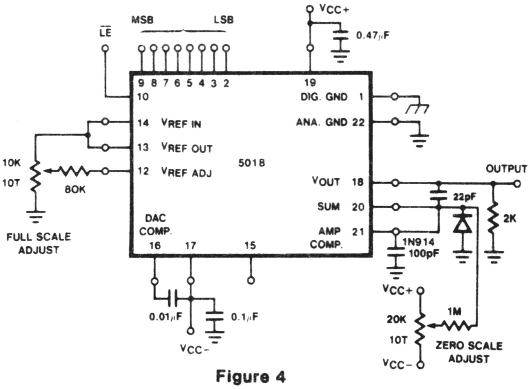

MSB
LSB
LE
VCC+
0.47μF
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
ANA. GND 22
14 VREF IN
13 VREF OUT
12 VREF ADJ
5018
10K
10T
80K
FULL SCALE ADJUST
VOUT 18
SUM 20
AMP COMP. 21
OUTPUT
22pF
2K
1N914
100pF
DAC COMP.
16
17
15
0.01μF
0.1μF
VCC-
VCC+
20K
10T
1M
ZERO SCALE ADJUST
VCC-

Figure 4

BIPOLAR OUTPUT OPERATION (−5 to +5V)

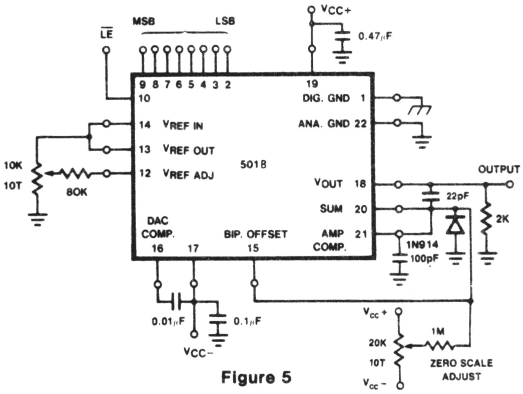

MSB
LSB
LE
VCC+
0.47μF
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
ANA. GND 22
14 VREF IN
13 VREF OUT
12 VREF ADJ
5018
10K
10T
80K
VOUT 18
SUM 20
AMP COMP. 21
OUTPUT
22pF
2K
1N914
100pF
DAC COMP.
BIP. OFFSET
16
17
15
0.01μF
0.1μF
VCC-
Vcc+
20K
10T
1M
ZERO SCALE ADJUST
Vcc-

Figure 5

SETTLING TIME AND PROPAGATION DELAY, LOW TO HIGH DATA

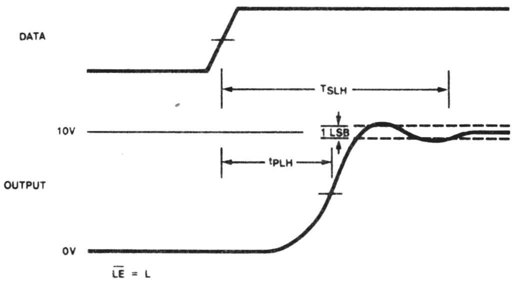

DATA
TSLH
10V
1 LSB
tPLH
OUTPUT
0V
LE = L

Figure 6

SETTLING TIME AND PROPAGATION DELAY, HIGH TO LOW DATA

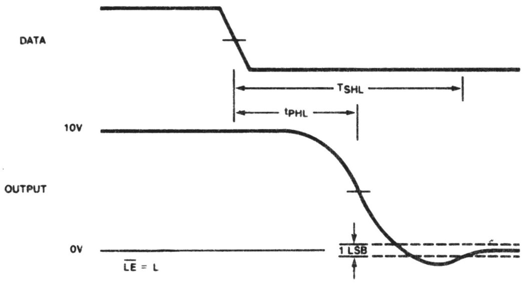

DATA
TSHL
tPHL
10V
OUTPUT
0V
1 LSB
LE = L

Figure 7

PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

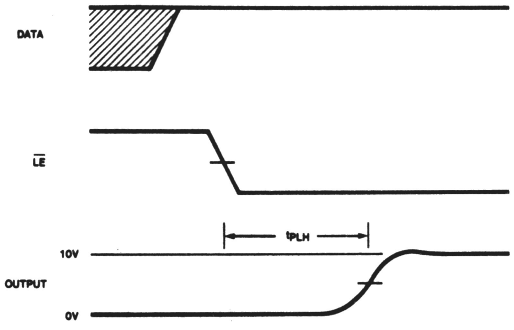

DATA
$\overline{LE}$
t_{PLH}
10V
OUTPUT
0V

Figure 8

PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

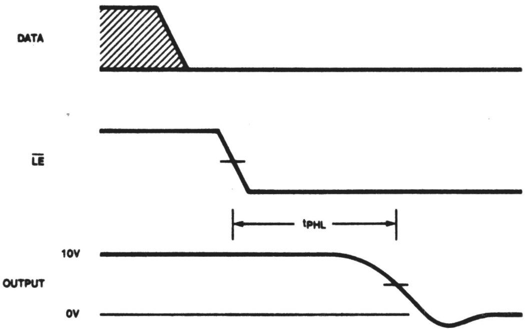

DATA
$\overline{LE}$
t_{PHL}
10V
OUTPUT
0V

Figure 9

LATCH ENABLE PULSE WIDTH, SET-UP AND HOLD TIMES

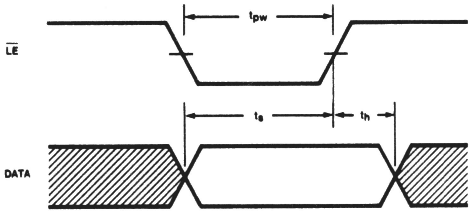

t_{pw}
$\overline{LE}$
t_s
t_h
DATA

Figure 10

8-BIT µP-COMPATIBLE D/A CONVERTER SE/NE5019

DESCRIPTION

The NE5019 is a complete 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most micro-processors.

The chip also comprises a stable voltage reference (5V nominal) and a high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

FEATURES

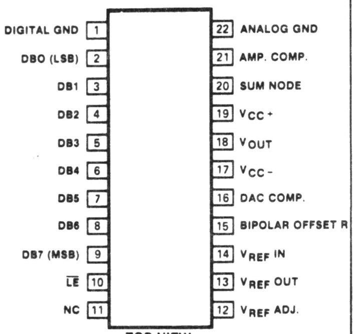
- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Output buffer amplifier**
- **Accurate to ± 1/4 LSB (.1%)**
- **Monotonic to 8 bits**
- **Amplifier and reference both short-circuit protected**
- **Compatible with 8085, 6800 and many other µP's**

APPLICATIONS

- **Precision 8-bit D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- **Measuring instruments**
- **Analog-digital multiplication**

PIN CONFIGURATION

F,N PACKAGE


DIGITAL GND 1
DB0 (LSB) 2
DB1 3
DB2 4
DB3 5
DB4 6
DB5 7
DB6 8
DB7 (MSB) 9
$\overline{LE}$ 10
NC 11
22 ANALOG GND
21 AMP. COMP.
20 SUM NODE
19 V_{CC+}
18 V_{OUT}
17 V_{CC-}
16 DAC COMP.
15 BIPOLAR OFFSET R
14 V_{REF} IN
13 V_{REF} OUT
12 V_{REF} ADJ.

TOP VIEW

ORDER NUMBERS
NE5019F SE5019F
NE5019N

BLOCK DIAGRAM

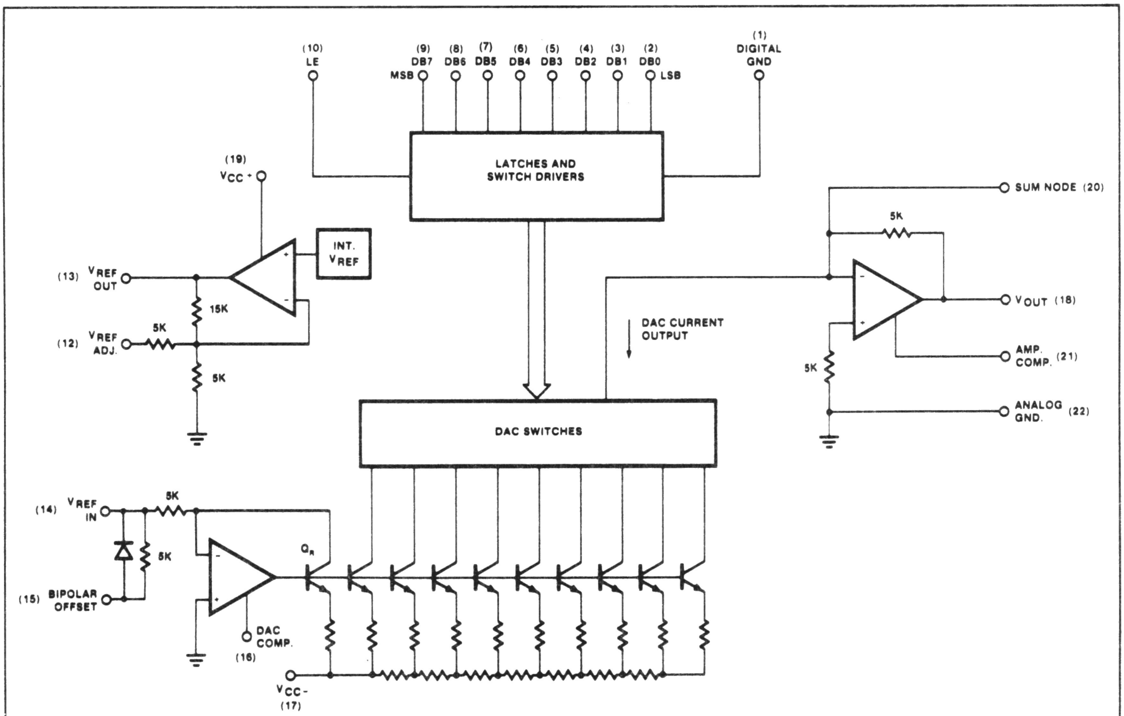

(10) LE
(9) DB7
(8) DB6
(7) DB5
(6) DB4
(5) DB3
(4) DB2
(3) DB1
(2) DB0
MSB
LSB
(1) DIGITAL GND
LATCHES AND SWITCH DRIVERS
(19) V_{CC+}
INT. V_{REF}
(13) V_{REF} OUT
15K
(12) V_{REF} ADJ.
5K
5K
DAC CURRENT OUTPUT
SUM NODE (20)
5K
V_{OUT} (18)
AMP. COMP. (21)
5K
ANALOG GND. (22)
DAC SWITCHES
(14) V_{REF} IN
5K
5K
(15) BIPOLAR OFFSET
Q_R
DAC COMP. (16)
V_{CC-} (17)

Figure 1

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF}IN$	Voltage at V_{REF} input	12	V
$V_{REF}ADJ$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at V_{REF} OUT	Continuous	
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	
P_D	Power dissipation*		
	-N package	800	mW
	-F package	1000	mW
T_A	Operating temperature range		
	SE5019	−55 to +125	°C
	NE5019	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES
For N package, derate at 120°C/W above 35°C
For F package, derate at 75°C/W above 75°C

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5019, $-55°C \leq T_A \leq 125°C$, NE5019, $0°C \leq T_A \leq 70°C$ unless otherwise specified.[1]
Typical values are specified at 25°C

	PARAMETER	TEST CONDITIONS	SE5019			NE5019			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy				±0.1			±0.1	%FS
$V_{CC}+$	Positive supply voltage		11.4	15		11.4	15		V
$V_{CC}-$	Negative supply voltage		−11.4	−15		−11.4	−15		V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, $2V < V_{IN} < 18V$		0.1	10		0.1	10	μA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, $-5V < V_{IN} < 0.8V$		−2.0	−10		−2.0	−10	μA
V_{FS}	Full scale output voltage	Unipolar operation $V_{REF\ IN} = 5.000V$, $T_A = 25°C$	9.50	9.961	10.50	9.50	9.961	10.50	V
V_{FS}	Full scale output voltage	Bipolar operation $V_{REF\ IN} = 5.000V$, $T_A = 25°C$	4.5 -5.040	+4.961 −5.000	5.5 -4.960	4.5 -5.040	+4.961 −5.000	5.5 -4.960	V
V_{ZS}	Zero scale voltage		-30	5	+30	-30	5	+30	mV
I_{OS}	Output short circuit current	$T_A = 25°C$ $V_{OUT} = 0V$		15	40		15	40	mA
$PSR+_{(out)}$	Output power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01		.001	.01	%FS/%VS
$PSR-_{(out)}$	Output power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq -16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01		.001	.01	%FS/%VS
TC_{FS}	Full scale temperature coefficient	$V_{REF\ IN} = 5.000V$		20			20		ppm/°C
TC_{ZS}	Zero scale temperature coefficient			5			5		ppm/°C

NOTE
1. Refer to Figure 2

DC ELECTRICAL CHARACTERISTICS (Cont'd) $V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5019. $-55°C \leq T_A \leq 125°C$, NE5019. $0°C \leq T_A \leq 70°C$ unless otherwise specified.[1] Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	SE5019			NE5019			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{REF}	Reference output current	Note 8			3			3	mA
I_{REFSC}	Reference short circuit current	T_A = 25°C $V_{REF\ OUT}$ = 0V		15	30		15	30	mA
$PSR+_{REF}$	Reference power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, I_{REF} = 1.0mA		.003	.01		.003	.01	%VR/ %VS
$PSR-_{REF}$	Reference power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq 16.5V$,		.003	.01		.003	.01	%VR/ %VS
V_{REF}	Reference voltage	I_{REF} = 1.0mA, T_A = 25°C	4.9	5.0	5.25	4.9	5.0	5.25	V
TC_{REF}	Reference voltage temperature coefficient	I_{REF} = 1.0mA, T_A = 25°C		60			60		ppm/°C
Z_{IN}	DAC V_{REF}IN input impedance	I_{REF} = 1.0mA T_A = 25°C	4.15	5.0	5.85	4.15	5.0	5.85	KΩ
$I_{CC}+$	Positive supply current	$V_{CC}+$ = 15V		7	14		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		−10	−15		−10	−15	mA
P_D	Power dissipation	I_{REF} = 1.0mA, V_{CC} = ±15V		255	435		255	435	mW

NOTE

1. Refer to Figure 2.

AC ELECTRICAL CHARACTERISTICS[2] V_{CC} = ±15V, T_A = 25°C

PARAMETER		TO	FROM	TEST CONDITIONS	SE/NE5019			UNIT
					Min	Typ	Max	
T_{SLH}	Settling time	±½ LSB	Input	All bits low to high[3]		1.8		µs
T_{SHL}	Settling time	±½ LSB	Input	All bits high to low[4]		2.3		µs
t_{plh}	Propagation delay	Output	Input	All bits switched low to high[3]		300		ns
t_{phl}	Propagation delay	Output	Input	All bits switched high to low[4]		150		ns
t_{plsb}	Propagation delay	Output	Input	1 LSB change[3,4]		150		ns
t_{plh}	Propagation delay	Output	$\overline{LE}$	low to high transition[5]		300		ns
t_{phl}	Propagation delay	Output	$\overline{LE}$	high to low transition[6]		150		ns
t_s	Set-up time	$\overline{LE}$	Input	2, 7	100			ns
t_h	Hold time	Input	$\overline{LE}$	2, 7	50			ns
t_{pw}	Latch enable pulse width			2, 7	150			ns

NOTES

2. Refer to Figure 3.
3. See Figure 6.
4. See Figure 7.
5. See Figure 8.
6. See Figure 9.
7. See Figure 10.
8. For reference currents > 3mA, use of an external buffer is required.

DC PARAMETRIC TEST CONFIGURATION

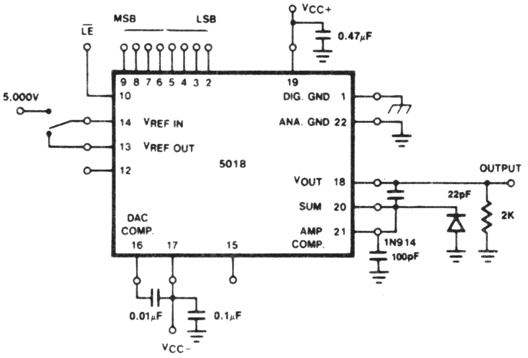

MSB
LSB
LE
VCC+
0.47µF
9 8 7 6 5 4 3 2
19
5.000V
10
DIG. GND 1
14 VREF IN
ANA. GND 22
13 VREF OUT
12
5018
OUTPUT
VOUT 18
SUM 20
22pF
2K
DAC COMP.
AMP COMP. 21
16 17 15
1N914
100pF
0.01µF
0.1µF
VCC−

Figure 2

AC PARAMETRIC TEST CONFIGUTATION

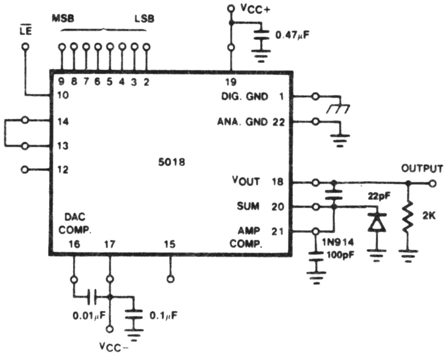

MSB
LSB
LE
VCC+
0.47µF
9 8 7 6 5 4 3 2
19
10
DIG. GND 1
14
ANA. GND 22
13
12
5018
OUTPUT
VOUT 18
SUM 20
22pF
2K
DAC COMP.
AMP COMP. 21
16 17 15
1N914
100pF
0.01µF
0.1µF
VCC−

Figure 3

FULL/ZERO SCALE ADJUST—UNIPOLAR OUTPUT (0-10V)

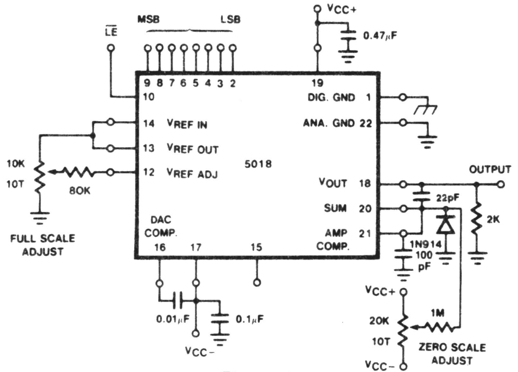

MSB
LSB
LE
VCC+
0.47µF
9 8 7 6 5 4 3 2
19
10
DIG. GND 1
14 VREF IN
ANA. GND 22
13 VREF OUT
10K
10T
80K
12 VREF ADJ
5018
FULL SCALE ADJUST
OUTPUT
VOUT 18
SUM 20
22pF
2K
DAC COMP.
AMP COMP. 21
16 17 15
1N914
100 pF
0.01µF
0.1µF
VCC−
VCC+
20K
10T
1M
ZERO SCALE ADJUST
VCC−

Figure 4

BIPOLAR OUTPUT OPERATION (−5 to +5V)

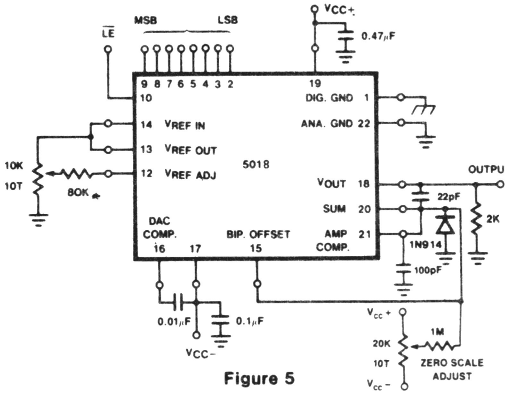

MSB
LSB
LE
VCC+
0.47µF
9 8 7 6 5 4 3 2
19
10
DIG. GND 1
14 VREF IN
ANA. GND 22
13 VREF OUT
10K
10T
80K
12 VREF ADJ
5018
OUTPUT
VOUT 18
SUM 20
22pF
2K
DAC COMP.
BIP. OFFSET
AMP COMP. 21
16 17 15
1N914
100pF
0.01µF
0.1µF
VCC−
VCC+
20K
10T
1M
ZERO SCALE ADJUST
VCC−

Figure 5

SETTLING TIME AND PROPAGATON DELAY, LOW TO HIGH DATA

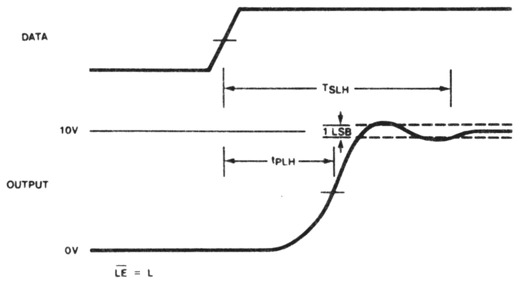

DATA
TSLH
10V
1 LSB
tPLH
OUTPUT
0V
LE = L

Figure 6

SETTLING TIME AND PROPAGATION DELAY, HIGH TO LOW DATA

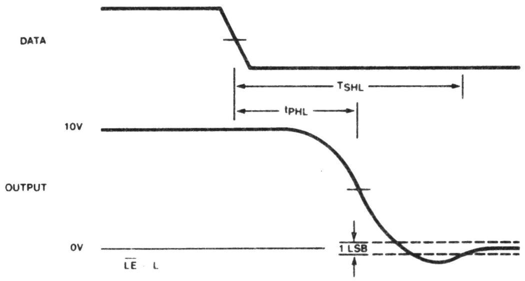

DATA
TSHL
tPHL
10V
OUTPUT
0V
1 LSB
LE L

Figure 7

PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

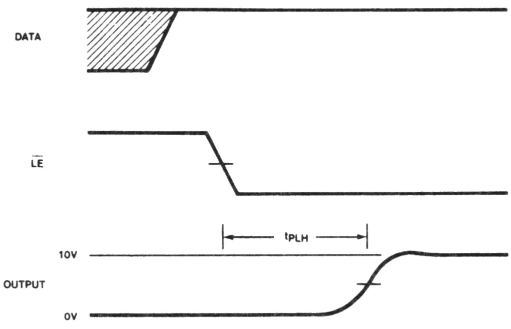

DATA
$\overline{LE}$
t_{PLH}
10V
OUTPUT
0V

Figure 8

PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

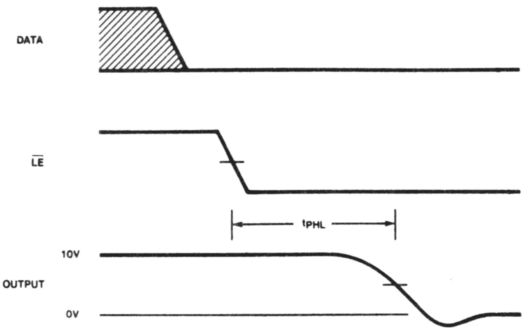

DATA
$\overline{LE}$
t_{PHL}
10V
OUTPUT
0V

Figure 9

LATCH ENABLE PULSE WIDTH, SET-UP AND HOLD TIMES

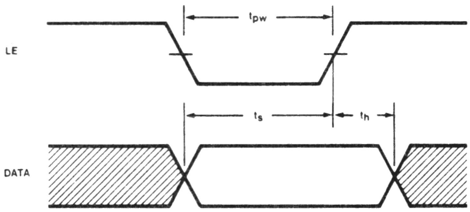

t_{pw}
LE
t_s
t_h
DATA

Figure 10

10-BIT µP-COMPATIBLE D/A CONVERTER NE5020

DESCRIPTION

The NE5020 is a microprocessor-compatible monolithic 10-bit digital to analog converter subsystem. This device offers 10-bit resolution and ±0.1% accuracy and monotonicity guaranteed over full operating temperature range.

Low loading latches, adjustable logic thresholds and addressing capability allow the NE5020 to directly interface with most microprocessor and logic controlled systems.

The NE5020 contains internal voltage reference, DAC switches and resistor ladder. Also, the input buffer and output summing amplifier are included. In addition, the matched application resistors for scaling either unipolar or bipolar output values are included on a single monolithic chip.

The result is a near minimum component count 10-bit resolution DAC system.

FEATURES

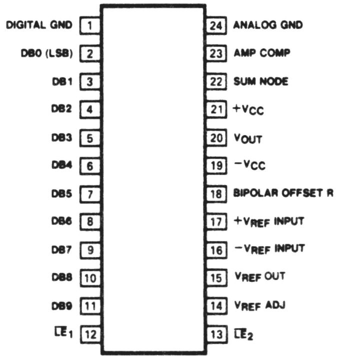
- **10-bit resolution**
- **Guaranteed monotonicity over operating range**
- **±0.1% relative accuracy**
- **Unipolar (0V to +10V) and Bipolar (±5V) output range**
- **Logic bus compatible**
- **5µsec settling time**

APPLICATIONS

- **Precision 10-bit D/A converters**
- **10-bit Analog to Digital converters**
- **Programmable power supplies**
- **Test equipment**
- **Measurement instruments**

PIN CONFIGURATION

F, N PACKAGE


DIGITAL GND 1
DB0 (LSB) 2
DB1 3
DB2 4
DB3 5
DB4 6
DB5 7
DB6 8
DB7 9
DB8 10
DB9 11
$\overline{LE}_1$ 12
24 ANALOG GND
23 AMP COMP
22 SUM NODE
21 +Vcc
20 Vout
19 −Vcc
18 BIPOLAR OFFSET R
17 +Vref INPUT
16 −Vref INPUT
15 Vref OUT
14 Vref ADJ
13 $\overline{LE}_2$

ORDER NUMBERS
NE5020F
NE5020N

BLOCK DIAGRAM

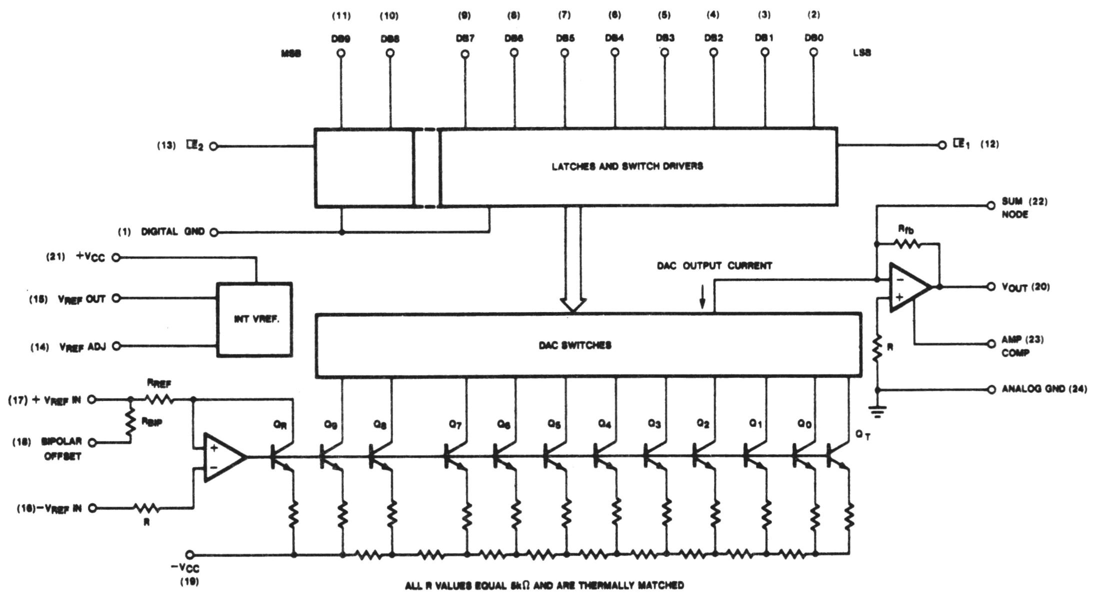

(11) DB9
(10) DB8
(9) DB7
(8) DB6
(7) DB5
(6) DB4
(5) DB3
(4) DB2
(3) DB1
(2) DB0
MSB
LSB
(13) $\overline{LE}_2$
$\overline{LE}_1$ (12)
LATCHES AND SWITCH DRIVERS
(1) DIGITAL GND
(21) +Vcc
(15) Vref OUT
(14) Vref ADJ
INT VREF.
DAC SWITCHES
DAC OUTPUT CURRENT
SUM (22) NODE
Rfb
Vout (20)
AMP (23) COMP
R
ANALOG GND (24)
(17) + Vref IN
RREF
RBIP
(18) BIPOLAR OFFSET
(16)−Vref IN
R
QR
Q9
Q8
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
QT
−Vcc (19)
ALL R VALUES EQUAL 5kΩ AND ARE THERMALLY MATCHED

Figure 1

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
V_{REF} IN	Voltage at $+V_{REF}$ input	12	V
V_{REF} ADJ	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at V_{REF} OUT	Continuous	
I_{OUTSC}	Short-circuit current to ground or either supply at V_{OUT}	Continuous	
P_D	Power dissipation*		
	-N package	800	mW
	F package	1000	mW
T_A	Operating temperature range		
	NE5020	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES
For N package, derate at 120°C/W above 35°C
For F package, derate at 75°C/W above 75°C

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, $0°C \leq T_A \leq 70°C$ unless otherwise specified.[1] Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	NE5020			UNIT
			Min	Typ	Max	
	Resolution				10	Bits
	Monotonicity				10	Bits
	Relative accuracy				±0.1	%FS
$V_{CC}+$	Positive supply voltage		11.4	15	16.5	V
$V_{CC}-$	Negative supply voltage		−11.4	−15	−16.5	V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, $2V < V_{IN} < 18V$		0.1	10	μA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, $-5V < V_{IN} < 0.8V$		−2.0	−10	μA
V_{FS}	Full scale output voltage	Unipolar operation $V_{REF\ IN} = 5.000V$, $T_A = 25°C$	9.5	9.9902	10.5	V
V_{FS}	Full scale output voltage	Bipolar operation	4.5	4.9902	5.5	V
		$V_{REF\ IN} = 5.000V$, $T_A = 25°C$	-5.040	−5.000	-4.960	
V_{ZS}	Zero scale voltage	Unipolar operation	-30	5	+30	mV
I_{OS}	Output short circuit current	$T_A = 25°C$ $V_{OUT} = 0V$		±15	±40	mA
$PSR+_{(out)}$	Output power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01	%FS/%VS
$PSR-_{(out)}$	Output power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq -16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01	%FS/%VS
TC_{FS}	Full scale temperature coefficient	$V_{REF\ IN} = 5.000V$		20		ppmFS/°C
TC_{ZS}	Zero scale temperature coefficient			5		ppmFS/°C

NOTE
1. Refer to Figure 2.

10-BIT μP-COMPATIBLE D/A CONVERTER NE5020

DC ELECTRICAL CHARACTERISTICS (Cont'd) $V_{CC}+ = +15V$, $V_{CC}- = -15V$, $0°C \le T_A \le 70°C$ unless otherwise specified.[1] Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	NE5020			UNIT
			Min	Typ	Max	
I_{REF}[2]	Reference output current				3	mA
$I_{REF\ SC}$	Reference short circuit current	$T_A = 25°C$ $V_{REF\ OUT} = 0V$		15	30	mA
$PSR+_{REF}$	Reference power supply rejection (+)	$V- = -15V$, $13.5V \le V+ \le 16.5V$, $I_{REF} = 1.0mA$		.003	.01	%VR/ %VS
$PSR-_{REF}$	Reference power supply rejection (−)	$V+ = 15V$, $-13.5V \le V- \le 16.5V$,		.003	.01	%VR/ %VS
V_{REF}	Reference voltage	$I_{REF} = 1.0mA$, $T_A = 25°C$	4.9	5.0	5.25	V
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$		60		ppm/°C
Z_{IN}	DAC $V_{REF}IN$ input impedance	$I_{REF} = 1.0mA$		5.0		kΩ
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		−10	−15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$		255	435	mW

NOTE

1. Refer to Figure 2.
2. For I_{REF} OUT greater than 3mA, an external buffer is required.

AC ELECTRICAL CHARACTERISTICS[3] $V_{CC} = \pm 15V$, $T_A = 25°C$

PARAMETER		TO	FROM	TEST CONDITIONS	NE5020			UNIT
					Min	Typ	Max	
T_{SLH}	Settling time	± ½ LSB	Input	All bits low to high[4]		5		μs
T_{SHL}	Settling time	± ½ LSB	Input	All bits high to low[5]		5		μs
t_{plh}	Propagation delay	Output	Input	All bits switched low to high[4]		300		ns
t_{phl}	Propagation delay	Output	Input	All bits switched high to low[5]		150		ns
t_{plsb}	Propagation delay	Output	Input	1 LSB change[4,5]		150		ns
t_{plh}	Propagation delay	Output	$\overline{LE}$	low to high transition[6]		300		ns
t_{phl}	Propagation delay	Output	$\overline{LE}$	high to low transition[7]		150		ns
t_s	Set-up time	$\overline{LE}$	Input	3, 8	100			ns
t_h	Hold time	Input	$\overline{LE}$	3, 8	50			ns
t_{pw}	Latch enable pulse width			3, 8	150			ns

NOTES

3. Refer to Figure 3.
4. See Figure 6.
5. See Figure 7.
6. See Figure 8.
7. See Figure 9.
8. See Figure 10.

DC PARAMETRIC TEST CONFIGURATION

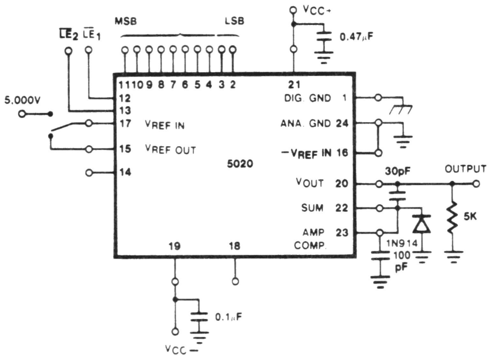

MSB
LSB
$\overline{LE}_2$ $\overline{LE}_1$
VCC+
0.47μF
11 10 9 8 7 6 5 4 3 2
21
12
13
17 VREF IN
15 VREF OUT
14
5.000V
DIG. GND 1
ANA. GND 24
−VREF IN 16
5020
VOUT 20
SUM 22
AMP COMP. 23
19
18
30pF
OUTPUT
5K
1N914
100 pF
0.1μF
VCC−

Figure 2

AC PARAMETRIC TEST CONFIGURATION

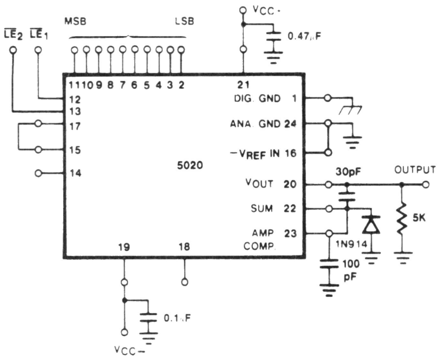

MSB
LSB
$\overline{LE}_2$ $\overline{LE}_1$
VCC+
0.47μF
11 10 9 8 7 6 5 4 3 2
21
12
13
17
15
14
DIG. GND 1
ANA. GND 24
−VREF IN 16
5020
VOUT 20
SUM 22
AMP COMP. 23
19
18
30pF
OUTPUT
5K
1N914
100 pF
0.1μF
VCC−

Figure 3

FULL/ZERO SCALE ADJUST—UNIPOLAR OUTPUT (0–10V)

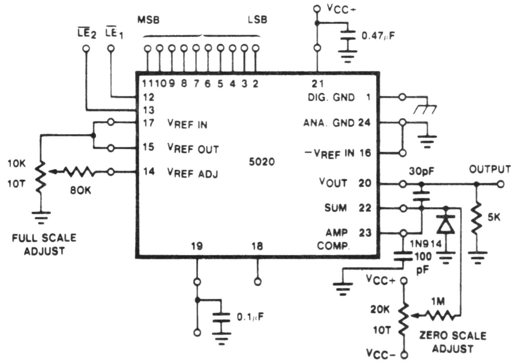

MSB
LSB
$\overline{LE}_2$ $\overline{LE}_1$
VCC+
0.47μF
11 10 9 8 7 6 5 4 3 2
21
12
13
17 VREF IN
15 VREF OUT
14 VREF ADJ
DIG. GND 1
ANA. GND 24
−VREF IN 16
5020
VOUT 20
SUM 22
AMP COMP. 23
19
18
10K
10T
80K
FULL SCALE ADJUST
30pF
OUTPUT
5K
1N914
100 pF
VCC+
20K
10T
1M
ZERO SCALE ADJUST
VCC−
0.1μF

Figure 4

BIPOLAR OUTPUT OPERATION (−5 to +5V)

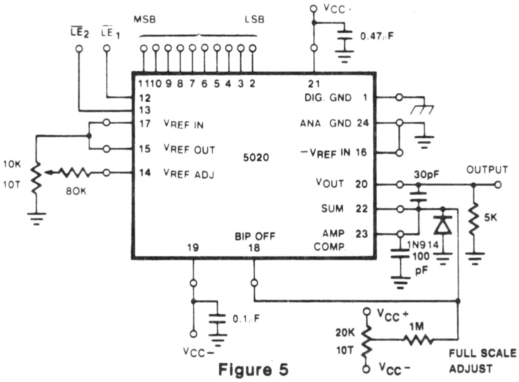

MSB
LSB
$\overline{LE}_2$ $\overline{LE}_1$
VCC+
0.47μF
11 10 9 8 7 6 5 4 3 2
21
12
13
17 VREF IN
15 VREF OUT
14 VREF ADJ
DIG. GND 1
ANA. GND 24
−VREF IN 16
5020
VOUT 20
SUM 22
AMP COMP. 23
19
BIP OFF 18
10K
10T
80K
30pF
OUTPUT
5K
1N914
100 pF
0.1μF
VCC−
VCC+
20K
10T
1M
VCC−
FULL SCALE ADJUST

Figure 5

SETTLING TIME AND PROPAGATION DELAY, LOW TO HIGH DATA

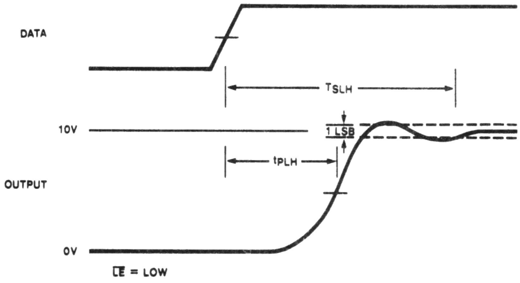


Figure 6

SETTLING TIME AND PROPAGATION DELAY, HIGH TO LOW DATA

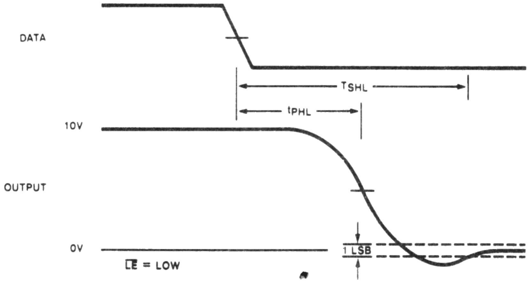


Figure 7

10-BIT μP-COMPATIBLE D/A CONVERTER

NE5020

PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

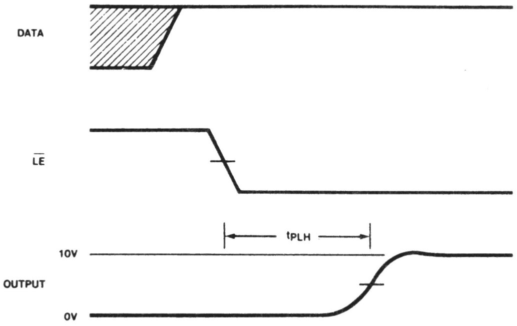


Figure 8

PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

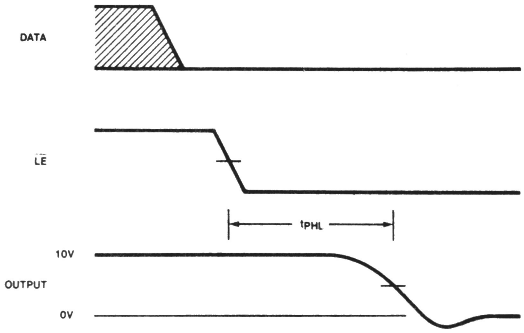


Figure 9

LATCH ENABLE PULSE WIDTH, SET-UP AND HOLD TIMES

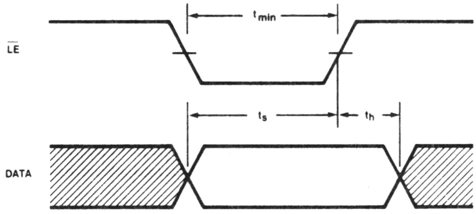


Figure 10

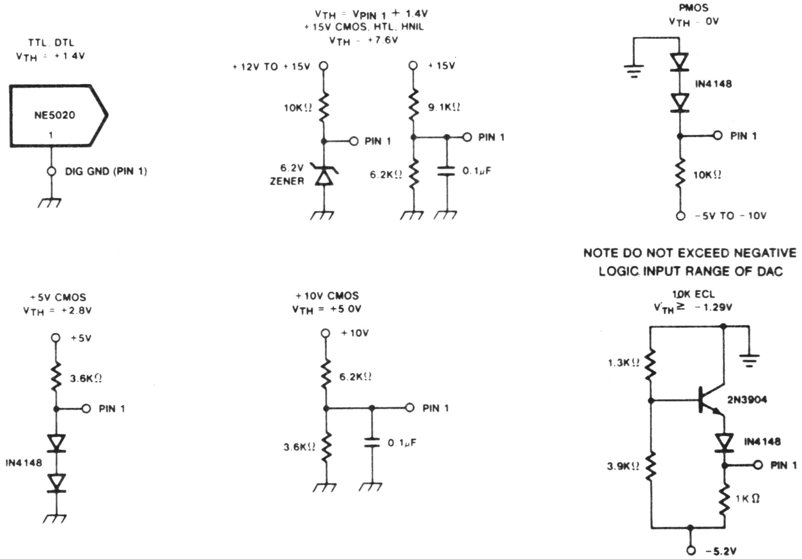

TTL, DTL
V_{TH} = +1.4V
NE5020
1
DIG GND (PIN 1)
V_{TH} = $V_{PIN 1}$ + 1.4V
+15V CMOS, HTL, HNIL
V_{TH} = +7.6V
+12V TO +15V
10KΩ
PIN 1
6.2V ZENER
+15V
9.1KΩ
PIN 1
6.2KΩ
0.1μF
PMOS
V_{TH} = 0V
IN4148
PIN 1
10KΩ
−5V TO −10V
+5V CMOS
V_{TH} = +2.8V
+5V
3.6KΩ
PIN 1
IN4148
+10V CMOS
V_{TH} = +5.0V
+10V
6.2KΩ
PIN 1
3.6KΩ
0.1μF
NOTE DO NOT EXCEED NEGATIVE LOGIC INPUT RANGE OF DAC
10K ECL
V_{TH} ≥ −1.29V
1.3KΩ
2N3904
IN4148
PIN 1
3.9KΩ
1KΩ
−5.2V

Figure 11

10-BIT μP-COMPATIBLE D/A CONVERTER **NE5020**

CIRCUIT DESCRIPTION

The NE5020 provides ten data latches, an internal voltage reference, application resistors, and a scaled output voltage, in addition to the basic DAC components (see block diagram, figure 1).

Latch Circuit

Digital interface with the NE5020 is readily accomplished through the use of two latch enable ports ($\overline{LE}_1$ and $\overline{LE}_2$) and ten data input latches. $\overline{LE}_2$ controls the two most significant bits of data (DB_9 and DB_8) while $\overline{LE}_1$ controls the eight lesser significant bits (DB_7 through DB_0). Both the latch enable ports ($\overline{LE}$) and the data inputs are static and threshold sensitive. When the latch enable ports ($\overline{LE}$) are high (Logic '1') the data inputs become very high impedances and essentially disappear from the data bus. Addressing the $\overline{LE}$ with a low (Logic '0') the latches become active and adapt the logic states present on the data bus. During this state, the output of the DAC will change to the value proportional to the data bus value. When the latch enable returns to a high state, the selected set of data inputs (i.e., depending on which $\overline{LE}$ goes high) memorize' the data bus logic states and the output changes to the unique output value corresponding to the binary word in the latch.

The data inputs are inactive and high impedance (typically requiring $-2\mu A$ for low (.8V max) or $0.1\mu A$ for high (2.0V min)) when the $\overline{LE}$ is high. Any changes on the data bus with $\overline{LE}$ high will have no effect on the DAC output.

The digital logic inputs ($\overline{LE}$ and DB) for the NE5020 utilize a differential input logic system with a threshold level of +1.4 volts with respect to the voltage level on the digital ground pin (Pin 1). Figure 11 details several bias schemes used to provide the proper threshold voltage levels for various logic families.

To be compatible with a bus orientated system the DAC should respond in as short a period as possible to insure full utilization of the microprocessor, controller and I/O control lines. Figure 10 shows the typical timing requirements of the latch and data lines. This figure indicates that data on the data bus should be stable for at least 50nsec after $\overline{LE}$ is changed to a high state.

The independent $\overline{LE}$ ($\overline{LE}_1$ and $\overline{LE}_2$) lines allow for direct interface from an 8 bit data bus (see figure 12). Data for the two MSB's is supplied and stored when $\overline{LE}_2$ is activated low and returned high according to the NE5020 timing requirements. Then $\overline{LE}_1$ is activated low and the remaining eight LSB's of data are transferred into the DAC. With $\overline{LE}_1$ returning high the loading of ten bit data word from an eight bit data bus is complete.

Occasionally the analog output must change to its data value within one data address operation. This is no problem using the NE5020 on a 16 bit bus or any other data bus with 10 or greater data bits.

This can be accomplished from an 8 bit data bus by utilizing an external latch circuit to preload the two MSB data values. Figure 13 shows the circuit configuration.

After preloading (via $\overline{LE}$ pre-load) the external latch with the two MSB values, $\overline{LE}_2$ is activated low and the eight LSB's and the

NE5020 μP INTERFACE 8-BIT DATA BUS EXAMPLE

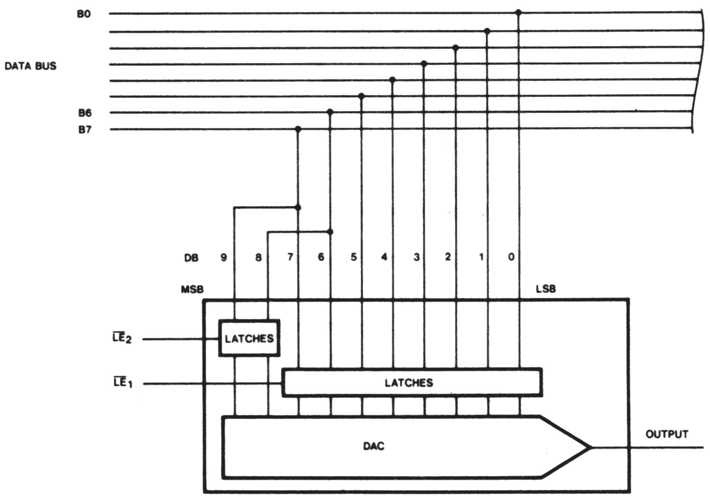


Figure 12

PRELOADING THE 2 MSB'S TO PROVIDE A SINGLE STEP OUTPUT

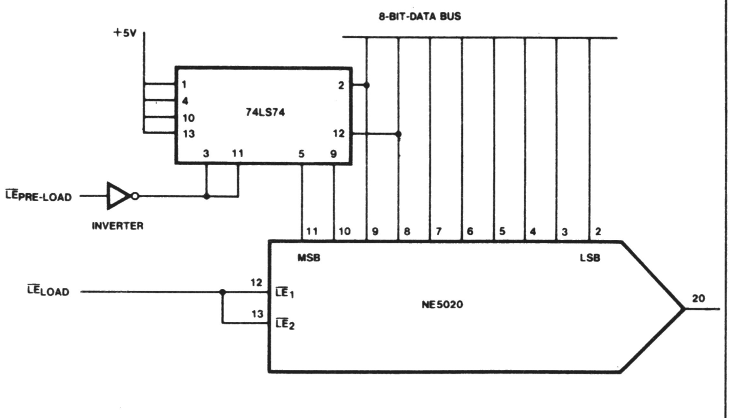


Figure 13

two MSB's are concurrently loaded into the DAC in one address operation. This permits the DAC output to make its appropriate change at one time.

Reference Interface

The NE5020 contains an internal bandgap voltage reference which is designed to have a very low temperature coefficient and excellent long term stability characteristics.

The internal bandgap reference (1.23V) is buffered and amplified to provide the 5 volt reference output. Providing a $V_{REF}ADJ$ (pin 14) allows trimming of the reference output. Utilization of the adjust circuit shown in figure 16 performs not only V_{REF} adjustment but also full scale output adjust. Notice that the $V_{REF}ADJ$ pin is essentially the sum node of an op amp and is sensitive to excessive node capacitance. Any capacitance on the node can be minimized by placing the external resistors as close as possible to the $V_{REF}ADJ$ pin and observing good layout practices.

The V_{REF} out node can drive loads greater than the DAC V_{REF} input requirements and can be used as an excellent system voltage reference. However, to minimize load effects on the DAC system accuracy, it is recommended that a buffer amplifier is used.

Input Amplifier

The DAC reference amplifier is a high gain internally compensated op amp used to convert the input reference voltage to a precision bias current for the DAC ladder network.

Figure 1 details the input reference amplifier and current ladder. The voltage to current converter of the DAC amp will generate a 1mA reference current through Q_R with a 5 volt V_{REF}. This current sets the input bias to the ladder network. Data bit 9 (DB_9)(Q_9), when turned on, will mirror this current and will contribute 1mA to the output. DB_8 (Q_8) will contribute ½ of that value or 0.5mA and so on. These current values act as current sinks and will add at the sum node to produce a DAC ladder to sum node function of:

$$I_{OUT} = \frac{2V_{REF}}{R_{REF}}\left(\frac{DB9}{2} + \frac{DB8}{4} + \frac{DB7}{8} + \frac{DB6}{16} + \frac{DB5}{32} + \frac{DB4}{64} + \frac{DB3}{128} + \frac{DB2}{256} + \frac{DB1}{512} + \frac{DB0}{1024}\right).$$

Because of the fixed internal compensation of the reference amp, the slew rate is limited to typically 0.7V/µsec and source impedances at the V_{REF} INPUT greater than 5kΩ should be avoided to maintain stability.

The $-V_{REF}$ INPUT pin is uncommitted to allow utilization of negative polarity reference voltages. In this mode $+V_{REF}$ INPUT is grounded and the negative reference is tied directly to the $-V_{REF}$ INPUT. The $-V_{REF}$ INPUT contains a 5kΩ resistor that matches a like resistor in the $+V_{REF}$ INPUT to reduce voltage offset caused by op amp input bias currents.

Output Amplifier and Interface

The NE5020 provides an on chip output op amp to eliminate the need for additional external active circuits. Its two stage design with feed forward compensation allows it to slew at 15V/µsec and settle to within ±½LSB in 5µsec. These times are typical when driving the rated loads of $R_L \geq 5k$ and $C_L \leq 50pF$ with recommended values of $C_{FF} = 1nF$ and $C_{FB} = 30pF$. Typical input offset voltages of 5mV and 50k open loop gain insure an accurate current to voltage conversion is performed when using the on chip R_{FB} resistor. R_{FB} is matched to R_{REF} and R_{BIP} to maintain accurate voltage gain over operating conditions. The diode shown from ground to sum node prevents the DAC current switches from saturating the op amp during large signal transitions which would otherwise increase the settling time.

The output op amp also incorporates output short circuit protection for both positive and negative excursions. During this fault condition I_{OUT} will limit at ±15mA typical. Recovery from this condition to rated accuracy will be determined by duration of short circuit and die temperature stabilization.

Bipolar Output Voltage

The NE5020 includes a thermally matched resistor, R_{BIP}, to offset the output voltage by 5 volts to obtain −5V to +5V output voltage range operation. This is accomplished by shorting pins 18 and 22 (see figure 14). This connection produces a current equal to ($V_{REF\ IN} - V_{sum\ node}$) ÷ R_{BIP}, (1mA nominal), which is injected into the sum node. Since full scale current out is approximately 2mA (1.9980mA), (2mA − 1mA)5k = 5V will appear at the output. For zero DAC output currents, 1mA is still injected into sum mode and $V_{OUT} = -(5k)(1mA) = -5V$. Zero scale adjust and full scale adjust are performed as described below, noting that full scale voltage is now approximately +5 volts, zero scale adjust may be used to trim V_{OUT} = 0.00 with the MSB high or V_{OUT} = −5.0V with all bits off.

Zero Scale Adjustment

The method of trimming the small offset error that may exist when all data bits are low is shown in figure 15. The trim is the result of injecting a current from resistor R_2 that counteracts the error current. Adjusting potentiometer R_1 until V_{OUT} equals 0.000 volts in the unipolar mode or −5.000 volts in the bipolar mode (see bipolar section) accomplishes this trim.

Full Scale Adjustment

A recommended full scale adjustment circuit when using the internal voltage reference is shown in figure 16. Potentiometer R_3 is adjusted until V_{OUT} equals 9.99023V. In many applications where the absolute accu-

BIPOLAR OUTPUT

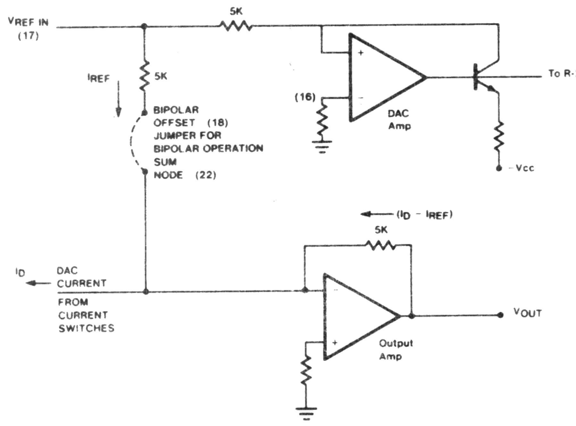


Figure 14

racy of full scale is of low importance when compared to the other system accuracy factors, then this adjustment circuit is optional.

As resistors R_{REF}, R_{fb} and R_{BIP} shown in figure 1 are integrated in close proximity, they match and track in value closely over wide ambient temperature variations. Typical matching is less than ±0.3% which implies that typical full scale (or gain) error is less than ±0.3% of ideal full scale value.

ZERO SCALE ADJUSTMENT

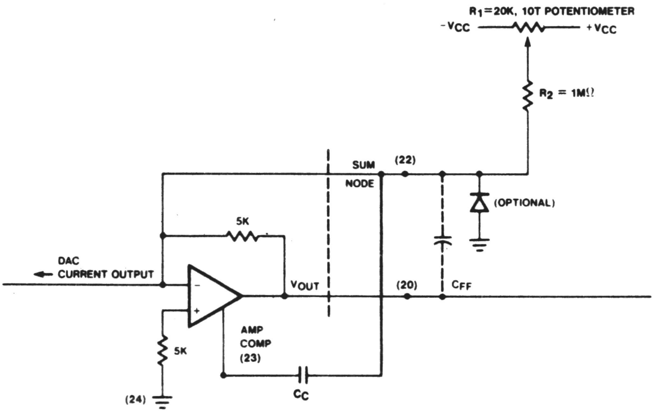

R1=20K, 10T POTENTIOMETER
-VCC
+VCC
R2 = 1MΩ
SUM NODE
(22)
(OPTIONAL)
5K
DAC
CURRENT OUTPUT
VOUT
(20)
CFF
AMP COMP (23)
5K
(24)
CC

Figure 15

REFERENCE ADJUST CIRCUIT

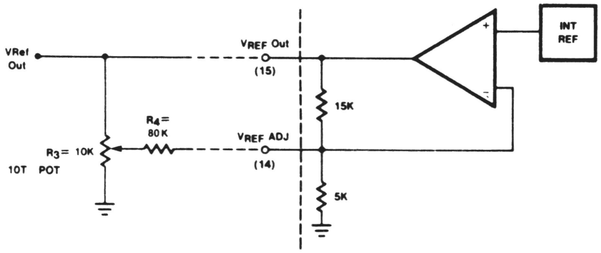

INT REF
VRef Out
VREF Out
(15)
15K
R4= 80K
R3= 10K
10T POT
VREF ADJ
(14)
5K

Figure 16

8-BIT µP-COMPATIBLE D/A CONVERTER—CURRENT OUTPUT SE/NE5118

DESCRIPTION

The NE5118 is a high-speed 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most microprocessors.

The chip also comprises a stable voltage reference (5V nominal). The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output has high voltage compliance increasing versatility.

FEATURES

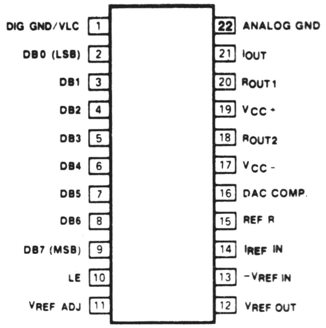
- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Fast settling output current—200ns**
- **Accurate to ± 1/2 LSB (.19%)**
- **Monotonic to 8 bits**
- **Reference short-circuit protected**
- **Compatible with 8086, 6800 and many other µP's**

APPLICATIONS

- **Precision 8-bit D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- **Measuring instruments**
- **Analog-digital multiplication**
- **CRT display drivers**
- **High-speed modems**

PIN CONFIGURATION

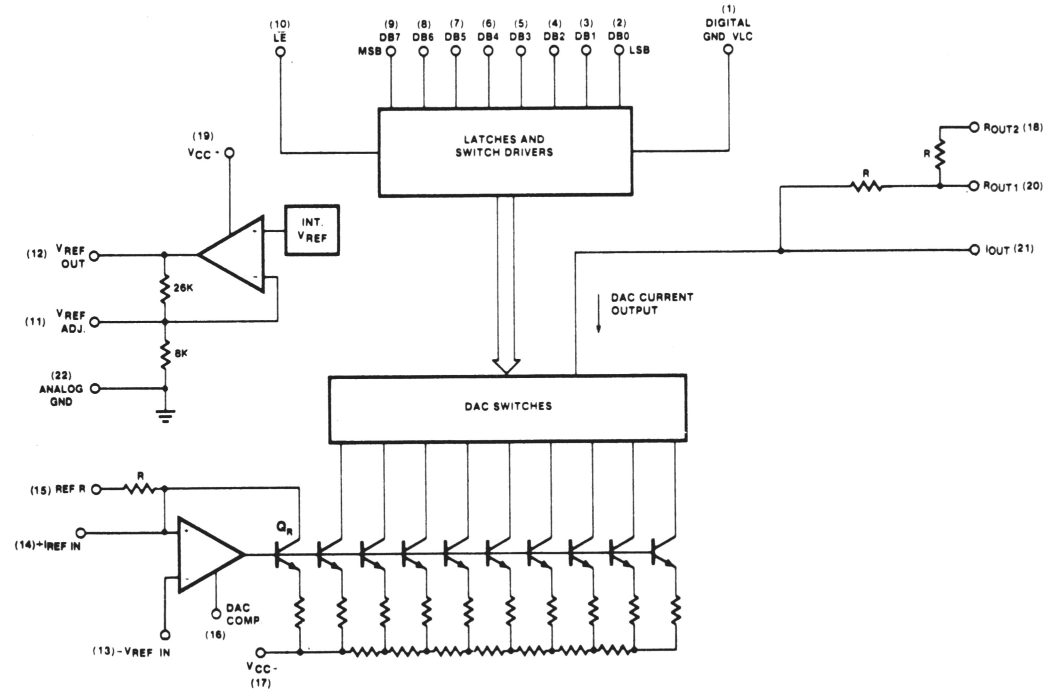
F,N PACKAGE


DIG GND/VLC 1
DB0 (LSB) 2
DB1 3
DB2 4
DB3 5
DB4 6
DB5 7
DB6 8
DB7 (MSB) 9
LE 10
VREF ADJ 11
22 ANALOG GND
21 IOUT
20 ROUT1
19 VCC+
18 ROUT2
17 VCC-
16 DAC COMP.
15 REF R
14 IREF IN
13 -VREF IN
12 VREF OUT

TOP VIEW

ORDER NUMBERS
NE5118F SE5118F
NE5118N

BLOCK DIAGRAM


(10) LE
(9) DB7 MSB
(8) DB6
(7) DB5
(6) DB4
(5) DB3
(4) DB2
(3) DB1
(2) DB0 LSB
(1) DIGITAL GND VLC
LATCHES AND SWITCH DRIVERS
(19) VCC+
INT. VREF
(12) VREF OUT
26K
(11) VREF ADJ.
8K
(22) ANALOG GND
ROUT2 (18)
R
R
ROUT1 (20)
IOUT (21)
DAC CURRENT OUTPUT
DAC SWITCHES
(15) REF R
R
(14)+IREF IN
QR
DAC COMP
(16)
(13)-VREF IN
VCC-
(17)

All R values equal 5kΩ and are thermally matched.

Figure 1

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF}IN$	Voltage at R_{REF} input	12	V
$V_{REF}ADJ$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at V_{REF} OUT	Continuous	
I_{REFIN}	Reference input current (Pin 14)	3	mA
P_D	Power dissipation*		
	-N package	800	mW
	-F package	1000	mW
T_A	Operating temperature range		
	SE5118	−55 to +125	°C
	NE5118	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES

For N package, derate at 120°C/W above 35°C

For F package, derate at 75° C/W above 75°C

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5118. $-55°C \leq T_A \leq 125°C$, NE5118. $0°C \leq T_A \leq 70°C$ unless otherwise specified. Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	SE5118			NE5118			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy				±0.19			±0.19	%FS
$V_{CC}+$	Positive supply voltage		11.4	15		11.4	15		V
$V_{CC}-$	Negative supply voltage		−11.4	−15		−11.4	−15		V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, $2V < V_{IN} < 18V$		0.1	10		0.1	10	µA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, $-5V < V_{IN} < 0.8V$		−2.0	−10		−2.0	−10	µA
I_{FS}	Full scale output current	Unipolar operation $V_{REF\ IN} = 5.000V$, $T_A = 25°C$	1.90	1.992	2.10	1.90	1.992	2.10	mA
I_{ZS}	Zero scale current		-6	1	+6	-6	1	+6	µA
V_{REF}	Reference voltage	$I_{REF} = 1mA$ $T_A = 25°C$	4.9	5.0	5.25	4.9	5.0	5.25	V
$PSR+_{(out)}$	Output power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01		.001	.01	%FS/%VS
$PSR-_{(out)}$	Output power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq -16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01		.001	.01	%FS/%VS
TC_{FS}	Full scale temperature coefficient	$V_{REFIN} = 5.000V$[1]		20			20		ppm/°C
TC_{ZS}	Zero scale temperature coefficient	$I_{REFIN} = 1.00mA$[2]		5			5		ppm/°C

NOTES

1. This is for voltage out only. See Unipolar Voltage Output schematic.
2. This is for current output mode.

DC ELECTRICAL CHARACTERISTICS

(Cont'd) $V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5118. $-55°C \leq T_A \leq 125°C$, NE5118. $0°C \leq T_A \leq 70°C$ unless otherwise specified. Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	SE5118			NE5118			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{REF}	Reference output current	Note 1			3			3	mA
I_{REFSC}	Reference short circuit current	$T_A = 25°C$ $V_{REF\ OUT} = 0V$		15	30		15	30	mA
$PSR+_{(REF)}$	Reference power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, $I_{REF} = 1.0mA$		.003	.01		.003	.01	%VR/ %VS
$PSR-_{(REF)}$	Reference power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq 16.5V$, $I_{REF} = 1.0mA$		.003	.01		.003	.01	%VR/ %VS
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$		60			60		ppm/°C
Z_{IN}	DAC $R_{REF}IN$ input impedance			5.0			5.0		kΩ
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		7	14		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		−10	−15		−10	−15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$		255	435		255	435	mW

AC ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 15V$, $T_A = 25°C$

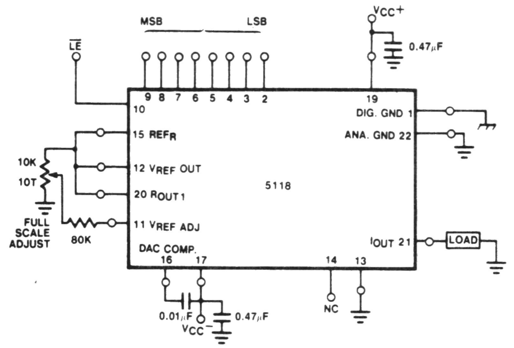
PARAMETER		TO	FROM	TEST CONDITIONS	SE/NE5118			UNIT
					Min	Typ	Max	
T_{SLH}	Settling time	± ½ LSB	Input	All bits Low-to-high		200		ns
T_{SHL}	Settling time	± ½ LSB	Input	All bits High-to-low		200		ns
t_{PLH}	Propagation delay	Output	Input	All bits switched Low-to-high		60		ns
t_{PHL}	Propagation delay	Output	Input	All bits switched High-to-low		60		ns
t_{PLSB}	Propagation delay	Output	Input	1 LSB change		60		ns
t_{PLH}	Propagation delay	Output	$\overline{LE}$	Low-to-high transition		60		ns
t_{PHL}	Propagation delay	Output	$\overline{LE}$	High-to-low transition		60		ns
t_s	Set-up time	$\overline{LE}$	Input		100			ns
t_h	Hold time	Input	$\overline{LE}$		50			ns
t_{pw}	Latch enable pulse width				150			ns

NOTES

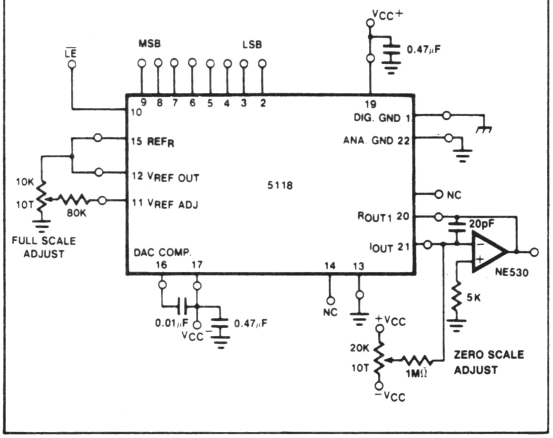
1. For reference currents > 3mA, use of an external buffer is required.

8-BIT μP-COMPATIBLE D/A CONVERTER—CURRENT OUTPUT SE/NE5118

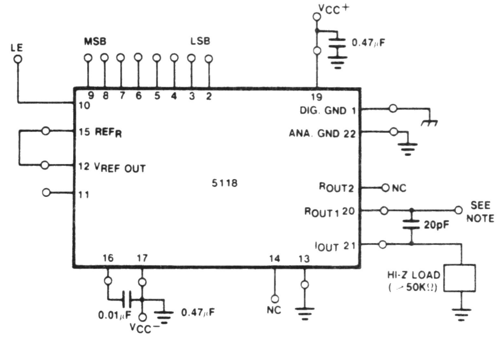
BIPOLAR OUTPUT OPERATION (−1mA TO +1mA)


MSB
LSB
Vcc+
0.47μF
LE
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
15 REFR
ANA. GND 22
10K
10T
12 VREF OUT
20 ROUT1
5118
FULL SCALE ADJUST
80K
11 VREF ADJ
DAC COMP.
16 17
14 13
IOUT 21
LOAD
0.01μF
0.47μF
Vcc−
NC

UNIPOLAR VOLTAGE OUTPUT (0 →+10V)


Vcc+
0.47μF
MSB
LSB
LE
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
15 REFR
ANA. GND 22
12 VREF OUT
5118
10K
10T
80K
11 VREF ADJ
NC
ROUT1 20
20pF
FULL SCALE ADJUST
DAC COMP.
16 17
14 13
IOUT 21
NE530
5K
0.01μF
0.47μF
Vcc−
NC
+Vcc
20K
10T
1MΩ
ZERO SCALE ADJUST
−Vcc

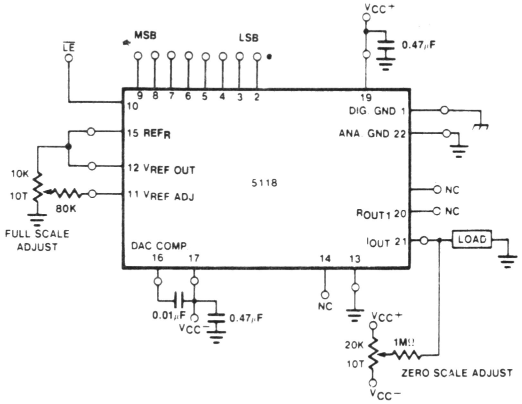
FAST VOLTAGE OUTPUT


Vcc+
0.47μF
LE
MSB
LSB
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
15 REFR
ANA. GND 22
12 VREF OUT
11
5118
ROUT2
NC
ROUT1 20
SEE NOTE
20pF
IOUT 21
16 17
14 13
HI-Z LOAD (>50KΩ)
0.01μF
0.47μF
Vcc−
NC

NOTE

DATA INPUT CODE	VOLTAGE OUTPUT (PIN 21)	
0 0 0 0 0 0 0 0	+10V	0V
1 1 1 1 1 1 1 1	0V	−10V
	Pin 20 tied to +10V	Pin 20 tied to 0V

BASIC UNIPOLAR CURRENT OUTPUT (0 →−2mA)


Vcc+
0.47μF
MSB
LSB
LE
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
15 REFR
ANA. GND 22
12 VREF OUT
5118
10K
10T
80K
11 VREF ADJ
NC
NC
FULL SCALE ADJUST
ROUT1 20
DAC COMP
16 17
14 13
IOUT 21
LOAD
0.01μF
0.47μF
Vcc−
NC
Vcc+
20K
10T
1MΩ
ZERO SCALE ADJUST
Vcc−

8-BIT µP-COMPATIBLE D/A CONVERTER—CURRENT OUTPUT SE/NE5119

DESCRIPTION

The SE/NE5119 is a high-speed 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have iput latches, controlled by a latch enable pin. The data and latch enable inputs are ultralow loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{\text{LE}}$ input is in he low state. When $\overline{\text{LE}}$ goes high, the input data present at the moment or transition is latched and retained until $\overline{\text{LE}}$ again goes low. This feature allows easy compatibility with most microprocessors.

The chip also comprises a stable voltage reference (5V nominal). The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output has high voltage compliance increasing versatility.

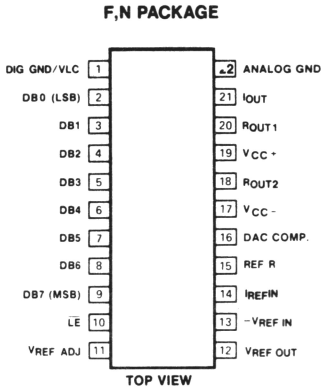
FEATURES

- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Fast settling output current—200ns**
- **Accurate to ± 1/4 LSB (.1%)**
- **Monotonic to 8 bits**
- **Reference short-circuit protected**
- **Compatible with 8086, 6800 and many other µP's**

APPLICATIONS

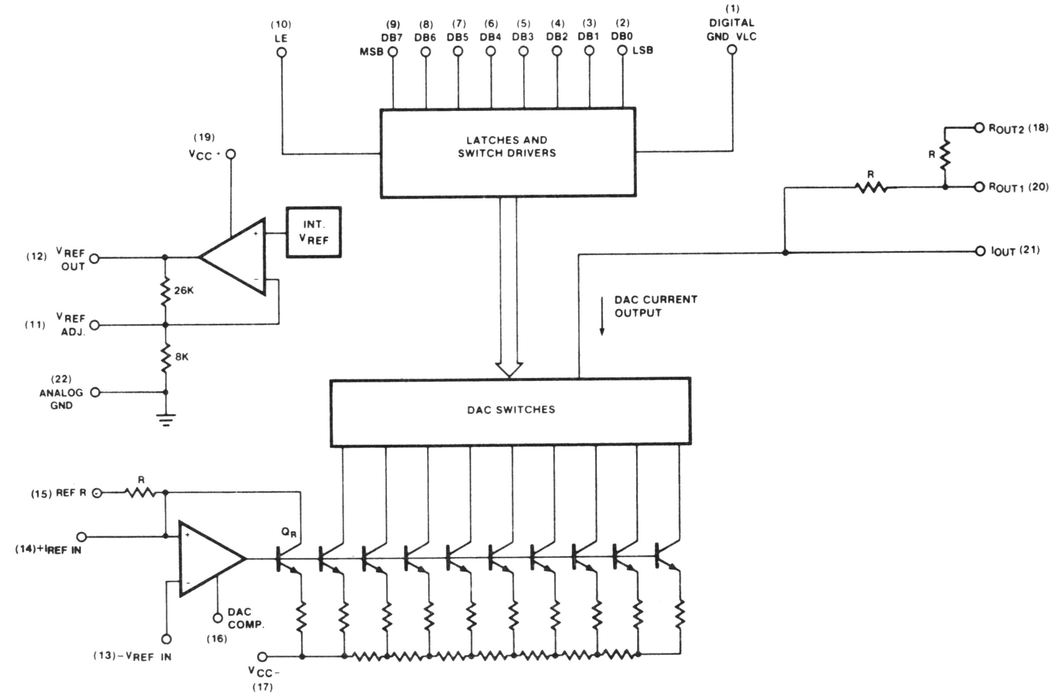
- **Precision 8-bit D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- **Measuring instruments**
- **Analog-digital multiplication**
- **CRT display drivers**
- **High-speed modems**

PIN CONFIGURATION


F,N PACKAGE
DIG GND/VLC 1
DB0 (LSB) 2
DB1 3
DB2 4
DB3 5
DB4 6
DB5 7
DB6 8
DB7 (MSB) 9
$\overline{\text{LE}}$ 10
VREF ADJ 11
22 ANALOG GND
21 IOUT
20 ROUT1
19 VCC+
18 ROUT2
17 VCC-
16 DAC COMP.
15 REF R
14 IREFIN
13 -VREF IN
12 VREF OUT
TOP VIEW

ORDER NUMBERS
NE5119F SE5119F
NE5119N

BLOCK DIAGRAM


(10) LE
(9) DB7 MSB
(8) DB6
(7) DB5
(6) DB4
(5) DB3
(4) DB2
(3) DB1
(2) DB0 LSB
(1) DIGITAL GND VLC
LATCHES AND SWITCH DRIVERS
(19) VCC+
INT. VREF
(12) VREF OUT
26K
(11) VREF ADJ.
8K
(22) ANALOG GND
ROUT2 (18)
R
R
ROUT1 (20)
IOUT (21)
DAC CURRENT OUTPUT
DAC SWITCHES
(15) REF R
R
(14)+IREF IN
QR
DAC COMP. (16)
(13)-VREF IN
VCC- (17)

All R values equal 5kΩ and are thermally matched.

Figure 1

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
$V_{CC}+$	Positive supply voltage	18	V
$V_{CC}-$	Negative supply voltage	−18	V
V_{IN}	Logic input voltage	0 to 18	V
$V_{REF}IN$	Voltage at R_{REF} input	12	V
$V_{REF}ADJ$	Voltage at V_{REF} adjust	0 to V_{REF}	V
V_{SUM}	Voltage at sum node	12	V
I_{REFSC}	Short-circuit current to ground at V_{REF} OUT	Continuous	
$I_{REF_{IN}}$	Reference input current (Pin 14)	3	mA
P_D	Power dissipation*		
	-N package	800	mW
	-F package	1000	mW
T_A	Operating temperature range		
	SE5119	−55 to +125	°C
	NE5119	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES

For N package, derate at 120°C/W above 35°C

For F package, derate at 75° C/W above 75°C

DC ELECTRICAL CHARACTERISTICS

$V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5119. $-55°C \leq T_A \leq 125°C$, NE5119. $0°C \leq T_A \leq 70°C$ unless otherwise specified. Typical values are specified at 25°C

	PARAMETER	TEST CONDITIONS	SE5119			NE5119			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Relative accuracy				±0.1			±0.1	%FS
$V_{CC}+$	Positive supply voltage		11.4	15		11.4	15		V
$V_{CC}-$	Negative supply voltage		−11.4	−15		−11.4	−15		V
$V_{IN(1)}$	Logic "1" input voltage	Pin 1 = 0V	2.0			2.0			V
$V_{IN(0)}$	Logic "0" input voltage	Pin 1 = 0V			0.8			0.8	V
$I_{IN(1)}$	Logic "1" input current	Pin 1 = 0V, $2V<V_{IN}<18V$		0.1	10		0.1	10	μA
$I_{IN(0)}$	Logic "0" input current	Pin 1 = 0V, $-5V<V_{IN}<0.8V$		−2.0	−10		−2.0	−10	μA
I_{FS}	Full scale output current	Unipolar operation $V_{REF\ IN} = 5.000V$, $T_A = 25°C$	1.90	1.992	2.10	1.90	1.992	2.10	mA
I_{ZS}	Zero scale current			1			1		μA
V_{REF}	Reference voltage	$I_{REF} = 1mA$ $T_A = 25°C$	4.9	5.0	5.25	4.9	5.0	5.25	V
$PSR+_{(out)}$	Output power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01		.001	.01	%FS/%VS
$PSR-_{(out)}$	Output power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq -16.5V$, external $V_{REF\ IN} = 5.000V$		.001	.01		.001	.01	%FS/%VS
TC_{FS}	Full scale temperature coefficient	$V_{REF_{IN}} = 5.000V$[1]		20			20		ppm/°C
TC_{ZS}	Zero scale temperature coefficient	$I_{REF_{IN}} = 1.00mA$[2]		5			5		ppm/°C

NOTES

1. This is for voltage out only. See Unipolar Voltage Output schematic
2. This is for current output mode

DC ELECTRICAL CHARACTERISTICS

(Cont'd) $V_{CC}+ = +15V$, $V_{CC}- = -15V$, SE5119. $-55°C \leq T_A \leq 125°C$, NE5119. $0°C \leq T_A \leq 70°C$ unless otherwise specified. Typical values are specified at 25°C

PARAMETER		TEST CONDITIONS	SE5119			NE5119			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{REF}	Reference output current	Note 1			3			3	mA
I_{REFSC}	Reference short circuit current	$T_A = 25°C$ $V_{REF\ OUT} = 0V$		15	30		15	30	mA
$PSR+_{(REF)}$	Reference power supply rejection (+)	$V- = -15V$, $13.5V \leq V+ \leq 16.5V$, $I_{REF} = 1.0mA$		.003	.01		.003	.01	%VR/ %VS
$PSR-_{(REF)}$	Reference power supply rejection (−)	$V+ = 15V$, $-13.5V \leq V- \leq 16.5V$, $I_{REF} = 1.0mA$		.003	.01		.003	.01	%VR/ %VS
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$		60			60		ppm/°C
Z_{IN}	DAC $R_{REF}IN$ input impedance			5.0			5.0		kΩ
$I_{CC}+$	Positive supply current	$V_{CC}+ = 15V$		7	14		7	14	mA
$I_{CC}-$	Negative supply current	$V_{CC}- = -15V$		−10	−15		−10	−15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$		255	435		255	435	mW

AC ELECTRICAL CHARACTERISTICS

$V_{CC} = \pm 15V$, $T_A = 25°C$

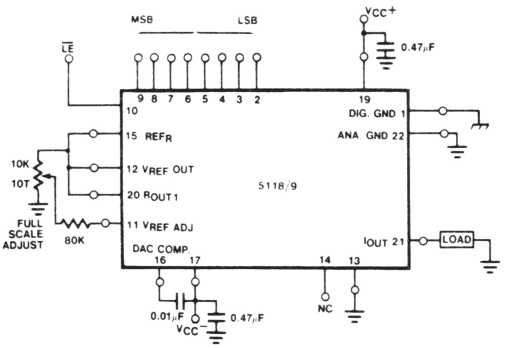
PARAMETER		TO	FROM	TEST CONDITIONS	SE/NE5119			UNIT
					Min	Typ	Max	
T_{SLH}	Settling time	± ½ LSB	Input	All bits Low-to-high		200		ns
T_{SHL}	Settling time	± ½ LSB	Input	All bits High-to-low		200		ns
t_{PLH}	Propagation delay	Output	Input	All bits switched Low-to-high		60		ns
t_{PHL}	Propagation delay	Output	Input	All bits switched High-to-low		60		ns
t_{PLSB}	Propagation delay	Output	Input	1 LSB change		60		ns
t_{PLH}	Propagation delay	Output	$\overline{LE}$	Low-to-high transition		60		ns
t_{PHL}	Propagation delay	Output	$\overline{LE}$	High-to-low transition		60		ns
t_s	Set-up time	$\overline{LE}$	Input		100			ns
t_h	Hold time	Input	$\overline{LE}$		50			ns
t_{pw}	Latch enable pulse width				150			ns

NOTES

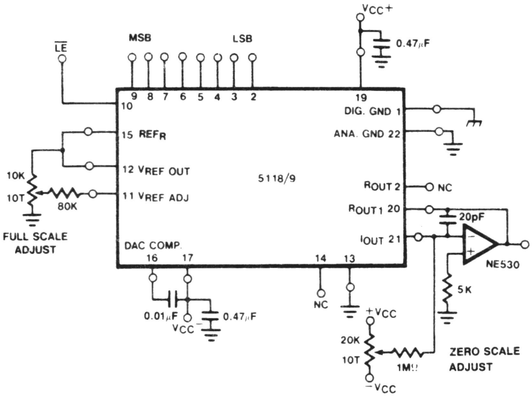
1. For reference currents > 3mA, use of an external buffer is required.

8-BIT µP-COMPATIBLE D/A CONVERTER—CURRENT OUTPUT SE/NE5119

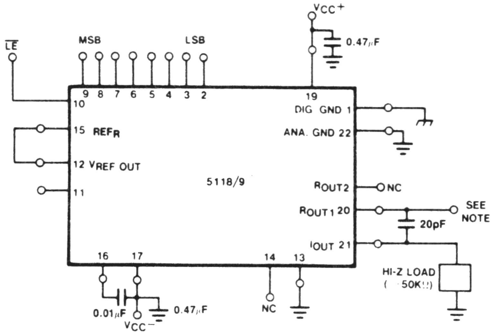
BIPOLAR OUTPUT OPERATION (−1mA TO +1mA)


MSB
LSB
Vcc+
0.47µF
LE
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
ANA. GND 22
15 REFR
12 VREF OUT
20 ROUT1
11 VREF ADJ
5118/9
10K
10T
FULL SCALE ADJUST
80K
DAC COMP.
16 17
14 13
IOUT 21
LOAD
0.01µF
0.47µF
VCC−
NC

UNIPOLAR VOLTAGE OUTPUT (0 → +10V)


Vcc+
0.47µF
LE
MSB
LSB
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
ANA. GND 22
15 REFR
12 VREF OUT
11 VREF ADJ
5118/9
10K
10T
80K
FULL SCALE ADJUST
ROUT2
NC
ROUT1 20
20pF
IOUT 21
NE530
5K
DAC COMP.
16 17
14 13
0.01µF
0.47µF
VCC−
NC
+VCC
20K
10T
1MΩ
ZERO SCALE ADJUST
−VCC

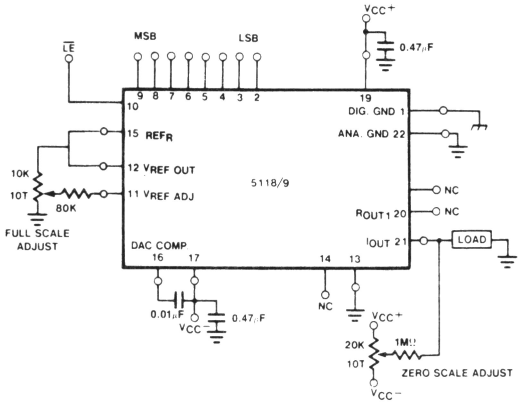
FAST VOLTAGE OUTPUT


Vcc+
0.47µF
LE
MSB
LSB
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
ANA. GND 22
15 REFR
12 VREF OUT
11
5118/9
ROUT2
NC
ROUT1 20
20pF
SEE NOTE
IOUT 21
16 17
14 13
HI-Z LOAD (≥50KΩ)
0.01µF
0.47µF
VCC−
NC

NOTE

DATA INPUT CODE	VOLTAGE OUTPUT (PIN 21)	
0 0 0 0 0 0 0 0	+10V	0V
1 1 1 1 1 1 1 1	0V	−10V
	Pin 20 tied to +10V	Pin 20 tied to 0V

BASIC UNIPOLAR CURRENT OUTPUT (0 → −2mA)


Vcc+
0.47µF
LE
MSB
LSB
9 8 7 6 5 4 3 2
10
19
DIG. GND 1
ANA. GND 22
15 REFR
12 VREF OUT
11 VREF ADJ
5118/9
10K
10T
80K
FULL SCALE ADJUST
NC
ROUT1 20
NC
IOUT 21
LOAD
DAC COMP.
16 17
14 13
0.01µF
0.47µF
VCC−
NC
Vcc+
20K
10T
1MΩ
ZERO SCALE ADJUST
Vcc−

10-BIT HIGH-SPEED MULTIPLYING D/A CONVERTER SE/NE5410

DESCRIPTION

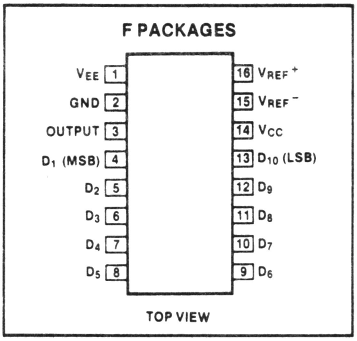
The NE5410/SE5410 are 10-Bit Multiplying Digital-to-Analog Converters pin-and-function compatible with the industry-standard MC3410, but with improved performance. These are capable of high-speed performance, and are used as general-purpose building blocks in cost-effective D/A systems.

The NE/SE5410 provides complete 10-bit accuracy and differential nonlinearity over temperature, and a wide compliance voltage range. Segmented current sources, in conjunction with an R/2R DAC provides the binary weighted currents. The output buffer amplifier and voltage reference have been omitted to allow greater speed, lower cost, and maximum user flexibility.

FEATURES

- **Pin-and-function compatible with MC3410**
- **10-bit resolution and accuracy (±0.05%)**
- **Guaranteed differential non-linearity over temperature**
- **Wide compliance voltage range— −2.5 to +2.5V**
- **Fast settling time—250ns typical**
- **Digital inputs are TTL and CMOS compatible**
- **High-speed multiplying input slew rate —20mA/μs**
- **Reference amplifier internally compensated**
- **Standard supply voltages +5V and −15V**

PIN CONFIGURATION


F PACKAGES
VEE 1
GND 2
OUTPUT 3
D1 (MSB) 4
D2 5
D3 6
D4 7
D5 8
16 VREF+
15 VREF−
14 VCC
13 D10 (LSB)
12 D9
11 D8
10 D7
9 D6
TOP VIEW

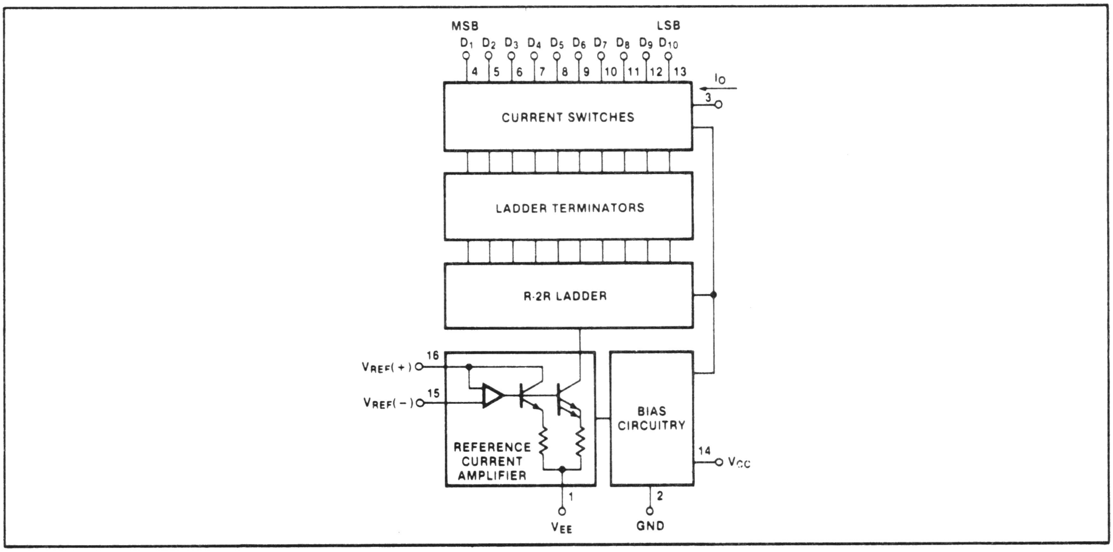
APPLICATIONS

- **Successive approximation A/D converters**
- **High-speed, automatic test equipment**
- **High-speed modems**
- **Waveform generators**
- **CRT displays**
- **Strip CHART and X-Y plotters**
- **Programmable power supplies**
- **Programmable gain and attenuation**

ABSOLUTE MAXIMUM RATINGS $T_A = +25°C$ unless otherwise noted

SYMBOL AND PARAMETER		RATING	UNIT
V_{CC}	Power Supply	+7.0	Vdc
V_{EE}		−18	Vdc
V_I	Digital Input Voltage	+15	Vdc
V_O	Applied Output Voltage	+4, −5.0	Vdc
$I_{REF(16)}$	Reference Current	2.5	mA
V_{REF}	Reference Amplifier Inputs	V_{CC}, V_{EE}	Vdc
$V_{REF(D)}$	Reference Amplifier Differential Inputs	0.7	Vdc
T_A	Operating Temperature Range		
	SE5410	−55 to +125	°C
	NE5410	0 to +70	°C
T_J	Junction Temperature		
	Ceramic Package	+175	°C
	Plastic Package	+150	°C

BLOCK DIAGRAM


MSB
LSB
D1 D2 D3 D4 D5 D6 D7 D8 D9 D10
4 5 6 7 8 9 10 11 12 13
IO
3
CURRENT SWITCHES
LADDER TERMINATORS
R-2R LADDER
VREF(+)
16
VREF(−)
15
REFERENCE CURRENT AMPLIFIER
BIAS CIRCUITRY
14
VCC
1
VEE
2
GND

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = +5.0$Vdc, $V_{EE} = -15$Vdc, $I_{REF} = 2.0$mA, all digital inputs at high logic level.
SE5410: $T_A = -55°C$ to $+125°C$, NE5410 Series: $T_A = 0°C$ to $+70°C$
unless otherwise noted.

SYMBOL AND PARAMETER		TEST CONDITIONS	NE/SE5410			UNIT
			Min	Typ	Max	
E_r	Relative accuracy (Error relative to full scale I_O)	Over temperature		±0.025	±0.05	%
				± 1/4	± 1/2	LSB
	Differential non-linearity	Over temperature		±0.025	±0.05	%
				± 1/4	± 1/2	LSB
t_s	Settling time to within ± ½ LSB (all bits low to high)	$T_A = 25°C$		250		ns
t_{PLH} t_{PHL}	Propagation delay time	$T_A = 25°C$		35 20		ns
TCI_O	Output full scale current drift			20	40	ppm/°C
V_{IH}	Digital Input Logic Levels (All bits) High Level, Logic "1" Low Level, Logic "0"		2.0		0.8	Vdc
I_{IH} I_{IL}	Digital Input Current (All bits) High Level, $V_{IH} = 5.5V$ Low Level, $V_{IL} = 0.8V$				20 −20	μA
$I_{REF(15)}$	Reference Input Bias Current (Pin 15)			−1.0	−5.0	μA
I_{OH}	Output Current (All bits high)	$V_{REF} = 2.000V$, $R_{16} = 1000Ω$	3.937	3.996	4.054	mA
I_{OL}	Output Current (All bits low)	$T_A = 25°C$		0	0.4	μA
V_O	Output Voltage Compliance	$T_A = 25°C$ $E_r < 0.05\%$ relative to full scale			−2.5 +2.5	Vdc
SR I_{REF}	Reference Amplifier Slew Rate			20		mA/μs
ST I_{REF}	Reference Amplifier Settling Time	0 to 4.0mA, ±0.1%		2.0		μs
PSRR(−)	Output Current Power Supply Sensitivity			0.003	0.01	%/%
C_O	Output Capacitance	$V_O = 0$		25		pF
C_I	Digital Input Capacitance (All bits high)			4.0		pF
I_{CC} I_{EE}	Power Supply Current (All bits low)			+2 −12	+4 −18	mA
V_{CC} V_{EE}	Power Supply Voltage Range	$T_A = 25°C$ $V_O = 0$	+4.75 −14.25	+5.0 −15	+5.25 −15.75	Vdc
	Power Consumption			190	300	mW

TYPICAL PERFORMANCE CHARACTERISTICS

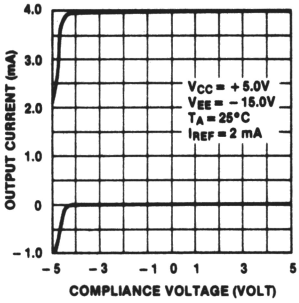


Figure 1. Output Current vs. Output Compliance Voltage

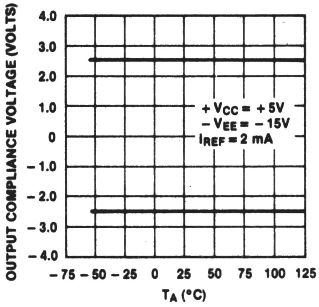


Figure 2. Maximum Output Compliance Voltage vs. Temperature

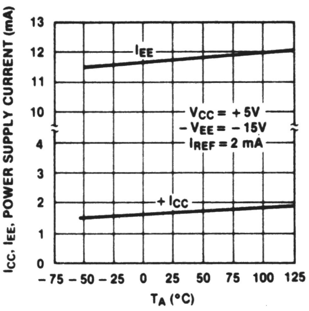


Figure 3. Power Supply Currents vs. Temperature

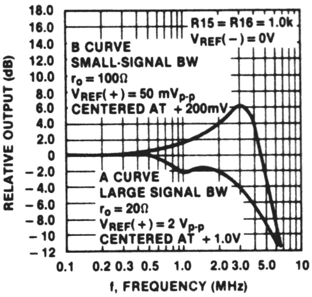


Figure 4. Reference Amplifier Frequency Response

10-BIT HIGH-SPEED MULTIPLYING D/A CONVERTER SE/NE5410

CIRCUIT DESCRIPTION

The NE5410 consists of four segment current sources which generate the 2 Most Significant Bits (MSBs), and an R/2R DAC implemented with ion implanted resistors for scaling the remaining 8 Least Significant Bits (LSBs). (See Figure 5.) This approach provides complete 10-bit accuracy without trimming.

The individual bit currents are switched ON or OFF by fully differential current switches. The switches use current steering for speed.

An on-chip high-slew reference current amplifier drives the R/2R ladder and segment decoder. The currents are scaled in such a way that, with all bits on, the maximum output current is two times 1023/1024 of the reference amplifier current, or nominally 3.996mA for a 2.000mA reference input current. The reference amplifier allows the user to provide a voltage input: Out-board resistor R16 (see Figure 6) converts this voltage to a usable current. A current mirror doubles this reference current and feeds it to the segment decoder and resistor ladder. Thus, for a reference voltage of 2.0 Volts and a 1kΩ resistor tied to Pin 16, the full scale current is approximately 4.0mA. This relationship will remain regardless of the reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 6a. For negative reference voltage inputs, or for bipolar reference voltage inputs in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. For a negative reference input, R16 should be grounded (Figure 6b). In addition, the negative voltage reference must be at least 3V above the V_{EE} supply voltage for best operation. Bipolar input signals may be handled by connecting R16 to a positive voltage equal to the peak positive input level at Pin 15.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5.0V supply, which drives logic, is to be used as the reference, R16 should be decoupled by connecting it to the +5.0V logic supply through another resistor and bypassing the junction of the two resistors with a 0.1μF capacitor to ground.

The reference amplifier is internally compensated with a 10pF feed-forward capacitor, which gives it its high slew rate and fast settling time. Proper phase margin is maintained with all possible values of R16 and reference voltages which supply

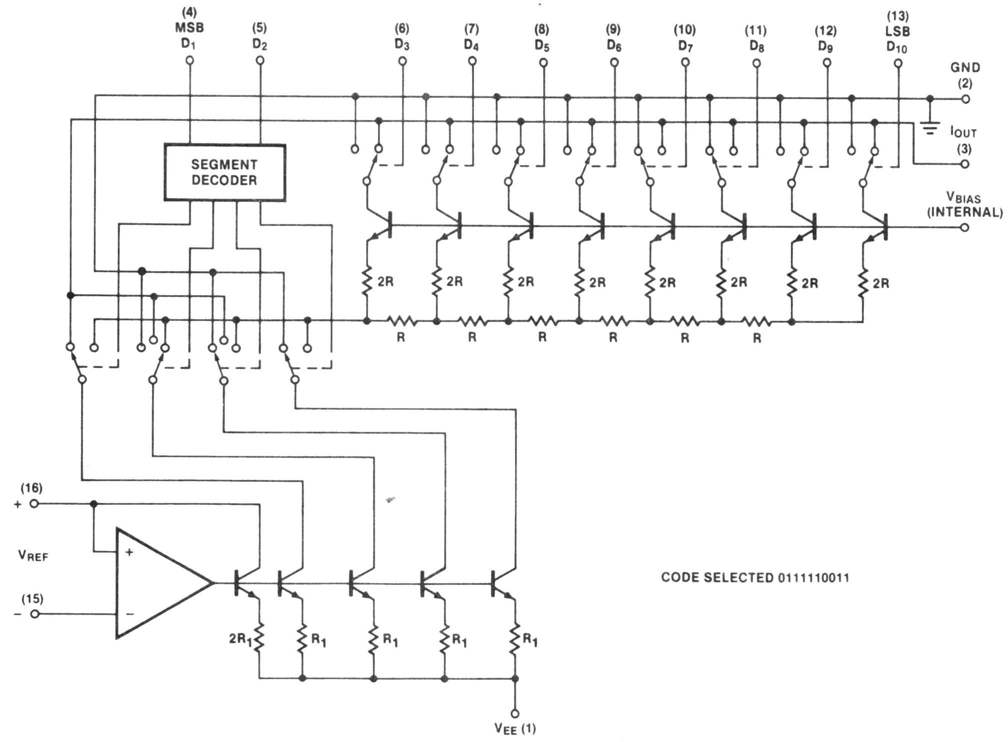
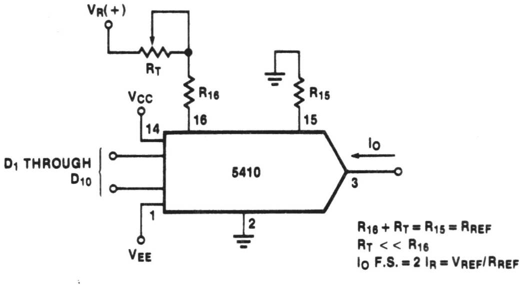


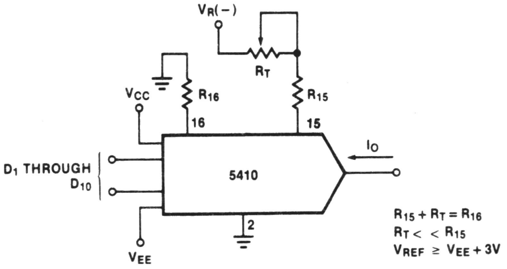
Figure 5. NE5410 Equivalent Circuit

10-BIT HIGH-SPEED MULTIPLYING D/A CONVERTER

SE/NE5410



a) POSITIVE REFERENCE VOLTAGE



b) NEGATIVE REFERENCE VOLTAGE

Figure 6. Basic Connections

2.0mA reference current into Pin 16. The reference current can also be supplied by a high impedance current source of 2.0mA. As R16 increases, the bandwidth of the amplifier decreases slightly and settling time increases. For a current source with a dynamic output impedance of 1.0MΩ, the bandwidth of the reference amplifier is approximately half what it is in the case of R16 = 1.0kΩ, and settling time is ≈ 10μs. The reference amplifier phase margin decreases as the current source value decreases in the case of a current source reference, so that the minimum reference current supplied from a current source is 0.5mA for stability.

OUTPUT VOLTAGE COMPLIANCE

The output voltage compliance ranges from − 2.5 to + 2.5V. As shown in Figure 2, this compliance range is nearly constant over temperature. At the temperature extremes, however, the compliance voltage may be reduced if $V_{EE} > -15V$.

ACCURACY

Absolute accuracy is a measure of each output current level with respect to its intended value. It is dependent upon relative accuracy and full scale current drift. Relative accuracy, or linearity, is the measure of each output current with respect to its intended fraction of the full scale current. The relative accuracy of the NE5410 is fairly constant over temperature due to the excellent temperature tracking, of the implanted resistors. The full scale current from the reference amplifier may drift with temperature causing a change in the absolute accuracy. However, the NE5410 has a low full scale current drift with temperature.

The SE5410 and the NE5410 are accurate to within ± 1/2 LSB at 25°C with a reference current of 2.0mA on Pin 16.

MONOTONICITY

The NE5410 and SE5410 are guaranteed monotonic over temperature. This means that for every increase in the input digital code, the output current either remains the same or increases but never decreases. In the multiplying mode, where reference input current will vary, monotonicity can be assured if the reference input current remains above 0.5mA.

SETTLING TIME

The worst case switching condition occurs when all bits are switched "on," which corresponds to a low-to-high transition for all bits. This time is typically 250ns for the output to settle to within ± 1/2 LSB for 10-bit accuracy, and 200ns for 8-bit accuracy. The turn-off time is typically 120ns. These times apply when the output swing is limited to a small (<0.7 Volt) swing and the external output capacitance is under 25pF.

The major carry (MSB off-to-on, all others on-to-off) settles in approximately the same time as when all bits are switched off-to-on.

If a load resistor of 625 Ohms is connected to ground, allowing the output to swing to −2.5 Volts, the settling time increases to 1.5μs.

Extra care must be taken in board layout as this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100μF supply bypassing, and minimum scope lead length are all necessary.

A typical test set-up for measuring settling time is shown in Figure 7. The same set-up for the most part can be used to measure the slew rate of the reference amplifier (Figure 9) by tying all data bits high, pulsing the voltage reference input between 0 and 2V, and using a 500Ω load resistor R_L.

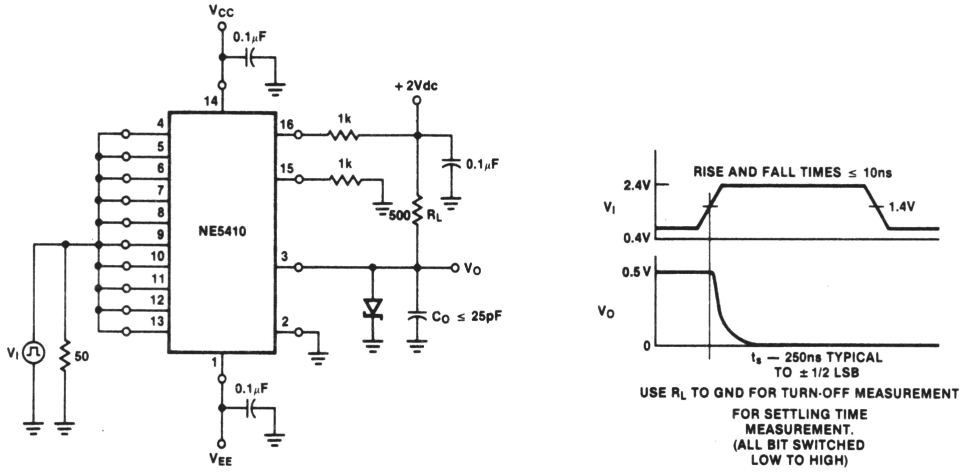

VCC
0.1μF
14
4
5
6
7
8
9
10
11
12
13
NE5410
16
1k
15
1k
+2Vdc
0.1μF
500
RL
3
VO
2
CO ≤ 25pF
1
0.1μF
VEE
VI
50
RISE AND FALL TIMES ≤ 10ns
2.4V
VI
1.4V
0.4V
0.5V
VO
0
ts — 250ns TYPICAL TO ± 1/2 LSB
USE RL TO GND FOR TURN-OFF MEASUREMENT
FOR SETTLING TIME MEASUREMENT. (ALL BIT SWITCHED LOW TO HIGH)

Figure 7. Settling Time

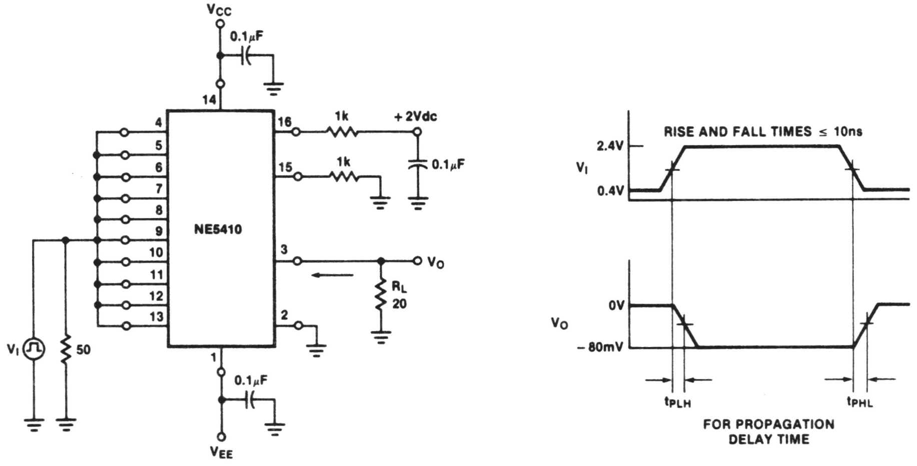

VCC
0.1μF
14
4
5
6
7
8
9
10
11
12
13
NE5410
16
1k
+2Vdc
15
1k
0.1μF
3
VO
RL
20
2
1
0.1μF
VEE
VI
50
RISE AND FALL TIMES ≤ 10ns
2.4V
VI
0.4V
0V
VO
−80mV
tPLH
tPHL
FOR PROPAGATION DELAY TIME

Figure 8. Propagation Delay Time

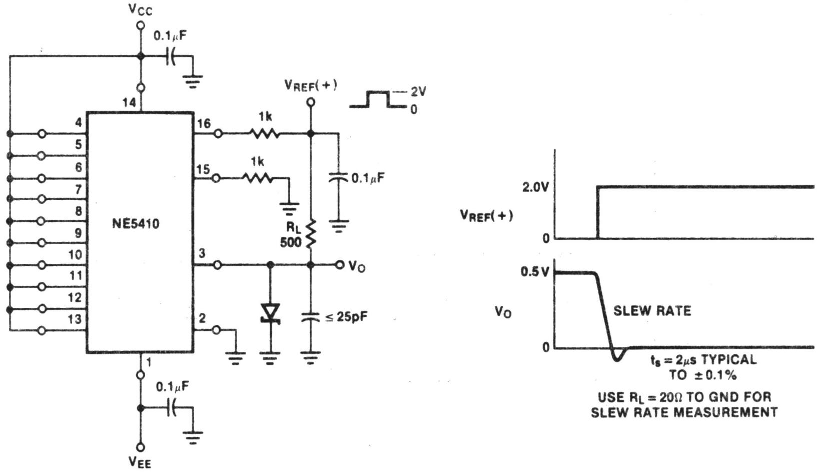
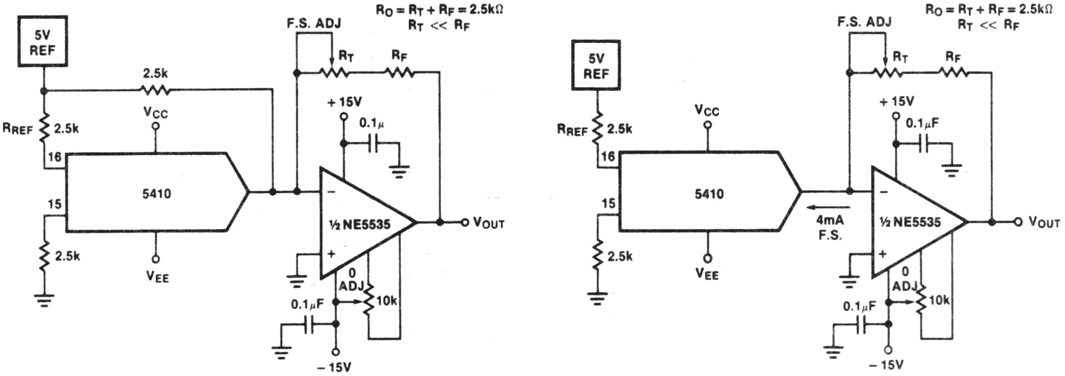

VCC
0.1μF
14
VREF(+)
2V
0
4
5
6
7
8
9
10
11
12
13
16
1k
15
1k
0.1μF
NE5410
RL
500
3
VO
2
≤ 25pF
1
0.1μF
VEE
2.0V
VREF(+)
0
0.5V
VO
SLEW RATE
0
ts = 2μs TYPICAL
TO ±0.1%
USE RL = 20Ω TO GND FOR
SLEW RATE MEASUREMENT

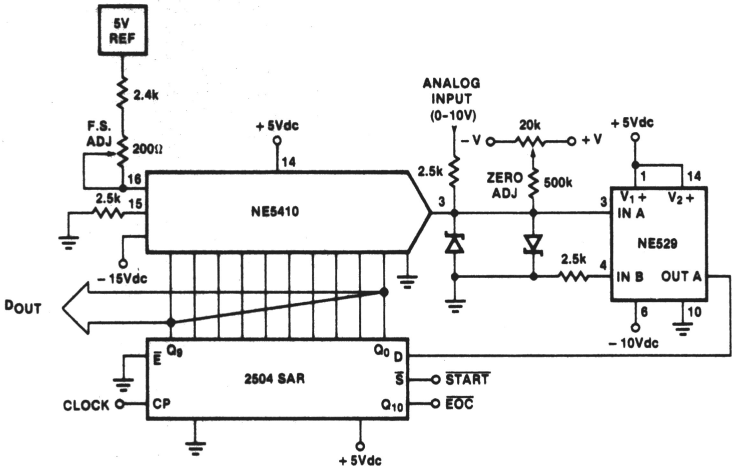
Figure 9. Reference Amplifier Settling Time and Slew Rate


5V
REF
2.5k
RREF
2.5k
16
15
2.5k
VCC
5410
VEE
F.S. ADJ
RO = RT + RF = 2.5kΩ
RT << RF
RT
RF
+15V
0.1μ
½ NE5535
VOUT
0
ADJ
10k
0.1μF
−15V
5V
REF
RREF
2.5k
16
15
2.5k
VCC
5410
VEE
4mA
F.S.
F.S. ADJ
RO = RT + RF = 2.5kΩ
RT << RF
RT
RF
+15V
0.1μF
½ NE5535
VOUT
0
ADJ
10k
0.1μF
−15V

a) Bipolar Output (-10 to +10V)

b) Unipolar Positive Output (0-10V)

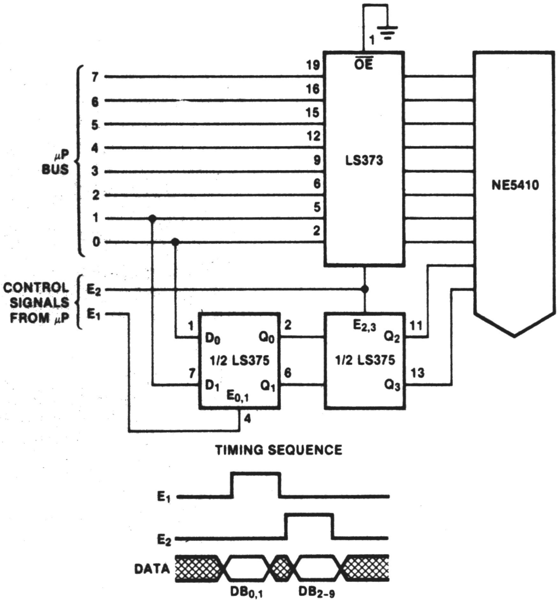
Figure 10. Voltage Output Circuits


5V REF
2.4k
F.S. ADJ
200Ω
2.5k
16
15
+5Vdc
14
NE5410
−15Vdc
ANALOG INPUT (0-10V)
−V
20k
+V
2.5k
3
ZERO ADJ
500k
+5Vdc
1
14
3
V1+
V2+
IN A
NE529
2.5k
4
IN B
OUT A
6
10
−10Vdc
DOUT
E
Q9
Q0
D
2504 SAR
S
START
CLOCK
CP
Q10
EOC
+5Vdc

10-BIT CONVERSION TIME = 3.3μs WITH 3MHz CLOCK.

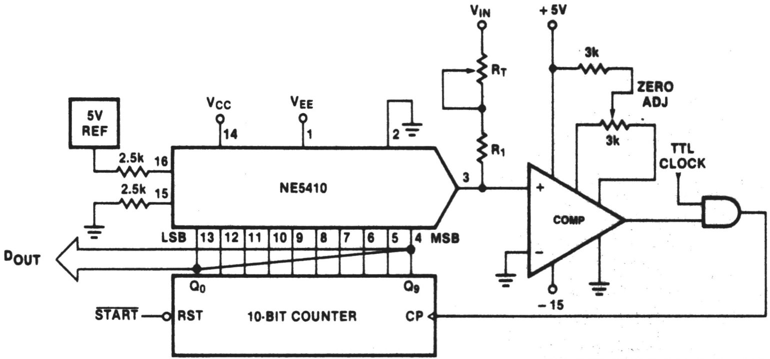
THIS CONVERTER USES A 2504 12-BIT SUCCESSIVE APPROXIMATION REGISTER IN THE SHORT CYCLE OPERATING MODE WHERE THE END OF CONVERSION SIGNAL IS TAKEN FROM THE FIRST UNUSED BIT OF THE SAR (Q_{10}).

Figure 11. Successive Approximation A/D Converter


1
OE
19
16
15
12
9
6
5
2
7
6
5
4
3
2
1
0
μP BUS
LS373
NE5410
CONTROL SIGNALS FROM μP
E2
E1
1
D0
Q0
2
1/2 LS375
7
D1
E0,1
Q1
6
4
E2,3
Q2
11
1/2 LS375
Q3
13
TIMING SEQUENCE
E1
E2
DATA
DB0,1
DB2-9

WITH THIS DOUBLE LATCH TECHNIQUE, VALID DATA WILL BE LATCHED TO THE DAC UNTIL UPDATED WITH THE E_2 PULSE. TIMING WILL DEPEND ON THE PROCESSOR USED.

Figure 12. 8-Bit μP Bus Interface


V_{IN}
+5V
3k
R_T
ZERO ADJ
3k
R_1
TTL CLOCK
5V REF
V_{CC}
V_{EE}
14
1
2
2.5k
16
2.5k
15
NE5410
3
+
COMP
−
−15
LSB
13
12
11
10
9
8
7
6
5
4
MSB
D_{OUT}
Q_0
Q_9
$\overline{START}$
RST
10-BIT COUNTER
CP

V_{IN} FULL SCALE = 4 mA $(R_1 + R_T)\left(\frac{1023}{1024}\right)$

Figure 13. Staircase A/D

SELECTOR GUIDE

COMPARATORS

DEVICE	COM-PLEXITY	TEMP. RANGE*	MAX. INP. OFFSET VOLT (mV)	MAX. INP. CURRENT		SUPPLY VOLTAGE (V)	RESPONSE TIME (Typ.) (ns)	COMMON MODE VOLTAGE RANGE (V)	OUTPUT VOLTAGE		OUTPUT STRUCTURE	VOLTAGE GAIN (Typ.) V/mV	TTL FANOUT	MAX. DIFF. INPUT VOLTAGE (V)
				BIAS (μA)	OFFSET (μA)				V_{OL} Max. (V)	V_{OH} Min. (V)				
LM111[1]	Single	M	4.00	0.15	0.02	± 15	200	± 14	0.4		O.C.	200	5	± 30
LM211	Single	I	4.00	0.15	0.02	to	200	± 14	0.4		O.C.	200	5	± 30
LM311	Single	C	10.0	0.30	0.07	+ 5 and GND	200	± 14	0.4		O.C.	200	5	± 30
NE527[2]	Single	C	10.0	4.00	1.0	± 5 to ± 10	16	± 5	0.5	2.7	TTL		5	± 5
SE527	Single	M	6.00	4.00	1.00	and GND	16	± 5	0.5	2.5	TTL		5	± 5
NE529[5]	Single	C	10.0	50.0	15.0	± 5 to ± 10	12	± 5	0.5	2.7	TTL		5	± 5
SE529	Single	M	6.00	36.0	9.00	and GND	12	± 5	0.5	2.5	TTL		5	± 5
LM119[3]	Dual	M	7.00	1.00	0.10	± 15	80	± 13	0.4		O.C.	40	2	± 5
LM219	Dual	I	7.00	1.00	0.10	to	80	± 13	0.4		O.C.	40	2	± 5
LM319	Dual	C	10.0	1.20	0.30	± 5 and GND	80	± 13	0.4		O.C.	40	2	± 5
LM193[3]	Dual	M	9.00	0.30	0.10	± 1 to ± 18	1300	0 to $V_S - 2$	0.7		O.C.	200	2	36
LM293	Dual	I	9.00	0.40	0.15	or	1300	0 to $V_S - 2$	0.7		O.C.	200	2	36
LM393	Dual	C	9.00	0.40	0.15	+ 2 to + 36 GND	1300	0 to $V_S - 2$	0.7		O.C.	200	2	36
LM2903	Dual	I	15.0	0.50	0.20		1300	0 to $V_S - 2$	0.7		O.C.	100	2	36
SE/NE521[4]	Dual	M/C	15/10.0	40.0	12.0	+ 5, − 5, GND	8	± 3	0.5	2.7	TTL		12	± 6
SE/NE522	Dual	M/C	15/10.0	40.0	12.0	+ 5, − 5, GND	10	± 3	0.5		O.C.		12	± 6
LM139[3]	Quad	M	9.00	0.30	0.10		1300	0 to $V_S - 2$	0.7		O.C.	200	2	36
LM239	Quad	I	9.00	0.40	0.15	± 1 to ± 18 or	1300	0 to $V_S - 2$	0.7		O.C.	200	2	36
LM339	Quad	C	9.00	0.40	0.15	+ 2 to + 36	1300	0 to $V_S - 2$	0.7		O.C.	200	2	36
LM2901	Quad	I	15.0	0.50	0.20		1300	0 to $V_S - 2$	0.7		O.C.	100	2	36
MC3302[3]	Quad	I	40.0	1.00	0.30	+ 2 to + 28 GND	2000	0 to $V_S - 2$	0.7		O.C.	100	2	28

Notes:

1. With strobe, will work from single supply.
2. Complementary output gates with individual strobes.
3. Will operate from single or dual supplies.
4. Ultra-high speed.

*Temperature Range
I = Industrial
C = Commercial
M = Military

VOLTAGE COMPARATOR

LM111/211/311

DESCRIPTION

The LM111 series are voltage comparators that have input currents approximately a hundred times lower than devices like the μA710. They are designed to operate over a wider range of supply voltages; from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Their output is compatible with RTL, DTL, and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50V at currents as high as 50mA.

Both the inputs and the outputs of the LM111 series can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the μA710 (200ns response time vs 40ns) the devices are also much less prone to spurious oscillations. The LM111 series has the same pin configuration as the μA710 series.

FEATURES

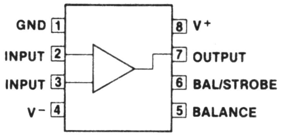
- **Operates from single 5V supply**
- **Maximum input bias current: 150nA (LM311 - 250nA)**
- **Maximum offset current: 20nA (LM311 - 50nA)**
- **Differential input voltage range: ±30V**
- **Power consumption: 135mW at ±15V**
- **High sensitivity—200V/mV**

APPLICATIONS

- **Zero crossing detector**
- **Precision squarer**
- **Positive/negative peak detector**
- **Low voltage adjustable reference supply**
- **Switching power amplifier**

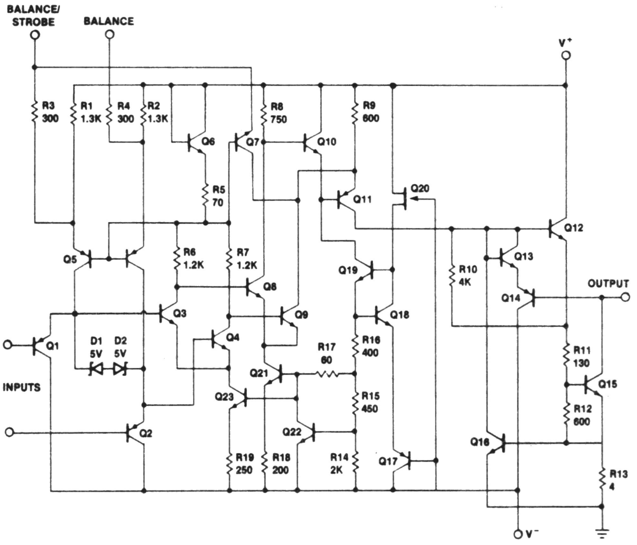
PIN CONFIGURATION

D, FE, N PACKAGE


GND 1
INPUT 2
INPUT 3
V− 4
8 V+
7 OUTPUT
6 BAL/STROBE
5 BALANCE

ORDER PART NO.
LM211N/LM311N
LM311D
LM111FE/LM211FE/LM311FE

EQUIVALENT SCHEMATIC


BALANCE/ STROBE
BALANCE
V+
R3 300
R1 1.3K
R4 300
R2 1.3K
R8 750
R9 600
Q6
Q7
Q10
R5 70
Q11
Q20
Q12
Q5
R6 1.2K
R7 1.2K
Q19
R10 4K
Q13
OUTPUT
Q8
Q14
Q3
Q9
Q18
Q1
D1 5V
D2 5V
Q4
R17 60
R16 400
R11 130
INPUTS
Q21
Q23
R15 450
Q15
R12 600
Q2
Q22
Q16
R19 250
R18 200
R14 2K
Q17
R13 4
V−

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Total supply voltage	36	V
Output to negative supply voltage:		
LM111/LM211	50	V
LM311	40	V
Ground to negative supply voltage	30	V
Differential input voltage	±30	V
Input voltage[1]	±15	V
Power dissipation[2]	500	mW
Output short circuit duration	10	sec
Operating temperature range		
LM111	-55 to +125	°C
LM211	-25 to +85	°C
LM311	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 10sec)	300	°C

VOLTAGE COMPARATOR LM111/211/311

DC ELECTRICAL CHARACTERISTICS [1,2,3]

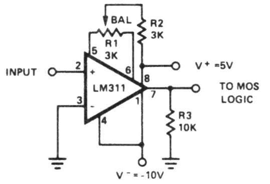
PARAMETER	TEST CONDITIONS	LM111/LM211			LM311			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage[4]	$T_A = 25^\circ C$, $R_S \le 50k\Omega$		0.7	3.0		2.0	7.5	mV
Input offset current[4]	$T_A = 25^\circ C$		4.0	10		6.0	50	nA
Input bias current	$T_A = 25^\circ C$		60	100		100	250	nA
Voltage gain	$T_A = 25^\circ C$		200			200		V/mV
Response time[5]	$T_A = 25^\circ C$		200			200		ns
Saturation voltage	$V_{IN} \le -5mV$, $I_{OUT} = 50mA$ $T_A = 25^\circ C$		0.75	1.5		0.75	1.5	V
Strobe on current	$T_A = 25^\circ C$		3.0			3.0		mA
Output leakage current	$V_{IN} \ge 5mV$, $V_{OUT} = 35V$ $T_A = 25^\circ C$, $I_{STROBE} = 3mA$		0.2	10		0.2	50	nA
Input offset voltage[4]	$R_S \le 50k\Omega$			4.0			10	mV
Input offset current[4]				20			70	nA
Input bias current				150			300	nA
Input voltage range	$V = \pm 15V$ (Pin 7 may go to 5V)	− 14.5	13.8, − 14.7	13.0	− 14.5	13.8, − 14.7	13.0	V
Saturation voltage	$V+ \ge 4.5V$, $V- = 0$ $V_{IN} \le -6mV$, $I_{SINK} \le 8mA$		0.23	0.4		0.23	0.4	V
Output leakage current	$V_{IN} \ge 5mV$, $V_{OUT} = 35V$		0.1	0.5				μA
Positive supply current	$T_A = 25^\circ C$		5.1	6.0		5.1	7.5	mA
Negative supply current	$T_A = 25^\circ C$		4.1	5.0		4.1	5.0	mA

NOTES

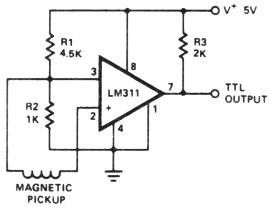
1. This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.
2. The maximum junction temperature of the LM311 is 110°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, in the N package, a thermal resistance of 162°C/W, and °C/W for the Ceramic package. The maximum junction temperature of the LM111 is 150°C, while that of the LM211 is 110°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient. The thermal resistance of the Cerdip package is 110°C/W, junction to ambient.
3. These specifications apply for $V_S = \pm 15V$ and $0^\circ C < T_A < 70^\circ C$ unless otherwise specified. With the LM211, however, all temperature specifications are limited to $-25^\circ C \le T_A \le 85^\circ C$ and for the LM111 is limited to $-55^\circ C < T_A < 125^\circ C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.
4. The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
5. The response time specified is for a 100mV input step with 5mV overdrive.
6. Do not short the strobe prin to ground; it should be current driven at 3mA to 5mA.

TYPICAL APPLICATIONS

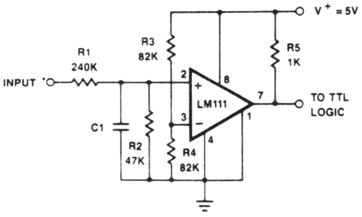
ZERO CROSSING DETECTOR DRIVING MOS LOGIC



DETECTOR FOR MAGNETIC TRANSDUCER



TTL INTERFACE WITH HIGH LEVEL LOGIC



*Values shown are for a 0 to 30V logic swing and a 15V threshold

†May be added to control speed and reduce susceptability to noise spikes

DUAL VOLTAGE COMPARATOR

LM119/219/319

DESCRIPTION

The LM119 series are precision high speed dual comparators fabricated on a single monolithic chip. They are designed to operate over a wide range of supply voltages down to a single 5V logic supply and ground. Further, they have higher gain and lower input currents than devices like the μA710. The uncommitted collector of the output stage makes the LM119 compatible with RTL, DTL and TTL as well as capable of driving lamps and relays at currents up to 25mA.

Although designed primarily for applications requiring operation from digital logic supplies, the LM119 series are fully specified for power supplies up to ±15V. It features faster response than the LM111 at the expense of higher power dissipation. However, the high speed, wide operating voltage range and low package count make the LM119 much more versatile than older devices like the μA711.

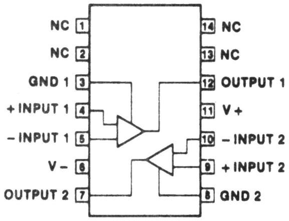
The LM119 is specified from -55°C to +125°C, the LM219 is specified from -25°C to +85°C, and the LM319 is specified from 0°C to +70°C.

FEATURES

- **Two independent comparators**
- **Operates from a single 5V supply**
- **Typically 80ns response time at ±15V**
- **Minimum fan-out of 3 (each side)**
- **Maximum input current of 1μA over temperature**
- **Inputs and outputs can be isolated from system ground**
- **High common mode slew rate**
- **MIL-STD-883 A, B, C available**

PIN CONFIGURATIONS

D,F,N PACKAGE

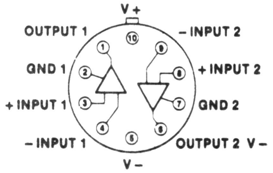

NC 1
NC 2
GND 1 3
+INPUT 1 4
−INPUT 1 5
V− 6
OUTPUT 2 7
14 NC
13 NC
12 OUTPUT 1
11 V+
10 −INPUT 2
9 +INPUT 2
8 GND 2

TOP VIEW

ORDER NUMBERS

LM119F LM219F LM319D,F,N

H PACKAGE*

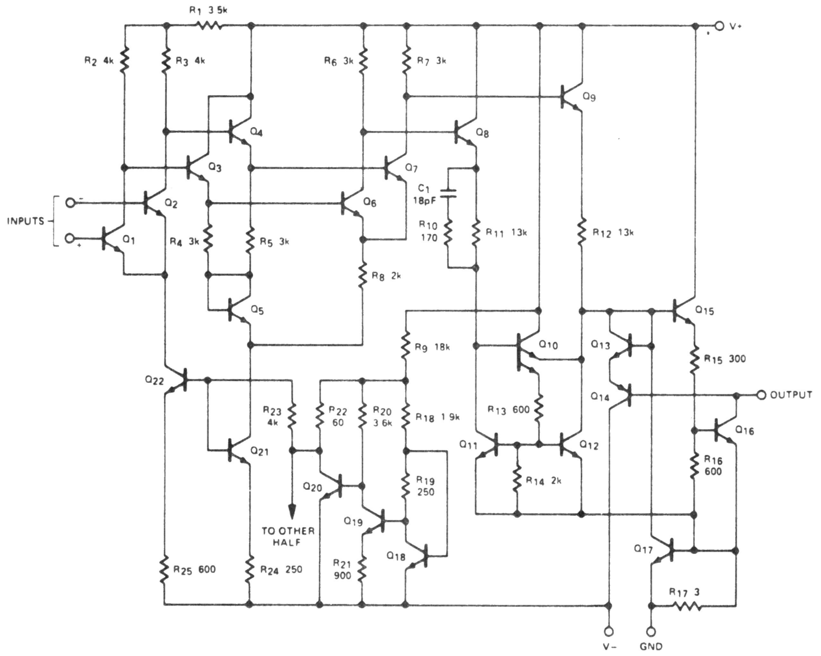

V+
OUTPUT 1
−INPUT 2
GND 1
+INPUT 2
+INPUT 1
GND 2
−INPUT 1
OUTPUT 2 V−
V−
1
2
3
4
5
6
7
8
9
10

ORDER NUMBERS

LM119H LM219H LM319H

*Metal cans (H) not recommended for new designs

EQUIVALENT SCHEMATIC


R1 3.5k
V+
R2 4k
R3 4k
R6 3k
R7 3k
Q9
Q4
Q8
Q3
Q7
C1 18pF
INPUTS
Q2
Q6
Q1
R4 3k
R5 3k
R10 170
R11 13k
R12 13k
R8 2k
Q5
Q15
R9 18k
Q10
Q13
R15 300
Q22
Q14
OUTPUT
R23 4k
R22 60
R20 3.6k
R18 1.9k
R13 600
Q16
Q11
Q12
Q21
R19 250
R16 600
Q20
R14 2k
Q19
TO OTHER HALF
Q17
Q18
R25 600
R24 250
R21 900
R17 3
V−
GND

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Total supply voltage	36	V
Output to negative supply voltage	36	V
Ground to negative supply voltage	25	V
Ground to positive supply voltage	18	V
Differential input voltage	±5	V
Input voltage[1]	±15	V
Power dissipation[2]	500	mW
Output short circuit duration	10	s
Operating temperature range		
LM119	-55 to +125	°C
LM219	-25 to +85	°C
LM319	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 10sec)	300	°C

NOTES

1. For supply voltages less than ±15V, the absolute maximum rating is equal to the supply voltage.
2. The absolute maximum junction temperature is 150°C. Device dissipation must be derated as follows:
   K package—150°C/watt above 75°C
   F package —110°C/watt above 95°C

DC ELECTRICAL CHARACTERISTICS

$V_S = \pm15V$, for LM119, $-55°C \le T_A \le 125°C$; LM219, $-25°C \le T_A \le 85°C$; LM319, $0°C \le T_A \le 70°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	LM119/219			LM319			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[1,2]	$R_S \le 5K\Omega$, $T_A = 25°C$		0.7	4.0		2.0	8.0	mV
		Over temp.			7			10	mV
I_{OS}	Input offset current[1,2]	$T_A = 25°C$		30	75		80	200	nA
		Over temp.			100			300	nA
I_B	Input bias current[1]	$T_A = 25°C$		150	500		250	1000	nA
		Over temp.			1000			1200	nA
A_V	Voltage gain	$T_A = 25°C$	10	40		8	40		V/mV
V_{OL}	Saturation voltage	$V_{IN} = 5mV$, $I_{OUT} = 25mA$, $T_A = 25°C$		0.75	1.5				V
		$V_{IN} = 10mV$, $I_{OUT} = 25mA$, $T_A = 25°C$					0.75	1.5	V
		$V^+ \ge 4.5V$, $V^- = 0$							
		$V_{IN} = 6mV$, $I_{OUT} = 3.2mA$							
		$T_A \ge 0°C$		0.23	0.4				V
		$T_A \le 0°C$			0.6				
		$V_{IN} = 10mV$, $I_{OUT} = 3.2mA$					0.3	0.4	V
I_{OH}	Output leakage current	$V^- = 0V$, $V_{IN} = 5mV$							
		$V_{OUT} = 35V$, $T_A = 25°C$		0.2	2				µA
		Over temp.		1	10				µA
		$V^- = 0V$, $V_{IN} = 10mV$							
		$V_{OUT} = 35V$, $T_A = 25°C$					0.2	10	µA
V_{IN}	Input voltage range	$V_S = \pm15V$		±13			±13		V
		$V^+ = 5V$, $V^- = 0V$	1		3	1		3	V
V_{ID}	Differential input voltage				±5			±5	V
I^+	Positive supply current	$V^+ = 5V$, $V^- = 0V$, $T_A = 25°C$		4.3			4.3		mA
I^+	Positive supply current	$V_S = \pm15V$, $T_A = 25°C$		8.0	11.5		8.0	12.5	mA
I^-	Negative supply current	$V_S = \pm15V$, $T_A = 25°C$		3.0	4.5		3.0	5.0	mA

NOTES

1. V_{OS}, I_{OS} and I_B specifications apply for a supply voltage range of $V_S = \pm15V$ down to a single 5V supply.
2. The offset voltages and offset currents given are the maximum values required to drive the output to within 1 volt of either supply with a 1mA load. Thus these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

AC ELECTRICAL CHARACTERISTICS

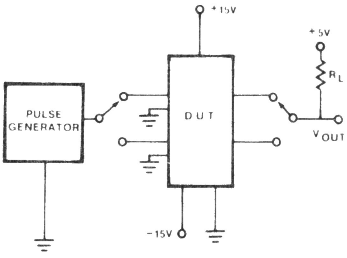
PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Response time*	$V_S = \pm15V$, $T_A = 25°C$ $R_L = 500\Omega$ (see test figure)		80		ns

*NOTE

The response time specified is for a 100mV step with 5mV overdrive.

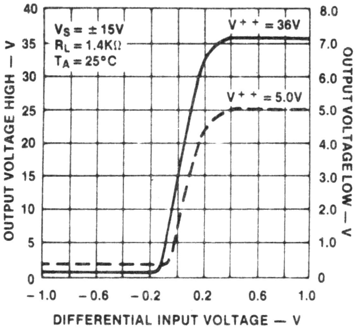
TEST CIRCUIT

RESPONSE TIME MEASUREMENT

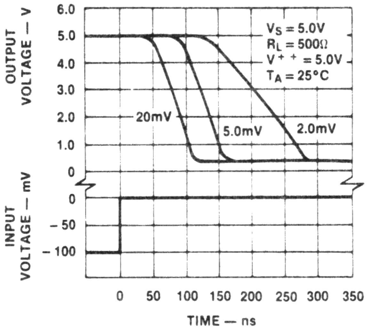


TYPICAL PERFORMANCE CHARACTERISTICS

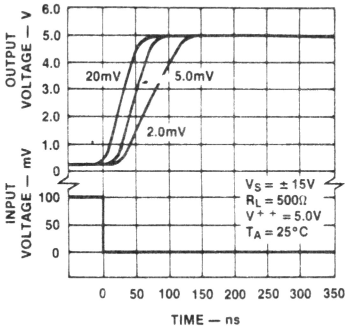
TRANSFER FUNCTION



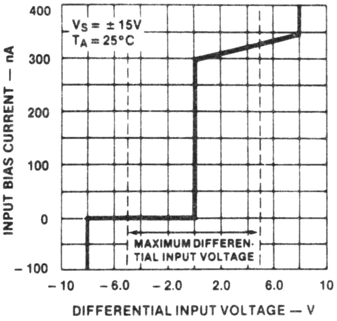
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



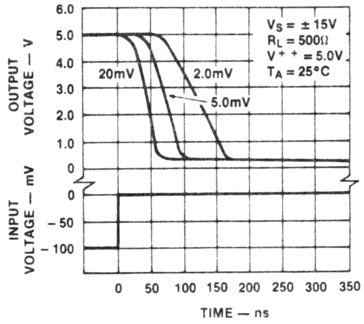
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



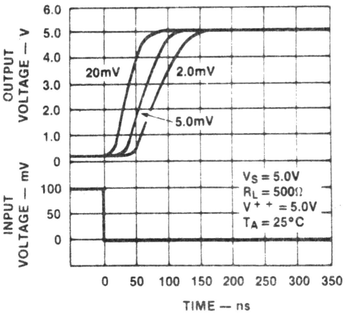
INPUT CHARACTERISTICS



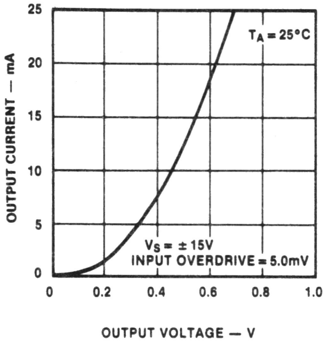
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

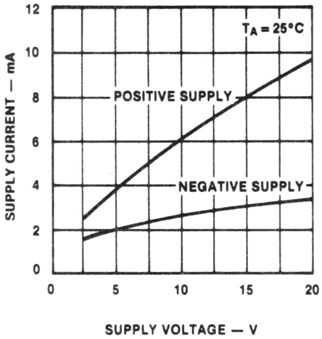


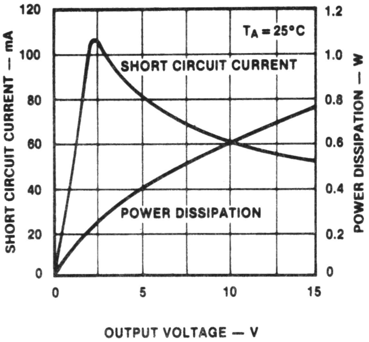
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

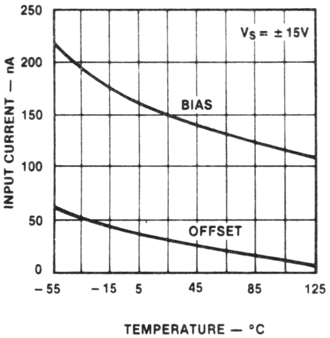


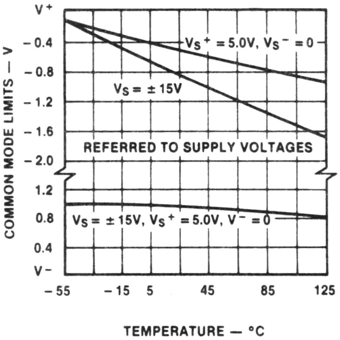
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

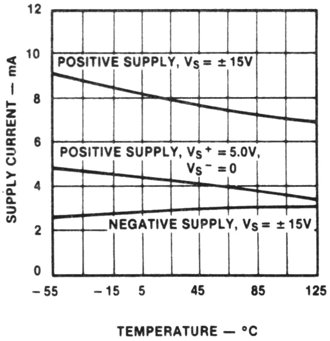

OUTPUT SATURATION VOLTAGE

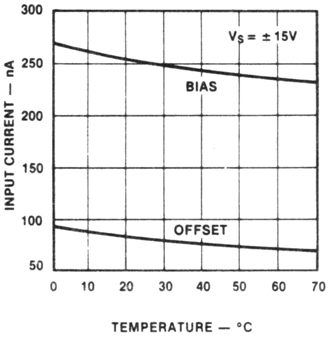

SUPPLY CURRENT

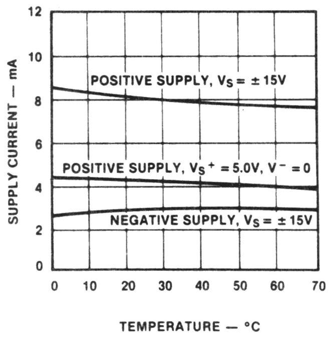

OUTPUT LIMITING CHARACTERISTICS

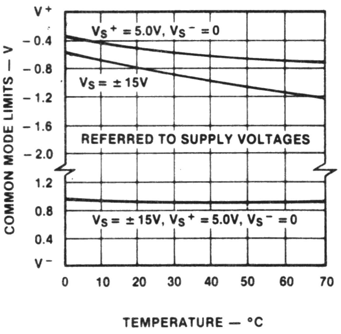

INPUT CURRENTS (LM119/219)


COMMON MODE LIMITS (LM119/219)


SUPPLY CURRENT (LM119/219)

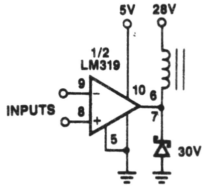

INPUT CURRENTS (LM319)


SUPPLY CURRENTS (LM319)

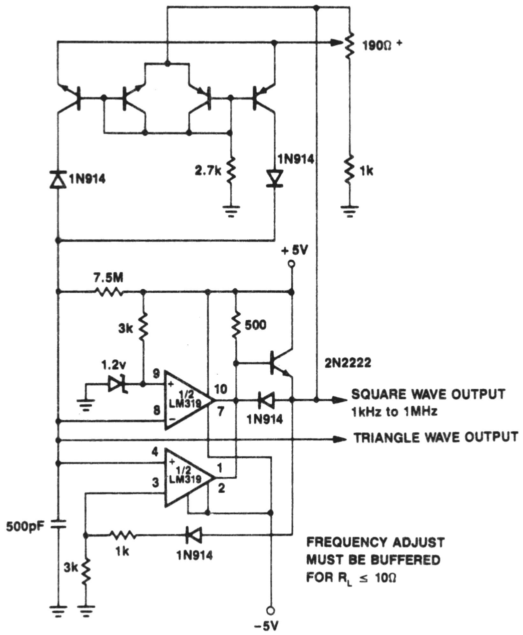

COMMON MODE LIMITS (LM319)

TYPICAL APPLICATIONS

RELAY DRIVER

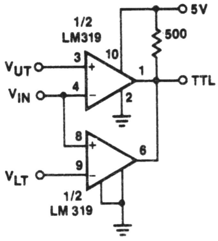

5V
28V
1/2
LM319
9
8
INPUTS
10
6
7
5
30V

WIDE RANGE VARIABLE OSCILLATOR


190Ω +
1N914
2.7k
1N914
1k
+5V
7.5M
3k
500
1.2v
9
8
10
7
1/2
LM319
2N2222
1N914
SQUARE WAVE OUTPUT
1kHz to 1MHz
TRIANGLE WAVE OUTPUT
4
3
1
2
1/2
LM319
500pF
1k
1N914
3k
-5V

FREQUENCY ADJUST MUST BE BUFFERED FOR $R_L \leq 10\Omega$

WINDOW DETECTOR


5V
500
1/2
LM319
3
10
1
TTL
V_{UT}
V_{IN}
4
2
8
6
9
V_{LT}
1/2
LM 319

$V_{OUT} = 5V$ for $V_{LT} < V_{IN} < V_{UT}$

$V_{OUT} = 0$ for $V_{IN} < V_{LT}$ or $V_{IN} > V_{UT}$

QUAD VOLTAGE COMPARATOR

LM139A/239A/339A/LM139/239/339/ LM2901/MC3302

DESCRIPTION

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2.0mV max for each comparator which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common mode voltage range includes ground, even though operated from a single power supply voltage.

The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM139 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

FEATURES

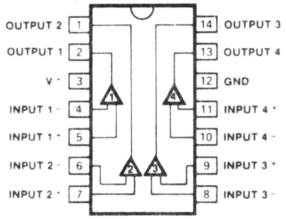
- **Wide single supply voltage range 2.0Vdc to 36Vdc or dual supplies ±1.0Vdc to ±18Vdc**
- **Very low supply current drain (0.8mA) independent of supply voltage (1.0mW/-comparator at 5.0Vdc)**
- **Low input biasing current 25nA**
- **Low input offset currrent ±5nA and offset voltage**
- **Input common-mode voltage range includes ground**
- **Differential input voltage range equal to the power supply voltage.**
- **Low output 250mV at 4mA saturation voltage**
- **Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems.**

APPLICATIONS

- **A/D converters**
- **Wide range VCO**
- **MOS clock generator**
- **High voltage logic gate**
- **Multivibrators**

PIN CONFIGURATION

D,F,N PACKAGE



TOP VIEW

ORDER NUMBERS

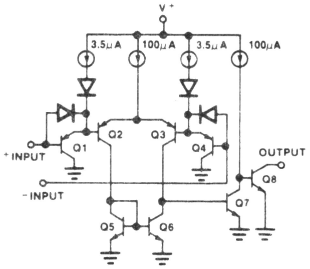
LM139/239/339F,N LM2901F,N
MC3302D,F,N LM339D

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V_{CC} supply voltage	36 or ±18	
Differential input voltage	36	
Input voltage	-0.3 to +36	
Power dissipation[1]		
N package	570	mW
F package	900	mW
Output short circuit to ground[2]	Continuous	
Input current (V_{IN} < -0.3Vdc)[3]	50	mA
Operating temperature range		
LM139/A	-55 to +125	°C
LM239/A	-25 to +85	°C
LM339/A	0 to +70	°C
LM2901/MC3302	-40 to +85	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 10 sec.)	300	°C

EQUIVALENT CIRCUIT

(1 Comparator Only)



QUAD VOLTAGE COMPARATOR

LM139A/239A/339A/LM139/239/339/ LM2901/MC3302

DC ELECTRICAL CHARACTERISTICS $V+ = 5Vdc$, LM139A/LM139: $-55°C \leq T_A \leq 125°C$ unless otherwise specified
LM239: $-25°C \leq T_A \leq 85°C$ unless otherwise specified
LM339: $0°C \leq T_A \leq 70°C$ unless otherwise specified
$V+ = 5Vdc$, LM339A: $°C \leq T_A \leq 70°C$ unless otherwise specified
LM239A: $-25°C \leq T_A \leq 85°C$ unless otherwise specified
LM2901/LM3302: $-40°C \leq T_A \leq 85°C$ unless otherwise specified

PARAMETER		TEST CONDITIONS	LM139A			LM239A/339A			LM139			LM239/339			LM2901			MC3302			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[5]	$T_A = 25°C$ Over temp.		± 1.0	± 2.0 4.0		± 1.0	± 2.0 ± 4.0		± 2.0	± 5.0 9.0		± 2.0	± 5.0 9.0		± 2.0 ± 9	± 7.0 ± 15		± 3.0	± 20 ± 40	mV
V_{CM}	Input common mode voltage range[6]	$T_A = 25°C$ Over temp.	0 0		V+ − 1.5 V+ − 2.0	0 0		V+ − 1.5 V+ − 2.0	0 0		V+ − 1.5 V+ − 2.0	0 0		V+ − 1.5 V+ − 2.0	0 0		V+ − 1.5 V+ − 2.0			V+ − 1.5 V+ − 2.0	V
V_{IDR}	Differential input[4] voltage[4]	Keep all $V_{INs} \geq 0Vdc$ (or V− if need)			V+			V+			V+			V+			V+			V+	V
I_B	Input bias current[7]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_A = 25°C$ Over temp.		25	100 300		25	250 400		25	100 300		25	250 400		25 200	250 500		25	500 1000	nA
I_{OS}	Input offset current	$I_{IN(+)} - I_{IN(-)}$ $T_A = 25°C$ Over temp.		± 3.0	± 25 ± 100		± 5.0	± 50 ± 150		± 3.0	± 25 ± 100		± 5.0	± 50 ± 150		± 5 ± 50	± 50 ± 200		± 5	± 100 ± 300	nA nA
I_{OL}	Output sink current	$V_{IN(-)} \geq 1Vdc$, $V_{IN(+)} = 0$, $V_O \leq 1.5Vdc$, $T_A = 25°C$ $V_O = 800mV$, over temp.	6.0	16		6.0	16		6.0	16		6.0	16		6.0	16		2.0	6		mA
I_{OH}	Output leakage current	$V_{IN(+)} \geq 1Vdc$, $V_{IN(-)} = 0$ $V_O = 5Vdc$, $T_A = 25°C$ $V_O = 30Vdc$, over temp.		0.1	1.0		0.1	1.0		0.1	1.0		0.1	1.0		0.1	1.0		0.1	1.0	nA μA
I_{CC}	Supply current	$V+ = 28V$ $R_L = \infty$ on comparators, $T_A = 25°C$ $V+ = 30V$		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2.0		0.8 1.0	2.0 2.5		.8	1.8	mA
A_V	Voltage gain	$R_L \geq 15k\Omega$, $V+ = 15Vdc$	50	200		50	200		50	200		50	200		25	100		2	100		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)} \geq 1Vdc$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4mA$ $T_A = 25°C$ Over temp.		250	400 700		250	400 700		250	400 700		250	400 700		400	400 700		150	400 700	mV
T_{LSR}	Large signal response time	V_{IN} = TTL logic swing, $V_{REF} = 1.4Vdc$, $V_{RL} = 5Vdc$, $R_L = 5.1k\Omega$, $T_A = 25°C$		300			300			300			300			300			300		ns
T_R	Response time[8]	$V_{RL} = 5Vdc$, $R_L = 5.1k\Omega$, $T_A = 25°C$		1.3			1.3			1.3			1.3			1.3			1.3		μs

See notes on following page.

QUAD VOLTAGE COMPARATOR

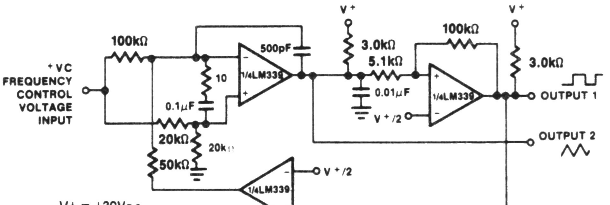
LM139A/239A/339A/LM139/239/339/ LM2901/MC3302

NOTES

1. For operating at high temperatures, the LM339/339A, LM2901 and MC3302 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air embient. The LM139/139A/239/239A must be derated on a 150°C maximum junction temperature. The low power dissipation and the "On-Off" characteristics of the outputs keep the chip dissipation very small ($P_D \leq$ 100mW), provided the output transistors are allowed to saturate.
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA independent of the magnitude of V+.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3Vdc.
4. Positive excursions of input voltage may exceed the power supply level by 17 volts. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3Vdc (or 0.3Vdc below the magnitude of the negative power supply, if used).
5. At output switch point, $V_O \cong$ 1.4Vdc, $R_S = 0\Omega$ with V+ from 5Vdc to 30Vdc; and over the full input common-mode range (0Vdc to V+ −1.5Vdc).
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ −1.5V, but either or both inputs can go to 30Vdc without damage.
7. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
8. The response time specified is for a 100mV input step with a 5mV overdrive. For larger overdrive signals, 300ns can be obtained, see typical performance characteristics section.

TYPICAL APPLICATIONS

TWO-DECADE HIGH-FREQUENCY VCO

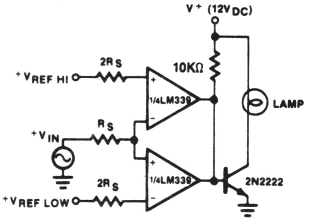

V+
V+
100kΩ
500pF
3.0kΩ
5.1kΩ
100kΩ
3.0kΩ
+VC FREQUENCY CONTROL VOLTAGE INPUT
10
1/4LM339
0.01μF
1/4LM339
V+/2
OUTPUT 1
0.1μF
20kΩ
20kΩ
50kΩ
OUTPUT 2
1/4LM339
V+/2

V+ = +30V$_{DC}$

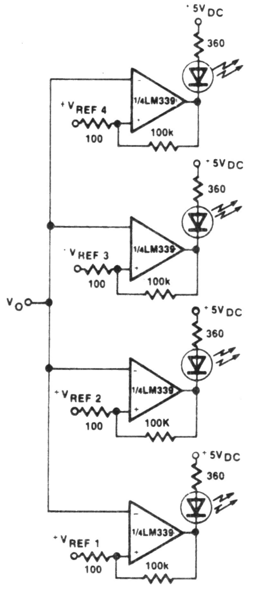
+250mV$_{DC}$ ≤ V$_C$ ≤ +50V$_{DC}$

700Hz ≤ f$_o$ ≤ 100kHz

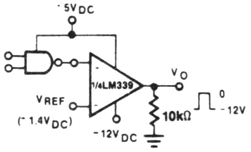
LIMIT COMPARATOR


V+ (12VDC)
+VREF HI
2RS
10KΩ
1/4LM339
LAMP
+VIN
RS
2RS
1/4LM339
2N2222
+VREF LOW

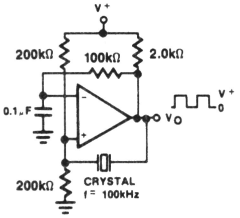
VISIBLE VOLTAGE INDICATOR


+5VDC
360
1/4LM339
+VREF 4
100
100k
+5VDC
360
1/4LM339
+VREF 3
100
100k
VO
+5VDC
360
1/4LM339
+VREF 2
100
100K
+5VDC
360
1/4LM339
+VREF 1
100
100k

TTL TO MOS LOGIC CONVERTER


+5VDC
VO
1/4LM339
VREF
(+1.4VDC)
-12VDC
10kΩ
0
-12V

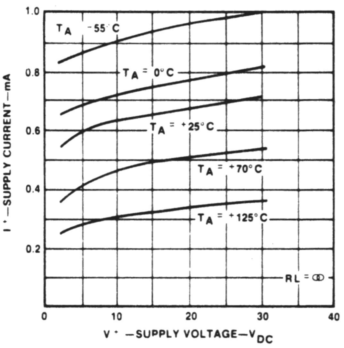
CRYSTAL CONTROLLED OSCILLATOR


V+
200kΩ
100kΩ
2.0kΩ
0.1μF
VO
V+
0
200kΩ
CRYSTAL
f = 100kHz

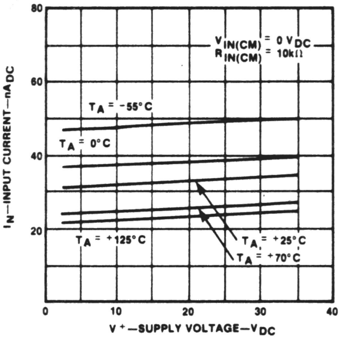
NOTE:
Inputs of unused comparators should be grounded.

QUAD VOLTAGE COMPARATOR

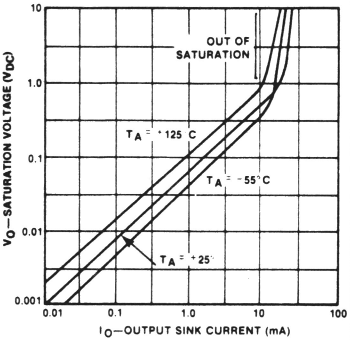
TYPICAL PERFORMANCE CHARACTERISTICS



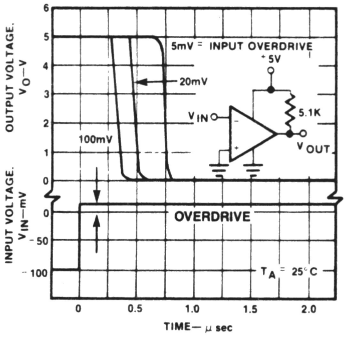
SUPPLY CURRENT



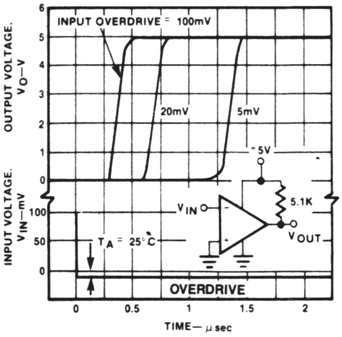
INPUT CURRENT



OUTPUT SATURATION VOLTAGE



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES— NEGATIVE TRANSITION



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES— POSITIVE TRANSITION

LOW POWER DUAL VOLTAGE COMPARATOR LM193/A/293/A/393/A/2903

DESCRIPTION

The LM193 series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common mode voltage range includes ground, even though operated from a single power supply voltage.

The LM193 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

FEATURES

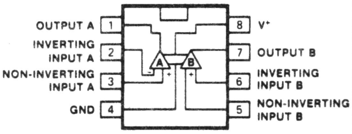
- **Wide single supply voltage range 2.0Vdc to 36Vdc or dual supplies ±1.0Vdc to ±18Vdc**
- **Very low supply current drain (0.8mA) independent of supply voltage (2.0mW/-comparator at 5.0Vdc)**
- **Low input biasing current 25nA**
- **Low input offset current ±5nA and offset voltage ±2mV**
- **Input common-mode voltage range includes ground**
- **Differential input voltage range equal to the power supply voltage.**
- **Low output 250mV at 4mA saturation voltage**
- **Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems.**

APPLICATIONS

- **A/D converters**
- **Wide range VCO**
- **MOS clock generator**
- **High voltage logic gate**
- **Multivibrators**

PIN CONFIGURATIONS

D,N,FE PACKAGE



TOP VIEW

ORDER NUMBERS

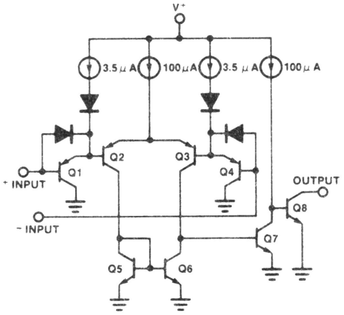
LM193FE
LM293FE
LM293AFE
LM293N
LM293AN
LM393D
LM393FE
LM393AFE
LM393N
LN393AN
LM2903N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V_{CC} supply voltage	36 or ±18	Vdc
Differential input voltage	36	Vdc
Input voltage	-0.3 to +36	Vdc
Power dissipation[1]		
N	570	mW
FE	900	mW
Output short circuit to ground[2]	Continuous	
Input current ($V_{IN} < -0.3$Vdc)[3]	50	mA
Operating temperature range		
LM193/193A	-55 to +125	°C
LM293/293A	-25 to +85	°C
LM393/393A	0 to +70	°C
LM2903	-40 to +85	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 10 sec.)	300	°C

EQUIVALENT CIRCUIT

(One Comparator Only)



DC ELECTRICAL CHARACTERISTICS (Cont'd) V+ = 5Vdc, LM193/193A: $-55°C \le T_A \le +125°C$ unless otherwise specified.
LM293/293A: $-25°C \le T_A \le +85°C$ unless otherwise specified.
LM393/393A: $0°C \le T_A \le +70°C$ unless otherwise specified.
LM2903: $-40°C \le T_A \le +85°C$ unless otherwise specified.[7]

PARAMETER		TEST CONDITIONS	LM193			LM293/393			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage[5]	$T_A = 25°C$ Over temp.		±2.0	±5.0 ±9.0		±2.0	±5.0 ±9.0	mV
V_{CM}	Input common mode voltage range[6,10]	$T_A = 25°C$ Over temp.	0 0		V±-1.5 V±-2.0	0 0		V±-1.5 V±-2.0	V
V_{IDR}	Differential input voltage[4]	Keep all $V_{IN's} \ge 0Vdc$ (or V-if need)			V+			V+	V
I_B	Input bias current[8]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_A = 25°C$ Over temp.		25	100 300		25	250 400	nA
I_{OS}	Input offset current	$I_{IN(+)} - I_{IN(-)}$ $T_A = 25°C$ Over temp.		±3.0	±25 ±100		±5.0	±50 ±150	nA nA
I_{OL}	Output sink current	$V_{IN(-)} \ge 1Vdc$, $V_{IN(+)} = 0$, $V_0 \le 1.5Vdc$, $T_A = 25°C$	6.0	16		6.0	16		mA
I_{OH}	Output leakage current	$V_{IN(+)} \ge 1Vdc$, $V_{IN(-)} = 0$ $V_0 = 5Vdc$, $T_A = 25°C$ $V_0 = 30Vdc$, over temp.		0.1	 1.0		0.1	 1.0	nA μA
I_{CC}	Supply current	$R_L = \infty$ on both comparators $T_A = 25°C$ V+ = 30V, over temp.		0.8	1 2.5		0.8	1 2.5	mA
A_V	Voltage gain	$R_L \ge 15K\Omega$, V+ = 15Vdc	50	200		50	200		V/mV
V_{OL}	Saturation voltage	$V_{IN(-)} \ge 1Vdc$, $V_{IN(+)} = 0$, $I_{SINK} \le 4mA$ $T_A = 25°C$ Over temp.		250	400 700		250	400 700	mV
T_{LSR}	Large signal response time	V_{IN} = TTL logic swing, $V_{REF} = 1.4Vdc$, $V_{RL} = 5Vdc$, $R_L = 5.1k\Omega$, $T_A = 25°C$		300			300		ns
T_R	Response time[9]	$V_{RL} = 5Vdc$, $R_L = 5.1k\Omega$, $T_A = 25°C$		1.3			1.3		μs

NOTES

1. For operating at high temperatures, the LM393/393A and LM2903 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM193/193A/293/293A must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "On-Off" characteristics of the outputs keeps the chip dissipation very small ($P_D \le 100mW$), provided the output transistors are allowed to saturate.
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA independent of the magnitude of V+.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3Vdc.
4. Positive excursions of input voltage may exceed the power supply level by 17 Volts. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -0.3Vdc (Vdc below the magnitude of the negative power supply, if used).
5. At output switch point, $V_0 \cong 1.4Vdc$, $R_S = 0\Omega$ with V+ from 5Vdc to 30Vdc; and over the full input common-mode range (0Vdc to V+ -1.5Vdc).
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ -1.5V, but either or both inputs can go to 30Vdc without damage.
7. With the LM293/293A, all temperature specifications are limited to $-25°C \le T_A \le +85°C$ and the LM393/393A, all temperature specifications are limited to $0°C \le T_A \le +70°C$. The LM2903 is limited to $-40°C \le T_A \le 85°C$.
8. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
9. The response time specified is for a 100mV input step with a 5mV overdrive.
10. For input signals that exceed V_{CC}, only the overdriven comparator is affected. With a 5V supply, V_{IN} should be limited to 25V max., and a limiting resistor should be used on all inputs that might exceed the positive supply.

LOW POWER DUAL VOLTAGE COMPARATOR LM193/A/293/A/393/A/2903

DC ELECTRICAL CHARACTERISTICS

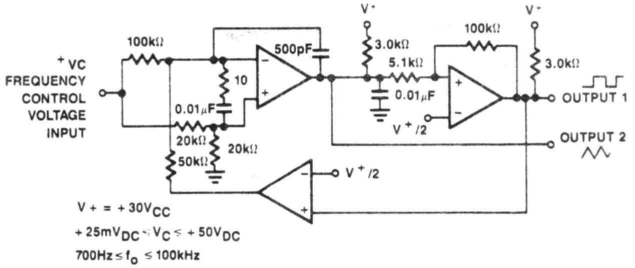
V+ = 5Vdc,
LM193/193A: −55°C ≤ T_A ≤ +125°C unless otherwise specified.
LM293/293A: −25°C ≤ T_A ≤ +85°C unless otherwise specified.
LM393/393A: 0°C ≤ T_A ≤ +70°C unless otherwise specified.
LM2903: −40°C ≤ T_A ≤ +85°C unless otherwise specified.[7]

PARAMETER	TEST CONDITIONS	LM193A			LM293A/393A			LM2903			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS} Input offset voltage[5]	T_A = 25°C Over temp.		±1.0	±2.0 ±4.0		±1.0	±2.0 ±4.0		±2.0 ±9	±7.0 ±15	mV
V_{CM} Input common mode voltage range[6,10]	T_A = 25°C Over temp.	0 0		V+−1.5 V+−2.0	0 0		V+−1.5 V+−2.0	0 0		V+−1.5 V+−2.0	V
V_{IDR} Differential input voltage[4]	Keep all V_{IN}'s ≥ 0Vdc (or V−if need)			V+			V+			V+	V
I_B Input bias current[8]	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range T_A = 25°C Over temp.		25	100 300		25	250 400		25 200	250 500	nA
I_{OS} Input offset current	$I_{IN(+)} - I_{IN(-)}$ T_A = 25°C Over temp.		±3.0	±25 ±100		±5.0	±50 ±150		±5 ±50	±50 ±200	nA nA
I_{OL} Output sink current	$V_{IN(-)}$ ≥ 1Vdc, $V_{IN(+)}$ = 0, V_O ≤ 1.5Vdc, T_A = 25°C	6.0	16		6.0	16		6.0	16		mA
I_{OH} Output leakage current	$V_{IN(+)}$ ≥ 1Vdc, $V_{IN(-)}$ = 0 V_O = 30Vdc Over temp. V_O = 5Vdc, T_A = 25°C		0.1	1.0		0.1	1.0		0.1	1.0	µA na
I_{CC} Supply current	R_L = ∞ on both comparators. T_A = 25°C V+ = 30V, over temp.		0.8 1	1 2.5		0.8 1	1 2.5		0.8 1	1 2.5	mA
A_V Voltage gain	R_L ≥ 15kΩ, V+ = 15Vdc, T_A = 25°C	50	200		50	200		25	100		V/mV
V_{OL} Saturation voltage	$V_{IN(-)}$ ≥ 1Vdc, $V_{IN(+)}$ = 0, I_{SINK} ≤ 4mA T_A = 25°C Over temp.		250	400 700		250	400 700		400	400 700	mV
T_{LSR} Large signal response time	V_{IN} = TTL logic swing, V_{REF} = 1.4Vdc, V_{RL} = 5Vdc, R_L = 5.1kΩ, T_A = 25°C		300			300			300		ns
T_R Response time[9]	V_{RL} = 5Vdc, R_L = 5.1kΩ, T_A = 25°C		1.3			1.3			1.3		µs

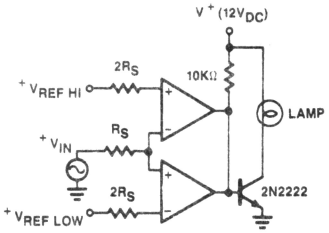
LOW POWER DUAL VOLTAGE COMPARATOR LM193/A/293/A/393/A/2903

TYPICAL APPLICATIONS

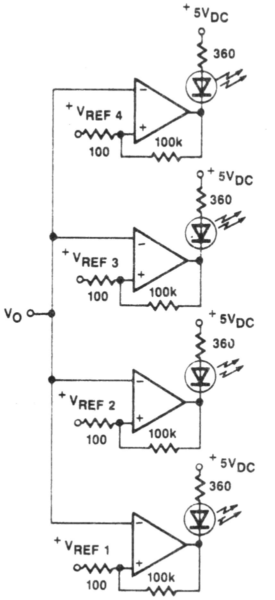
TWO-DECADE HIGH-FREQUENCY VCO


+VC FREQUENCY CONTROL VOLTAGE INPUT
100kΩ
500pF
10
0.01µF
20kΩ
20kΩ
50kΩ
V+
3.0kΩ
5.1kΩ
0.01µF
V+/2
100kΩ
V+
3.0kΩ
OUTPUT 1
OUTPUT 2
V+/2
V+ = +30VCC
+25mVDC ≤ VC ≤ +50VDC
700Hz ≤ fo ≤ 100kHz

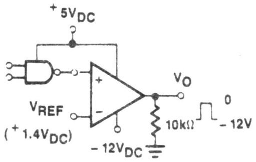
LIMIT COMPARATOR


V+ (12VDC)
+VREF HI
2RS
10KΩ
LAMP
+VIN
RS
2RS
+VREF LOW
2N2222

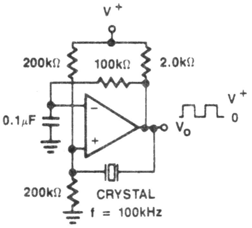
VISIBLE VOLTAGE INDICATOR


+5VDC
360
+VREF 4
100
100k
+5VDC
360
+VREF 3
100
100k
VO
+5VDC
360
+VREF 2
100
100k
+5VDC
360
+VREF 1
100
100k

TTL TO MOS LOGIC CONVERTER


+5VDC
VO
0
VREF
(+1.4VDC)
10kΩ
−12V
−12VDC

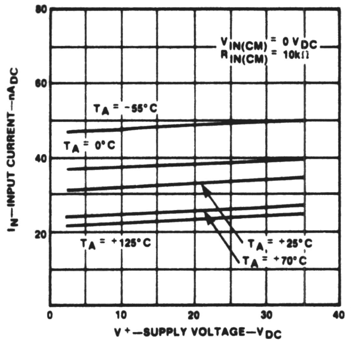
CRYSTAL CONTROLLED OSCILLATOR


V+
200kΩ
100kΩ
2.0kΩ
0.1µF
V+
0
VO
200kΩ
CRYSTAL
f = 100kHz

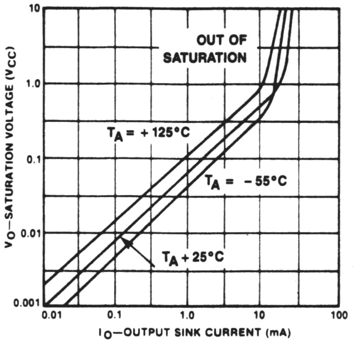
All pins of any unused comparators should be grounded.

TYPICAL PERFORMANCE CHARACTERISTICS

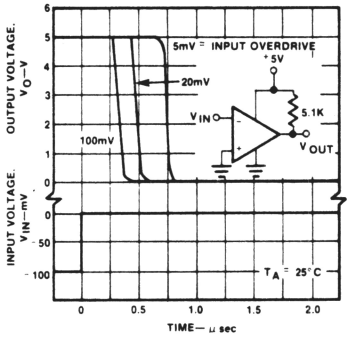
INPUT CURRENT



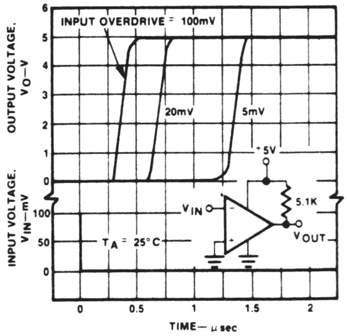
OUTPUT SATURATION VOLTAGE



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES— NEGATIVE TRANSITION



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES— POSITIVE TRANSITION



HIGH SPEED DUAL DIFFERENTIAL COMPARATOR/SENSE AMP SE/NE521

FEATURES

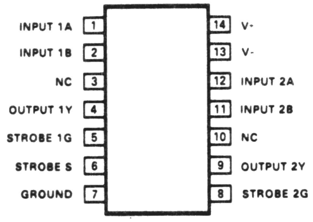
- **12ns maximum guaranteed propagation delay**
- **20μA maximum input bias current**
- **TTL compatible strobes and outputs**
- **Large common mode input voltage range**
- **Operates from standard supply voltages**
- **Military qualifications pending**

APPLICATIONS

- **MOS memory sense amp**
- **A-to-D conversion**
- **High speed line receiver**

PIN CONFIGURATION

D,F,N PACKAGE


INPUT 1A 1
INPUT 1B 2
NC 3
OUTPUT 1Y 4
STROBE 1G 5
STROBE S 6
GROUND 7
14 V-
13 V-
12 INPUT 2A
11 INPUT 2B
10 NC
9 OUTPUT 2Y
8 STROBE 2G

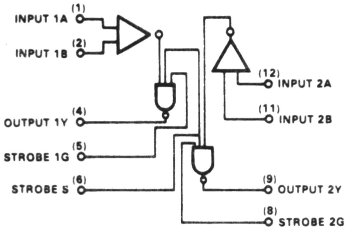
TOP VIEW

ORDER NUMBERS
NE521D,F,N SE521F

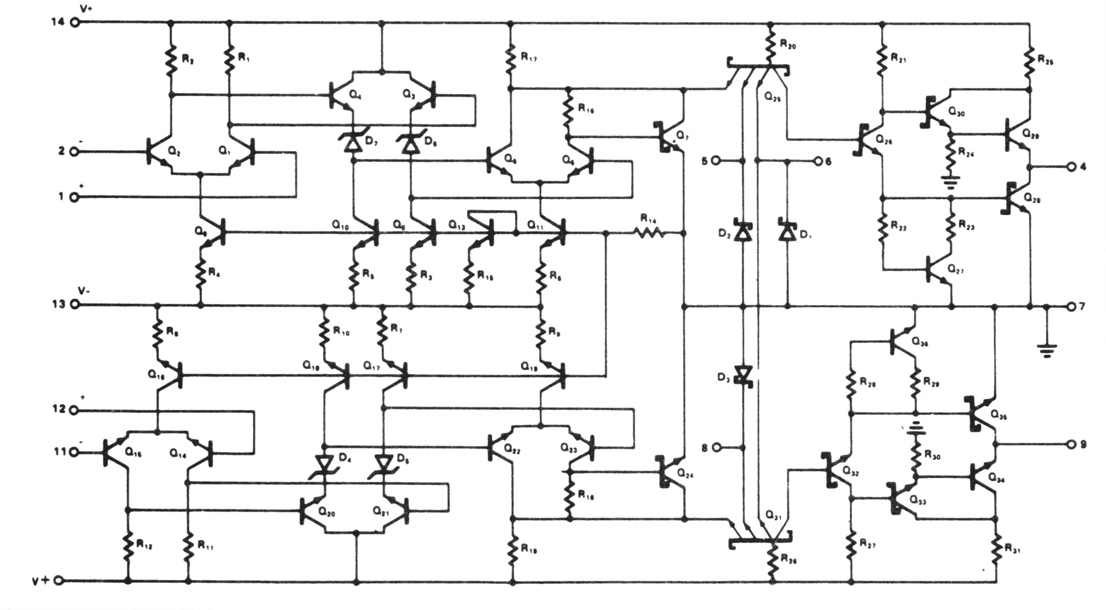
ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
	Supply voltage		V
V+	Positive	+7	
V-	Negative	-7	
V_{IDR}	Differential input voltage	±6	V
V_{IN}	Input voltage		V
	Common mode	±5	
	Strobe/gate	+5.25	
P_D	Power dissipation	600	mW
T_A	Operating temperature range		
	NE521	0 to 70	°C
	SE521	-55 to +125	
T_{stg}	Storage temperature range	-65 to +150	°C
	Lead temperature (solder, 60 sec)	+300	°C

BLOCK DIAGRAM


INPUT 1A (1)
INPUT 1B (2)
OUTPUT 1Y (4)
STROBE 1G (5)
STROBE S (6)
(12) INPUT 2A
(11) INPUT 2B
(9) OUTPUT 2Y
(8) STROBE 2G

EQUIVALENT SCHEMATIC


V+
14
2 -
1 +
V-
13
12 +
11 -
V+
5
6
4
7
8
9
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q12 Q13 Q14 Q15 Q16 Q17 Q18 Q19 Q20 Q21 Q22 Q23 Q24 Q25 Q26 Q27 Q28 Q29 Q30 Q31 Q32 Q33 Q34 Q35 Q36
R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 R11 R12 R14 R15 R16 R17 R18 R19 R20 R21 R22 R23 R24 R25 R26 R27 R28 R29 R30 R31
D1 D2 D3 D4 D5 D6 D7

DC ELECTRICAL CHARACTERISTICS V+ = +5V, V- = -5V, T_A = -55 to +125°C unless otherwise specified

PARAMETER		TEST CONDITIONS	SE LIMITS			UNITS
			Min	Typ	Max	
V_{OS}	Input offset voltage	V+ = +4.5V, V- = -4.5V				mV
	At 25°C			6	7.5	
	Over temperature range				15	
I_{BIAS}	Input bias current	V+ = +5.5V, V- = -5.5V				µA
	At 25°C			7.5	20	
	Over temperature range				40	
I_{OS}	Input offset current	V+ = +5.5V, V- = -5.5V				µA
	At 25°C			1.0	5	
	Over temperature range				12	
V_{CM}	Common mode voltage range	V+ = +4.5V, V- = -4.5V	±3			V
V_{IL}	Low level input voltage					V
	At 25°C				0.8	
	Over temperature				0.7	
V_{IH}	High level input voltage		2.0			V
	Input current	V+ = +5.5V, V- = -5.5V				
I_{IH}	High	V_{IH} = 2.7V				
		1G or 2G strobe			50	µA
		Common strobe S			100	µA
I_{IL}	Low	V_{IL} = 0.5V				
		1G or 2G strobe			-2.0	mA
		Common strobe S			-4.0	mA
	Output voltage	$V_{I(S)}$ = 2.0V				V
V_{OH}	High	V+ = +4.5V, V- = -4.5V, I_{LOAD} = -1mA	2.5	3.4		
V_{OL}	Low	V+ = +4.5V, V- = -4.5V, I_{LOAD}= 10mA			0.5	
		T_A = 25°C, I_{LOAD} = 20mA			0.5	
	Supply voltage					V
V+	Positive		4.5	5.0	5.5	
V-	Negative		-4.5	-5.0	-5.5	
	Supply current	V+ = 5.5V, V- = -5.5V, T_A = 25°C				mA
I_{CC+}	Positive			27	35	
I_{CC-}	Negative			-15	-28	
I_{SC}	Short circuit output current		-35		-115	mA

DC ELECTRICAL CHARACTERISTICS (Cont'd) $V+ = +5V$, $V- = -5V$, $T_A = 0$ to 70°C unless otherwise specified

PARAMETER		TEST CONDITIONS	NE LIMITS			UNITS
			Min	Typ	Max	
V_{OS}	Input offset voltage	V+ = +4.75V, V- = -4.75V				mV
	At 25°C			6	7.5	
	Over temperature range				10	
I_{BIAS}	Input bias current	V+ = +5.25V, V- = -5.25V				µA
	At 25°C			7.5	20	
	Over temperature range				40	
I_{OS}	Input offset current	V+ = +5.25V, V- = -5.25V				µA
	At 25°C			1.0	5	
	Over temperature range				12	
V_{CM}	Common mode voltage range	V+ = +4.75V, V- = -4.75V	±3			V
	Input current	V+ = +5.25V, V- = -5.25V				
I_{IH}	High	$V_{IH} = 2.7V$				
		1G or 2G strobe			50	µA
		Common strobe S			100	µA
I_{IL}	Low	$V_{IL} = 0.5V$				
		1G or 2G strobe			-2.0	mA
		Common strobe S			-4.0	mA
	Output voltage	$V_{I(S)} = 2.0V$				V
V_{OH}	High	V+ = +4.75V, V- = -4.75V, $I_{LOAD} = -1mA$	2.7	3.4		
V_{OL}	Low	V+ = +5.25V, V- = -5.25V, $I_{LOAD} = 20mA$			0.5	
	Supply voltage					V
V+	Positive		4.75	5.0	5.25	
V-	Negative		-4.75	-5.0	-5.25	
	Supply current	V+ = 5.25V, V- = -5.25V, $T_A = 25°C$				mA
I_{CC+}	Positive			27	35	
I_{CC-}	Negative			-15	-28	
I_{SC}	Short circuit output current		-40		-100	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $R_L = 280\Omega$ $C_L = 15pF$ $V+ = +5V$ $V- = -5V$

PARAMETER		FROM INPUT	TO OUTPUT	LIMITS			UNIT
				Min	Typ	Max	
Large Signal Switching Speed							
	Propagation delay						ns
$t_{PLH(D)}$	Low to high[1]	Amp	Output		8	12	
$t_{PHL(D)}$	High to low[1]	Amp	Output		6	9	
$t_{PLH(S)}$	Low to high[2]	Strobe	Output		4.5	10	
$t_{PHL(S)}$	High to low[2]	Strobe	Output		3.0	6	
	Maximum operating frequency			40	55		MHz

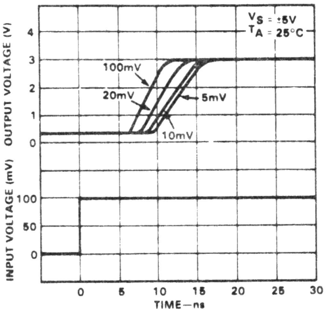
NOTES

1 Response time measured from 0V point of ±100mV p-p 10MHz square wave to the 1.5V point of the output

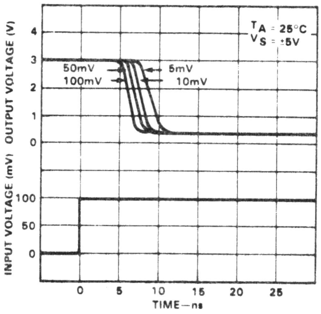
2 Response time measured from 1.5V point of input to 1.5V point of the output

TYPICAL PERFORMANCE CHARACTERISTICS

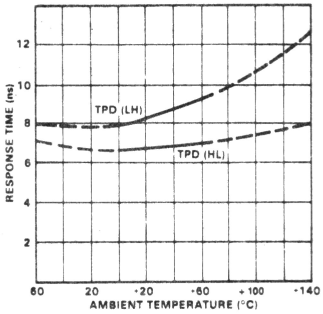
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



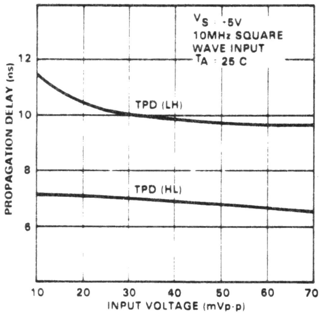
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



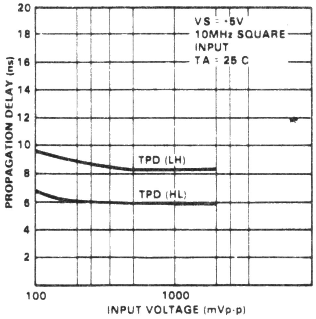
RESPONSE TIME vs TEMPERATURE



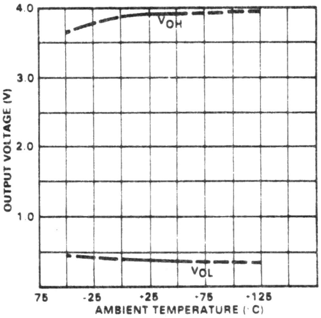
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGE



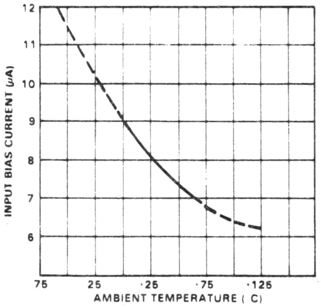
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



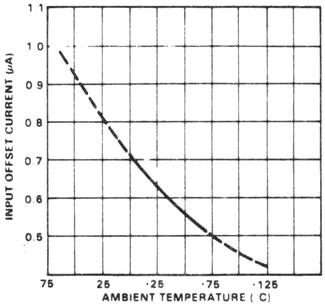
OUTPUT VOLTAGE vs AMBIENT TEMPERATURE



INPUT BIAS CURRENT vs AMBIENT TEMPERATURE



INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE



HIGH SPEED DUAL DIFFERENTIAL COMPARATOR/SENSE AMP SE/NE522

FEATURES

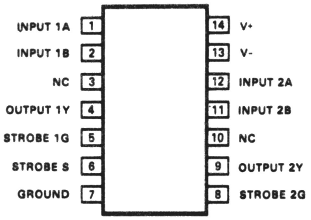
- **15ns maximum guaranteed propagation delay**
- **20μA maximum input bias current**
- **TTL compatible strobes and outputs**
- **Open collector output for wire-OR'd applications**
- **Large common mode input voltage range**
- **Operates from standard supply voltages**

APPLICATIONS

- **MOS memory sense amp**
- **A-to-D conversion**
- **High speed line receiver**

PIN CONFIGURATION

D,F,N PACKAGE


INPUT 1A 1
INPUT 1B 2
NC 3
OUTPUT 1Y 4
STROBE 1G 5
STROBE S 6
GROUND 7
14 V+
13 V-
12 INPUT 2A
11 INPUT 2B
10 NC
9 OUTPUT 2Y
8 STROBE 2G

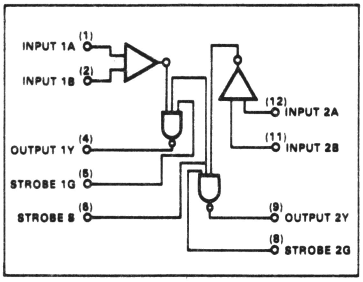
TOP VIEW

ORDER NUMBERS
NE522D,F,N SE522F

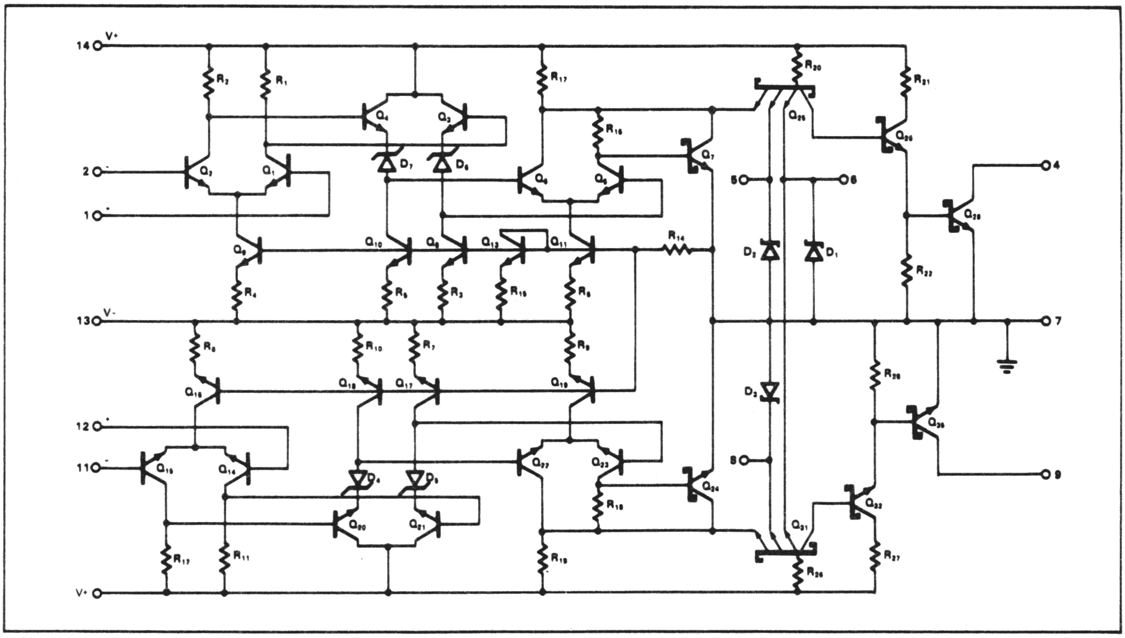
ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
	Supply voltage		V
V+	Positive	+7	
V-	Negative	-7	
V_{IDR}	Differential input voltage	±6	V
V_{IN}	Input voltage		V
	Common mode	±5	
	Strobe/gate	±5.25	
P_D	Power dissipation	600	mW
T_A	Operating temperature range NE	0 to 70	°C
	SE	-55 to +125	
T_{stg}	Storage temperature range	-65 to +150	°C
	Lead temperature (solder, 60 sec)	+300	°C

BLOCK DIAGRAM


INPUT 1A (1)
INPUT 1B (2)
OUTPUT 1Y (4)
STROBE 1G (5)
STROBE S (6)
(12) INPUT 2A
(11) INPUT 2B
(9) OUTPUT 2Y
(8) STROBE 2G

EQUIVALENT SCHEMATIC


14 V+
2
1
13 V-
12
11
V+
5
6
5
4
7
9

DC ELECTRICAL CHARACTERISTICS ±5V ±10%, T_A = -55 to 125°C unless otherwise specified

PARAMETER		TEST CONDITIONS	SE LIMITS			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage	V+ = +4.5V, V- = -4.5V				mV
	At 25°C			6	7.5	
	Over temperature range				15.	
I_{BIAS}	Input bias current	V+ = +5.5V, V- = -5.5V				µA
	At 25°C			7.5	20.	
	Over temperature range				40.	
I_{OS}	Input offset current	V+ = +5.5V, V- = -5.5V				µA
	At 25°C			1.0	5.	
	Over temperature range				12.	
V_{CM}	Common mode voltage range	V+ = +4.5V, V- = -4.5V	±3			V
V_{IL}	Low level input					V
	Voltage at 25°C				0.8	
	over temperature				0.7	
V_{IH}	High level temperature		2.0			V
	Input current	V+ = +5.5V, V- = -5.5V				
I_{IH}	High	V_{IH} = 2.7V				
		1G or 2G strobe			50	µA
		Common strobe S			100	µA
I_{IL}	Low	V_{IL} = 0.5V				
		1G 2G strobe			-2	mA
		Common strobe S			-4	mA
	Output voltage					V
V_{OL}	Low	V+ = +4.5V, V- = -4.5V				
		I_{OL} = 20mA, T_A = 25°C			.5	
		I_{OL} = 10mA			.5	
	Output current					µA
I_{OH}	High	V_{CC+} = +4.5, V_{CC-} = -4.5V, V_{OH} = 5.5V				
					250	
	Supply voltage					V
V+	Positive		4.5	5.0	5.5	
V-	Negative		-4.5	-5.0	-5.5	
	Supply current	V+ = 5.5V, V- = -5.5V				mA
I_{CC+}	Positive			27	35	
I_{CC-}	Negative			-15	– 28	

HIGH SPEED DUAL DIFFERENTIAL COMPARATOR/SENSE AMP SE/NE522

DC ELECTRICAL CHARACTERISTICS (Cont'd) ±5V ±5%, T_A = 0 to 70°C unless otherwise specified

PARAMETER		TEST CONDITIONS	NE LIMITS			UNIT
			Min	Typ	Max	
V_{OS}	Input offset voltage	V+ = +4.75V, V- = -4.75V				mV
	At 25°C			6	7.5	
	Over temperature range				10	
I_{BIAS}	Input bias current	V+ = +5.25V, V- = -5.25V				µA
	At 25°C			7.5	20	
	Over temperature range				40	
I_{OS}	Input offset current	V+ = +5.25V, V- = -5.25V				µA
	At 25°C			1.0	5	
	Over temperature range				12	
V_{CM}	Common mode voltage range	V+ = +4.75V, V- = -4.75V	±3			V
	Input current	V+ = +5.25V, V- = -5.25V				
I_{IH}	High	V_{IH} = 2.7V				
		1G or 2G strobe			50	µA
		Common strobe S			100	µA
I_{IL}	Low	V_{IL} = 0.5V				
		1G 2G strobe			-2.0	mA
		Common strobe S			-4.0	mA
	Output voltage	V+ = +5.25V, V- = -5.25V, $V_{I(S)}$ = 2.0V				V
V_{OL}	Low	I_{LOAD} = 20mA			0.5	
	Output current					µA
I_{OH}	High	V_{CC+} = +4.75, V_{CC-} = -4.75V, V_{OH} = 5.25V			250	
	Supply voltage					V
V+	Positive		4.75	5.0	5.25	
V-	Negative		-4.75	-5.0	-5.25	
	Supply current	V+ = 5.25V, V- = -5.25V, T_A = 25°C				mA
I_{CC+}	Positive			27	50	
I_{CC-}	Negative			-15	-28	

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, R_L = 280Ω, C_L = 15pF

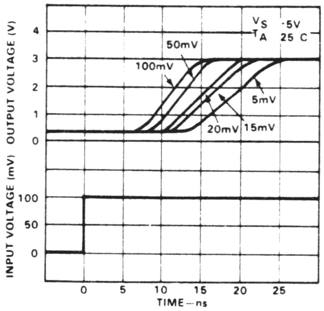
PARAMETER		FROM INPUT	TO OUTPUT	LIMITS			UNIT
				Min	Typ	Max	
	Input resistance				4		kΩ
	Input capacitance				3		pF
Large Signal Switching Speed							
	Propagation delay						ns
$t_{PLH(D)}$	Low to high[1]	Amp	Output		10	15	
$t_{PHL(D)}$	High to low[1]	Amp	Output		8	12	
$t_{PLH(S)}$	Low to high[2]	Strobe	Output		6	13	
$t_{PHL(S)}$	High to low[2]	Strobe	Output		5	9	
	Maximum operating frequency			25	35		MHz

NOTES

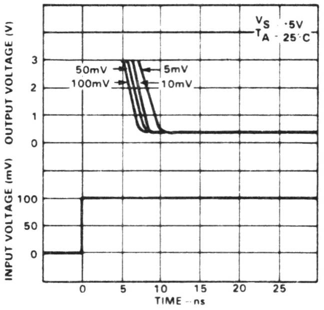
1. Response time measured from 0V point of +100mV p-p 10MHz square wave to the 1.5V point of the output
2. Response time measured from 1.5V point of input to 1.5V point of the output

TYPICAL PERFORMANCE CHARACTERISTICS

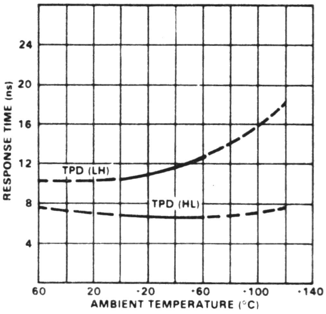
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



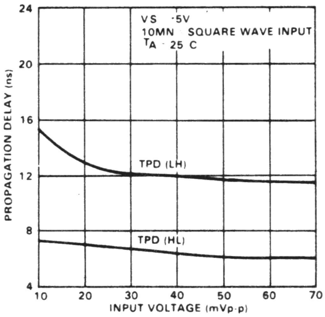
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



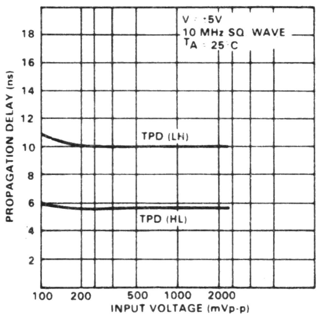
RESPONSE TIME vs TEMPERATURE



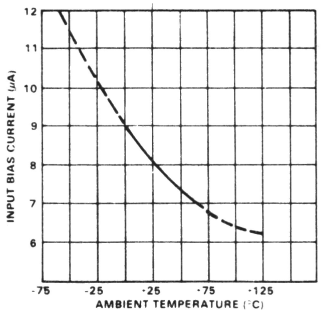
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



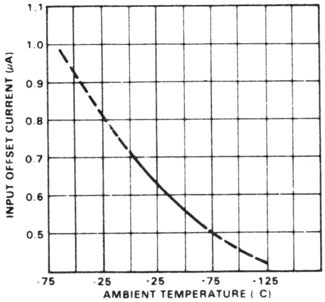
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



INPUT BIAS CURRENT vs AMBIENT TEMPERATURE



INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE



VOLTAGE COMPARATOR SE/NE527

DESCRIPTION

The SE/NE527 is a high speed analog voltage comparator which, in the first time mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed T²L gates with a precision linear amplifier on a single monolithic chip. The SE/NE527 is similar in design to the Signetics SE/NE529 voltage comparator except that it incorporates a "Emitter Follower" input stage for extremely low input currents. This opens the door to a whole new range of applications for analog voltage comparators.

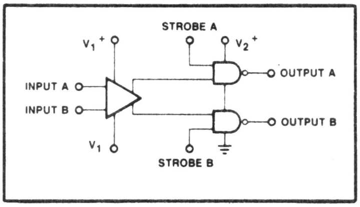
FEATURES

- **15ns propagation delay**
- **Complementary output gates**
- **TTL or ECL compatible outputs**
- **Wide common mode and differential voltage range**
- **Mil std 883A,B,C available**
- **Typical Gain of 5000**

APPLICATIONS

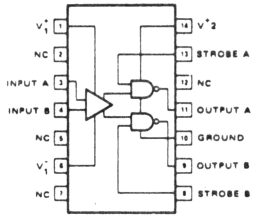
- **A/D conversion**
- **ECL to TTL interface**
- **TTL to ECL interface**
- **Memory sensing**
- **Optical data coupling**

BLOCK DIAGRAM


STROBE A
V_1^+
V_2^+
INPUT A
INPUT B
OUTPUT A
OUTPUT B
V_1^-
STROBE B

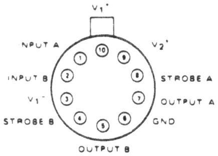
PIN CONFIGURATIONS

D,F,N PACKAGE


V_1^+ 1
NC 2
INPUT A 3
INPUT B 4
NC 5
V_1^- 6
NC 7
14 V_2^+
13 STROBE A
12 NC
11 OUTPUT A
10 GROUND
9 OUTPUT B
8 STROBE B

TOP VIEW
ORDER NUMBERS
NE527D,N,F SE527F

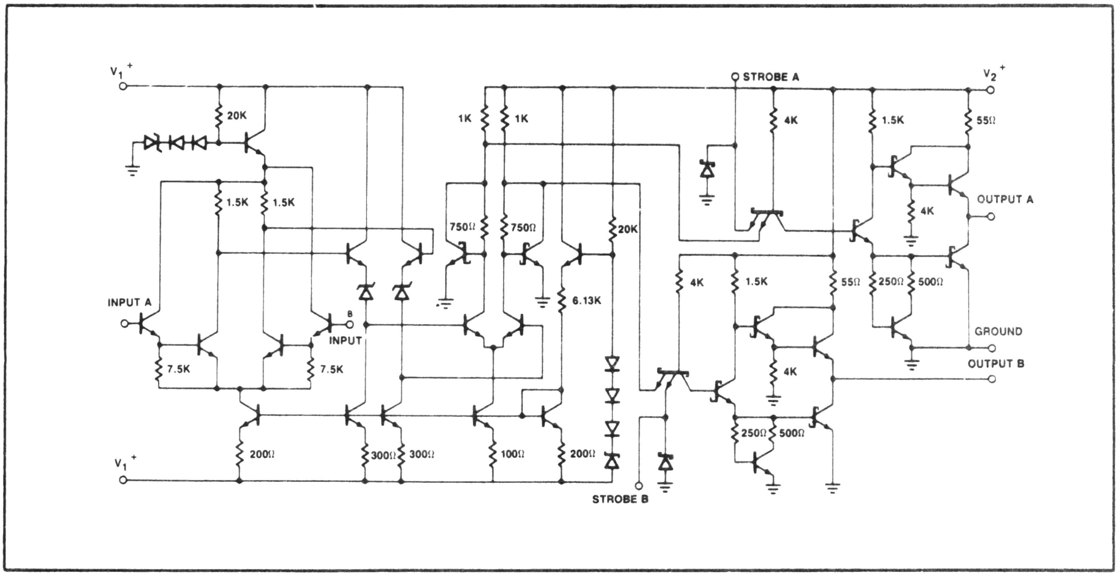
H PACKAGE*


V_1^+
INPUT A
V_2^+
INPUT B
STROBE A
V_1^-
OUTPUT A
STROBE B
GND
OUTPUT B

ORDER NUMBERS
SE/NE527H

*Metal cans (H) not recommended for new designs

EQUIVALENT SCHEMATIC


V_1^+
20K
1.5K
1.5K
INPUT A
7.5K
7.5K
B INPUT
200Ω
300Ω
300Ω
100Ω
200Ω
V_1^-
1K
1K
750Ω
750Ω
20K
6.13K
STROBE A
4K
4K
1.5K
55Ω
1.5K
55Ω
4K
250Ω
500Ω
4K
250Ω
500Ω
V_2^+
OUTPUT A
GROUND
OUTPUT B
STROBE B

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply voltage (V1+)	+15	V
Negative supply voltage (V1-)	-15	V
Gate supply voltage (V2+)	+7	V
Output voltage	+7	V
Differential input voltage	±5	V
Input common mode voltage	±6	V
Power dissipation	600	mW
Operating temperature range		
NE527	0 to +70	°C
SE527	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	+300	°C

DC ELECTRICAL CHARACTERISTICS $V_{1}^{+} = 10V, V_{1}^{-} = -10V, V_{2}^{+} = +5.0V$

PARAMETER	TEST CONDITIONS	SE527			NE527			UNIT
		Min	Typ	Max	Min	Typ	Max	
INPUT CHARACTERISTICS								
Input offset voltage @ 25°C				4			6	mV
Over temperature range				6			10	mV
Input bias current @ 25°C				2			2	μA
Over temperature range				4			4	μA
Input offset current @ 25°C				0.5			0.75	μA
Over temperature range	$V_{IN} = 0V$			1			1	μA
Common mode voltage range				±5				V
GATE CHARACTERISTICS								
Output voltage								
"1" State	$V_{2}^{+} = 4.75V, I_{SOURCE} = -1mA$	2.5	3.3		2.7	3.3		V
"0" State	$V_{2}^{+} = 4.75V, I_{SINK} = 10mA$			0.5			0.5	V
Strobe inputs								
"0" Input current[1]	$V_{2}^{+} = 5.25V, V_{STROBE} = 0.5V$			-2			-2	mA
"1" Input current @ 25°C[1]	$V_{2}^{+} = 5.25V, V_{STROBE} = 2.7V$			50			100	μA
Over temperature range	$V_{2}^{+} = 5.25V, V_{STROBE} = 2.7V$			200			200	μA
"0" Input voltage	$V_{2}^{+} = 4.75V$			0.8			0.8	V
"1" Input voltage	$V_{2}^{+} = 4.75V$	2.0			2.0			V
Short circuit Output current	$V_{2}^{+} = 5.25V, V_{OUT} = 0V$	-18		-70	-18		-70	mA
POWER SUPPLY REQUIREMENTS								
Supply voltage								
V_{1}^{+}		5		10	5		10	V
V_{1}^{-}		-6		-10	-6		-10	V
V_{2}^{+}		4.5	5	5.5	4.75	5	5.25	V
Supply current	$V_{1}^{+} = 10V, V_{1}^{-} = -10V$ $V_{2}^{+} = 5.25V$							
I_{1}^{+}	Over temp.			5			5	mA
I_{1}^{-}	Over temp.			10			10	mA
I_{2}^{+}	Over temp.			20			20	mA

NOTES

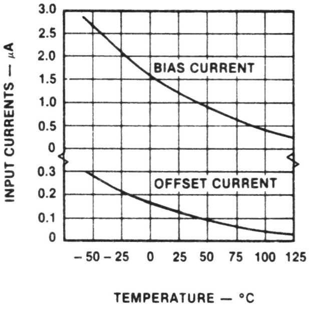
1. See logic function table.

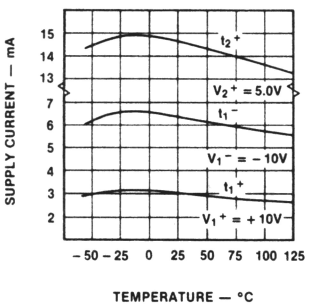
VOLTAGE COMPARATOR SE/NE527

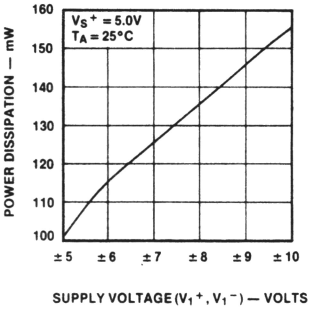
AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

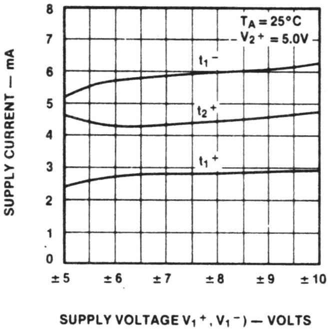
PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Transient response propagation delay time	$V_{IN} = \pm100mV$ step				
t_{PLH}			16	26	ns
t_{PHL}			14	24	ns
Delay between output A and B			2	5	ns
Strobe delay time					
t_{on} Turn-on time			6		ns
t_{off} Turn-off time			6		ns

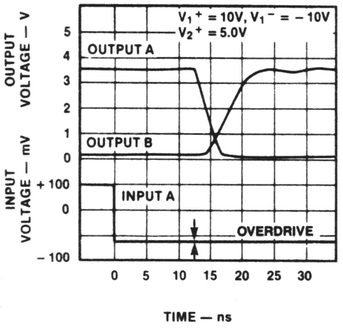
TYPICAL PERFORMANCE CHARACTERISTICS

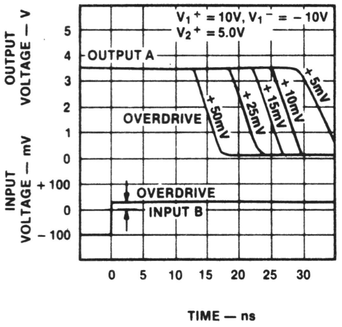

INPUT CURRENTS vs TEMPERATURE


SUPPLY CURRENT vs TEMPERATURE


POWER DISSIPATION vs SUPPLY VOLTAGE


SUPPLY CURRENT vs SUPPLY VOLTAGE

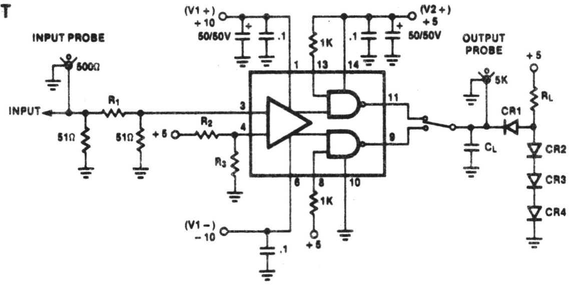

OUTPUT PROPAGATION DELAYS


RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

VOLTAGE COMPARATOR

SE/NE527

RESPONSE TIME TEST CIRCUIT


(V1+)
+10
50/50V
.1
1K
(V2+)
+5
50/50V
INPUT PROBE
500Ω
INPUT
R₁
51Ω
51Ω
+5
R₂
R₃
1
13
14
3
4
11
9
6
8
10
1K
(V1−)
−10
.1
+5
OUTPUT PROBE
5K
C_L
CR1
+5
R_L
CR2
CR3
CR4

CR1 – CR4 = IN914
R1 SELECTED FOR 15:1 DIVIDER
R2,3 SELECTED FOR 100mV AT PIN 4

INPUT
PRR = 1MHz
P_W = 50ns
Tr = Tf = 2ns
AMPLITUDE = 3.00V

APPLICATIONS

One of the main features of the device is that supply voltages (V1+, V1−) need not be balanced, as indicated in the following diagrams. For proper operation, however, negative supply (V1−) should always be at least six volts more negative than the ground terminal (pin 6). Input Common Mode range should be limited to values of two volts less than the supply voltages (V1+ and V1−) up to a maximum of ±6 volts as supply voltages are increased.

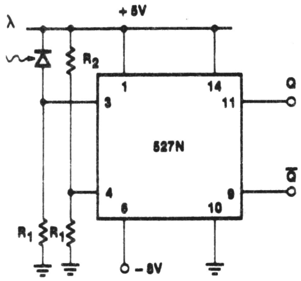
NE527 LOGIC FUNCTION

V_{IN} (A^+, B^-)	STR 'A'	STR 'B'	OUT 'A'	OUT 'B'	COMMENT
$> V_{off}$	X	h/l	H	l/h	Read I_{ILB}, I_{IHA}
$< -V_{off}$	h/l	X	l/h	H	Read I_{ILA}, I_{IHB}

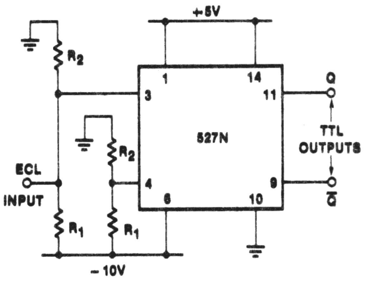
It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

TYPICAL APPLICATIONS

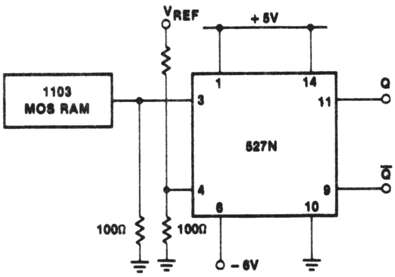
PHOTODIODE DETECTOR


λ
+5V
R₂
1
14
3
11
Q
527N
4
9
Q̄
6
10
R₁
R₁
−5V

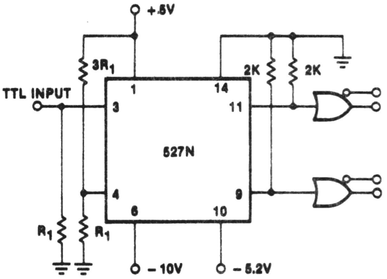
ECL TO TTL INTERFACE


+5V
R₂
1
14
3
11
Q
527N
TTL OUTPUTS
R₂
ECL INPUT
4
9
Q̄
6
10
R₁
R₁
−10V

MOS MEMORY SENSE AMP


VREF
+5V
1103 MOS RAM
1
14
3
11
Q
527N
4
9
Q̄
6
10
100Ω
100Ω
−6V

TTL TO ECL INTERFACE


+5V
3R₁
2K
2K
TTL INPUT
1
14
3
11
527N
4
9
6
10
R₁
R₁
−10V
−5.2V

VOLTAGE COMPARATOR SE/NE529

DESCRIPTION

The SE/NE529 is a high speed analog voltage comparator which, for the first time mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed T2L gates with a precision linear amplifier on a single monolithic chip.

FEATURES

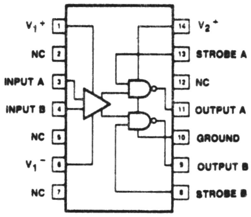
- **10ns propagation delay**
- **Complementary output gates**
- **TTL or ECL compatible outputs**
- **Wide common mode and differential voltage range**
- **Typical Gain 5000**

APPLICATIONS

- **A/D conversion**
- **ECL to TTL interface**
- **TTL to ECL interface**
- **Memory sensing**
- **Optical data coupling**
- **Mil std 883A,B,C available**

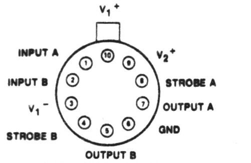
PIN CONFIGURATION

D,F,N PACKAGE


V1+ 1
NC 2
INPUT A 3
INPUT B 4
NC 5
V1- 6
NC 7
14 V2+
13 STROBE A
12 NC
11 OUTPUT A
10 GROUND
9 OUTPUT B
8 STROBE B

TOP VIEW
ORDER NUMBERS
SE/NE529F, NE529N,D

H PACKAGE*

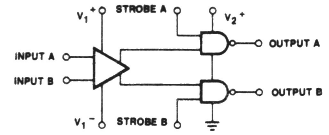

V1+
INPUT A
INPUT B
V1-
STROBE B
OUTPUT B
GND
OUTPUT A
STROBE A
V2+

ORDER NUMBERS
SE/NE529H
*Metal cans (H) not recommended for new designs

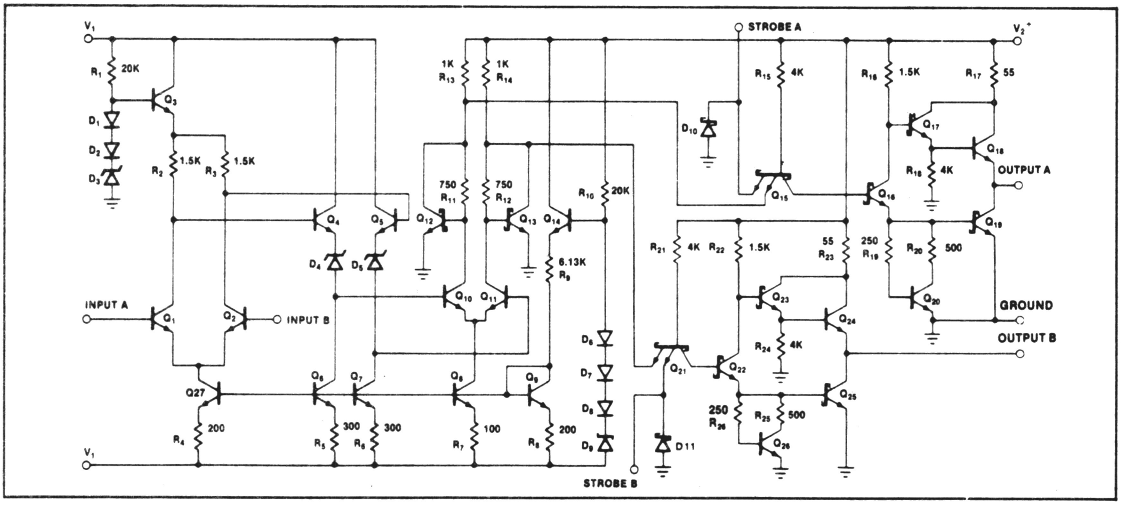
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply voltage (V1+)	+15	V
Negative supply voltage (V1-)	-15	V
Gate supply voltage (V2+)	+7	V
Output voltage	+7	V
Differential input voltage	±5	V
Input common mode voltage	±6	V
Power dissipation	600	mW
Operating temperature range		
NE529	0 to +70	°C
SE529	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60 sec)	+300	°C

BLOCK DIAGRAM


V1+
STROBE A
V2+
INPUT A
INPUT B
OUTPUT A
OUTPUT B
V1-
STROBE B

EQUIVALENT SCHEMATIC


V1
R1 20K
Q3
D1
D2
D3
R2 1.5K
R3 1.5K
Q4
Q5
D4
D5
INPUT A
Q1
Q2
INPUT B
Q27
R4 200
V1
Q6
Q7
R5 300
R6 300
1K R13
1K R14
750 R11
750 R12
Q12
Q13
Q14
Q10
Q11
Q8
Q9
R7 100
R8 200
R10 20K
6.13K R9
D6
D7
D8
D9
STROBE B
STROBE A
D10
R15 4K
Q15
R21 4K
R22 1.5K
Q21
D11
Q22
Q23
R24 4K
Q24
250 R26
R25 500
Q26
Q25
55 R23
250 R19
R16 1.5K
R17 55
Q17
Q18
R18 4K
Q16
OUTPUT A
Q19
R20 500
Q20
GROUND
OUTPUT B
V2+

VOLTAGE COMPARATOR

SE/NE529

DC ELECTRICAL CHARACTERISTICS $V_1+ = +10V$, $V_2+ = +5.0V$, $V_1- = -10V$

PARAMETER	TEST CONDITIONS	SE529			NE529			UNIT
		Min	Typ	Max	Min	Typ	Max	
INPUT CHARACTERISTICS								
Input offset voltage @25°C				4			6	mV
Over temperature range				6			10	mV
Input bias current @25°C			5	12		5	20	μA
Over temperature range	$V_{IN} = 0V$			36			50	μA
Input offset current @25°C			2	3		2	5	μA
Over temperature range	$V_{IN} = 0V$			9			15	μA
Common mode voltage range			0	±5		0	±5	V
GATE CHARACTERISTICS								
Output voltage								
"1" state	$V_2+ = 4.75V$, $I_{source} = -1mA$	2.5	3.3		2.7	3.3		V
"0" state	$V_2+ = 4.75V$, $I_{sink} = 10mA$			0.5			0.5	V
Strobe inputs								
"0" Input current[1]	$V_2+ = 5.25V$, $V_{strobe} = 0.5V$			-2			-2	mA
"1" Input current @ 25°C[1]	$V_2+ = 5.25V$, $V_{strobe} = 2.7V$			50			100	μA
Over temperature range	$V_2+ = 5.25V$, $V_{strobe} = 2.7V$			200			200	μA
"0" input voltage	$V_2+ = 4.75V$			0.8			0.8	V
"1" input voltage	$V_2+ = 4.75V$	2.0			2.0			V
Short circuit								
Output current	$V_2+ = 5.25V$, $V_{OUT} = 0V$	-18		-70	-18		-70	mA
POWER SUPPLY REQUIREMENTS								
Supply voltage								
V_1+		5		10	5		10	V
V_1-		-6		-10	-6		-10	V
V_2+		4.5	5	5.5	4.75	5	5.25	V
Supply current	$V_1+ = 10V$, $V_1- = -10V$ $V_2+ = 5.25V$							
I_1+	Over temp.			5			5	mA
I_1-	Over temp.			10			10	mA
I_2+	Over temp.			20			20	mA

NOTES

1. See logic function table.

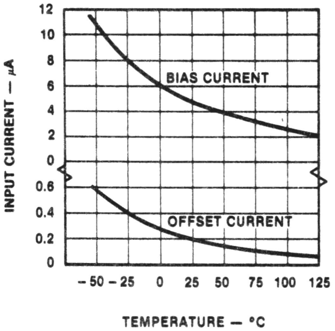
AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Transient response	$V_{IN} = \pm 100mV$ step				
Propagation delay time					
t_{PLH}			12	22	ns
t_{PHL}			10	20	ns
Delay between output A and B			2	5	ns
Strobe delay time					
t_{ON} turn-on time			6		ns
t_{OFF} turn-off time			6		ns

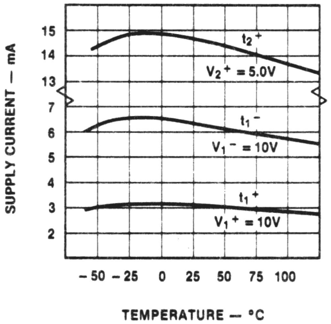
VOLTAGE COMPARATOR SE/NE529

TYPICAL PERFORMANCE CHARACTERISTICS

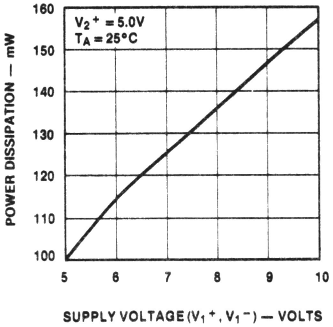
INPUT CURRENTS vs TEMPERATURE



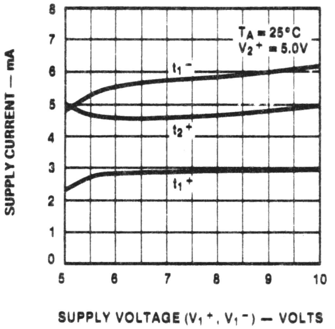
SUPPLY CURRENT vs TEMPERATURE



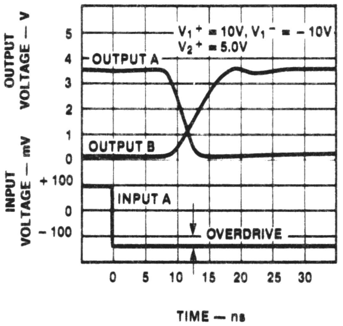
POWER DISSIPATION vs SUPPLY VOLTAGE



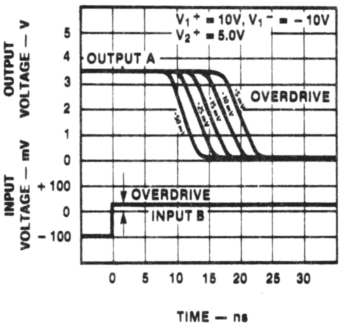
SUPPLY CURRENT vs SUPPLY VOLTAGE



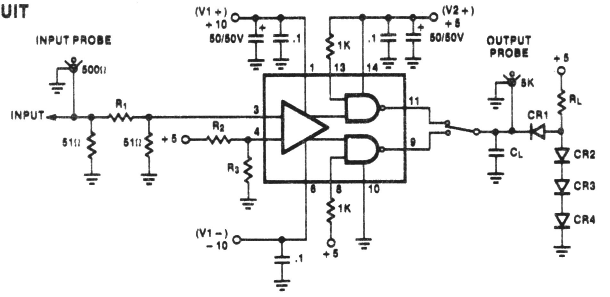
OUTPUT PROPAGATION DELAYS



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME TEST CIRCUIT


(V1+)
+10
50/50V
.1
1K
.1
50/50V
(V2+)
+5
INPUT PROBE
500Ω
INPUT
R1
51Ω
51Ω
+5
R2
R3
3
4
1
13
14
11
9
6
8
10
1K
+5
(V1−)
−10
.1
OUTPUT PROBE
5K
CL
CR1
+5
RL
CR2
CR3
CR4

CR1 – CR4 = IN914
R1 SELECTED FOR 15:1 DIVIDER
R2,3 SELECTED FOR 100mV AT PIN 4

INPUT
PRR = 1MHz
P_W = 50ns
$T_r = T_f$ = 2ns
AMPLITUDE = 3.00V

VOLTAGE COMPARATOR SE/NE529

APPLICATIONS

One of the main features of the device is that supply voltages (V1+, V1-) need not be balanced, as indicated in the following diagrams. For proper operation, however, negative supply (V1-) should always be at least six volts more negative than the ground terminal (pin 6). Input Common Mode range should be limited to values of two volts less than the supply voltages (V1+ and V1-) up to a maximum of ±6 volts as supply voltages are increased.

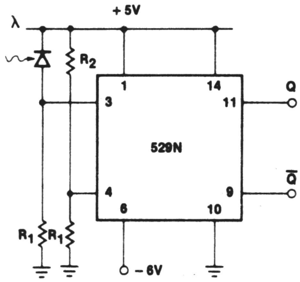
It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

NE529 LOGIC FUNCTION

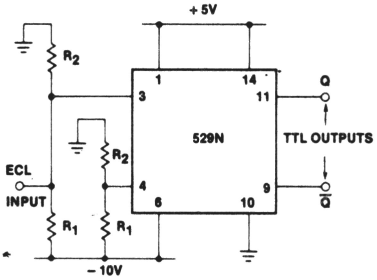
V_{IN} (A^+, B^-)	STR 'A'	STR 'B'	OUT 'A'	OUT 'B'	COMMENT
$> V_{off}$	X	h/l	H	l/h	Read I_{ILB}, I_{IHA}
$< -V_{off}$	h/l	X	l/h	H	Read I_{ILA}, I_{IHB}

TYPICAL APPLICATIONS

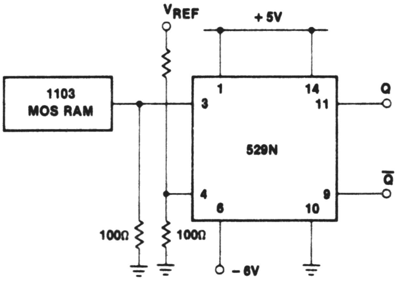
PHOTODIODE DETECTOR


λ
+5V
R2
1
14
3
11
Q
529N
Q̄
4
9
6
10
R1
R1
-6V

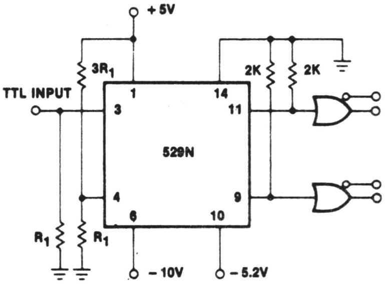
ECL TO TTL INTERFACE


+5V
R2
1
14
3
11
Q
529N
TTL OUTPUTS
R2
ECL
INPUT
4
9
6
10
Q̄
R1
R1
-10V

MOS MEMORY SENSE AMP


VREF
+5V
1103
MOS RAM
1
14
3
11
Q
529N
Q̄
4
9
6
10
100Ω
100Ω
-6V

TTL TO ECL INTERFACE


+5V
3R1
2K
2K
TTL INPUT
1
14
3
11
529N
4
9
6
10
R1
R1
-10V
-5.2V

DISPLAY DRIVER—SYMBOLS AND DEFINITIONS

Absolute Maximum Rating

Operating safe zones. Exceeding these limits could cause permanent damage to the device and are not meant to imply that devices can operate at these limits.

BCD

Binary Coded Decimal.

$\overline{BI}$/RBO

Blanking Input or Ripple Blanking Output.

CE

Chip Enable.

CLR

Clear. Clear command will preset all internal circuits to a predetermined state.

Duty Cycle

Ratio of time on to time off. Generally expressed in percentage.

F_{MAX}

The maximum clock frequency: the maximum input frequency at a clock input for the predictable performance. Above this frequency the device may cease to function.

I_B

Input Bias Current. Current into an analog circuit input, specified at a particular voltage level.

I_{CC} ($-I_{CC}$)

Supply Current. The current flowing into the $+V_{CC}$ ($-V_{CC}$) supply terminal of the circuit with specified input conditions and open outputs. Input conditions are chosen to guarantee worst case operation unless specified.

I_{CEX}

Output Leakage Current. The current flowing out of or into a disabled (off) output with a specified High output voltage applied.

I_{IH}

Input High Current. The current flowing into or out of an input when a specified High level voltage is applied to that input.

I_{IL}

Input Low Current. The current flowing out of an input when a specified Low level voltage is applied to that input.

I_{OH}

Output Current Source the device can supply while maintaining a specified voltage output level.

I_{OL}

Output Low Current. The current flowing into an output when it is in the Low State.

I_{OS}

Output Short-Circuit Current. The current flowing out of an output which is in the High state when that output is shorted to ground.

I_S

Source Current. Current flowing into the V_S supply terminal of the device with specified operating conditions.

I_{SEG}

Segment Current. The amount of current supplied to each segment as a display. Current ratios are generally compared to segment 'b'.

LED

Light Emitting Diode.

Package Type Designation

See full package designations in Appendix.

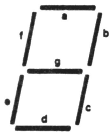
Power Dissipation

The power that the device can safely handle at 15°C. The dissipation must be derated as indicated for the individual package type.

$\overline{RBI}$

Ripple Blanking Input.

Segment Identification



T_A

Ambient temperature range. Allowable range of the surrounding environment of the operating device.

t_h

Hold Time. The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the current logic level may be released prior to the active transition of the timing pulse and still be recognized.

T_J

Junction Temperature. The maximum temperature of the device. 150°C is standard for silicon devices.

t_{PHL}

Propagation Delay Times. The time between the specified reference points on the input and output waveforms with the output changing from the defined HIGH level to the defined LOW level.

t_{PLH}

Propagation Delay Time. The time between the specified reference points on the input and output waveforms with the output changing from the defined LOW level to the defined HIGH level.

t_{rec}

Recovery Time. The time between the reference point on the trailing edge of an asynchronous input control pulse and the reference point on the activating edge of a synchronous (clock) pulse input such that the device will respond to the synchronous input.

t_s

Setup Time. The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

DISPLAY DRIVER—SYMBOLS AND DEFINITIONS

DISPLAY DRIVER DEFINITIONS (Cont'd)

Truth Tables

0 is logic level low
1 is logic level high
X — don't care condition — has no effect under circuit conditions listed.

Typical Value

The typical value of a particular parameter at 25°C determined by characterization of the device or sampling. Usually indicates that the particular device is not 100% tested for the parameter because it does not vary or can be determined by design and other tested variables. Occasionally typical values are given rather than min-max values because 100% testing would raise the cost of the product to a prohibitive level. If a typical value must be guaranteed to ensure specific operation, custom testing can often be provided at an additional cost to the user.

V_{BR}

Output Breakdown Voltage. Maximum voltage applied to a disabled (off) output to ensure a leakage current less than the specified value.

V_{CC} ($-V_{CC}$)

Supply Voltage. The range of power supply voltage over which the device will operate safely.

V_F

Forward voltage drop of a device at a specified current level.

V_{IH}

Input High Voltage. The range of input voltages recognized by the device as a logic high.

V_{IL}

Input Low Voltage. The range of input voltages recognized by the device as a logic low.

V_{IN}

The range of voltage on any input which the device can safely handle or a specified input voltage to the device.

V_{OH}

Output High Voltage. The minimum guaranteed High voltage at an output terminal for the specified output current I_{OH} and at the minimum V_{CC} value.

V_{OL}

Output Low Voltage. The maximum guaranteed low voltage at an output terminal sinking the specified load current I_{OL}.

V_{OUT}

The range of voltage on any output which the device can safely handle or a specified output voltage to the device.

V_S

Source Voltage. A separate V_{CC} line depending on part type.

$\overline{XX}$

Negate Bar — when it appears over a function indicates that the "true" or valid condition of that function is a logic low level.
i.e. LE — would require a logic high level to cause a latch enable
$\overline{LE}$ — would require a logic low level to cause a latch enable.

QUAD LINE DRIVER

MC1488

DESCRIPTION

The MC1488 is a quad line driver which converts standard DTL/TTL input logic levels through one stage of inversion to output levels which meet EIA Standard No. RS-232C and CCITT Recommendation V.24.

FEATURES

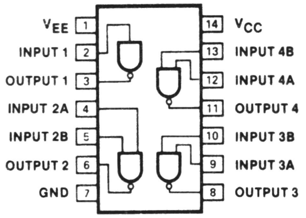
- **Current limited output: ±10mA Typ**
- **Power-off source impedance: 300Ω Min**
- **Simple slew rate control with external capacitor**
- **Flexible operating supply range**
- **Inputs are DTL/TTL compatible**

APPLICATIONS

- **Computer port driver**
- **Digital transmission over long lines**
- **Slew rate control**
- **TTL/DTL to MOS translation**

PIN CONFIGURATION

D,F,N PACKAGE


V_{EE} 1
INPUT 1 2
OUTPUT 1 3
INPUT 2A 4
INPUT 2B 5
OUTPUT 2 6
GND 7
14 V_{CC}
13 INPUT 4B
12 INPUT 4A
11 OUTPUT 4
10 INPUT 3B
9 INPUT 3A
8 OUTPUT 3

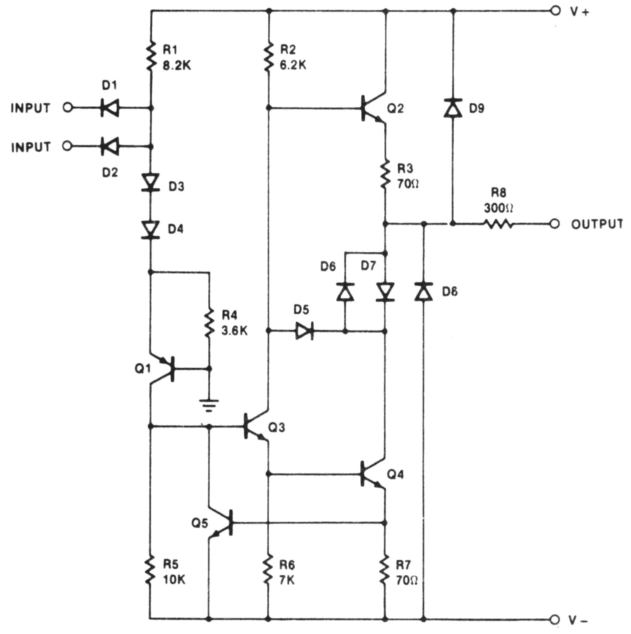
TOP VIEW

ORDER NUMBERS
MC1488D MC1488F, MC1488N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage V+	+15	V
V-	-15	V
Input voltage (V_{IN})	$-15 \le V_{IN} \le 7.0$	V
Output voltage	±15	V
Power dissipation:		
F package	1000	mW
N package	800	mW
Operating temperature range	0 to +75	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 10sec)	300	°C

CIRCUIT SCHEMATIC


V+
R1 8.2K
R2 6.2K
D1
INPUT
INPUT
D2
D3
D4
Q2
D9
R3 70Ω
R8 300Ω
OUTPUT
D6
D7
D8
D5
R4 3.6K
Q1
Q3
Q4
Q5
R5 10K
R6 7K
R7 70Ω
V-

1/4 CIRCUIT

QUAD LINE DRIVER

MC1488

DC ELECTRICAL CHARACTERISTICS

V+ = +9.0V ± 1%, V- = -9.0V ± 1%, T_A = 0°C to +75°C
unless otherwise specified.
All typicals are for V+ = 9.0V, V- = -9.0V, and T_A = 25°C.*

PARAMETER	TEST CONDITIONS		LIMITS			UNIT
			Min	Typ	Max	
Logic "0" input current	V_{IN} = 0V			-1.0	-1.6	mA
Logic "1" input current	V_{IN} = +5.0V			.005	10.0	µA
High level output voltage	R_L = 3.0kΩ V_{IN} = 0.8V	V+ = 9.0V V- = -9.0V	6.0	7.0		V
		V+ = 13.2V V- = -13.2V	9.0	10.5		V
Low level output voltage	R_L = 3.0kΩ V_{IN} = 1.9V	V+ = 9.0V V- = -9.0V	-6.0	-6.8		V
		V+ = 13.2V V- = -13.2V	-9.0	-10.5		V
High level output Short-circuit current	V_{OUT} = 0V V_{IN} = 0.8V		-6.0	-10.0	-12.0	mA
Low level output Short-circuit current	V_{OUT} = 0V V_{IN} = 1.9V		5.0	10.0	12.0	mA
Output resistance	V+ = V- = 0V V_{OUT} = ±2V		300			Ω
Positive supply current (output open)	V_{IN} = 1.9V	V+ = 9.0V, V- = -9.0V		15.0	20.0	mA
		V+ = 12V, V- = -12V		19.0	25.0	mA
		V+ = 15V, V- = -15V		25.0	34.0	mA
	V_{IN} = 0.8V	V+ = 9.0V, V- = -9.0V		4.5	6.0	mA
		V+ = 12V, V- = -12V		5.5	7.0	mA
		V+ = 15V, V- = -15V		8.0	12.0	mA
Negative supply current (output open)	V_{IN} = 1.9V	V+ = 9.0V, V- = -9.0V		-13.0	-17.0	mA
		V+ = 12V, V- = -12V		-18.0	-23.0	mA
		V+ = 15V, V- = -15V		-25.0	-34.0	mA
	V_{IN} = 0.8V	V+ = 9.0V, V- = -9.0V		-1	-15	µA
		V+ = 12V, V- = -12V		-1	-15	µA
		V+ = 15V, V- = -15V		-.01	-2.5	mA
Power dissipation	V+ = 9.0V, V- = -9.0V			252	333	mW
	V+ = 12V, V- = -12V			444	576	mW
Propagation delay to "1" (t_{pd1})	R_L = 3.0kΩ, C_L = 15pF, T_A = 25°C			275	560	ns
Propagation delay to "0" (t_{pd0})	R_L = 3.0kΩ, C_L = 15pF, T_A = 25°C			70	175	ns
Rise time (t_r)	R_L = 3.0kΩ, C_L = 15pF, T_A = 25°C			75	100	ns
Fall time (t_f)	R_L = 3.0kΩ, C_L = 15pF, T_A = 25°C			40	75	ns

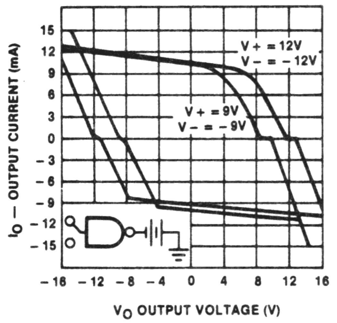
NOTE

*Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.

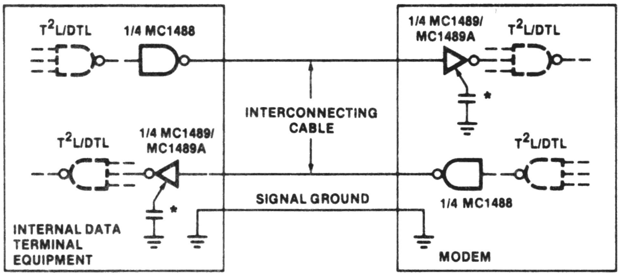
QUAD LINE DRIVER MC1488

TYPICAL PERFORMANCE CHARACTERISTICS

OUTPUT VOLTAGE AND CURRENT-LIMITING CHARACTERISTICS



RS232C DATA TRANSMISSION

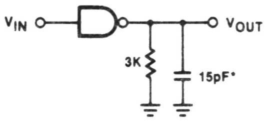


T^2L/DTL
1/4 MC1488
1/4 MC1489/ MC1489A
T^2L/DTL
INTERCONNECTING CABLE
T^2L/DTL
1/4 MC1489/ MC1489A
T^2L/DTL
SIGNAL GROUND
1/4 MC1488
INTERNAL DATA TERMINAL EQUIPMENT
MODEM
*
*

NOTE

*Optional for noise filtering

AC LOAD CIRCUIT

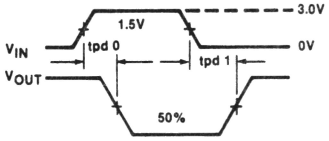


V_{IN}
V_{OUT}
3K
15pF*

NOTE

*C_L includes probe and jig capacitance.

SWITCHING WAVEFORMS



3.0V
1.5V
0V
V_{IN}
tpd 0
tpd 1
V_{OUT}
50%

NOTE

t_r and t_f are measured between 10% and 90% of the output waveform

APPLICATIONS

By connecting a capacitor to each driver output the slew rate can be controlled utilizing the output current limiting characteristics of the MC1488. For a set slew rate the appropriate capacitor value may be calculated using the following relationship

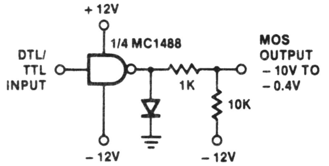
$$C = I_{SC}\ (\Delta T/\Delta V)$$

where C is the required capacitor, I_{SC} is the short circuit current value, and $\Delta V/\Delta T$ is the slew rate.

RS232C specifies that the output slew rate must not exceed 30V per microsecond. Using the worst case output short circuit current of 12mA in the above equation, calculations result in a required capacitor of 400pF connected to each output.

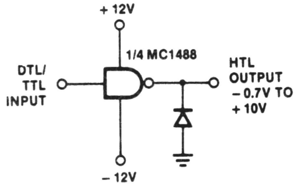
TYPICAL APPLICATIONS

DTL/TTL-TO-MOS TRANSLATOR



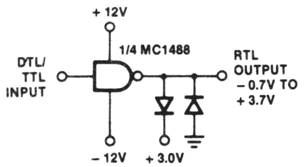
+12V
1/4 MC1488
DTL/ TTL INPUT
MOS OUTPUT −10V TO −0.4V
1K
10K
−12V
−12V

DTL/TTL-TO-HTL TRANSLATOR



+12V
1/4 MC1488
DTL/ TTL INPUT
HTL OUTPUT −0.7V TO +10V
−12V

DTL/TTL-TO-RTL TRANSLATOR



+12V
1/4 MC1488
DTL/ TTL INPUT
RTL OUTPUT −0.7V TO +3.7V
−12V
+3.0V

QUAD LINE RECEIVERS

MC1489/MC1489A

DESCRIPTION

The MC1489/MC1489A are quad line receivers designed to interface data terminal equipment with data communications equipment. They are constructed on a single monolithic silicon chip. These devices satisfy the specifications of EIA standard No. RS232C.

FEATURES

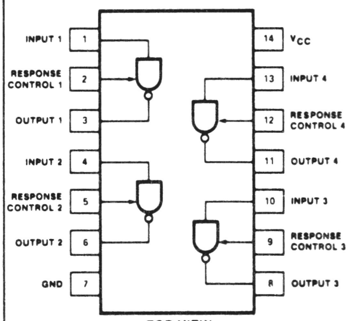
- **Four totally separate receivers per package**
- **Programmable threshold**
- **Built-in input threshold hysteresis**
- **"Fail safe" operating mode**
- **Inputs withstand ±30V**

APPLICATIONS

- **Computer port inputs**
- **Modems**
- **Eliminating noise in digital circuitry**
- **MOS to TTL/DTL translation**

PIN CONFIGURATION

D, F, N PACKAGE

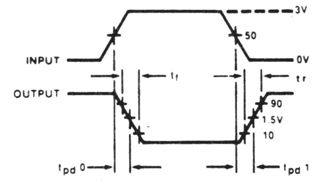

INPUT 1
1
RESPONSE CONTROL 1
2
OUTPUT 1
3
INPUT 2
4
RESPONSE CONTROL 2
5
OUTPUT 2
6
GND
7
14
Vcc
13
INPUT 4
12
RESPONSE CONTROL 4
11
OUTPUT 4
10
INPUT 3
9
RESPONSE CONTROL 3
8
OUTPUT 3

TOP VIEW
ORDER NUMBERS
MC1489D, MC1489AD
MC1489F, MC1489AF, MC1489N, MC1489AN

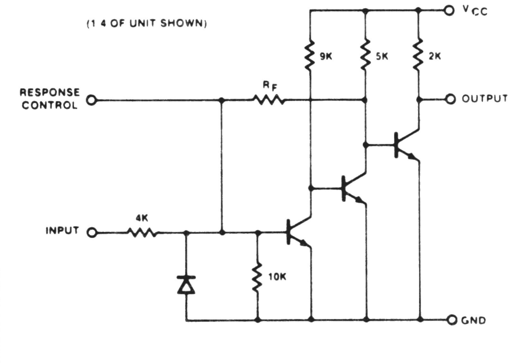
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Power supply voltage	10	V
Input voltage range	±30	V
Output load current	20	mA
Power dissipation		
F package	1	W
N package	800	mW
Operating temperature range	0 to +75	°C
Storage temperature range	-65 to +150	°C

VOLTAGE WAVEFORMS

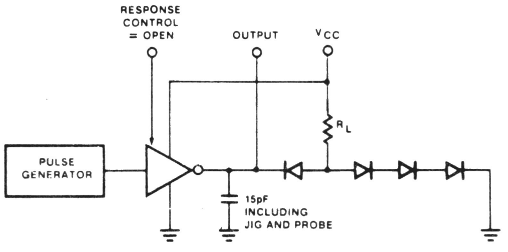

3V
50
INPUT
0V
tf
tr
OUTPUT
90
1.5V
10
tpd 0
tpd 1

EQUIVALENT SCHEMATIC


(1/4 OF UNIT SHOWN)
VCC
9K
5K
2K
RESPONSE CONTROL
RF
OUTPUT
4K
INPUT
10K
GND

MC1489: RF = 10k
MC1489A: RF = 2k

AC TEST CIRCUIT


RESPONSE CONTROL = OPEN
OUTPUT
VCC
RL
PULSE GENERATOR
15pF INCLUDING JIG AND PROBE

QUAD LINE RECEIVERS MC1489/MC1489A

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ± 1%, 0°C ≤ T_A ≤ +75°C unless otherwise specified.[1,2]

PARAMETER	TEST CONDITIONS	MC1489			MC1489A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input high threshold voltage	T_A = 25°C, V_{OUT} ≤ 0.45V, I_{OUT} = 10mA	1.0		1.5	1.75		2.25	V
Input low threshold voltage	T_A = 25°C, V_{OUT} ≤ 2.5V, I_{OUT} = -0.5mA	0.75		1.25	0.75		1.25	V
	V_{IN} = +25V V_{IN} = -25V	+3.6 -3.6	+5.6 -5.6	+8.3 -8.3	+3.6 -3.6	+5.6 -5.6	+8.3 -8.3	mA
Input current	V_{IN} = +3V V_{IN} = -3V	+0.43 -0.43	+0.53 -0.53		+0.43 -0.43	+0.53 -0.53		mA
Output high voltage	V_{IN} = 0.75V, I_{OUT} = -0.5mA	2.6	3.8	5.0	2.6	3.8	5.0	V
	Input = Open, I_{OUT} = -0.5mA	2.6	3.8	5.0	2.6	3.8	5.0	V
Output low voltage	V_{IN} = 3.0V, I_{OUT} = 10mA		0.33	0.45		0.33	0.45	V
Output short circuit current	V_{IN} = 0.75V		3.0			3.0		mA
Supply current	V_{IN} = 5.0V		20	26		20	26	mA
Power dissipation	V_{IN} = 5.0V		100	130		100	130	mW

NOTES

1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. These specifications apply for response control pin = open.

AC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ± 1%, T_A = 25°C unless otherwise specified.[1,2]

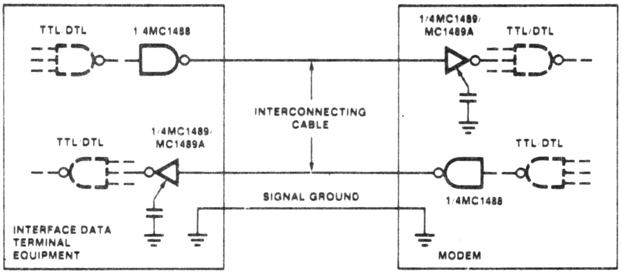
PARAMETER	TEST CONDITIONS	MC1489			MC1489A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input to output "high" Propagation delay (t_{pd1})	R_L = 3.9kΩ (AC test circuit)		25	85		25	85	ns
Input to output "low" Propagation delay (t_{pd0})	R_L = 390Ω (AC test circuit)		20	50		20	50	ns
Output rise time	R_L = 3.9kΩ (AC test circuit)		110	175		110	175	ns
Output fall time	R_L = 390Ω (AC test circuit)		9	20		9	20	ns

NOTES

1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. These specifications apply for response control pin = open.

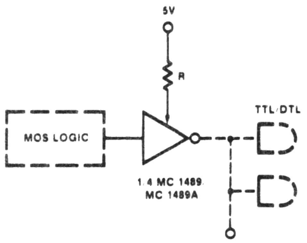
TYPICAL APPLICATIONS

RS232C DATA TRANSMISSION


TTL/DTL
1/4MC1488
1/4MC1489/ MC1489A
TTL/DTL
INTERCONNECTING CABLE
TTL/DTL
1/4MC1489/ MC1489A
TTL/DTL
SIGNAL GROUND
1/4MC1488
INTERFACE DATA TERMINAL EQUIPMENT
MODEM

*Optional for noise filtering

MOS TO TTL/DTL TRANSLATOR


5V
R
MOS LOGIC
TTL/DTL
1/4 MC 1489 MC 1489A

ADDRESSABLE RELAY DRIVER NE5090

DESCRIPTION

The NE5090 addressable relay driver is a high current latched driver, similar in function to the 9934 address decoder. The device has 8 open collector Darlington power outputs, each capable of 150mA load current. The outputs are turned on or off by respectively loading a logic "1" or logic "0" into the device data input. The required output is defined by a 3 bit address. The device must be enabled by a $\overline{CE}$ input line which also serves the function of further address decoding. A common clear input, $\overline{CLR}$, turns all outputs off when a logic "0" is applied. The device is packaged in a 16 pin plastic or CERDIP package.

FEATURES

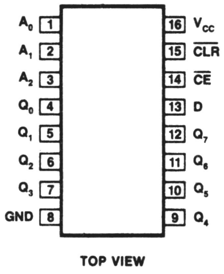
- **8 high current outputs**
- **Low-loading bus compatible inputs**
- **Power-on clear ensures safe operation**
- **Will operate in addressable or demultiplex mode**
- **Allows random (addressed) data entry**
- **Easily expandable**
- **Pin compatible with 9334**

APPLICATIONS

- **Relay driver**
- **Indicator lamp driver**
- **Triac trigger**
- **LED display digit driver**
- **Stepper motor driver**

PIN CONFIGURATION

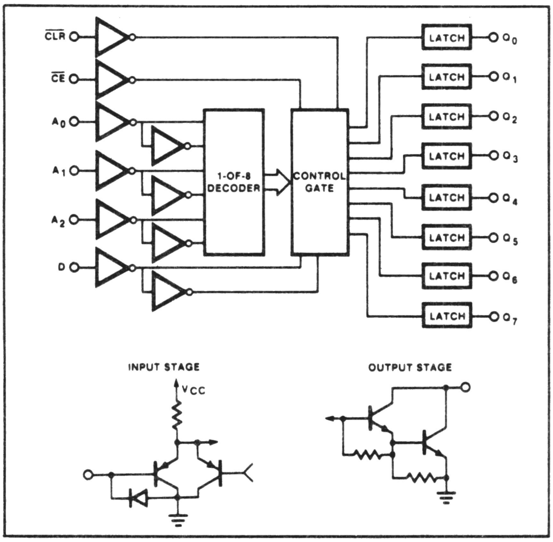
D[1],F,N PACKAGE



ORDER NUMBERS
NE5090N
NE5090F
NE5090D[1]

NOTES:
1. SOL - Released in Large SO package only.
2. SOL and non-standard pinout.
3. SO and non-standard pinouts.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

$T_A = 25°C$ unless otherwise specified.

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	− 0.5 to + 7	V
V_{IN}	Input voltage	− 0.5 to + 15	V
V_{OUT}	Output voltage	0 to + 30	V
I_{GND}	Ground current	500	mA
I_{OUT}	Output current Each output	200	mA
P_D	Power dissipation[1]	1	W
Ambient temperature range			°C
T_A	NE5090	0 to + 70	
T_J	Junction	150	
T_{STG}	Storage	− 65 to + 150	
T_{sold}	Lead soldering temperature (10 sec max)	300	°C

ADDRESSABLE RELAY DRIVER NE5090

PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION
1-3	A0-A2	A 3-bit binary address on these pins defines which of the 8 output latches is to receive the data.
4-7, 9-12	Q0-Q7	The 8 device outputs.
13	D	The data input. When the chip is enabled, this data bit is transferred to the defined output such that: "1" turns output switch "ON" "0" turns output switch "OFF"
14	CE	The chip enable. When this input is low, the output latches will accept data. When CE goes high, all outputs will retain their existing state, regardless of address of data input conditions.
15	CLR	The clear input. When CLR goes low all output switches are turned "OFF". The high data input will override the clear function on the addressed latch.

TRUTH TABLE

INPUTS						OUTPUTS								MODE
$\overline{CLR}$	$\overline{CE}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
L	H	X	X	X	X	H	H	H	H	H	H	H	H	Clear
L	L	L	L	L	L	H	H	H	H	H	H	H	H	Demultiplex
L	L	H	L	L	L	L	H	H	H	H	H	H	H	
L	L	L	H	L	L	H	H	H	H	H	H	H	H	
L	L	H	H	L	L	H	L	H	H	H	H	H	H	
L	L	L	H	H	H	H	H	H	H	H	H	H	H	
L	L	H	H	H	H	H	H	H	H	H	H	H	L	
H	H	X	X	X	X	Q_{N-1} →								Memory
H	L	L	L	L	L	H	Q_{N-1} →							Addressable Latch
H	L	H	L	L	L	L	Q_{N-1} →							
H	L	L	H	L	L	Q_{N-1}	H	Q_{N-1} →						
H	L	H	H	L	L	Q_{N-1}	L	Q_{N-1}						
H	L	L	H	H	H	Q_{N-1} →							H	
H	L	H	H	H	H	Q_{N-1} →							L	

X = Don't care condition
Q_{N-1} = Previous output state
L = Low voltage level/"ON" output state
H = High voltage level/"OFF" output state

DC ELECTRICAL CHARACTERISTICS V_{CC} = 4.75V to 5.25V, 0°C ≤ T_A ≤ 70°C unless otherwise specified (NE5090)[2].

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IH}	High		2.0			
V_{IL}	Low				0.8	
	Output voltage					V
V_{OL}	Low	I_{OL} = 150mA, T_A = 25°C		1.05	1.30	
		Over temperature			1.50	
	Input current					µA
I_{IH}	High	$V_{IN} = V_{CC}$		< 1.0	10	
I_{IL}	Low	V_{IN} = 0V		– 3.0	– 250	
I_{OH}	Leakage current	V_{OUT} = 28V,		5	250	µA
	Supply current					mA
I_{CCL}	All outputs low	V_{CC} = 5.25V NE5090		35	60	
I_{CCH}	All outputs high			22	50	

NOTES

1. Derate power dissipation as indicated above threshold ambient temperature
   NE5090 N at 9.3mW/°C above 85°C
   NE5090 F at 7.5mW/°C above 65°C
2. All typical values are at V_{CC} = 5V and T_A = 25°C

SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$, $V_{OUT} = 5V$, $I_{OUT} = 100mA$, $V_{IL} = 0.8V$, $V_{IH} = 2.0V$

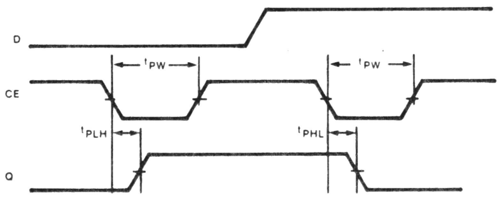
PARAMETER		TO	FROM	Min	Typ	Max	UNIT
 t_{PLH} t_{PHL}	Propagation delay time Low to high[1] High to low[1]	Output	$\overline{CE}$		 900 130	 1800 260	ns
t_{PLH} t_{PHL}	Low to high[2] High to low[2]	Output	Data		920 130	1850 260	ns
t_{PLH} t_{PHL}	Low to high[3] High to low[3]	Output	Address		900 130	1800 260	ns
t_{PLH} t_{PHL}	Low to high[4] High to low[4]	Output	$\overline{CLR}$		920	1850	ns
SWITCHING SETUP REQUIREMENTS							
$t_{s(H)}$[5] $t_{s(L)}$[5]		Chip enable Chip enable	High data Low data	5 10	20 30		ns
$t_{s(A)}$[6]		Chip enable	Address	0	20		ns
$t_{h(H)}$[5] $t_{H(L)}$[5]		Chip enable Chip enable	High data Low data	+ 10 + 10	0 0		ns
$t_{pw(E)}$[1]	Chip enable pulse width[1]			0	20		ns

NOTES

1. See Turn-On and Turn-Off Delays, Enable to Output and Enable Pulse Width timing diagram.
2. See Turn-On and Turn-Off Delays, Data to Output timing diagram.
3. See Turn-On and Turn-Off Delays, Address to Output timing diagram.
4. See Turn-Off Delay, Clear to Output timing diagram.
5. See Setup and Hold Time, Data to Enable timing diagram.
6. See Setup Time, Address to Enable timing diagram.

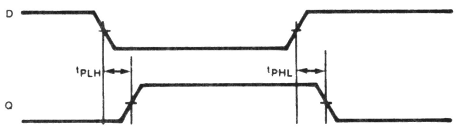
TIMING DIAGRAMS

TURN-ON AND TURN-OFF DELAYS, ENABLE TO OUTPUT AND ENABLE PULSE WIDTH



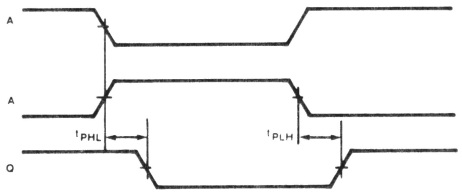
Other Inputs: $\overline{CLR}$ = H, A = Stable.

TURN-ON AND TURN-OFF DELAYS, DATA TO OUTPUT



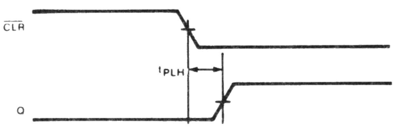
Other Inputs: $\overline{CE}$ = L, $\overline{CLR}$ = H, A = Stable

TURN-ON AND TURN-OFF DELAYS, ADDRESS TO OUTPUT



Other Inputs: $\overline{CE}$ = L, $\overline{CLR}$ = L, D = H

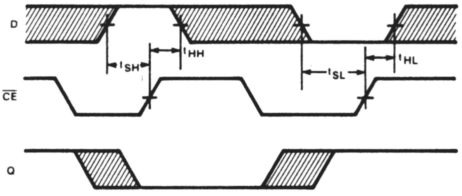
TURN-OFF DELAY, CLEAR TO OUTPUT



Other Inputs: $\overline{CE}$ = H.

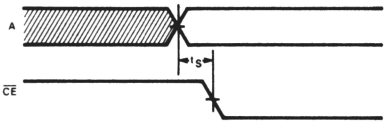
TIMING DIAGRAMS (Cont'd)

SETUP AND HOLD TIME, DATA TO ENABLE


D
t_{SH}
t_{HH}
t_{SL}
t_{HL}
$\overline{CE}$
Q

Other Inputs: $\overline{CLR}$ = H. A = Stable.

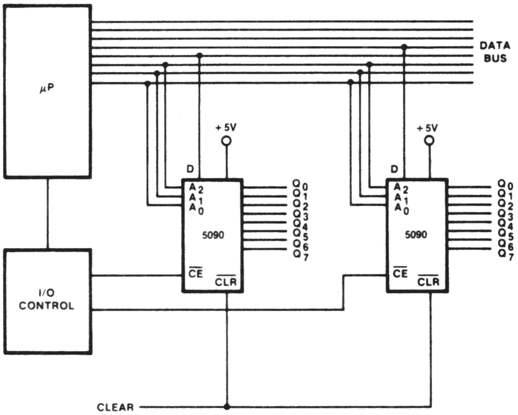
SETUP TIME, ADDRESS TO ENABLE


A
t_S
$\overline{CE}$

Other Inputs: $\overline{CLR}$ = H.

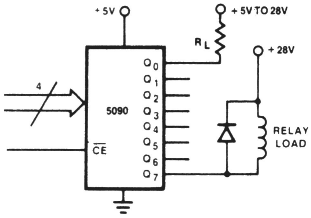
TYPICAL APPLICATIONS

INTERFACING WITH A MICROPROCESSOR SYSTEM

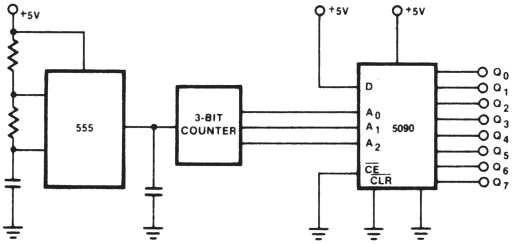

μP
DATA BUS
I/O CONTROL
+5V
D
A_2
A_1
A_0
5090
$\overline{CE}$
$\overline{CLR}$
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
CLEAR

A_0, A_1, A_2, may be connected to the address bus if permitted by system design.

DRIVING SIMPLE LOADS

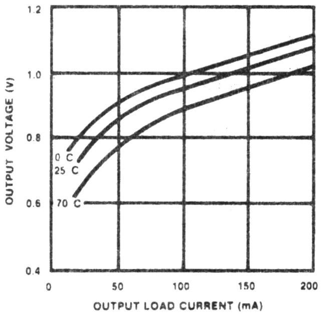

+5V
+5V TO 28V
R_L
+28V
4
5090
$\overline{CE}$
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
RELAY LOAD

OPERATING IN DEMULTIPLEX MODE


+5V
555
3-BIT COUNTER
+5V
+5V
D
A_0
A_1
A_2
5090
$\overline{CE}$
$\overline{CLR}$
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7

TYPICAL PERFORMANCE CHARACTERISTICS

OUTPUT VOLTAGE VS LOAD CURRENT



LED DECODER/DRIVER NE587

DESCRIPTION

The NE587 is a latch/decoder/driver for 7-segment common anode LED displays. The NE587 has a programmable current output up to 50mA which is essentially independent of output voltage, power supply voltage, and temperature. The data (BCD) inputs and $\overline{LE}$ (latch enable) input are low-loading so that they are compatible with any data bus system. The 7-segment decoding is implemented with a ROM so that alternative fonts can be made available.

FEATURES

- **Latched BCD inputs**
- **Low loading bus-compatible inputs**
- **Ripple-blanking on leading and/or trailing edge zeros**

APPLICATIONS

- **Digital panel meters**
- **Measuring instruments**
- **Test equipment**
- **Digital clocks**
- **Digital bus monitoring**

ABSOLUTE MAXIMUM RATINGS

$T_A = 25°C$ unless otherwise specified

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7	V
V_{IN}	Input voltage (D_0 - D_3, $\overline{LE}$, $\overline{RBI}$)	−0.5 to +15	V
V_{OUT}	Output voltage (a-g, RBO)	−0.5 to +7	V
P_D	Power dissipation (25°C)[1]	1000	mW
T_A	Ambient temperature range	0 to 70	°C
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Soldering temperature (10 sec. max)	300	°C

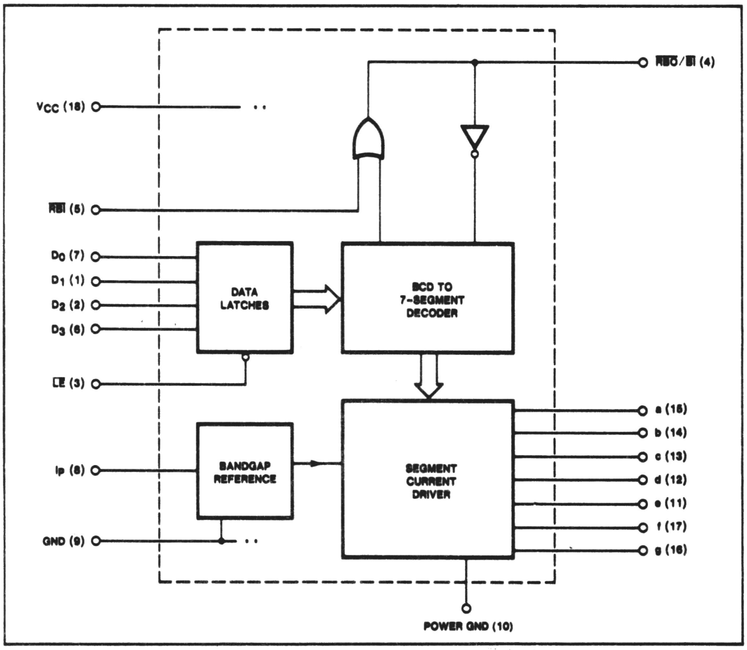
NOTE

Derate power dissipation as indicated

N package - 95°C/watt above 55°C

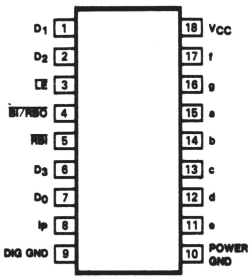
F package - 100°C/watt above 50°C

BLOCK DIAGRAM


$\overline{RBO}$/$\overline{BI}$ (4)
V_{CC} (18)
$\overline{RBI}$ (5)
D_0 (7)
D_1 (1)
D_2 (2)
D_3 (6)
DATA LATCHES
BCD TO 7-SEGMENT DECODER
$\overline{LE}$ (3)
I_P (8)
BANDGAP REFERENCE
SEGMENT CURRENT DRIVER
GND (9)
a (15)
b (14)
c (13)
d (12)
e (11)
f (17)
g (16)
POWER GND (10)

PIN CONFIGURATIONS

F,N PACKAGE

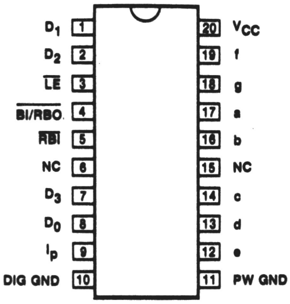

D_1 1
D_2 2
$\overline{LE}$ 3
$\overline{BI}/\overline{RBO}$ 4
$\overline{RBI}$ 5
D_3 6
D_0 7
I_P 8
DIG GND 9
18 V_{CC}
17 f
16 g
15 a
14 b
13 c
12 d
11 e
10 POWER GND

TOP VIEW

ORDER NUMBERS

NE587F NE587N

D^2 PACKAGE


D_1 1
D_2 2
$\overline{LE}$ 3
$\overline{BI/RBO}$ 4
$\overline{RBI}$ 5
NC 6
D_3 7
D_0 8
I_P 9
DIG GND 10
20 V_{CC}
19 f
18 g
17 a
16 b
15 NC
14 c
13 d
12 e
11 PW GND

TOP VIEW

NE587D^2

NOTES:

1. SOL - Released in Large SO package only.
2. SOL and non-standard pinout.
3. SO and non-standard pinouts.

LED DECODER/DRIVER

NE587

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.75 to 5.25V, 0°C < T_A < 70°C.
Typical values are at V_{CC} = 5V, T_A = 25°C, R_P = 1kΩ (± 1%) unless otherwise stated.

PARAMETER		TEST CONDITIONS	NE587			UNIT
			Min	**Typ**	**Max**	
V_{CC}	Operating supply voltage		4.75	5.00	5.25	V
V_{IH}	Input high voltage	All inputs except $\overline{BI}$ $\overline{BI}$	2.0 2.0		15 5.5	V
V_{IL}	Input low voltage				0.8	V
V_{IC}	Input clamp voltage	I_{IN} = −12mA, T_A = 25°C			−1.5	V
I_{IH}	Input high current	Inputs D_0 −D_3, $\overline{LE}$, $\overline{RBI}$ V_{IN} = 2.4V V_{IN} = 15V Input $\overline{BI}$ (pin 4) $\overline{RBI}$ = H V_{IN} = V_{CC} = 5.25V	 1.0 15 10		 10 15 100	μA μA
I_{IL}	Input low current	V_{IN} = 0.4V, Inputs D_0 − D_3 $\overline{LE}$, $\overline{RBI}$		−5 −200		μA
		Input $\overline{BI}$ V_{CC} = 5.25V $\overline{RBI}$ = H, V_{IN} = 0.4V		−0.7		mA
V_{OL}	Output low voltage	Output $\overline{RBO}$ I_{out} = 3.0mA		.2	.5	V
V_{OH}	Output high voltage	Output $\overline{RBO}$ I_{OUT} = −50μA $\overline{RBI}$ = H	3.5	4.5		V
I_{OUT}	Output segment "ON" current	Outputs "a" thru "g" V_{OUT} = 2.0V	20	25	30	mA
ΔI_{OUT}	Output current ratio (all outputs ON)	With reference to "b" segment V_{OUT} = 2.0V	0.90	1.00	1.10	
I_{OFF}	Output segment "OFF" current	Outputs "a" thru "g" V_{OUT} = 5.0V		20	250	μA
I_{CCO}	Supply current	V_{CC} = 5.25V All outputs "ON" V_{OUT} > 1V		33	55	mA
I_{CCI}	Supply current	V_{CC} = 5.25V All outputs blanked		50	70	mA

NOTE

NE587 PROGRAMMING

The NE587 output current can be programmed, provided a program resistor, Rp, be connected between Ip (pin 8) and Ground (pin 9). The voltage at Ip (pin 8) is constant (≈ 1.3V). Thus, a current through Rp is $I_P \approx \frac{1.3V}{R_P}$, as shown in Figure 5. $\frac{I_O}{I_P}$ is 20 in the 15 to 50mA output current range.

LED DECODER/DRIVER NE587

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 5V$ $T_A = 25°C$. $R_L = 130\Omega$, $C_L = 30pF$ including probe capacity.

PARAMETER		TEST CONDITIONS	NE587			UNIT
			Min	Typ	Max	
$t_{D_{av.}}$	Propagation delay Figure 2	From data to output		135		ns
$t_{D_{av.}}$	Propagation delay Figure 3	From $\overline{\text{LE}}$ to output		135		ns
t_W	Latch enable pulse width Figure 4		30			ns
t_S	Latch enable setup time Figure 4	From data to $\overline{\text{LE}}$	20			ns
t_H	Latch enable hold time Figure 4	From $\overline{\text{LE}}$ to data	0			ns

NOTE

$t_{D_{av.}} = ½ (t_{HL} + t_{LH})$

TRUTH TABLE

BINARY INPUT	INPUTS						OUTPUTS								DISPLAY
	$\overline{\text{LE}}$	$\overline{\text{RBI}}$	D_3	D_2	D_1	D_0	a	b	c	d	e	f	g	$\overline{\text{RBO}}$	
–	H	•	X	X	X	X	STABLE							••	STABLE
0	L	L	L	L	L	L	H	H	H	H	H	H	H	L	BLANK
0	L	H	L	L	L	L	L	L	L	L	L	L	H	H	0
1	L	X	L	L	L	H	H	L	L	H	H	H	H	H	1
2	L	X	L	L	H	L	L	L	H	L	L	H	L	H	2
3	L	X	L	L	H	H	L	L	L	L	H	H	L	H	3
4	L	X	L	H	L	L	H	L	L	H	H	L	L	H	4
5	L	X	L	H	L	H	L	H	L	L	H	L	L	H	5
6	L	X	L	H	H	L	L	H	L	L	L	L	L	H	6
7	L	X	L	H	H	H	L	L	L	H	H	H	H	H	7
8	L	X	H	L	L	L	L	L	L	L	L	L	L	H	8
9	L	X	H	L	L	H	L	L	L	L	H	L	L	H	9
10	L	X	H	L	H	L	H	H	H	H	H	H	L	H	-
11	L	X	H	L	H	H	L	H	H	L	L	L	L	H	E
12	L	X	H	H	L	L	H	L	L	H	L	L	L	H	H
13	L	X	H	H	L	H	H	H	H	L	L	L	H	H	L
14	L	X	H	H	H	L	L	L	H	H	L	L	L	H	P
15	L	X	H	H	H	H	H	H	H	H	H	H	H	H	blank
••BI	X	X	X	X	X	X	H	H	H	H	H	H	H	L••	blank

NOTES

H = HIGH voltage level, output is "OFF"

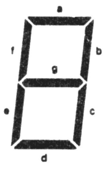
L = LOW voltage level, output is "ON"

X = Don't care

• The $\overline{\text{RBI}}$ will blank the display only if a binary zero is stored in the latches.

•• $\overline{\text{RBO}}/\overline{\text{BI}}$ used as an input overrides all other input conditions.

SEGMENT IDENTIFICATION



LED DECODER/DRIVER NE587

NE587 PROGRAMMING

NE587 output current can be programmed by using a programming resistor, R_P, connected between r_P (pin 8) and Gnd (pin 9). The voltage at r_P (pin 8) is constant ($\approx$1.40V). A partial schematic of the voltage reference used in the NE587 is shown in figure 1.

Output current to program current ratio, I_O/I_P, is 20 in the 15mA to 50mA range. Note that I_P must be derived from a resistor (R_P), and not from a high impedance source such as an I_{OUT} DAC used to control display brightness.

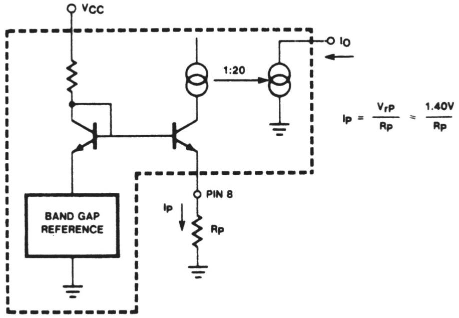


Figure 1

TIMING DIAGRAMS

PROPAGATION DELAY, DATA TO OUTPUT

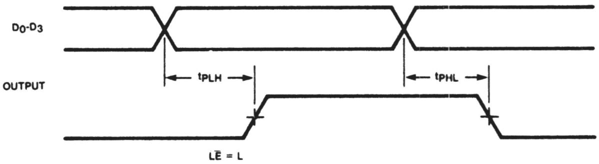


Figure 2

PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

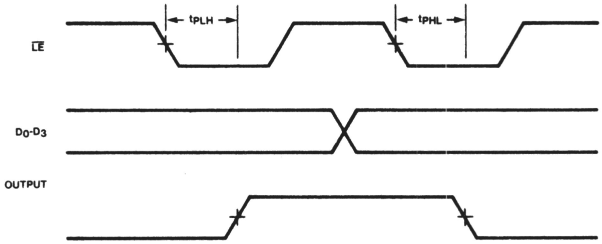


Figure 3

POWER DISSIPATION CONSIDERATIONS

LED displays are power-hungry devices, and inevitably somewhat inefficient in their use of the power supply necessary to drive them. Duty cycle control does afford one way of improving display efficiency, provided that the LEDS are not driven too far into saturation, but the improvement is marginal. Operation at higher peak currents has the added advantage of giving much better matching of light output, both from segment-to-segment and digit-to-digit.

An output current of 10 to 50mA was chosen so that it would be suitable for multiplexed operation of large size LED digits. When designing a display system, particular care must be taken to minimize power dissipation within the IC display driver. Since the output is a constant current source, all the remaining supply voltage, which is not dropped across the LED (and the digit driver, if used), will appear across the output. Thus, the power dissipation will go up sharply if the display power supply voltage rises. Clearly, then, it is good design practice to keep the display supply voltage as low as possible consistent with proper operation of the supply output current sources. Inserting a resistor or diode in series with the display supply is a good way of reducing the power dissipation within the integrated circuit segment driver, although, of course, total system power remains the same.

Power dissipation may be calculated as follows. Referring to figure 6, the two system power supplies are V_{CC} and V_S. In many cases, these will be the same voltage. Necessary parameters are:

V_{CC},	Supply voltage to driver
V_S,	Supply voltage to display
I_{CC},	Quiescent supply current of driver
I_{SEG},	LED segment current
V_F,	LED segment forward voltage at I_{seg}
K_{DC},	% Duty cycle

V_F, the forward LED drop, depends upon the type of LED material (hence the color) and the forward current. The actual forward voltage drops should be obtained from the LED display manufacturer's literature for the peak segment current selected; however, approximate voltages at nominal rated currents are:

Red	1.6 to 2.0V
Orange	2.0 to 2.5V
Yellow	2.2 to 3.5V
Green	2.5 to 3.5V

TIMING DIAGRAMS (Cont'd)

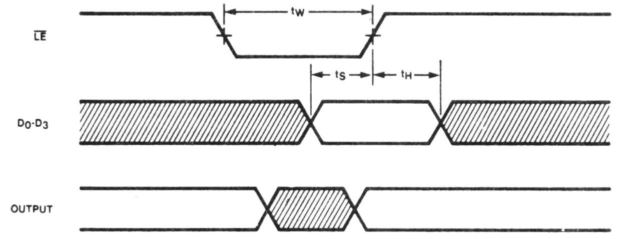


Figure 4

These voltages are all for single diode displays. Some early red displays had 2 series LEDS per segment; hence the forward voltage drop was around 3.5V.

Thus a maximum power dissipation calculation when all segments are on, is:

$P_d = V_{CC} \times I_{CC} + (V_S - V_F) \times 7 \times I_{seg} \times K_{DC}$ mW

Assuming $V_S = V_{CC} = 5.25V$

$V_F = 2.0V$

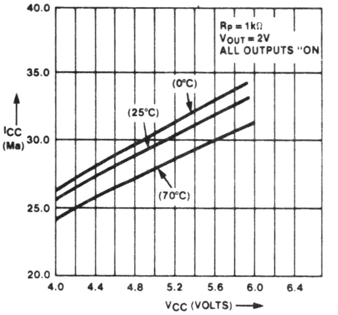
$K_{DC} = 100\%$

$P_{d\ max} = 5.25 \times 50 + 3.25 \times 7 \times 30$ mW

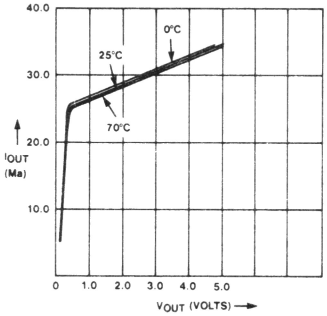
$= 945$ mW

TYPICAL PERFORMANCE CURVES

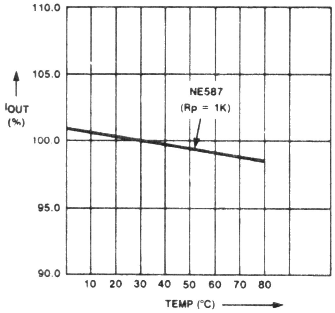
SUPPLY CURRENT VS SUPPLY VOLTAGE
NE587



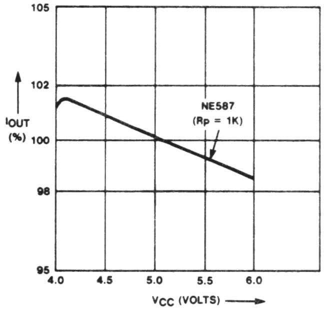
OUTPUT CURRENT VS OUTPUT VOLTAGE
NE587
Rp = 1Kohms



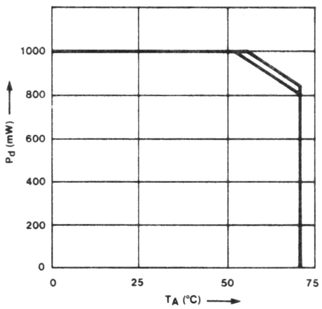
NORMALIZED OUTPUT CURRENT VS TEMPERATURE
$V_{CC} = 5.0V$



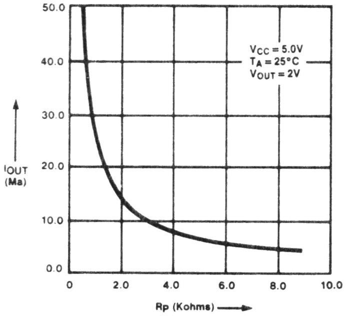
NORMALIZED OUTPUT CURRENT VS SUPPLY VOLTAGE
$V_O = 2V$
$T_A = 25°C$



MAXIMUM POWER DISSIPATION VS TEMPERATURE

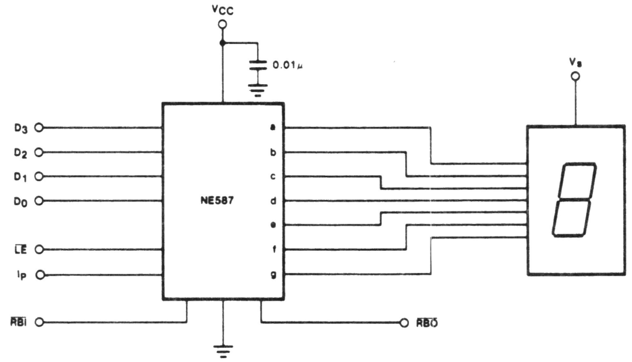


OUTPUT CURRENT VS PROGRAM RESISTOR



TYPICAL APPLICATIONS

DRIVING A SINGLE DIGIT



NOTE
Decoupling capacitor on V_{CC} should be 0.01 µF ceramic

Figure 6

However, the average power dissipation will be considerably less than this. Assuming 5 segments are on (the average for all output code combinations), then

$$P_{d\ av} = 5.0 \times 30 + 3.00 \times 5 \times 25 \text{ mW} = 525 \text{ mW}$$

Operating temperature range limitations can be deduced from the power dissipation graph. (See Typical Performance Characteristics).

However, a major portion of this power dissipation ($P_{d\ max}$) is because the current source output is operating with 3.25 V across it. In practice, the outputs operate satisfactorily down to 0.5V, and so the extra voltage may be dropped external to the integrated circuit.

Suppose the worst case V_{CC}/V_S supply is 4.75 to 5.25V, and that the maximum V_E for the LED display is 2.25V. Only 2.75V is required to keep the display active, and hence 2.0V may be dropped externally with a resistor from V_{CC} to V_S. The value of this resistor is calculated by:

$$R_S = \frac{2.0}{7 \times I_{seg}} \simeq 10\Omega \text{ (½ W rating)}$$

assuming worst case I_{seg} of 30 mA

Hence now $P_{d\ max} = V_{CC} \times I_{CC} + (V_S - V_V - R_X \times 7 \times I_{seg}) \times 7 \times X\, I_{seg} \times K_{DC}$
$= 5.25 \times 50 + 1.25 \times 7 \times 30$ mW
$= 525$ mW

and $P_{d\ av} = 5.0 \times 30 + 1.25 \times 5 \times 25$
$= 306$ mW

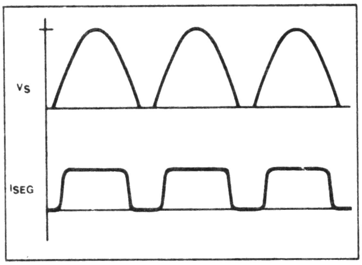
If a diode (or 2) is used to reduce voltage to the display, then the voltage appearing across the display driver will be independent of the number of "ON" segments and will be equal to

$$V_S - V_F - nV_d\,.\ V_D \simeq 0.8\text{V}$$

Where n is the number of diodes used, power dissipation can be calculated in a similiar manner.

In a multiplexed display system, the voltage drop across the digit driver must also be considered in computing device power dissipation. It may even be an advantage to use a digit driver which drops an appreciable voltage, rather than the saturating PNP transistors shown in figure 9. For example a darlington PNP or NPN emitter follower may be preferable. Figure 8 shows the NE591 as the digit driver in a multiplexed display system. The NE591 output drops about 1.8V which means that the power dissipation is evenly distributed between the two integrated circuits.

Where V_S and V_{CC} are two different supplies, the V_S supply may be optimized for minimum system power dissipation and/or cost. Clearly, good regulation in the V_S supply is totally unnecessary, and so this supply can be made much cheaper than the regulated 5V supply used in the rest of the system. In fact a simple unsmoothed full-wave rectified sine wave works extremely well if a slight loss in brightness can be tolerated. A transformer voltage of about 3-4.5V rms works well in most LED display systems. Waveforms are shown below:



The duty cycle for this system depends upon V_S, V_F and the output characteristics of the display driver.

With
$V_S = 4.9$V pk.
$V_F = 2.0$V

The duty cycle is approximately 60%.

TYPICAL APPLICATIONS (Cont'd)

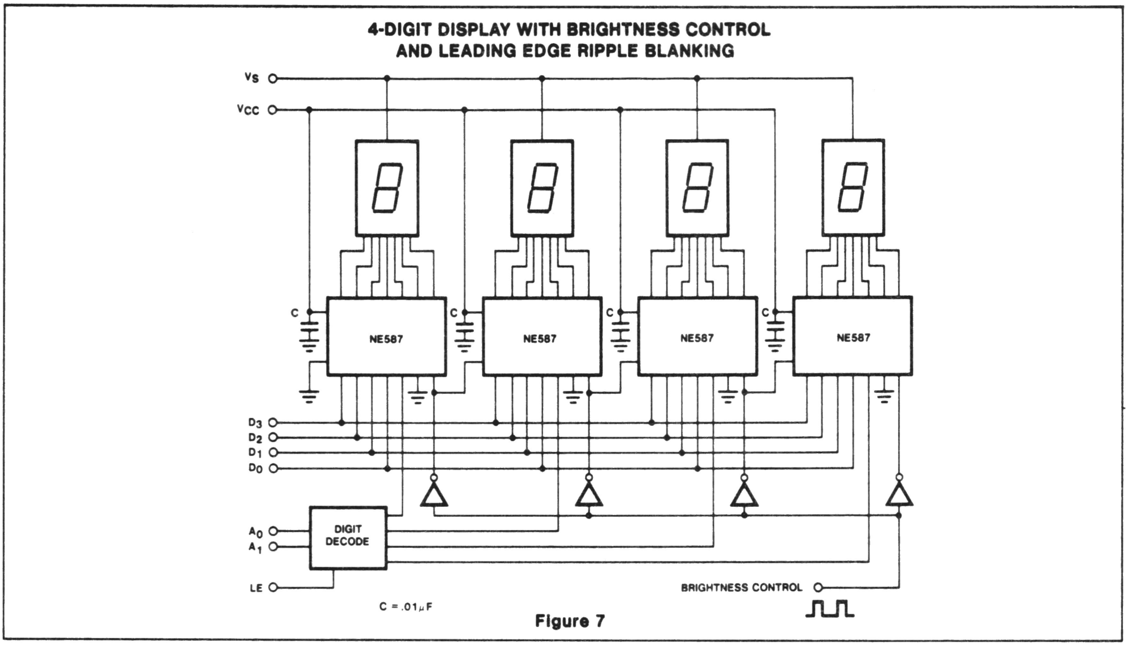

4-DIGIT DISPLAY WITH BRIGHTNESS CONTROL
AND LEADING EDGE RIPPLE BLANKING
VS
VCC
C
NE587
NE587
NE587
NE587
D3
D2
D1
D0
A0
A1
DIGIT DECODE
LE
C = .01μF
BRIGHTNESS CONTROL

Figure 7

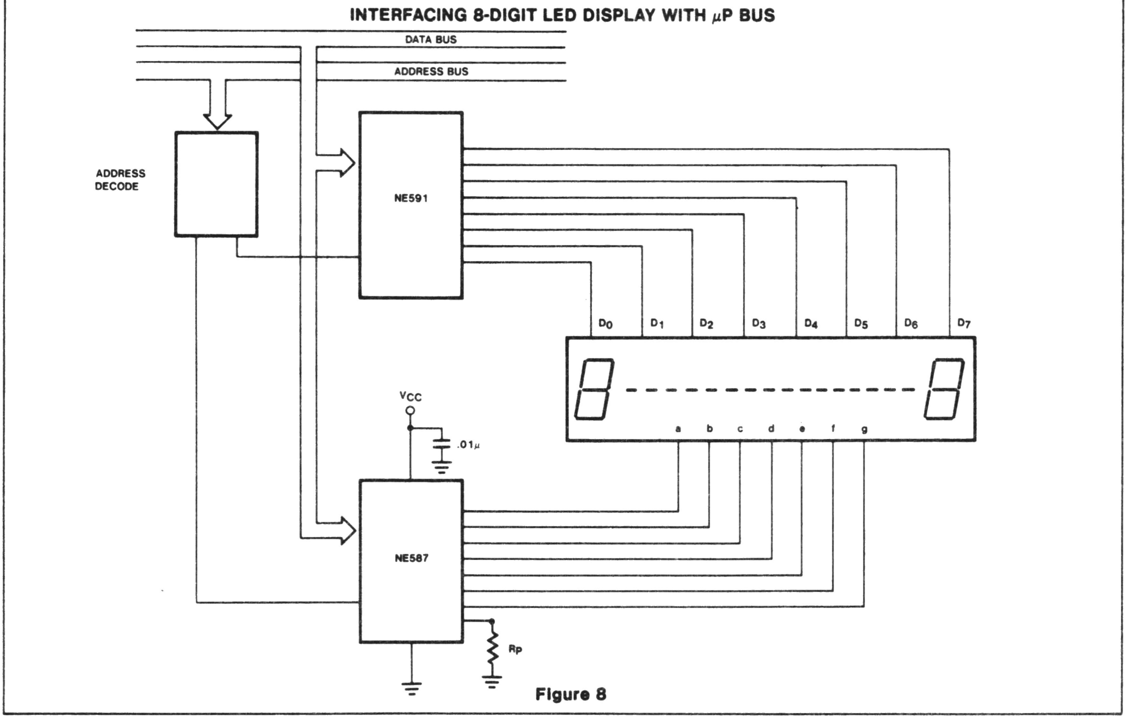
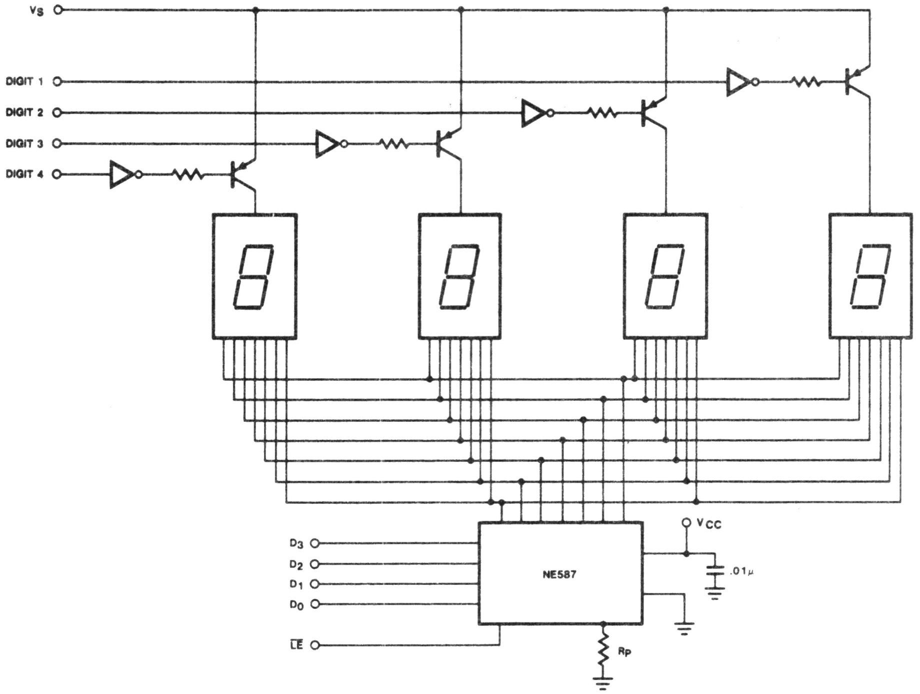

INTERFACING 8-DIGIT LED DISPLAY WITH μP BUS
DATA BUS
ADDRESS BUS
ADDRESS DECODE
NE591
D0
D1
D2
D3
D4
D5
D6
D7
a
b
c
d
e
f
g
VCC
.01μ
NE587
Rp

Figure 8

TYPICAL APPLICATIONS (Cont'd)

4-DIGIT MULTIPLEXED LED DISPLAY



V_S
DIGIT 1
DIGIT 2
DIGIT 3
DIGIT 4
D_3
D_2
D_1
D_0
$\overline{LE}$
NE587
V_{CC}
.01μ
Rp

Figure 9

For additional information, refer to the Applications Section.

LED DECODER/DRIVER NE589

DESCRIPTION

The NE589 is a latch/decoder/driver for 7-segment common cathode LED displays. The NE589 has a programmable current output up to 50mA which is essentially independent of output voltage, power supply voltage, and temperature. The data (BCD) inputs and $\overline{LE}$ (latch enable) input are low-loading so that they are compatible with any data bus system. The 7-segment decoding is implemented with a ROM so that alternative fonts can be made available.

FEATURES

- Latched BCD inputs
- Low loading bus-compatible inputs
- Ripple-blanking on leading and/or trailing edge zeros

APPLICATIONS

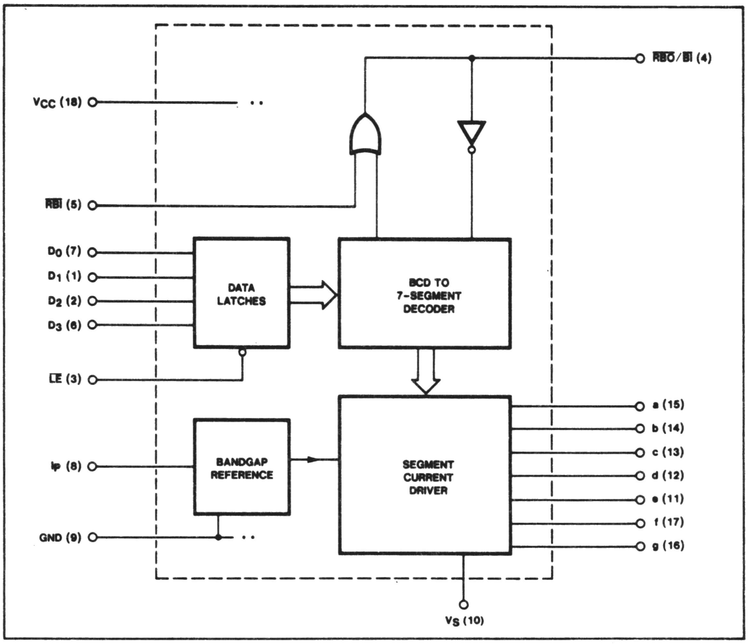
- Digital panel meters
- Measuring instruments
- Test equipment
- Digital clocks
- Digital bus monitoring

ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$ unless otherwise specified

PARAMETER		RATING	UNIT
V_{CC}, V_S	Supply voltage	−0.5 to +7	V
V_{IN}	Input voltage (D_0 - D_3, $\overline{LE}$, $\overline{RBI}$)	−0.5 to +15	V
V_{OUT}	Output voltage (a-g, RBO)	−0.5 to +7	V
P_D	Power dissipation (25°C)[1]	1000	mW
T_A	Ambient temperature range	0 to 70	°C
T_J	Junction temperature	150	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Soldering temperature (10 sec. max)	300	°C

NOTE
Derate power dissipation as indicated
N package - 95°C/watt above 55°C
F package - 100°C/watt above 50°C

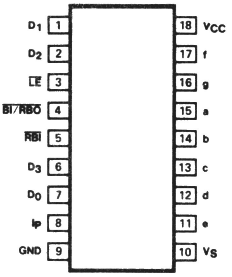
BLOCK DIAGRAM



$\overline{RBO}/\overline{BI}$ (4)
V_{CC} (18)
$\overline{RBI}$ (5)
D_0 (7)
D_1 (1)
D_2 (2)
D_3 (6)
DATA LATCHES
BCD TO 7-SEGMENT DECODER
$\overline{LE}$ (3)
I_P (8)
BANDGAP REFERENCE
SEGMENT CURRENT DRIVER
GND (9)
a (15)
b (14)
c (13)
d (12)
e (11)
f (17)
g (16)
V_S (10)

PIN CONFIGURATION

F,N PACKAGE

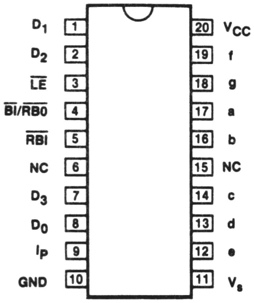


D_1 1
D_2 2
$\overline{LE}$ 3
$\overline{BI}/\overline{RBO}$ 4
$\overline{RBI}$ 5
D_3 6
D_0 7
I_P 8
GND 9
18 V_{CC}
17 f
16 g
15 a
14 b
13 c
12 d
11 e
10 V_S

TOP VIEW

ORDER NUMBERS
NE589F NE589N

D² PACKAGE



D_1 1
D_2 2
$\overline{LE}$ 3
$\overline{BI}/\overline{RBO}$ 4
$\overline{RBI}$ 5
NC 6
D_3 7
D_0 8
I_P 9
GND 10
20 V_{CC}
19 f
18 g
17 a
16 b
15 NC
14 c
13 d
12 e
11 V_s

TOP VIEW
NE589D²

NOTES:
1. SOL - Released in Large SO package only.
2. SOL and non-standard pinout.
3. SO and non-standard pinouts.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.75 to 5.25V, 0°C < T_A < 70°C. Typical values are at $V_{CC} = V_S = 5V$, $T_A = 25°C$, $R_P = 7k\Omega$ (±1%) unless otherwise stated.

PARAMETER		TEST CONDITIONS	NE589			UNIT
			Min	Typ	Max	
V_{CC}, V_S	Operating supply voltage		4.75	5.00	5.25	V
V_{IH}	Input high voltage	All Inputs except $\overline{BI}$ $\overline{BI}$	2.0 2.0		15 5.5	V
V_{IL}	Input low voltage				0.8	V
V_{IC}	Input clamp voltage	$I_{IN} = -12mA$, $T_A = 25°C$			−1.5	V
I_{IH}	Input high current	Inputs $D_0 - D_3$, $\overline{LE}$, $\overline{RBI}$ $V_{IN} = 2.4V$ $V_{IN} = 15V$		 0.1 10	 10 15	 μA μA
I_{IH}	Input high current	Input $\overline{BI}$ (pin 4) $\overline{RBI} = H$ $V_{IN} = V_{CC} = 5.25V$		10		μA
I_{IL}	Input low current	$V_{IN} = 0.4V$, Inputs $D_0 - D_3$ $\overline{LE}$, $\overline{RBI}$		−5 −200		μA
I_{IL}	Input low current	Input $\overline{BI}$ $V_{CC} = 5.25V$ $\overline{RBI} = H$, $V_{IN} = 0.4V$		−0.7		mA
V_{OL}	Output low voltage	Output $\overline{RBO}$ $I_{OUT} = 3.0mA$		0.2	0.5	V
V_{OH}	Output high voltage	Output $\overline{RBO}$ $I_{OUT} = -50\mu A$ $\overline{RBI} = H$	3.5	4.5		V
I_{OUT}	Output segment "ON" current	Outputs "a" thru "g" $V_{OUT} = 2.0V$	20	25	30	mA
ΔI_{OUT}	Output current ratio (all outputs ON)	With reference to "b" segment $V_{OUT} = 2.0V$	0.90	1.00	1.10	
I_{OFF}	Output segment "OFF" current	Outputs "a" thru "g"		20	250	μA
I_{CCO}	Supply current	$V_{CC} = 5.25V$ All outputs "ON" $V_{OUT} > 1V$		25	55	mA
I_{CCI}	Supply current	$V_{CC} = 5.25V$ All outputs blanked		30	65	mA

AC ELECTRICAL CHARACTERISTICS $V_{CC} = V_S = 5V$ $T_A = 25°C$, $R_L = 130\Omega$, $C_L = 30pF$ including probe capacity.

PARAMETER		TEST CONDITIONS	NE589			UNIT
			Min	Typ	Max	
$t_{Dav.}$	Propagation delay Figure 2	From data to output		135		ns
$t_{Dav.}$	Propagation delay Figure 3	From $\overline{LE}$ to output		135		ns
t_W	Latch enable pulse width Figure 4		85			ns
t_S	Latch enable setup time Figure 4	From data to $\overline{LE}$	75			ns
t_H	Latch enable hold time Figure 4	From $\overline{LE}$ to data	0			ns

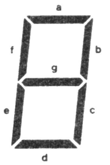
NOTE:
$t_{D_{AV.}} = \max(t_{HL} + t_{LH})$

TRUTH TABLE

BINARY INPUT	INPUTS						OUTPUTS								DISPLAY
	$\overline{LE}$	$\overline{RBI}$	D_3	D_2	D_1	D_0	a	b	c	d	e	f	g	$\overline{RBO}$	
–	H	*	X	X	X	X	STABLE								STABLE BLANK
0	L	L	L	L	L	L	L	L	L	L	L	L	L	L	
0	L	H	L	L	L	L	H	H	H	H	H	H	L	H	0
1	L	X	L	L	L	H	L	H	H	L	L	L	L	H	1
2	L	X	L	L	H	L	H	H	L	H	H	L	H	H	2
3	L	X	L	L	H	H	H	H	H	H	L	L	H	H	3
4	L	X	L	H	L	L	L	H	H	L	L	H	H	H	4
5	L	X	L	H	L	H	H	L	H	H	L	H	H	H	5
6	L	X	L	H	H	L	H	L	H	H	H	H	H	H	6
7	L	X	L	H	H	H	H	H	H	L	L	L	L	H	7
8	L	X	H	L	L	L	H	H	H	H	H	H	H	H	8
9	L	X	H	L	L	H	H	H	H	H	L	H	H	H	9
10	L	X	H	L	H	L	H	H	H	L	H	H	H	H	a
11	L	X	H	L	H	H	L	L	H	H	H	H	H	H	b
12	L	X	H	H	L	L	H	L	L	H	H	H	L	H	c
13	L	X	H	H	L	H	L	H	H	H	H	L	H	H	d
14	L	X	H	H	H	L	H	L	L	H	H	H	H	H	e
15	L	X	H	H	H	H	H	L	L	L	H	H	H	H	f
**BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L**	blank

NOTES
H = HIGH voltage level, output is "ON"
L = LOW voltage level, output is "OFF"
X = Don't care
* The $\overline{RBI}$ will blank the display only if a binary zero is stored in the latches.
** $\overline{RBO/BI}$ used as an input overrides all other input conditions.

SEGMENT IDENTIFICATION



NE589 PROGRAMMING

NE589 output current can be programmed by using a programming resistor, R_P, connected between r_P (pin 8) and Gnd (pin 9). The voltage at r_P (pin 8) is constant ($\approx$ 1.3V). A partial schematic of the voltage reference used in the NE589 is shown in figure 1.

Output current to program current ratio, I_O/I_P, is 120 in the 10mA to 50mA range. Note that I_P must be derived from a resistor (R_P), and not from a high impedance source such as an I_{OUT} DAC used to control display brightness.

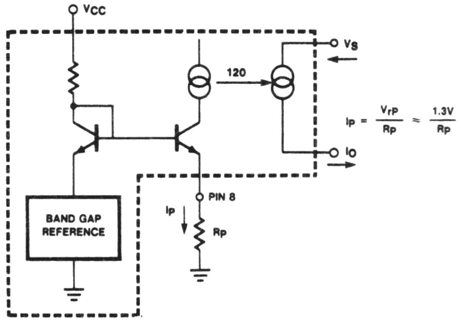


Figure 1

TIMING DIAGRAMS

PROPAGATION DELAY, DATA TO OUTPUT

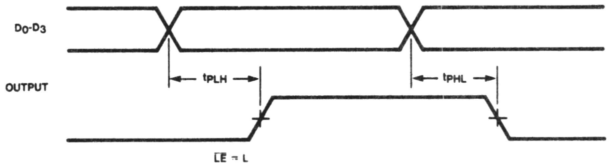


Figure 2

PROPAGATION DELAY, LATCH ENABLE TO OUTPUT

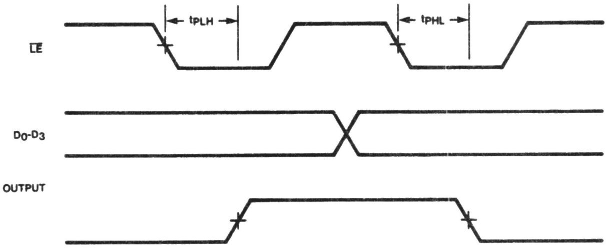


Figure 3

POWER DISSIPATION CONSIDERATIONS

LED displays are power-hungry devices, and inevitably somewhat inefficient in their use of the power supply necessary to drive them. Duty cycle control does afford one way of improving display efficiency, provided that the LEDS are not driven too far into saturation, but the improvement is marginal. Operation at higher peak currents has the added advantage of giving much better matching of light output, both from segment-to-segment and digit-to-digit.

An output current of 10 to 50mA was chosen so that it would be suitable for multiplexed operation of large size LED digits. When designing a display system, particular care must be taken to minimize power dissipation within the IC display driver. Since the output is a constant current source, all the remaining supply voltage, which is not dropped across the LED (and the digit driver, if used), will appear across the output. Thus, the power dissipation will go up sharply if the display power supply voltage rises. Clearly, then, it is good design practice to keep the display supply voltage as low as possible consistent with proper operation of the supply output current sources. Inserting a resistor or diode in series with the display supply is a good way of reducing the power dissipation within the integrated circuit segment driver, although, of course, total system power remains the same.

Power dissipation may be calculated as follows. Referring to figure 5, the two system power supplies are V_{CC} and V_S. In many cases, these will be the same voltage. Necessary parameters are:

V_{CC},	Supply voltage to driver
V_S,	Supply voltage to display
I_{CC},	Quiescent supply current of driver
I_{SEG},	LED segment current
V_F,	LED segment forward voltage at I_{seg}
K_{DC},	% Duty cycle

V_F, the forward LED drop, depends upon the type of LED material (hence the color) and the forward current. The actual forward voltage drops should be obtained from the LED display manufacturer's literature for the peak segment current selected; however, approximate voltages at nominal rated currents are:

Red	1.6 to 2.0V
Orange	2.0 to 2.5V
Yellow	2.2 to 3.5V
Green	2.5 to 3.5V

TIMING DIAGRAMS (Cont'd)

LATCH ENABLE PULSE WIDTH, SET-UP AND HOLD TIMES

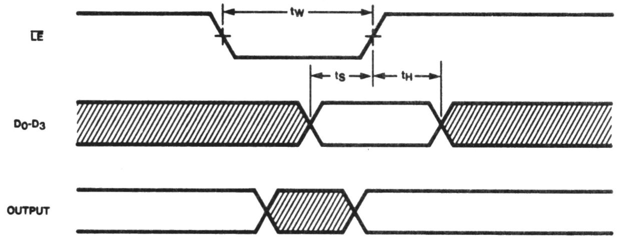


Figure 4

These voltages are all for single diode displays. Some early red displays had 2 series LEDS per segment; hence the forward voltage drop was around 3.5V.

Thus a maximum power dissipation calculation when all segments are on, is:

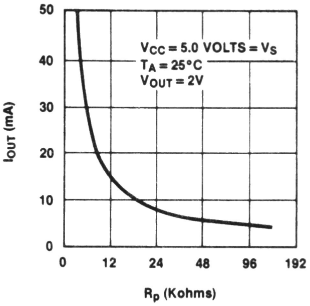
$P_d = V_{CC} \times I_{CC} + (V_S - V_F) \times 7 \times I_{seg} \times K_{DC}$ mW

Assuming $V_S = V_{CC} = 5.25V$
$V_F = 2.0V$
$K_{DC} = 100\%$

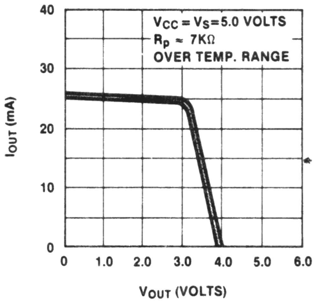
$P_{d\,max} = 5.25 \times 50 + 3.25 \times 7 \times 30$ mW
$= 945$ mW

TYPICAL PERFORMANCE CURVES

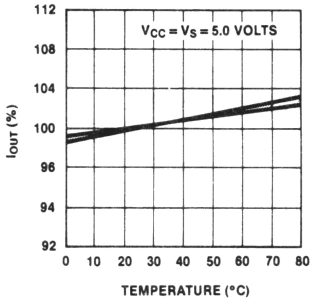
OUTPUT CURRENT VS PROGRAM RESISTOR



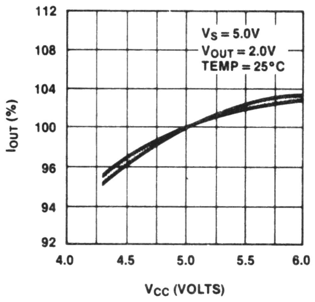
OUTPUT CURRENT VS OUTPUT VOLTAGE



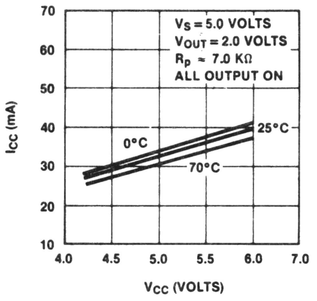
NORMALIZED OUTPUT CURRENT VS TEMPERATURE



NORMALIZED OUTPUT CURRENT VS SUPPLY VOLTAGE



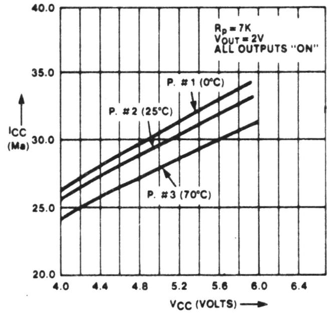
SUPPLY CURRENT VS SUPPLY VOLTAGE



LED DECODER/DRIVER NE589

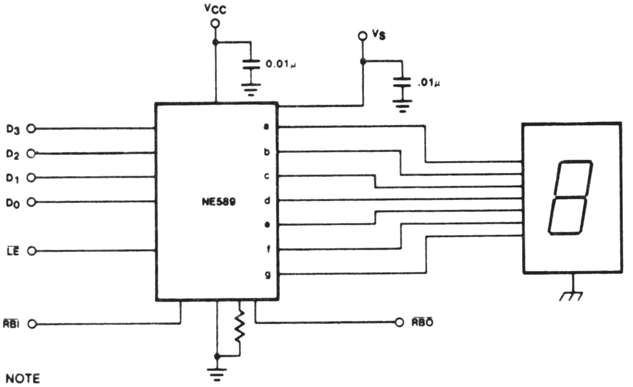
TYPICAL PERFORMANCE CURVES (Cont'd)

SUPPLY CURRENT VS SUPPLY VOLTAGE
NE589



TYPICAL APPLICATIONS

DRIVING A SINGLE DIGIT



NOTE
Decoupling capacitor on V_{CC} should be 0.01 μF ceramic

Figure 5

However, the average power dissipation will be considerably less than this. Assuming 5 segments are on (the average for all output code combinations), then

$$P_{d\ av} = 5.0 \times 30 + 3.00 \times 5 \times 25 \text{ mW}$$
$$= 525 \text{ mW}$$

Operating temperature range limitations can be deduced from the power dissipation graph in figure 9.

However, a major portion of this power dissipation ($P_{d\ max}$) is because the current source output is operating with 3.25 V across it. In practice, the outputs operate satisfactorily down to 0.5V, and so the extra voltage may be dropped external to the integrated circuit.

Suppose the worst case V_{CC}/V_S supply is 4.75 to 5.25V, and that the maximum V_E for the LED display is 2.25V. Only 2.75V is required to keep the display active, and hence 2.0V may be dropped externally with a resistor from V_{CC} to V_S. The value of this resistor is calculated by:

$$R_S = \frac{2.0}{7 \times I_{seg}} \simeq 10\Omega \text{ (½ W rating)}$$

assuming worst case I_{seg} of 30 mA

Hence now $P_{d\ max} = V_{CC} \times I_{CC} + (V_S - V_V - R_X \times 7 \times I_{seg}) \times 7 \times X\, I_{seg} \times K_{DC}$
$= 5.25 \times 50 + 1.25 \times 7 \times 30$ mW
$= 525$ mW

and $P_{d\ av} = 5.0 \times 30 + 1.25 \times 5 \times 25$
$= 306$ mW

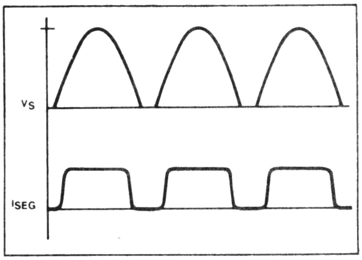
If a diode (or 2) is used to reduce voltage to the display, then the voltage appearing across the display driver will be independent of the number of "ON" segments and will be equal to

$$V_S - V_F - nV_d\,,\ V_D \simeq 0.8V$$

Where n is the number of diodes used, power dissipation can be calculated in a similiar manner.

In a multiplexed display system, the voltage drop across the digit driver must also be considered in computing device power dissipation. It may even be an advantage to use a digit driver which drops an appreciable voltage, rather than the saturating PNP transistors shown in figure 8. For example a darlington PNP or NPN emitter follower may be preferable. Figure 7 shows the NE591 as the digit driver in a multiplexed display system. The NE591 output drops about 1.8V which means that the power dissipation is evenly distributed between the two integrated circuits.

Where V_S and V_{CC} are two different supplies, the V_S supply may be optimized for minimum system power dissipation and/or cost. Clearly, good regulation in the V_S supply is totally unnecessary, and so this supply can be made much cheaper than the regulated 5V supply used in the rest of the system. In fact a simple unsmoothed full-wave rectified sine wave works extremely well if a slight loss in brightness can be tolerated. A transformer voltage of about 3-4.5V rms works well in most LED display systems. Waveforms are shown below:



The duty cycle for this system depends upon V_S, V_F and the output characteristics of the display driver.

With
V_S = 4.9V pk.
V_F = 2.0V

The duty cycle is approximately 60%.

TYPICAL APPLICATIONS (Cont'd)

4-DIGIT DISPLAY WITH BRIGHTNESS CONTROL AND LEADING EDGE RIPPLE BLANKING

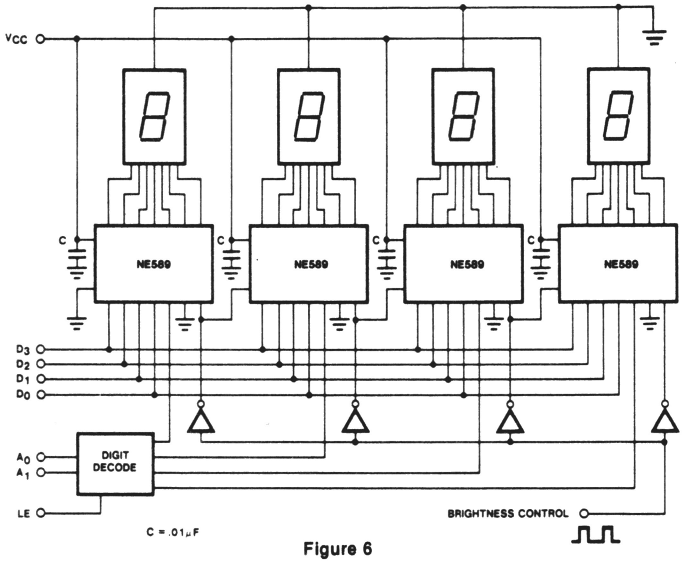

VCC
C
NE589
NE589
NE589
NE589
D3
D2
D1
D0
A0
A1
DIGIT DECODE
LE
C = .01μF
BRIGHTNESS CONTROL

Figure 6

INTERFACING 8-DIGIT LED DISPLAY WITH μP BUS

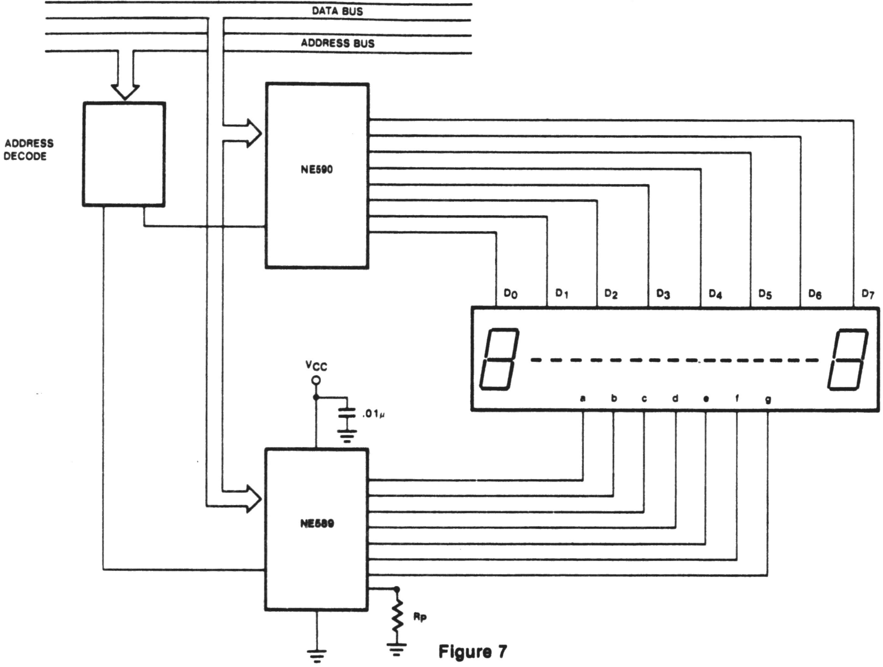

DATA BUS
ADDRESS BUS
ADDRESS DECODE
NE590
D0
D1
D2
D3
D4
D5
D6
D7
a
b
c
d
e
f
g
VCC
.01μ
NE589
Rp

Figure 7

TYPICAL APPLICATIONS (Cont'd)

4-DIGIT MULTIPLEXED LED DISPLAY

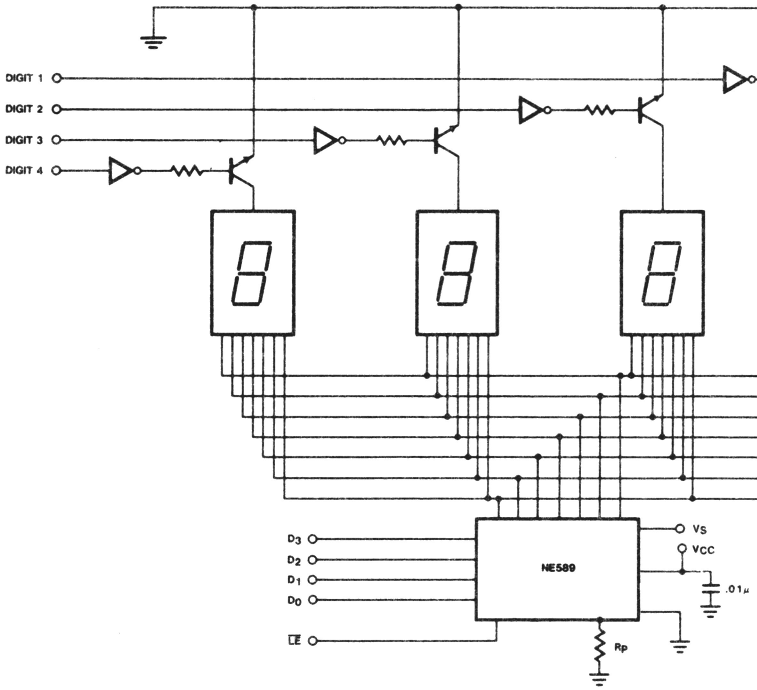

DIGIT 1
DIGIT 2
DIGIT 3
DIGIT 4
D3
D2
D1
D0
LE
NE589
VS
VCC
.01μ
RP

Figure 8

For additional information, refer to the Applications Section.

ADDRESSABLE PERIPHERAL DRIVERS NE590/NE591

DESCRIPTION

The NE590/591 addressable peripheral drivers are high current latched drivers, similar in function to the 9334 address decoder. The device has 8 Darlington power outputs, each capable of 250mA load current. The outputs are turned on or off by respectively loading a logic high or logic low into the device data input. The required output is defined by a 3-bit address. The device must be enabled by a $\overline{CE}$ input line. A common clear input, $\overline{CLR}$, turns all outputs off when a logic low is applied.

The NE590 has 8 open collector Darlington outputs which sink current to ground. The device is packaged in a 16-pin molded or cerdip package.

The NE591 has 8 open emitter Darlington outputs which source current to an external load from a common collector line, V_S. This V_S line need not necessarily be the same as the 5 volt V_{CC} supply. The device is packaged in an 18-pin molded or cerdip package.

FEATURES

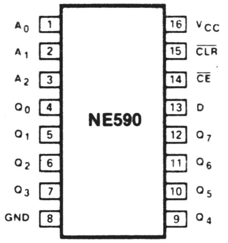
- **8 high current outputs**
- **Low-loading bus compatible inputs**
- **Power-on clear ensures safe operation**
- **NE590 will operate in addressable or demultiplex mode**
- **Allows random (addressed) data entry**
- **Easily expandable**
- **NE590 is pin compatible with 54/74LS259**

APPLICATIONS

- **Relay driver**
- **Indicator lamp driver**
- **Triac trigger**
- **LED display digit driver**
- **Stepper motor driver**

PIN CONFIGURATION

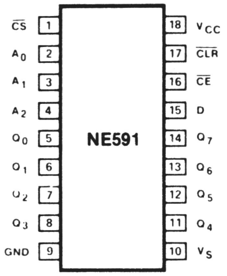
F,N PACKAGE



TOP VIEW

ORDER NUMBERS
NE590N,F

F,N PACKAGE



TOP VIEW

ORDER NUMBERS
NE591N,F

PIN DESIGNATION

590 PIN NO.	591 PIN NO.	SYMBOL	NAME & FUNCTION
1-3	2-4	A_0-A_2	A 3-bit binary address on these pins defines which of the 8 output latches is to receive the data.
4-7, 9-12	5-8, 11-14	Q_0-Q_7	The 8 device outputs. The NE590 has open collector Darlington outputs. The NE591 has open emitter follower outputs.
13	15	D	The data input. When the chip is enabled, this data bit is transferred to the defined output such that: "1" turns output switch "ON" "0" turns output switch "OFF" Thus in logic terms, the NE590 inverts data to the relevant output. The NE591 retains true data at the output.
14	16	$\overline{CE}$	The chip enable. When this input is low, the output latches will accept data. When $\overline{CE}$ goes high, all outputs will retain their existing state, regardless of address or data input conditions.
15	17	$\overline{CLR}$	The clear input. When $\overline{CLR}$ goes low all output switches are turned "OFF". On the NE590, a high data input will override the clear function on the addressed latch. On the NE591, $\overline{CLR}$ low will override any other condition.
—	1	$\overline{CS}$	The chip select input provides for an additional level of address decoding.
—	10	V_S	The V_S line provides the power to all 8 output devices. It is connected to the collectors of all 8 output transistors. This pin may be connected to the V_{CC} or another supply.

ADDRESSABLE PERIPHERAL DRIVERS

NE590/NE591

TRUTH TABLE (NE590)

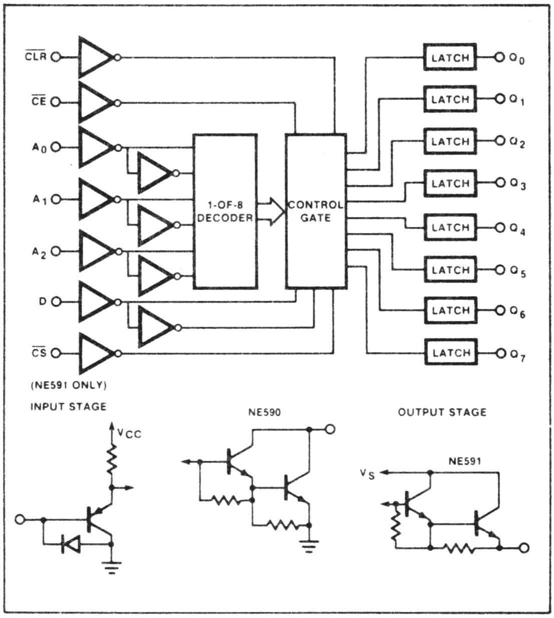
INPUTS						OUTPUTS								MODE
$\overline{CLR}$	$\overline{CE}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
L	H	X	X	X	X	H	H	H	H	H	H	H	H	Clear
L	L	L	L	L	L	H	H	H	H	H	H	H	H	Demultiplex
L	L	H	L	L	L	L	H	H	H	H	H	H	H	
L	L	L	H	L	L	H	H	H	H	H	H	H	H	
L	L	H	H	L	L	H	L	H	H	H	H	H	H	
L	L	L	H	H	H	H	H	H	H	H	H	H	H	
L	L	H	H	H	H	H	H	H	H	H	H	H	L	
H	H	X	X	X	X	Q_{N-1}	→	→	→	→	→	→	→	Memory
H	L	L	L	L	L	H	Q_{N-1}	→	→	→	→	→	→	Addressable Latch
H	L	H	L	L	L	L	Q_{N-1}	→	→	→	→	→	→	
H	L	L	H	L	L	Q_{N-1}	H	Q_{N-1}	→	→	→	→	→	
H	L	H	H	L	L	Q_{N-1}	L	Q_{N-1}						
H	L	L	H	H	H	Q_{N-1}	→	→	→	→	→	→	H	
H	L	H	H	H	H	Q_{N-1}	→	→	→	→	→	→	L	

X Don't care condition
Q_{N-1} Previous output state
L Low voltage level/"ON" output state
H High voltage level/"OFF" output state

(NE591)

INPUTS							OUTPUTS								MODE
$\overline{CLR}$	$\overline{CE}$	$\overline{CS}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	
L	X	X	X	X	X	X	L	L	L	L	L	L	L	L	Clear
H	H	H	X	X	X	X	Q_{N-1}	→	→	→	→	→	→	→	Memory
H	H	L	X	X	X	X	Q_{N-1}	→	→	→	→	→	→	→	
H	L	H	X	X	X	X	Q_{N-1}	→	→	→	→	→	→	→	
H	L	L	L	L	L	L	L	Q_{N-1}	→	→	→	→	→	→	Addressable Latch
H	L	L	H	L	L	L	H	Q_{N-1}	→	→	→	→	→	→	
H	L	L	L	H	L	L	Q_{N-1}	L	Q_{N-1}	→	→	→	→	→	
H	L	L	H	H	L	L	Q_{N-1}	H	Q_{N-1}	→	→	→	→	→	
H	L	L	L	H	H	H	Q_{N-1}	→	→	→	→	→	→	L	
H	L	L	H	H	H	H	Q_{N-1}	→	→	→	→	→	→	H	

X = Don't care
Q_{N-1} = Previous output state
L = Low voltage level/"OFF" output state
H = High voltage level/"ON" output state



ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise specified.

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7	V
V_{IN}	Input voltage	-0.5 to +15	V
V_{OUT}	Output voltage		V
	NE590	0 to +7	
	NE591	0 to V_{CC}	
V_S	Source bus voltage		V
	NE591 only	-0.5 to +7	
V_S-V_{CC}	Source/supply differential voltage		V
	NE591 only	-5 to +2	
I_{OUT}	Output current		mA
	Each output	300	
	All outputs	1000	
P_D	Power dissipation[1]	1	W
	Temperature range		°C
T_A	Ambient	0 to +70	
T_J	Junction	165	
T_{STG}	Storage	-65 to +150	
T_{sold}	Lead soldering temperature (10sec max)	300	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 4.75 to 5.25V, 0°C ≤ T_A ≤ 70°C unless otherwise specified.[2,3]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IH}	High		2.0			
V_{IL}	Low				0.8	
	Output voltage					V
V_{OL}	Low (NE590 only)	I_{OL} = 250mA, T_A = 25°C		1.0	1.3	
		Over temperature			1.5	
V_{OH}	High (NE591 only)	I_{OH} = -250mA, V_{CC} = V_S = 5V	2.9			
	Input current					µA
I_{IH}	High	V_{in} = V_{CC}		0.1	10	
I_{IL}	Low	V_{in} = 0V				
	$\overline{CE}$ input			-25	-60	
	All other inputs			-15	-50	
I_{OH}	Leakage current	V_{OUT} = 5.25V		10	250	µA
	Supply current[4]	V_S = V_{CC} = 5V				mA
I_{CCL}	All outputs low					
	NE590			33	50	
	NE591			15	50	
I_{CCH}	All outputs high					
	NE590			15	50	
	NE591			30	50	

NOTES

1. Derate power dissipation as indicated above threshold ambient temperature:
   - NE590N at 9.3 mW/°C above 85°C
   - NE590F at 7.5 mW/°C above 65°C
   - NE591N at 11.5 mW/°C above 100°C
   - NE591F at 10.7 mW/°C above 72°C
2. All typical values are at V_{CC} = 5V and T_A = 25°C.
3. For the NE591, V_S = V_{CC} in all tests.
4. Supply current for the NE591 is measured with no output load.

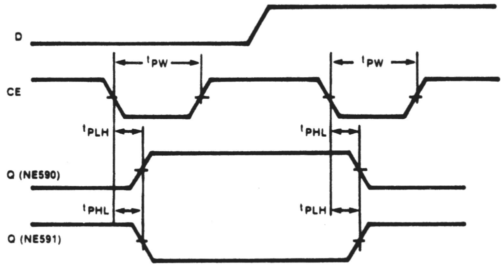
SWITCHING CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$

PARAMETER		TO	FROM	NE590			NE591			UNIT
				Min	Typ	Max	Min	Typ	Max	
	Propagation delay time									ns
t_{PLH}	Low to high^5	Output	$\overline{CE}$		65	150		50	80	
t_{PHL}	High to low^5				115	230		70	120	
t_{PLH}	Low to high^6	Output	Data		65	130		45	70	
t_{PHL}	High to low^6				120	240		65	100	
t_{PLH}	Low to high^7	Output	Address		100	200		45	80	
t_{PHL}	High to low^7				130	260		75	140	
t_{PLH}	Low to high^8	Output	$\overline{CLR}$		65	130				
t_{PHL}	High to low^8							45	140	
t_{PLH}	Low to high^5	Output	$\overline{CS}$					40	80	
t_{PHL}	High to low^5							70	120	
SWITCHING SET-UP REQUIREMENTS										
$t_{s(H)}$^{9}		Chip enable	High data	210	60		50	15		ns
$t_{s(L)}$^{9}		Chip enable	Low data	210	105		80	60		ns
$t_{s(A)}$^{10}		Chip enable	Address	+ 20	− 5		+ 20	− 20		ns
$t_{h(H)}$^{9}		Chip enable	High data	− 20	60		0	− 60		ns
$t_{h(L)}$^{9}		Chip enable	Low data	− 20	60		+ 10	− 15		ns
$t_{s(CS)}$^{9}		Chip enable	Low chip select				80	50		ns
$t_{pw(E)}$	Chip enable pulse width^5			300	140		100	50		ns

NOTES

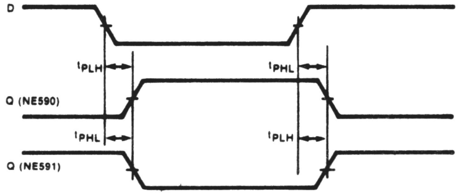
5. See Turn-On and Turn-Off Delays, Enable to Output and Enable Pulse Width timing diagram.
6. See Turn-On and Turn-Off Delays, Data to Output timing diagram.
7. See Turn-On and Turn-Off Delays, Address to Output timing diagram.
8. See Turn-Off Delay, Clear to Output timing diagram.
9. See Setup and Hold Time, Data to Enable timing diagram.
10. See Setup Time, Address to Enable timing diagram.

TURN-ON AND TURN-OFF DELAYS, ENABLE TO OUTPUT AND ENABLE PULSE WIDTH



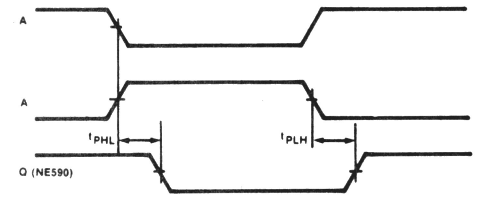
Other Inputs: $\overline{CLR}$ H, A Stable, $\overline{CS}$ L

TURN-ON AND TURN-OFF DELAYS, DATA TO OUTPUT



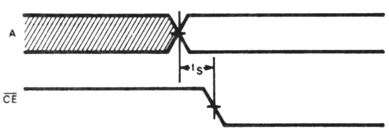
Other Inputs: $\overline{CE}$ $\overline{CS}$ L, $\overline{CLR}$ H, A Stable

TURN-ON AND TURN-OFF DELAYS, ADDRESS TO OUTPUT


A
A
t_{PHL}
t_{PLH}
Q (NE590)

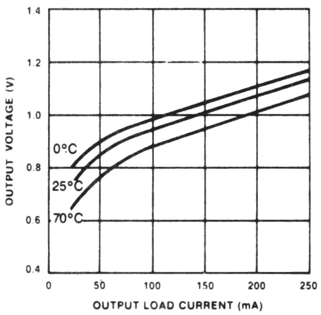
Other Inputs: $\overline{CE}$ = L, $\overline{CLR}$ = L, D = H

SETUP TIME, ADDRESS TO ENABLE

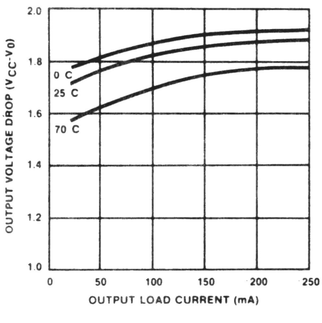

A
t_S
$\overline{CE}$

Other Inputs: $\overline{CLR}$ = H, $\overline{CS}$ = L

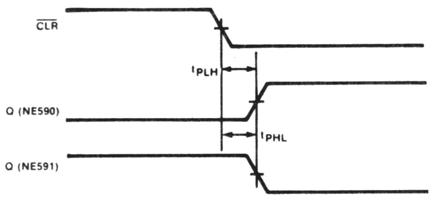
OUTPUT VOLTAGE VS LOAD CURRENT(NE590)



OUTPUT VOLTAGE DROP VS LOAD CURRENT(NE591)

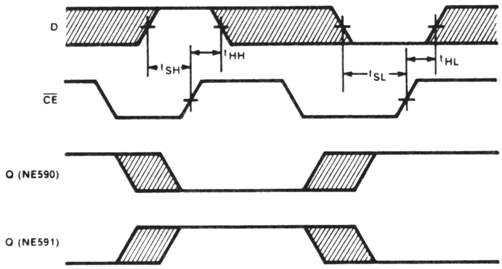


TURN-OFF DELAY, CLEAR TO OUTPUT


$\overline{CLR}$
t_{PLH}
Q (NE590)
t_{PHL}
Q (NE591)

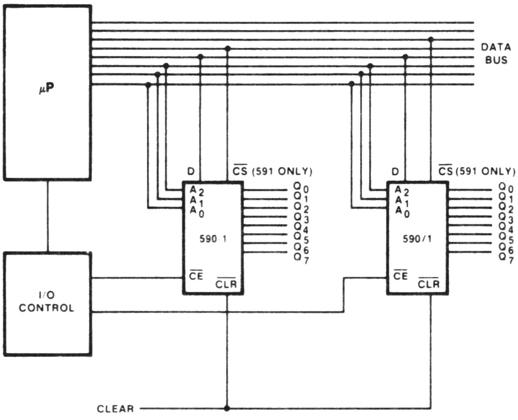
Other Inputs: $\overline{CE}$ = H, $\overline{CS}$ = H

SETUP AND HOLD TIME, DATA TO ENABLE


D
t_{SH}
t_{HH}
t_{SL}
t_{HL}
$\overline{CE}$
Q (NE590)
Q (NE591)

Other Inputs: $\overline{CLR}$ H, A Stable, $\overline{CS}$ = L

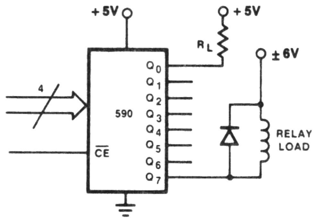
INTERFACING THE 590/591 WITH A MICROPROCESSOR SYSTEM


μP
DATA BUS
D
$\overline{CS}$ (591 ONLY)
A_2
A_1
A_0
590/1
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
$\overline{CE}$
$\overline{CLR}$
I/O CONTROL
CLEAR

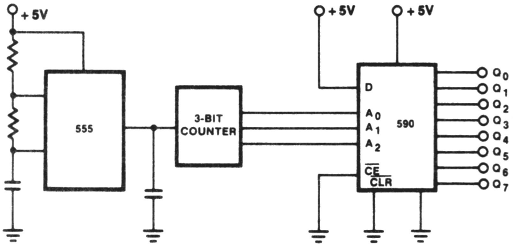
A_0, A_1, A_2, and $\overline{CS}$ may be connected to the address bus if permitted by system design.

TYPICAL APPLICATIONS (Cont'd)

NE590 DRIVING SIMPLE LOADS


+5V
+5V
R_L
±6V
4
590
CE
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
RELAY LOAD

NE590 OPERATING IN DEMULTIPLEX MODE


+5V
+5V
+5V
555
3-BIT COUNTER
D
A_0
A_1
A_2
590
CE
CLR
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7

VACUUM FLUORESCENT DISPLAY DRIVER

SA/NE594

DESCRIPTION

The SA/NE594 is a display driver interface for vacuum fluorescent displays. The device is comprised of 8 drivers and a bias network and is capable of driving the digits and/or segments of most vacuum fluorescent displays.

The inputs are designed to be compatible with TTL, DTL, NMOS, PMOS or CMOS output circuitry.

There is an active pull-down circuit on each output so that display ghosting is minimized and no external components are required for most fluorescent display applications.

FEATURES

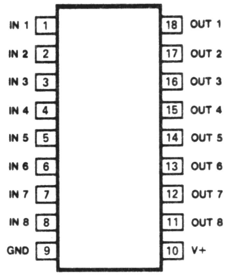
- **Digit and/or segment drivers**
- **Active output pull-down circuitry**
- **High output breakdown voltage**
- **Low supply voltage**
- **Input compatible with all logic outputs**

APPLICATIONS

- **Digital clocks**
- **Dashboard displays**
- **Panel displays**

PIN CONFIGURATION

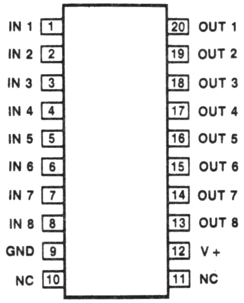
N, F PACKAGE


IN 1 1
IN 2 2
IN 3 3
IN 4 4
IN 5 5
IN 6 6
IN 7 7
IN 8 8
GND 9
18 OUT 1
17 OUT 2
16 OUT 3
15 OUT 4
14 OUT 5
13 OUT 6
12 OUT 7
11 OUT 8
10 V+

TOP VIEW

ORDER NUMBERS
SA/NE594N SA/NE594F

D¹ PACKAGE


IN 1 1
IN 2 2
IN 3 3
IN 4 4
IN 5 5
IN 6 6
IN 7 7
IN 8 8
GND 9
NC 10
20 OUT 1
19 OUT 2
18 OUT 3
17 OUT 4
16 OUT 5
15 OUT 6
14 OUT 7
13 OUT 8
12 V+
11 NC

TOP VIEW

ORDER NUMBER
NE594D¹

NOTES:
1. SOL - Released in Large SO package only.
2. SOL and non-standard pinout.
3. SO and non-standard pinouts.

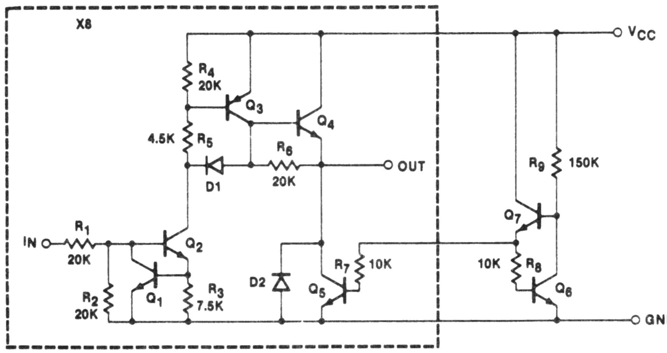
ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise noted)

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	45	V
V_{OUT}	Output voltage	V_{CC}	
V_{IN}	Input voltage	−0.3, +20	V
I_{OUT}	Output current		
	Each output	50	mA
	All outputs	200	mA
Pd	Power dissipation* (at 25°C)	800	mW
T_A	Operating temperature range		
	NE	0 to 70	°C
	SA	−40 to +85	°C
T_{STG}	Storage temperature range	+65 to +150	°C
T_J	Maximum junction temperature	− 165	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C

NOTE

*Derate N (Plastic) Package above 38°C at 7.14 mW/°C.
Derate F (Ceramic) Package above 75°C at 10.8 mW/°C.

EQUIVALENT SCHEMATIC


X8
VCC
R4
20K
Q3
Q4
4.5K
R5
R6
D1
20K
OUT
R9
150K
Q7
R1
IN
20K
Q2
Q1
R2
20K
R3
7.5K
D2
Q5
R7
10K
10K
R8
Q6
GND

VACUUM FLUORESCENT DISPLAY DRIVER

SA/NE594

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +4.75 to +40V, T_A (NE) = 0 to 70°C, T_A (SA) = −40 to +85°C unless otherwise stated.

PARAMETER		TEST CONDITIONS		LIMITS			UNIT
				Min	Typ	Max	
V_{CC}	Supply voltage range			4.75	35	40	V
I_{CCH}	Supply current (all outputs high)	V_{CC} = 40V	V_{IN} = 3.5V		3	6	mA
I_{CCL}	Supply current (all outputs low)	V_{CC} = 40V	V_{IN} = 0.4V		0.4	1	mA
V_{IN}	Input voltage range			0		15	V
V_{IH}	Input voltage to ensure logic '1'			2.6			V
V_{IL}	Input voltage to ensure logic '0'					0.8	V
I_{IH}	Input current to ensure logic '1'			100			µA
I_{IL}	Input current to ensure logic '0'					10	µA
I_{IN}	Input current	V_{IN} = 2.6V			60	130	µA
		V_{IN} = 5.0V			180	330	µA
		V_{IN} = 15.0V			.68	1.3	mA
V_{OH}	Output high voltage	V_{IN} = 3.5V	T_A = 25°C	$V_{CC}-1.5$	$V_{CC}-1.1$		V
		I_{OUT} = −25mA	Over Temp.	$V_{CC}-2$	$V_{CC}-1.3$		V
		V_{OUT} with respect to V_{CC}					
V_{OH}	Output high, *no load* voltage	V_{IN} = 3.5V I_{OUT} = 0, T_A=25°C V_{OUT} with respect to V_{CC}		$V_{CC}-1$	$V_{CC}-0.8$		V
V_{OFF}	Output 'OFF' voltage level	V_{IN} = 0.8V I_{OUT} = 0			10	200	mV
I_{OH}	Available output current	V_{CC} = 35V V_{OUT} = 30V T_A = 25°C	V_{IN} = 3.5V	−35			mA
I_{OUT}	Output pulldown current	V_{CC} = V_{OUT} = 35V Inputs open		100	200	400	µA
I_{CEX}	Output leakage current	T_A = 25°C	V_{IN} = 0.4V		−1		µA
		V_{CC} = 40V,	V_{OUT} = 0V		−1		

AC ELECTRICAL CHARACTERISTICS[1]

V_{CC} = 35V, T_A = 25°C

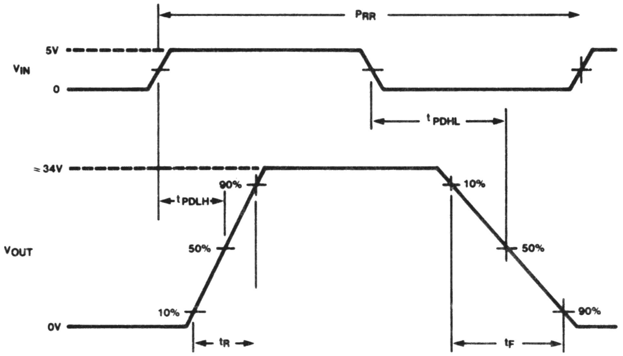
PARAMETER		TEST CONDITIONS	NE/SA594			UNIT
			Min	Typ	Max	
t_{PdLH}	Propagation delay - low to high output transition.	50% V_{IN} to 50% V_{OUT}		1	5	µS
t_{PdHL}	Propagation delay - high to low output transition.	50% V_{IN} to 50% V_{OUT}		3	10	µS
t_R	Output rise time	10% V_{OUT} to 90% V_{OUT}		0.5	3	µS
t_F	Output fall time	90% V_{OUT} to 10% V_{OUT}		1.5	5	µS

NOTE

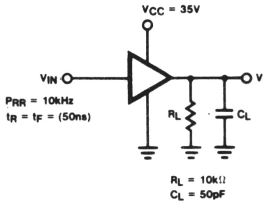
[1] See figure 1

SWITCHING TIMES OF DRIVERS

VOLTAGE WAVEFORMS


PRR
5V
VIN
0
tPDHL
≈34V
90%
tPDLH
10%
VOUT
50%
50%
10%
90%
0V
tR
tF

TEST CIRCUIT

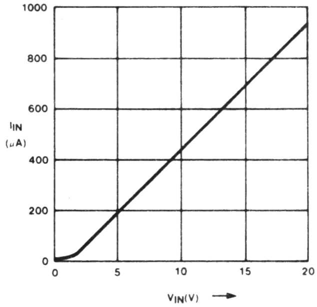

VCC = 35V
VIN
VOUT
PRR = 10kHz
tR = tF = (50ns)
RL
CL
RL = 10kΩ
CL = 50pF

INCLUDES PROBE AND FIXTURE CAPACITANCE

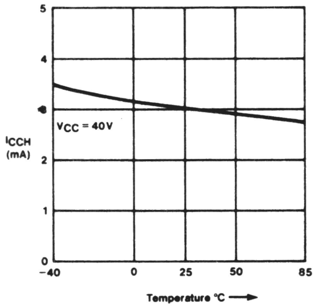
Figure 1

TYPICAL PERFORMANCE CHARACTERISTICS

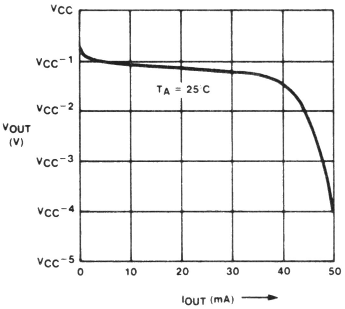
I_{IN} VS V_{IN}



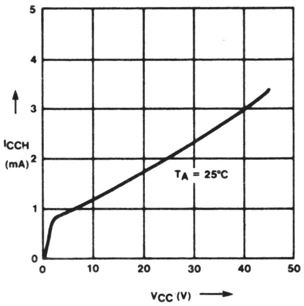
I_{CCH} VS TEMPERATURE



OUTPUT VOLTAGE VS OUTPUT CURRENT



I_{CC} VS V_{CC} (ALL INPUTS HIGH)



TYPICAL APPLICATION
DIGITAL CLOCK WITH ALARM

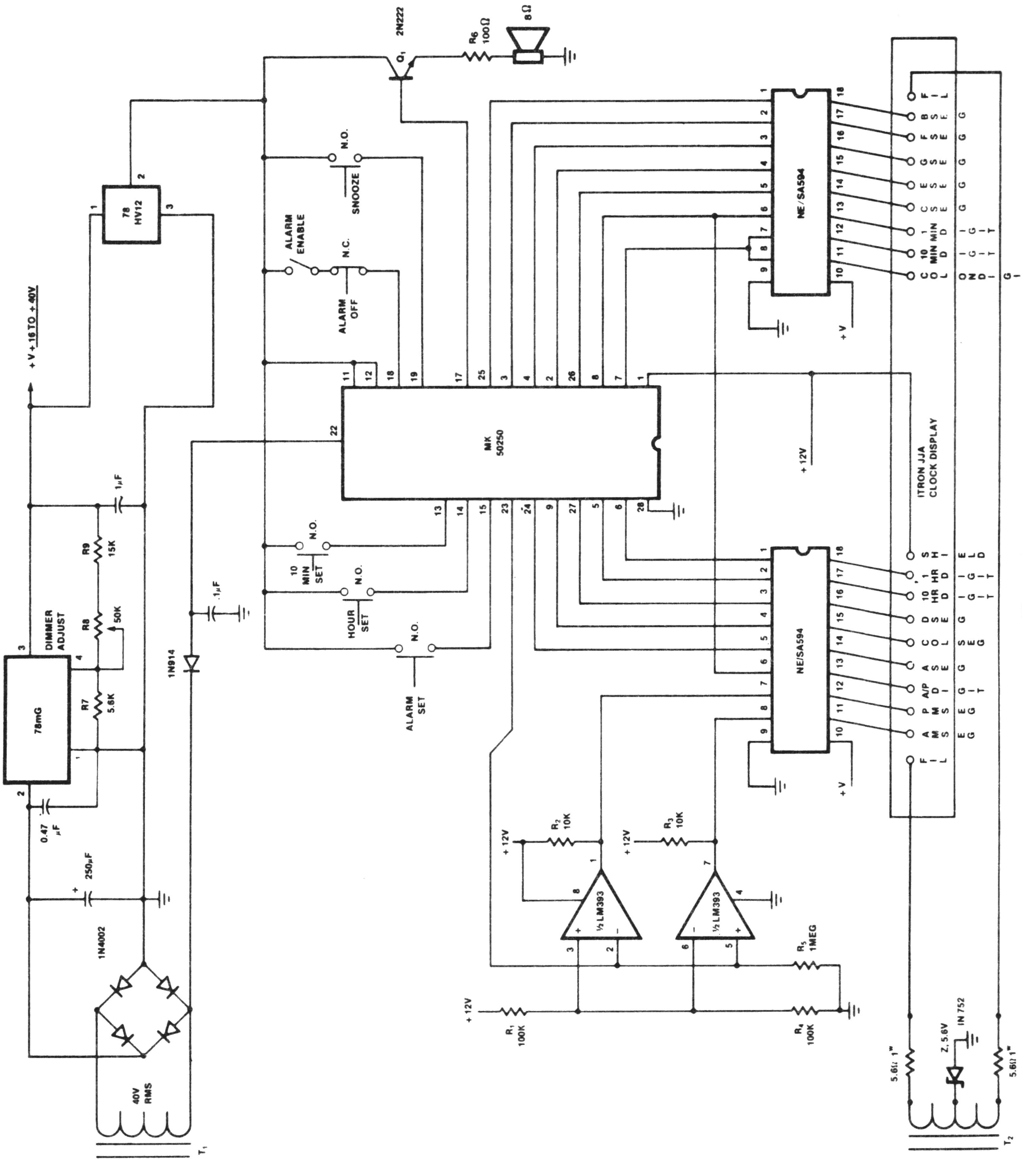

+V +16 TO +40V
78 HV12
78mG
DIMMER ADJUST
R9 15K
R8 50K
R7 5.8K
1μF
0.47 μF
250μF
1N4002
40V RMS
T1
1N914
.1μF
ALARM ENABLE
N.C.
ALARM OFF
N.O.
SNOOZE
10 MIN SET
HOUR SET
ALARM SET
Q1 2N222
R6 100Ω
8Ω
MK 50250
NE/SA594
+V
+12V
ITRON JJA CLOCK DISPLAY
R2 10K
R3 10K
½ LM393
R5 1MEG
R1 100K
R4 100K
Z, 5.6V IN 752
5.6Ω 1W
T2

Figure 2

HIGH VOLTAGE/HIGH CURRENT DARLINGTON TRANSISTOR ARRAYS **ULN2003/04**

DESCRIPTION

These high-voltage, high-current Darlington transistor arrays are comprised of seven silicon NPN Darlington pairs on a common monolithic substrate. All units feature open collector outputs and integral suppression diodes for inductive loads. Peak inrush currents to 600mA are allowable, making them ideal for driving tungsten filament lamps also.

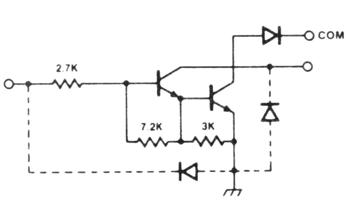
The Type ULN2003 has a series base resistor to each Darlington pair, and thus allows operation directly with TTL or CMOS 5V supply voltage.

The Type ULN2004 has an appropriate series input resistor to allow its operation directly from CMOS or PMOS outputs utilizing supply voltages of 6 to 15V. The required input current is below that of the Type ULN2003.

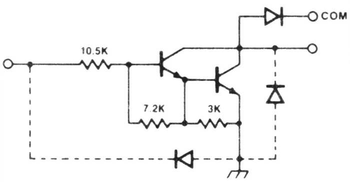
In all cases, the individual Darlington pair collector current rating is 500mA. However, outputs may be paralleled for higher load current capability. All devices are supplied in a 16-pin dual in-line plastic package.

EQUIVALENT SCHEMATICS

TYPE ULN2003
(each driver)

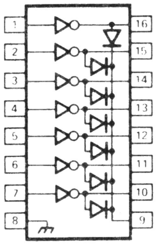


TYPE ULN2004
(each driver)



PIN CONFIGURATION

D,N,F PACKAGE



TOP VIEW

ORDER NUMBERS
ULN2003D,N,F
ULN2004D,N,F

FEATURES

- **Peak inrush current 600mA**
- **Protected internally against inductive loads**
- **Open collector topology**
- **Compatible with most logic technologies**

ABSOLUTE MAXIMUM RATINGS

at 25° C Free-Air temperature for any one Darlington pair unless otherwise specified.

PARAMETER		RATING	UNIT
V_{CE}	Output voltage	50	V
V_{IN}	Input voltage	30	V
V_{EBO}	Emitter base voltage	6	V
I_C	Continuous collector current	500	mA
I_B	Continuous base current	25	mA
P_D	Power dissipation	1.3	W
	Derating factor above 25° C	95	° C/W
T_A	Ambient temperature range (operating)	0 to +85	°C
T_S	Storage temperature range	-65 to +150	°C

*NOTE
Under normal operating conditions, these units will sustain 350mA per output with $V_{CE(SAT)}$ = 1.6V at 70° C with a pulse width of 20 ms and a duty cycle of 30%.

DC ELECTRICAL CHARACTERISTICS T_A = 25°C unless otherwise specified.[1,2,3]

PARAMETER		TEST CONDITIONS	Test Fig.	LIMITS			UNIT
				Min	Typ	Max	
I_{CEX}	Output leakage current	V_{CE} = 50V, T_A = 70°C	1A	—	—	100	µA
	Type ULN2004	V_{CE} = 50V, T_A = 70°C, V_{IN} = 1V	1B	—	—	500	µA
$V_{CE(SAT)}$	Collector-emitter	I_C = 350mA, I_B = 500µA	2	—	1.25	1.6	V
	Saturation voltage	I_C = 200mA, I_B = 350µA	2	—	1.1	1.3	V
		I_C = 100mA, I_B = 250µA	2	—	0.9	1.1	V
$I_{IN(ON)}$	Input current						
	Type ULN2003	V_{IN} = 3.85V	3	—	0.93	1.35	mA
	Type ULN2004	V_{IN} = 5V	3	—	0.35	0.5	mA
		V_{IN} = 12V	3	—	1.0	1.45	mA
$I_{IN(OFF)}$	Input current	I_C = 500µA, T_A = 70°C	4	50	65	—	µA
$V_{IN(ON)}$	Input voltage						
	Type ULN2003	V_{CE} = 2V, I_C = 200mA	5	—	—	2.4	V
		V_{CE} = 2V, I_C = 250mA	5	—	—	2.7	V
		V_{CE} = 2V, I_C = 300mA	5	—	—	3.0	V
	Type ULN2004	V_{CE} = 2V, I_C = 125mA	5	—	—	5.0	V
		V_{CE} = 2V, I_C = 200mA	5	—	—	6.0	V
		V_{CE} = 2V, I_C = 275mA	5	—	—	7.0	V
		V_{CE} = 2V, I_C = 350mA	5	—	—	8.0	V
C_{IN}	Input capacitance		—	—	15	30	pF
I_R	Clamp diode leakage current	V_R = 50V	6	—	—	50	µA
V_F	Clamp diode forward voltage	I_F = 350mA	7	—	1.7	2	V

NOTES

1. All limits stated apply to the complete Darlington series except as specified for a single device type.
2. The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
3. The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C unless otherwise specified.[1,2,3]

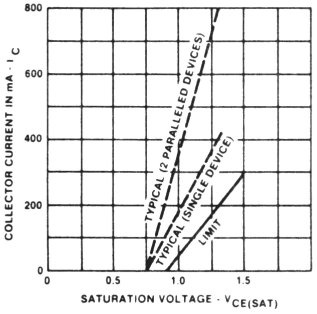
PARAMETER		TEST CONDITIONS	Test Fig.	LIMITS			UNIT
				Min	Typ	Max	
t_{PLH}	Turn-on delay	0.5 E_{IN} to 0.5 E_{OUT}	—	—	1.0	5	µs
t_{PHL}	Turn-off delay	0.5 E_{IN} to 0.5 E_{OUT}	—	—	1.0	5	µs

NOTES

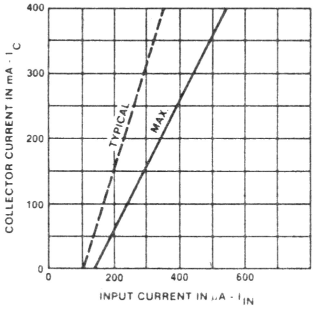
1. All limits stated apply to the complete Darlington series except as specified for a single device type.
2. The $I_{IN(OFF)}$ current limit guarantees against partial turn-on of the output.
3. The $V_{IN(ON)}$ voltage limit guarantees a minimum output sink current per the specified test conditions.

TYPICAL PERFORMANCE CHARACTERISTICS

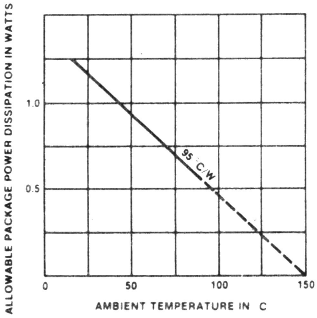
COLLECTOR CURRENT AS A FUNCTION OF SATURATION VOLTAGE



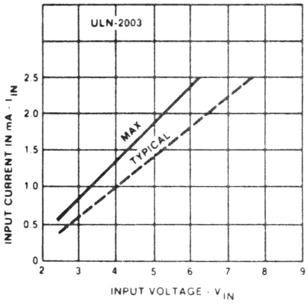
COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT



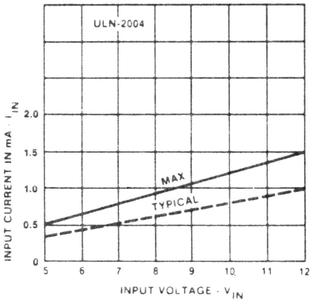
ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE FOR TYPE ULN2003



INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE FOR TYPE ULN2004



TEST FIGURES

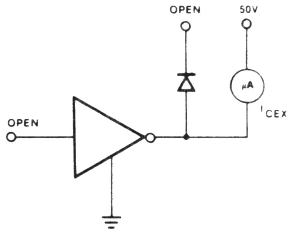

OPEN
50V
OPEN
µA
I_{CEX}

Figure 1A

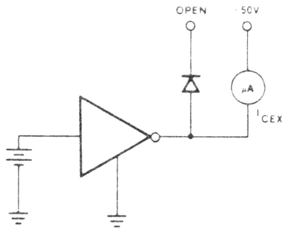

OPEN
50V
µA
I_{CEX}

Figure 1B

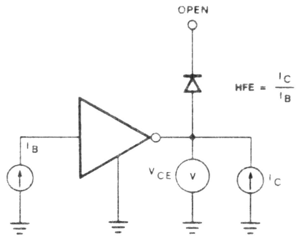

OPEN
$HFE = \frac{I_C}{I_B}$
I_B
V_{CE}
V
I_C

Figure 2

TEST FIGURES (Cont'd)

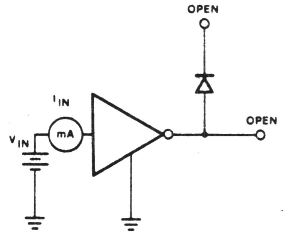

OPEN
I_IN
mA
V_IN
OPEN

Figure 3

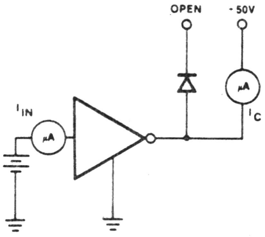

OPEN
-50V
μA
I_IN
μA
I_C

Figure 4

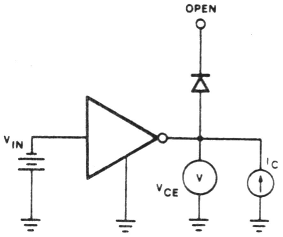

OPEN
V_IN
V
V_CE
I_C

Figure 5

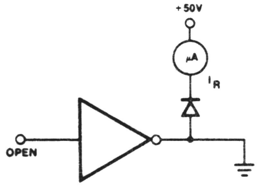

+50V
μA
I_R
OPEN

Figure 6

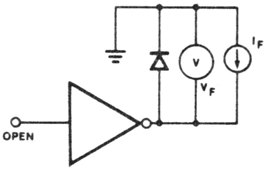
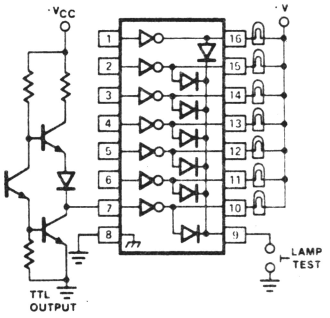


Figure 7

TYPICAL APPLICATIONS

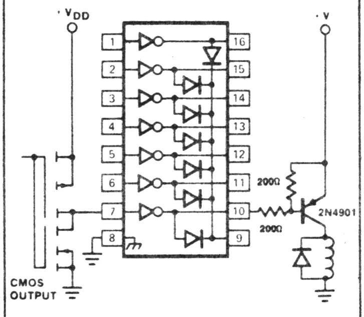
TTL TO LOAD

ULN2003


+V_CC
+V
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
LAMP TEST
TTL OUTPUT

BUFFER FOR HIGHER CURRENT LOADS

ULN2004


+V_DD
+V
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
200Ω
200Ω
2N4901
CMOS OUTPUT

LVDT SIGNAL CONDITIONER NE5520

DESCRIPTION

The NE5520 is a signal conditioning circuit for use with Linear Variable Differential Transformers (LVDT). The chip includes a low distortion amplitude stable sine wave oscillator with programmable frequency to drive the primary of the LVDT; a synchronous demodulator to convert the LVDT output amplitude and phase to position information; and an output amp to provide gain and filtering.

FEATURES

- **Oscillator frequency: 1kHz to 20kHz**
- **Low distortion**
- **Capable of ratiometric operation**
- **Single supply operation 5V to 20V or dual supply ± 2.5V to ± 10V**
- **Low power consumption**

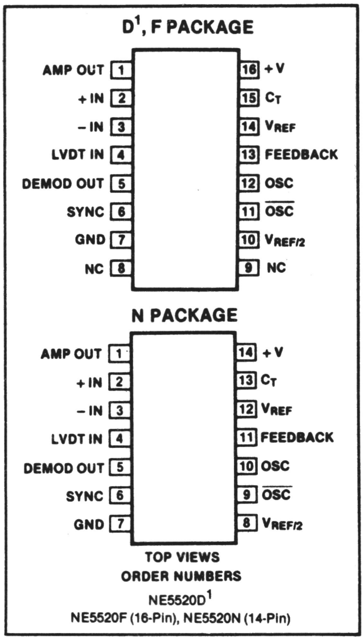
APPLICATIONS

- **LVDT signal conditioning**
- **RVDT signal conditioning**

ABSOLUTE MAXIMUM RATINGS

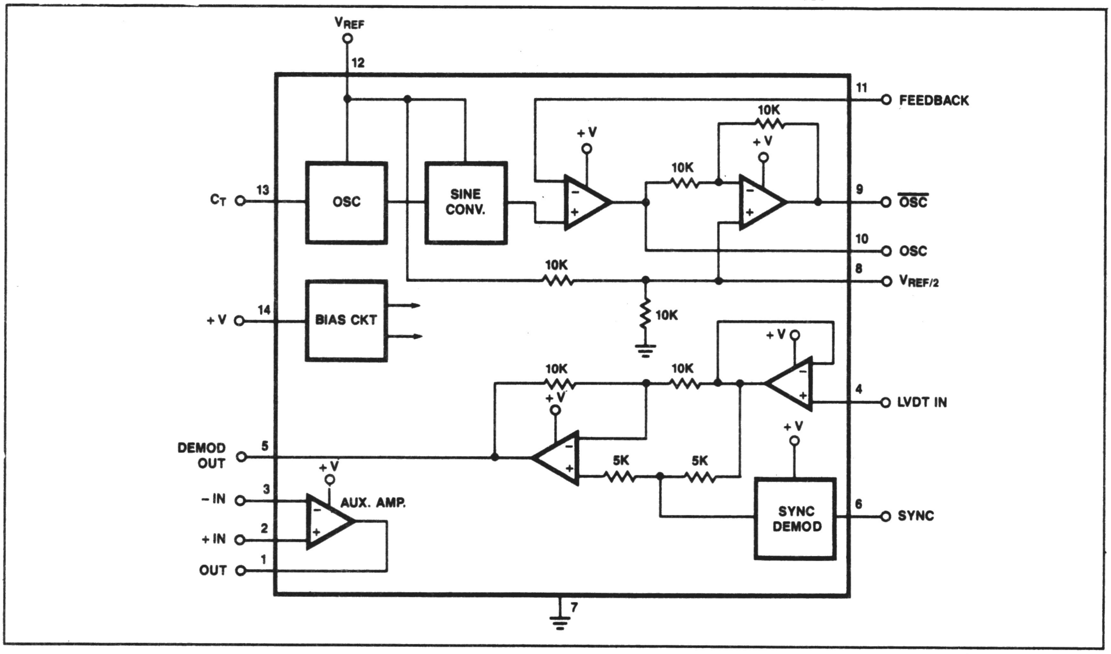
PARAMETER	RATING	UNIT
Supply voltage	+ 20	V
Split supply voltage	± 10	V
Operating temperature range	0 to + 70	°C
Storage temperature range	− 65 to + 165	°C
Power Dissipation (Note 1)	840	mW

PIN CONFIGURATION


D¹, F PACKAGE
AMP OUT 1
+IN 2
−IN 3
LVDT IN 4
DEMOD OUT 5
SYNC 6
GND 7
NC 8
16 +V
15 CT
14 VREF
13 FEEDBACK
12 OSC
11 OSC
10 VREF/2
9 NC
N PACKAGE
AMP OUT 1
+IN 2
−IN 3
LVDT IN 4
DEMOD OUT 5
SYNC 6
GND 7
14 +V
13 CT
12 VREF
11 FEEDBACK
10 OSC
9 OSC
8 VREF/2
TOP VIEWS
ORDER NUMBERS
NE5520D¹
NE5520F (16-Pin), NE5520N (14-Pin)

NOTES:
1. SOL - Released in Large SO package only.
2. SOL and non-standard pinout.
3. SO and non-standard pinouts.

BLOCK DIAGRAM


VREF
12
11
FEEDBACK
+V
10K
+V
10K
CT
13
OSC
SINE CONV.
9
OSC
10
OSC
10K
8
VREF/2
+V
14
BIAS CKT
10K
+V
10K
10K
+V
4
LVDT IN
+V
DEMOD OUT
5
5K
5K
+V
−IN
3
AUX. AMP.
+IN
2
OUT
1
SYNC DEMOD
6
SYNC
7

NOTES:
1. Supplied only in large SO (Small Outline) package. See package diagram.
2. Pin numbers are for N package.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_R = V+ = 10V$ unless otherwise specified.

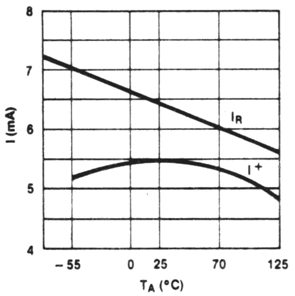
PARAMETER	TEST CONDITIONS	NE5520			UNIT
		Min	Typ	Max	
Supply current	Over temp.		7.0	10	mA
Reference current	Over temp.		5.5	10	mA
Reference voltage range	Over temp.	5		V +	V
Power dissipation			120	220	mW
Oscillator section					
Oscillator output			$\frac{V_R}{8.7}$		Vrms
Sine wave distortion			4		%
Initial amplitude error				± 3	%
Tempco of amplitude				0.05	%/°C
Voltage coef. of amplitude error				2.5	%/V
Initial accuracy of osc. frequency				20	%
Tempco of frequency error			0.05		%/°C
Voltage coef. of frequency			2.5		%/V (V_R)
Oscillator output load current			15		mA (rms)
	Over temp.	8			mA (rms)
Demodulator section					
Linearity error	Over temp.		0.05	0.1	%
Maximum demodulator input	Over temp. range	$\frac{V_R}{2} - 0.5$		$\frac{V_R}{2} + 0.5$	V
Demodulator offset voltage	Over temp. range			65	mV
Demodulator input current	Over temp.	– 1000	– 300		nA
$V_R/2$ accuracy	Over temp.	– 3	± 0.5	+ 3	%
Auxiliary Output Amplifier					
Input offset voltage	Over temp.	– 10		10	mV
Input bias current	Over temp. range	– 500	– 300		nA
Input offset current		– 100		100	nA
Gain	$R_L = 10k\Omega$ over temp.		100		V/mV
Slew rate			1.5		V/μsec
Gain bandwidth	$A_v = 1$		1		MHz
Output voltage swing	$R_L = 10K$ over temp.	1.5		V+ –1.5	V
Output short circuit current			50		mA

NOTE

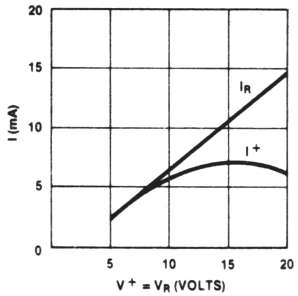
Rating applies to ambient temperatures up to 70°C. Above 70°C derate linearly at 7.6mW/°C for the plastic package and 7.3mW/°C for the cerdip package.

TYPICAL PERFORMANCE CHARACTERISTICS

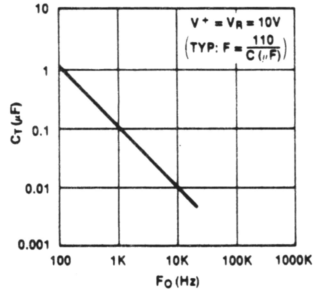
I_R AND I^+ vs TEMPERATURE



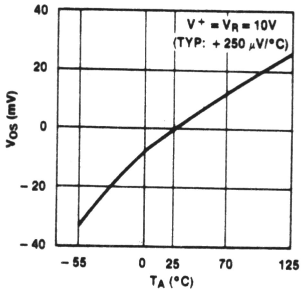
I_R AND I^+ vs VOLTAGE



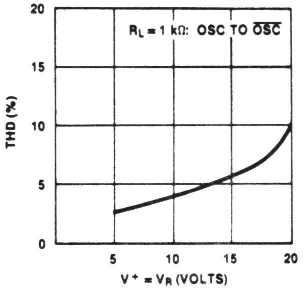
F_O vs C_T



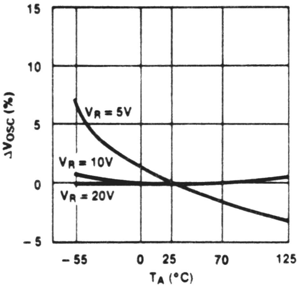
DEMODULATOR OFFSET
vs TEMPERATURE
(NORMALIZED TO 25°C)



DISTORTION OF SINE WAVE
vs REFERENCE VOLTAGE

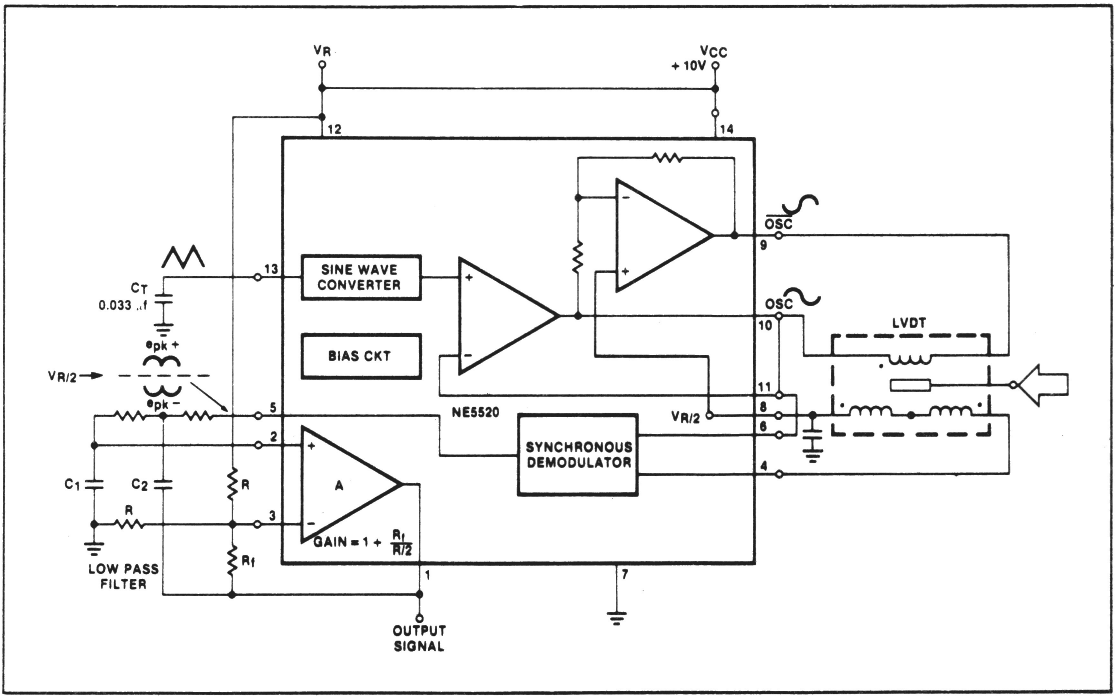


OSCILLATOR AMPLITUDE VARIATION
WITH TEMPERATURE



LVDT SIGNAL CONDITIONER NE5520

TYPICAL SINGLE SUPPLY LVDT CIRCUIT


VR
VCC
+10V
12
14
OSC
9
OSC
10
LVDT
13
SINE WAVE CONVERTER
BIAS CKT
CT
0.033 µf
epk +
VR/2
epk −
5
2
3
11
8
6
4
NE5520
VR/2
SYNCHRONOUS DEMODULATOR
A
GAIN = 1 + Rf/(R/2)
C1
C2
R
R
Rf
LOW PASS FILTER
1
7
OUTPUT SIGNAL

For additional information, refer to the Applications Section.

SAMPLE AND HOLD CIRCUITS—SYMBOLS AND DEFINITIONS

Acquisition Time

The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

Aperture Delay Time

The time elapsed from the hold command to the opening of the switch.

Aperture Jitter

Also called "aperture uncertainty time", it's the time variation or uncertainty with which the switch opens, or the time variation in aperture delay.

Aperture Time

The delay required between "hold" command and an input analog transition, so that the transition does not affect the hold output.

Dynamic Sampling Error

The error introduced into the held output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

Effective Aperture Delay

The time difference between the hold command and the time at which the input signal is at the held voltage.

Figure Of Merit

The ratio of the available charging current during sample mode to the leakage current during hold mode.

Gain Error

The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

Hold-Mode Droop

The output voltage change per unit of time while in hold. Commonly specified in V/s, μV/μs or other convenient units.

Hold-Mode Feed Through

This percentage of an input sinusoidal signal that is measured at the output of a sample-hold when it's in hold mode.

Hold Settling Time

The time required for the output to settle within 1mV of final value after the "hold" logic command.

Hold Step

The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (dc) analog input voltage. Logic swing is 5V.

Sample-To-Hold Offset Error

The difference in output voltage between the time the switch starts to open, and the time when the output has settled completely. It is caused by charge being transferred to the hold capacitor switch as it opens.

Slew Rate

The fastest rate at which the sample & hold output can change (specified in V/μs).

Threshold

Level shall be defined as that level which causes the switch control to change state.

MONOLITHIC SAMPLE AND HOLD CIRCUITS

LF198/LF298/LF398

DESCRIPTION

The Signetics LF198/LF298/LF398 are monolithic sample and hold circuits which utilize high-voltage Ion Implant JFET technology to obtain ultra-high DC accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, DC gain accuracy is 0.002% typical and acquisition time is as low as 6μs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin and does not degrade input offset drift. The wide bandwidth allows the LF198 to be included inside the feedback loop of 1MHz op amps without having stability problems. Input impedance of $10^{10}\Omega$ allows high source impedances to be used without degrading accuracy.

P-channel junction FET's are combined with bipolar devices in the output amplifier to give droop rates as low as 5mV/min with a 1μF hold capacitor. The JFET's have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feed-through from input to output in the hold mode even for input signals equal to the supply voltages.

Logic inputs are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS. Differential threshold is 1.4V. The LF198/LF298/LF398 will operate from ±5V to ±18V supplies. They are available in an 8-lead TO-5 package, or an 8-pin plastic DIP.

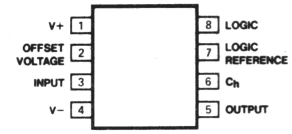
FEATURES

- **Operates from ±5V to ±18V supplies**
- **Less than 10μs acquisition time**
- **TTL, PMOS, CMOS compatible logic input**
- **0.5mV typical hold step at $C_h = 0.01\mu F$**
- **Low input offset**
- **0.002% gain accuracy**
- **Low output noise in hold mode**
- **Input characteristics do not change during hold mode**
- **High supply rejection ratio in sample or hold**
- **Wide bandwidth**

APPLICATIONS

- **The LF198/LF298/LF398 are ideally suited for a wide variety of sample and hold applications including data acquisition, analog-to-digital conversion, synchronous demodulation, and automatic test setup.**

F,N PACKAGE

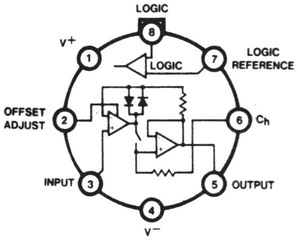

V+ 1
OFFSET VOLTAGE 2
INPUT 3
V− 4
8 LOGIC
7 LOGIC REFERENCE
6 Ch
5 OUTPUT

TOP VIEW

ORDER NUMBERS

LF198F, LF298F, LF398F
LF198N, LF298N, LF398N

H PACKAGE

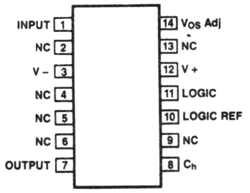

LOGIC
8
V+
1
LOGIC
7
LOGIC REFERENCE
OFFSET ADJUST
2
6
Ch
INPUT
3
5
OUTPUT
4
V−

TOP VIEW

ORDER NUMBERS

LF198H, LF298H, LF398H

D³ PACKAGE


INPUT 1
NC 2
V− 3
NC 4
NC 5
NC 6
OUTPUT 7
14 VOS Adj
13 NC
12 V+
11 LOGIC
10 LOGIC REF
9 NC
8 Ch

TOP VIEW

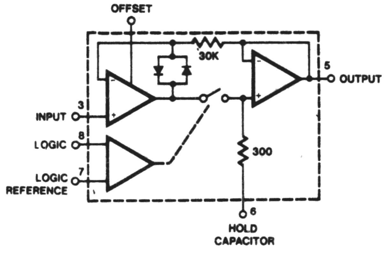
ORDER NUMBER

LF398D

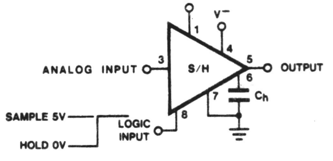
NOTES:

1. SOL - Released in Large SO package only.
2. SOL and non-standard pinout.
3. SO and non-standard pinouts.

FUNCTIONAL DIAGRAM


OFFSET
30K
5
OUTPUT
3
INPUT
8
LOGIC
7
LOGIC REFERENCE
300
6
HOLD CAPACITOR

TYPICAL APPLICATIONS


V+
V−
1
4
ANALOG INPUT
3
S/H
5
OUTPUT
6
7
Ch
SAMPLE 5V
HOLD 0V
LOGIC INPUT
8

MONOLITHIC SAMPLE AND HOLD CIRCUITS

LF198/LF298/LF398

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	± 18	V
Power dissipation (package limitation)[1]	500	mW
Operating ambient temperature range		
LF198	−55 to +125	°C
LF298	−25 to +85	°C
LF398	0 to +70	°C
Storage temperature range	−65 to +150	°C
Input voltage	Equal to supply voltage	
Logic to logic reference differential voltage[2]	+7, −30	V
Output short circuit duration	Indefinite	
Hold capacitor short circuit duration	10	sec
Lead temperature (soldering, 10sec)	300	°C

DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S = \pm 15V$, $T_j = 25°C$, $-11.5V \le V_{IN} \le +11.5V$, $C_h = 0.01\mu F$, and $R_L = 10k\Omega$. Logic reference voltage = OV and logic voltage = 2.5V.

PARAMETER	TEST CONDITIONS	LF198/LF298			LF398			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage[6]	$T_j = 25°C$		1	3 5		2	7 10	mV mV
Input bias current[6]	$T_j = 25°C$ Full temperature range		5	25 75		10	50 100	nA nA
Input impedance	$T_j = 25°C$		10^{10}			10^{10}		Ω
Gain error	$T_j = 25°C$, $R_L = 10K$ Full temperature range		0.002	0.005 0.02		0.004	0.01 0.02	% %
Feedthrough attenuation ratio at 1kHz	$T_j = 25°C$, $C_h = 0.01\mu F$	86	96		80	90		dB
Output impedance	$T_j = 25°C$, "HOLD" mode Full temperature range		0.5	2 4		0.5	4 6	Ω Ω
"HOLD" step[4]	$T_j = 25°C$, $C_h = 0.01\mu F$, $V_{OUT} = 0$		0.5	2.0		1.0	2.5	mV
Supply current[6]	$T_j \le 25°C$		4.5	5.5		4.5	6.5	mA
Logic and logic reference input current	$T_j = 25°C$		2	10		2	10	μA
Leakage current into hold capacitor[6]	$T_j = 25°C$[5], Hold mode		30	100		30	200	pA
Acquisition time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000pF$ $C_h = 0.01\mu F$		4 20			4 20		μs μs
Hold capacitor charging current	$V_{IN} - V_{OUT} = 2V$		5			5		mA
Supply voltage rejection ratio	$V_{OUT} = 0$	80	110		80	110		dB
Differential logic threshold	$T_j = 25°C$	0.8	1.4	2.4	0.8	1.4	2.4	V

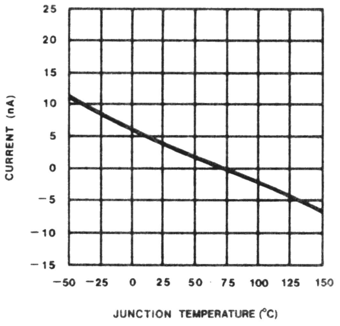
NOTES

1. The maximum junction temperature of the LF398 is 150°C. When operating at elevated ambient temperature, the TO-5 and plastic DIP packages must be derated based on a thermal resistance (θjA) of 150°C/W.
2. Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.
3. Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S = \pm 15V$, $T_j = 25°C$, $-11.5V \le V_{IN} \le +11.5V$, $C_h = 0.01\mu F$, and $R_L = 10k$. Logic reference voltage = OV and logic voltage = 2.5V.
4. Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01μF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.
5. Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.
6. The parameters guaranteed over a supply voltage of ±5 to ±18V.

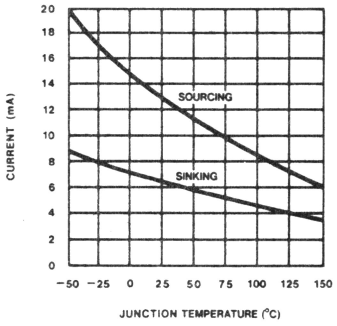
MONOLITHIC SAMPLE AND HOLD CIRCUITS LF198/LF298/LF398

TYPICAL DC PERFORMANCE CHARACTERISTICS

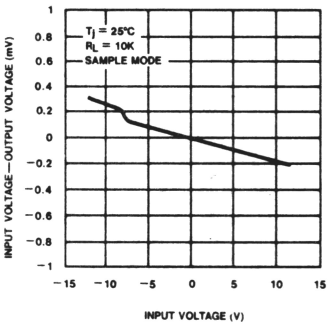
INPUT BIAS CURRENT



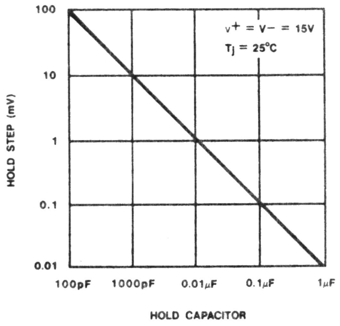
OUTPUT SHORT CIRCUIT CURRENT



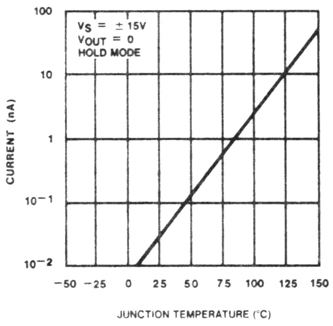
GAIN ERROR



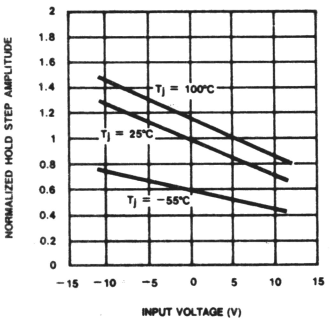
HOLD STEP



LEAKAGE CURRENT INTO HOLD CAPACITOR

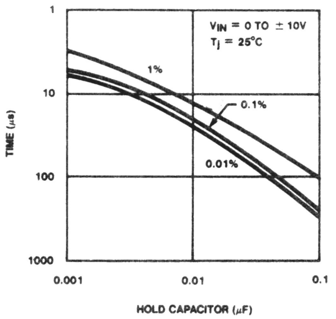


HOLD STEP INPUT VOLTAGE

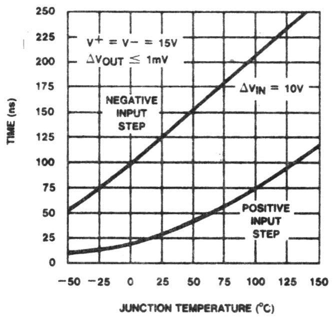


TYPICAL AC PERFORMANCE CHARACTERISTICS

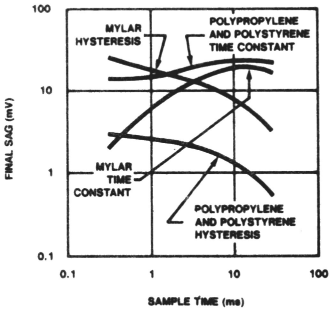
ACQUISITION TIME



APERTURE TIME

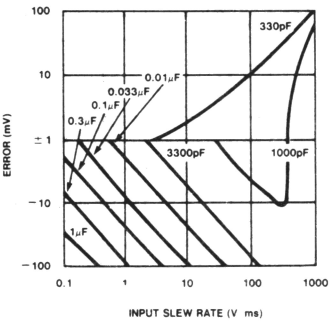


CAPACITOR HYSTERESIS

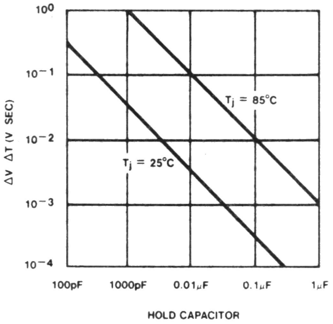


TYPICAL AC PERFORMANCE CHARACTERISTICS (cont'd)

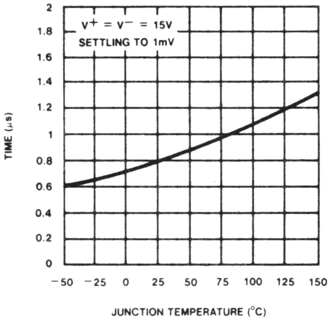
DYNAMIC SAMPLING ERROR



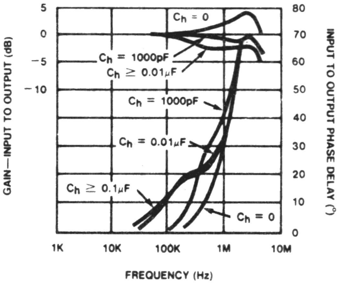
OUTPUT DROOP RATE



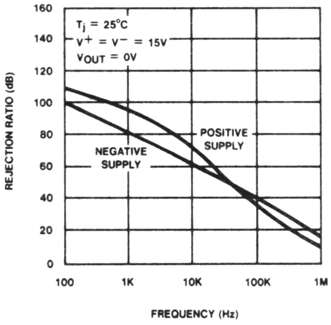
"HOLD" SETTLING TIME



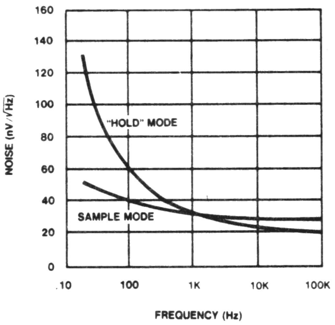
PHASE AND GAIN
(INPUT TO OUTPUT, SMALL SIGNAL)



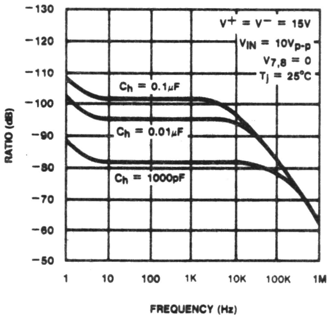
POWER SUPPLY REJECTION



OUTPUT NOISE



FEEDTHROUGH REJECTION RATIO
(HOLD MODE)



SAMPLE AND HOLD AMPLIFIER

SE/NE5537

DESCRIPTION

The NE5537 monolithic Sample and Hold amplifier combines the best features of ion implanted JFET's with bipolar devices to obtain high accuracy, fast acquisition time, and low droop rate. This device is pin compatible with the LF198, and features superior performance in droop rate and output drive capability. The circuit shown in Figure 1 contains two operational amplifiers which function as a unity gain amplifier in the Sample mode. The first amplifier has bipolar input transistors which gives the system a low offset voltage. The second amplifier has JFET input transistors to achieve low leakage current from the hold capacitor. A unique circuit design for leakage current cancellation using current mirrors gives the NE5537 a low droop rate at higher temperature. The output stage has the capability to drive a 2KΩ load. The logic input is compatible with TTL, PMOS or CMOS logic. The differential logic threshold is 1.4V with the Sample mode occurring when the logic input is high. It is available in 8-lead TO-5 and 8-pin plastic DIP packages.

FEATURES

- Operates from ± 5V to ± 18V supplies
- Hold leakage current 6pA @ T_j25°C
- Less than 4μs acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5mV typical hold step at $C_h = 0.01\mu F$
- Low input offset: 1MV (typical)
- 0.002% gain accuracy with $R_L = 2k\Omega$
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	± 18	V
Power dissipation (package limitation)[1]	500	mW
Operating ambient temperature range		
SE5537	−55 to +125	°C
NE5537	0 to +70	°C
Storage temperature range	−65 to +150	°C
Input voltage	Equal to supply voltage	
Logic to logic reference differential voltage[2]	+7, −30	V
Output short circuit duration	Indefinite	
Hold capacitor short circuit duration	10	sec
Lead temperature (soldering, 10sec)	300	°C

NOTES

1. The maximum junction temperature of the SE5537 is 150°C and for the NE5537 is 100°C. When operating at elevated ambient temperature, the TO-5 and plastic DIP packages must be derated based on a thermal resistance (θja) of 150°C/W.
2. Although the differential voltage may not exceed the limits given, the common mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

BLOCK DIAGRAM

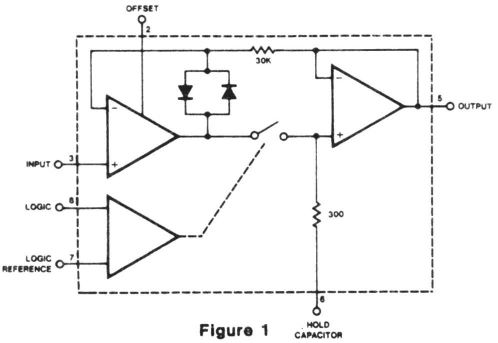
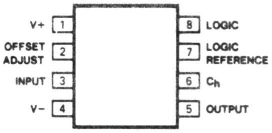


Figure 1

PIN CONFIGURATION

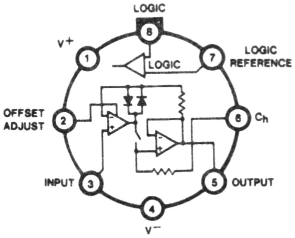
N PACKAGE



TOP VIEW

ORDER NUMBERS
NE/SE5537N

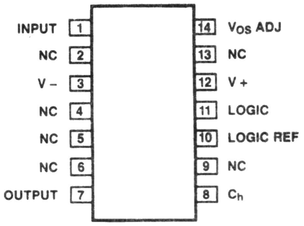
H PACKAGE
Metal Can Package



TOP VIEW

ORDER NUMBERS
NE/SE5537-H

D^3 PACKAGE



TOP VIEW

ORDER NUMBER
NE5537D

NOTES:
1. SOL - Released in Large SO package only.
2. SOL and non-standard pinout.
3. SO and non-standard pinouts.

ELECTRICAL CHARACTERISTICS[3]

PARAMETER	TEST CONDITIONS	SE5537			NE5537			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage[6]	T_j = 25°C Full temperature range		1	3 5		2	7 10	mV mV
Input bias current[6]	T_j = 25°C Full temperature range		5	25 75		10	50 100	nA nA
Input impedance	T_j = 25°C		10^{10}			10^{10}		Ω
Gain error	T_j = 25°C, −10V ≤ V_{IN} ≤ 10V, R_L = 2K −11.5V ≤ V_{IN} ≤ 11.5V, R_L = 10K Full temperature range		0.002	0.007 0.02		0.004	0.01 0.02	% %
Feedthrough attenuation ratio at 1kHz	T_j = 25°C, C_h = 0.01μF	86	96		80	90		dB
Output impedance	T_j = 25°C, "HOLD" mode full temperature range		0.5	2 4		0.5	4 6	Ω
"HOLD" Step[4]	T_j = 25°C, C_h = 0.01μF, V_{OUT} = 0		0.5	2.0		1.0	2.5	mV
Supply current[6]	T_j=25°C		4.5	6.5		4.5	7.5	mA
Logic and logic reference input current	T_j = 25°C		2	10		2	10	μA
Leakage current into hold capacitor[6]	T_j = 25°C hold mode[5]		6	50		6	100	pA
Acquisition time to 0.1%	V_{OUT} = 10V, C_h = 1000pF C_h = 0.01μf		4 20			4 20		μs μs
Hold capacitor charging current	$V_{IN} - V_{OUT}$ = 2V		5			5		mA
Supply voltage rejection ratio	V_{OUT} = 0	80	110		80	110		dB
Differential logic threshold	T_j = 25°C	0.8	1.4	2.4	0.8	1.4	2.4	V

NOTES

[3] Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, V_S = ± 15V, T_j = 25°C, −11.5V ≤ V_{IN} ≤ 11.5V, C_h = 0.01μF, and R_L = 2kΩ. Logic reference voltage = 0V and logic voltage = 2.5V.

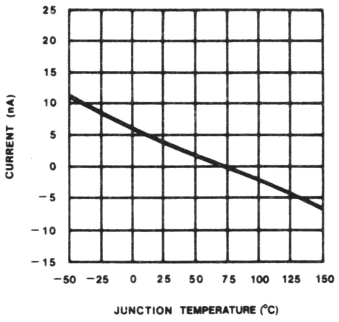
[4] Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01F hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.

[5] Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.

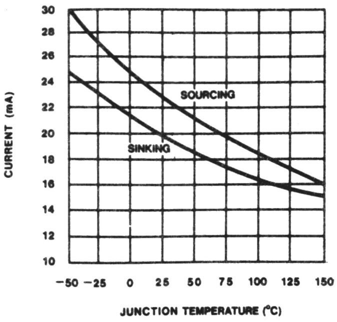
[6] These parameters guaranteed over a supply voltage range of ±5 to ±18V.

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT BIAS CURRENT

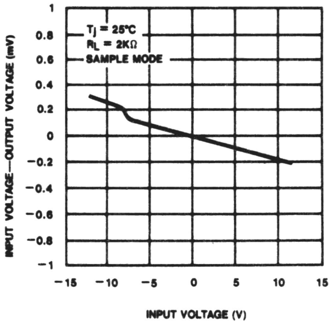


OUTPUT SHORT CIRCUIT CURRENT

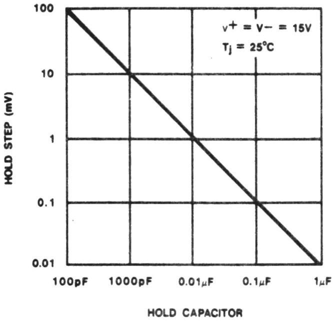


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd.)

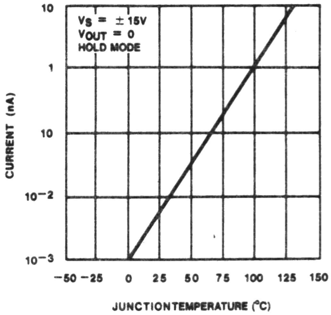
GAIN ERROR



HOLD STEP

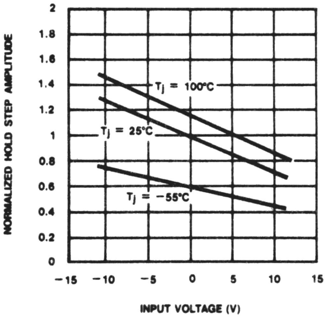


LEAKAGE CURRENT INTO HOLD CAPACITOR

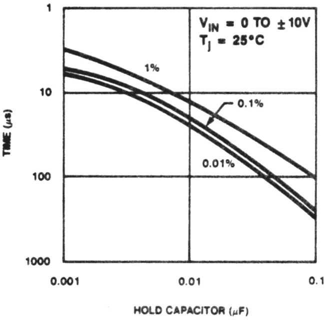


4

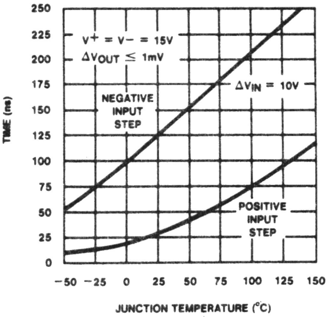
HOLD STEP vs INPUT VOLTAGE



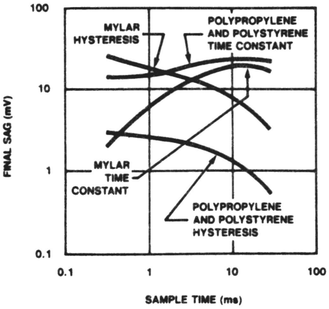
ACQUISITION TIME



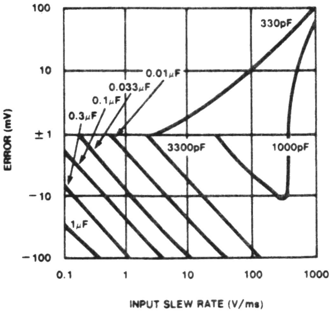
APERTURE TIME



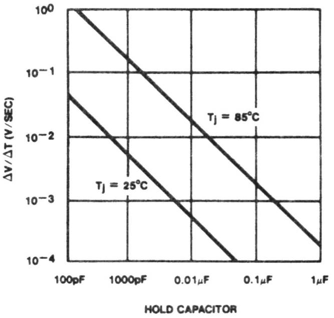
CAPACITOR HYSTERESIS



DYNAMIC SAMPLING ERROR

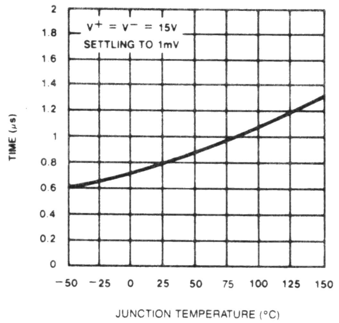


OUTPUT DROOP RATE

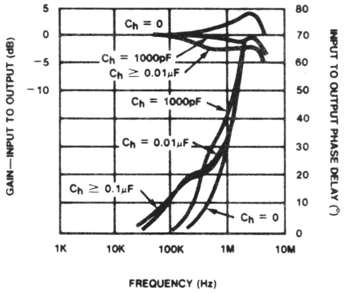


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

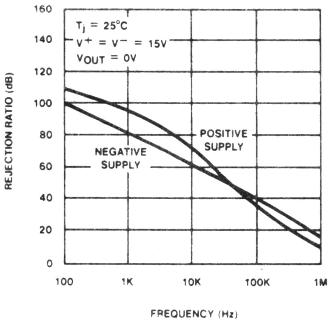
"HOLD" SETTLING TIME



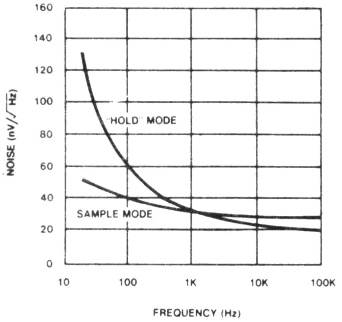
PHASE AND GAIN (INPUT TO OUTPUT, SMALL SIGNAL)



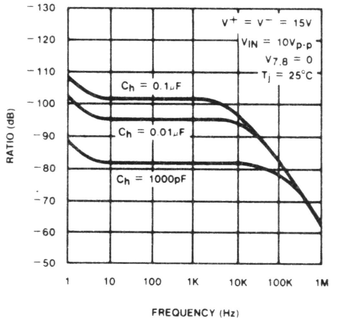
POWER SUPPLY REJECTION



OUTPUT NOISE



FEEDTHROUGH REJECTION RATIO (HOLD MODE)



SAMPLE AND HOLD

INTRODUCTION

For many years designers have used the sample and hold (or track and hold) to operate on analog information in a time frame which is expedient.

By sampling a segment of the information and holding it until the proper timing for converting to some form of control signal or readout allows the designer certain freedom in performing predetermined manipulative functions. Therefore, the sample and hold can be defined as a "selective analog memory cell".

The memory is volatile and will also decay with time.

When using the sample and hold method for evaluating signal information, the designer is given the added feature of eliminating outside noise elements. With the analog to digital converter products available today the "dc memory" of the sample and hold can be easily converted to digital format and further incorporated into microprocessor based systems.

Parametric evaluation of the sample and hold will be discussed in the following paragraphs.

DEFINITION OF TERMS

ACQUISITION TIME: The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

APERTURE DELAY TIME: The time elapsed from the hold command to the opening of the switch.

APERTURE JITTER: Also called "aperture uncertainty time", it's the time variation or uncertainty with which the switch opens, or the time variation in aperture delay.

APERTURE TIME: The delay required between "hold" command and an input analog transition, so that the transition does not affect the held output.

BANDWIDTH: The frequency at which the gain is down 3dB from its dc value. It's measured in sample (track) mode with a small-signal sine wave that doesn't exceed the slew rate limit.

EFFECTIVE APERTURE DELAY: The time difference between the hold command and the time at which the input signal is at the held voltage.

FIGURE OF MERIT: The ratio of the available charging current during sample mode to the leakage current during hold mode.

HOLD-MODE DROOP: The output voltage change per unit of time while in hold. Commonly specified in V/s, μV/μs or other convenient units.

HOLD-MODE FEEDTHROUGH: The percentage of an input sinusoidal signal that is measured at the output of a sample-hold when it's in hold mode.

HOLD SETTLING TIME: The time required for the output to settle within 1mV of final value after the "hold" logic command.

SAMPLE-TO-HOLD OFFSET ERROR: The difference in output voltage between the time the switch starts to open, and the time when the output has settled completely. It is caused by charge being transferred to the hold capacitor switch as it opens.

SLEW RATE: The fastest rate at which the sample & hold output can change (specified in V/μs).

HOLD STEP: The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (dc) analog input voltage. Logic swing is 5V.

SAMPLE AND HOLD AMPLIFIER

SE/NE5537

DYNAMIC SAMPLING ERROR: The error introduced into the held output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

GAIN ERROR: The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

THRESHOLD: Level shall be defined as that level which causes the switch control to change state.

BASIC BLOCK DIAGRAM

The basic circuit concept of the sample and hold circuit incorporates the use of two (2) operational amplifiers and a switch control mechanism (which determines sample, hold or track conditions). Reference figure 1.

The block diagram of the NE5537 is a closed loop non-inverting unity gain sample and hold system. The input buffer amplifier supplies the current necessary to charge the hold capacitor, while the output buffer amplifier closes the loop such that the output voltage is identical to the input voltage (with consideration for input offset voltage, offset current, and temperature variations which are common to *all* sample and hold circuits, be they monolithic, hybrid or modular).

When the sampling switch is open (in the hold mode) the clamping diodes close the loop around the input amplifier to keep it from being overdriven into saturation.

The switch control is driven by external logic levels via a timing sequence remote from the sample and hold device. Reference figure 2. The switch control has a floating reference (pin 7), referred to as the logic reference which makes the sample and hold device compatible to several types of external logic signals (TTL, PMOS, & CMOS). The switching device operates at a threshold level of 1.4V.

The switch mechanism is on (sampling an information stream) when the logic level is high (pin 8 is 1.4 volts higher than pin 7) and presents a load of 5 microamperes to the input logic signal. The analog sampled signal is amplified, stored (in the external holding capacitor), and buffered. At the end of the sampling period the internal switch mechanism turns off (switch opens) and the "stored analog memory" information on the external capacitor (pin 6) is loaded down by an operational amplifier connected in the unity gain non-inverting configuration. This amplifier, whose input impedance is effectively:

$$R = R_{IN}(A_{OL})/(1 + 1/A)$$

where R = Effective input impedance
R_{IN} = Open loop input impedance
A_{OL} = Open loop gain
A = AC loop gain

Therefore, the higher the open loop gain of the second operational amplifier, the larger the effective loading on the capacitor. The larger the load, the lower the "leakage" current and the better the droop characteristics.

In actuality the amplifiers are designed with special leakage current cancellation circuits along with FET input devices. The leakage current cancellation circuits give better high temperature operation (remember that the FET amplifiers double in required bias current for every 10 degree increase in junction temperature).

Sampling time for the NE5537 is less than 10μsec, (measured to 0.1% of input signal). Leakage current is 6pA at a rate output load of 2kΩ.

BASIC APPLICATIONS

Multiplying DAC

As depicted in the block diagram of figure 3, the sample and hold circuit is used to supply a "variable" reference to the digital to analog converter. As the input reference varies, the output will change in accordance with equation 1, shown in figure 3.

Varying the input signal reference level can aid the system in performing both compression and expansion operations. The multiplying DAC's used are the Signetics SE/NE 5008; however, if the rate of change of the reference variation is kept slow enough a microprocessor compatible DAC can be incorporated, such as the NE5018 or the NE5020.

DATA ACQUISITION SYSTEMS

As mentioned earlier, the designer may wish to operate on several different segments of an "analog" signal; however he is limited by the fact that only one analog to digital converter channel is available to him. Figure 4 shows the means by which a multiplexing system may be accomplished.

APPLICATION HINTS

Hold Capacitor

A significant source of error in an accurate sample and hold circuit is dielectric absorption in the hold capacitor. A mylar cap, for instance, may "sag back" up to 0.2% after a quick change in voltage. A long "soak" time is required before the circuit can be put back into the hold mode with this type of capacitor. Dielectrics with very low hysteresis are polystyrene, polypropylene, and Teflon. Other types such as mica and polycarbonate are not nearly as good. Ceramic is unusable with >1% hysteresis. The advantage of polypropylene over polystyrene is that it extends the maximum ambient temperature from 85°C to 100°C. The hysteresis relaxation time constant in polystyrene, for instance, is 10-50ms. If A-to-D conversion can be made within 1ms, hysteresis error will be reduced by a factor of ten.

DC Zeroing

DC Zeroing is accomplished by connecting the offset adjust pin to the wiper of a 1kΩ potentiometer which has one end tied to V^+ and the other end tied through a resistor to ground. The resistor should be selected to give ≃0.6mA through the 1KΩ potentiometer.

Sampling Dynamic Signals

Sampling errors due to moving (changing) input signals are of significant concern to designers employing sample and hold circuits. There exist finite phase delays through the sample and hold circuit causing an input-output phase differential for moving signals. In addition, the series protection resistor (300Ω to pin 6 of the NE5537) will add an RC time constant, over and above the slew rate limitation of the input buffer/current drive amplifier. This means that at the moment the "hold" command arrives, the hold capacitor voltage may be somewhat different than the actual analog input. The effect of these delays is opposite to the effect created by delays in the logic which switches the circuit from sample to hold. For example, consider an analog input of 20 Vp-p at 10kHz. Maximum dV/dt is 0.6V/μs. With no analog phase delay and 100ns logic delay, one could expect up to (0.1μs) (0.6V/μs) = 60mV error if the "hold" signal arrived near maximum dV/dt of the input. A positive going input would give a ±60mV error. Now assume a 1MHz (3dB) bandwidth for the overall analog loop. This generates a phase delay of 160ns. If the hold capacitor sees this exact delay, then error due to analog delay will be (0.16μs) (0.6V/μs) = −96mV (analog) for a total of −36mV. To add to the confusion, analog delay is proportional to hold capacitor value while digital delay remains constant. A family of curves (dynamic sampling error) is included to help estimate errors.

SAMPLE AND HOLD AMPLIFIER

A curve labeled *Aperture Time* has been included for sampling conditions where the input is steady during the sampling period, but may experience a sudden change nearly coincident with the "hold" command. This curve is based on a 1mV error fed into the output.

A second curve, *Hold Settling Time* indicates the time required for the output to settle to 1mV after the "hold" command.

Digital Feedthrough

Fast rise time logic signals can cause hold errors by feeding externally into the analog input at the same time the amplifier is put into the hold mode. To minimize this problem, board layout should keep logic lines as far as possible from the analog input. Grounded guarding traces may also be used around the input line, especially if it is driven from a high impedance source. Reducing high amplitude logic signals to 2.5V will also help.

Logic signals also couple to the hold capacitor. This hold capacitor should be guarded by a P.C. card trace connected to the sample-and-hold output. This will also minimize board leakage.

SPECIAL NOTES

1. Not all definitions herein defined are measured parametrically for the NE5537, but are legitimate terms used in sample and hold systems.
2. Reference should be made to Design Engineering, volumes 23 (Nov. 8, 1978), 25 (Dec. 6, 1978) and 26 (Dec. 20, 1978) for articles written by Eugene Zuch of Datel Systems, Inc. for a further discussion of sample and hold circuits.
3. Reference also made to National Semiconductor Corporation's Special Functions Data Book (1976).

TYPICAL APPLICATIONS

TYPICAL CONNECTION

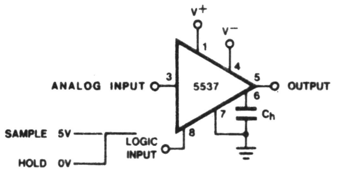
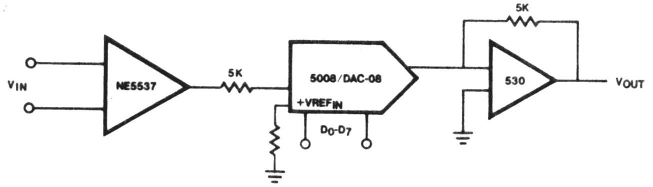

V+
V−
1
4
3
5
6
7
8
ANALOG INPUT
5537
OUTPUT
Ch
SAMPLE 5V
HOLD 0V
LOGIC INPUT

Figure 2

MULTIPLYING DAC APPLICATION


VIN
NE5537
5K
5008/DAC-08
+VREFIN
D0-D7
5K
530
VOUT

$$V_{OUT} = V_{IN} \times \frac{1}{256} \left\{ 2^0 D_0 + 2^1 D_1 + \quad 2^7 D_7 \right\} \quad \text{EQUATION 1}$$

Figure 3

ANALOG DATA MULTIPLEXING

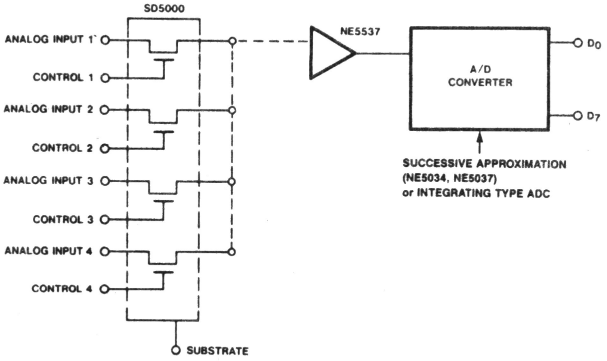

SD5000
ANALOG INPUT 1
CONTROL 1
ANALOG INPUT 2
CONTROL 2
ANALOG INPUT 3
CONTROL 3
ANALOG INPUT 4
CONTROL 4
SUBSTRATE
NE5537
A/D CONVERTER
D0
D7
SUCCESSIVE APPROXIMATION (NE5034, NE5037) or INTEGRATING TYPE ADC

Figure 4

Section 5
Communication

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SECTION 5 — COMMUNICATION

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COMPANDOR NE570/571/SA571

DESCRIPTION

The NE570/571 is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expandor. Each channel has a full wave rectifier to detect the average value of the signal; a linerarized, temperature compensated variable gain cell; and an operational amplifier.

The NE570/571 is well suited for use in cellular radio and radio communications systems, modems, telephone, and satellite broadcast/receive audio sytems.

FEATURES

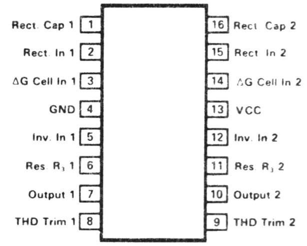
- **Complete compressor and expandor in 1 IC**
- **Temperature compensated**
- **Greater than 110dB dynamic range**
- **Operates down to 6Vdc**
- **System levels adjustable with external components**
- **Distortion may be trimmed out**

APPLICATIONS

- **Cellular radio**
- **Telephone trunk compandor—570**
- **Telephone subscriber compandor—571**
- **High level limiter**
- **Low level expandor—noise gate**
- **Dynamic noise reduction systems**
- **Voltage controlled amplifier**
- **Dynamic filters**

PIN CONFIGURATION

D^1, F, N PACKAGE



Order Part No.

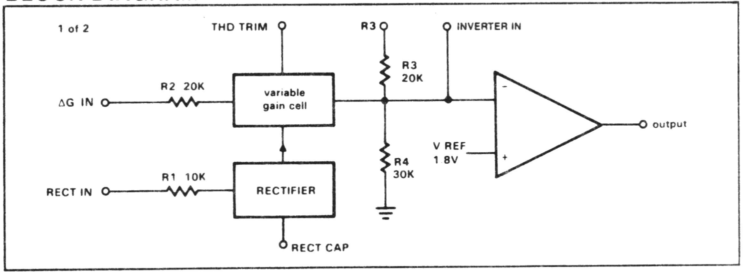
NE570 F,N	**NE571 F,N**
SA571 F,N	**NE571D¹**

NOTES:
1. SOL - Released in Large SO package only.
2. SOL and non-standard pinout.
3. SO and non-standard pinouts.

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
	Positive supply		Vdc
	570	24	
	571	18	
T_A	Operating temperature range		
	NE	0 to 70	°C
	SA	-40 to +85	°C
P_D	Power dissipation	400	mW

BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The NE570/571 compandor building blocks, as shown in the block diagram, are a full wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

The full wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at V_{REF}. The rectified current is averaged on an external filter capacitor tied to the C_{RECT} terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively coupled voltage inputs as shown in the following equation. Note that for capacitively coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than .1μA.

$$G \propto \frac{|V_{IN} - V_{REF}| \text{ avg.}}{R_1}$$

or

$$G \propto \frac{|V_{IN}| \text{ avg.}}{R_1}$$

The speed with which gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expandor or compressor application, this would lead to third harmonic distortion, so there is a tradeoff to be made between fast attack and decay times, and distortion. For step changes in amplitude, the change in gain with time is shown by this equation.

$$G(t) = (G_{initial} - G_{final})\ e^{-t/\tau}$$

$$+ G_{final};\ \tau = 10K \times C_{RECT}$$

The variable gain cell is a current in, current out device with the ratio I_{OUT}/I_{IN} controlled by the rectifier. I_{IN} is the current which flows from the ΔG input to an internal summing node biased at V_{REF}. The following equation applies for capacitively coupled inputs. The output current, I_{OUT}, is fed to the summing node of the op amp.

$$I_{IN} = \frac{V_{IN} - V_{REF}}{R_2} = \frac{V_{IN}}{R_2}$$

A compensation scheme built into the ΔG cell compensates for temperature, and cancels out odd harmonic distortion. The only distortion which remains is even harmonics, and they exist only because of internal offset voltages. The THD trim terminal provides a means for nulling the internal offsets for low distortion operation.

The operational amplifier (which is internally compensated) has the non-inverting input tied to V_{REF}, and the inverting input connected to the ΔG cell output as well as brought out externally. A resistor, R_3, is brought out from the summing node and allows compressor or expandor gain to be determined only by internal components.

Note:
1. Supplied only in large SO (Small Outline) package.

COMPANDOR

NE570/571/SA571

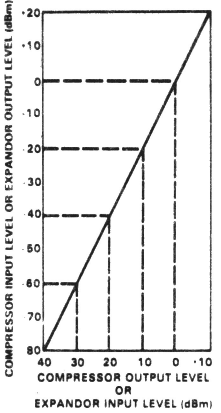
The output stage is capable of ±20mA output current. This allows a +13dBm (3.5V rms) output into a 300Ω load which, with a series resistor and proper transformer, can result in +13dBm with a 600Ω output impedance.

A band gap reference provides the reference voltage for all summing nodes, a regulated supply voltage for the rectifier and ΔG cell, and a bias current for the ΔG cell. The low tempco of this type of reference provides very stable biasing over a wide temperature range.

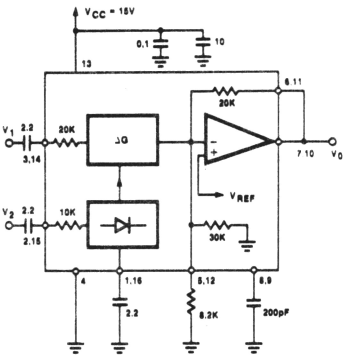
The typical performance characteristics illustration shows the basic input-output transfer curve for basic compressor or expandor circuits.

TYPICAL PERFORMANCE CHARACTERISTICS

BASIC INPUT-OUTPUT TRANSFER CURVE



TYPICAL TEST CIRCUIT



DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 15$ Except where indicated, the 571 specifications are identical to 570

PARAMETER	TEST CONDITIONS	NE570			NE/SA571[5]			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{CC} Supply voltage		6		24	6		18	V
I_{CC} Supply current	No signal		3.2	4.8		3.2	4.8	mA
Output current capability		±20			± 20			mA
Output slew rate			±.5			± .5		V/us
Gain cell distortion[2]	Untrimmed		.3	1.0		.5	2.0	%
	Trimmed		05			.1		
Resistor tolerance			±5	±15		± 5	± 15	%
Internal reference voltage		1.7	1.8	1.9	1.65	1.8	1.95	V
Output dc shift[3]	Untrimmed		±20	±50		±30	±100	mV
Expandor output noise	No signal, 15Hz-20kHz[1]		20	45		20	60	μV
			-15					dBRNC
Unity gain level		-1	0	+1	-1.5	0	+1.5	dBm
Gain change[2,4]	-40°C < T < 70°C		±.1			±.1		dB
	0°C < T < 70°C		±.1	±.2		±.1	±.4	
Reference drift[4]	-40°C < T < 70°C		+2, -25	+10, -40		+2, -25	+20, -50	mV
	0°C < T < 70°C		±5	±10		±5	±20	
Resistor drift[4]	-40°C < T < 70°C		+8,-0					%
	0°C < T < 70°C		+1,-0					
Tracking error (measured relative to value at unity gain) equals $[V_O - V_O(\text{unity gain})]$ $dB - V_2 dBm$	Rectifier input, V_2 = $V_2 = +6dBm$, $V_1 = OdB$		±.2					dB
	$V_2 = -30dBm$, $V_1 = OdB$		+.2	-.5,+1		+.2	-1,+1.5	
Channel Separation		60				60		dB

NOTES:

1. Input to V_1 and V_2 grounded.
2. Measured at OdBm, 1kHz.
3. Expandor ac input change from no signal to OdBm.
4. Relative to value at $T_A = 25°C$.
5. Electrical characteristics for the SA571 only are specified over −40 to +85°C temperature range.

COMPANDOR

NE570/571/SA571

INTRODUCTION

Much interest has been expressed in high performance electronic gain control circuits. For non-critical applications, an integrated circuit operational transconductance amplifier can be used, but when high performance is required, one has to resort to complex discrete circuitry with many expensive, well matched components. This paper describes an inexpensive integrated circuit, the NE570 Compandor, which offers a pair of high performance gain control circuits featuring low distortion (<.1%), high signal to noise ratio (90dB), and wide dynamic range (110dB).

CIRCUIT BACKGROUND

The NE570 Compandor was originally designed to satisfy the requirements of the telephone system. When several telephone channels are multiplexed onto a common line, the resulting signal to noise ratio is poor and companding is used to allow a wider dynamic range to be passed through the channel. Figure 1 graphically shows what a compandor can do for the signal to noise ratio of a restricted dynamic range channel. The input level range of +20 to −80dB is shown undergoing a 2 to 1 compression where a 2dB input level change is compressed into a 1dB output level change by the compressor. The original 100dB of dynamic range is thus compressed to a 50dB range for transmission through a resticted dynamic range channel. A complementary expansion on the receiving end restores the original signal levels and reduces the channel noise by as much as 45dB.

The significant circuits in a compressor or expandor are the rectifier and the gain control element. The phone system requires a simple full wave averaging rectifier with good accuracy, since the rectifier accuracy determines the (input) output level tracking accuracy. The gain cell determines the distortion and noise characterics, and the phone system specifications here are very loose. These specs could have been met with a simple operational transconductance multiplier, or OTA, but the gain of an OTA is proportional to temperature and this is very undesirable. Therefore, a linearized transconductance multiplier was designed which is insensitive to temperature and offers low noise and low distortion performance. These features make the circuit useful in audio and data systems as well as in telecommunications systems.

BASIC CIRCUIT HOOKUP AND OPERATION

Figure 2 shows the block diagram of one half of the chip, (there are two identical channels on the I.C.). The full wave averaging rectifier provides a gain control current, I_G, for the variable gain (ΔG) cell. The output of the ΔG cell is a current which is fed to the summing node of the operational amplifier. Resistors are provided to establish circuit gain and set the output dc bias.

RESTRICTED DYNAMIC RANGE CHANNEL

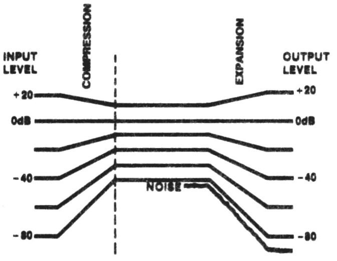


Figure 1

CHIP BLOCK DIAGRAM (1 OF 2 CHANNELS)

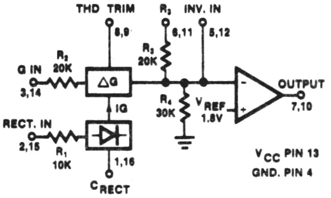


Figure 2

The circuit is intended for use in single power supply systems, so the internal summing nodes must be biased at some voltage above ground. An internal band gap voltage reference provides a very stable, low noise 1.8 volt reference denoted V_{ref}. The non-inverting input of the op amp is tied to V_{ref}, and the summing nodes of the rectifier and ΔG cell (located, at the right, of R_1 and R_2) have the same potential. The THD trim pin is also at the V_{ref} potential.

Figure 3 shows how the circuit is hooked up to realize an expandor. The input signal. V_{in}, is applied to the inputs of both the rectifier and the ΔG cell. When the input signal drops by 6dB, the gain control current will drop by a factor of 2, and so the gain will drop 6dB. The output level at V_{out} will thus drop 12dB, giving us the desired 2 to 1 expansion.

Figure 4 shows the hookup for a compressor. This is essentially an expandor placed in the feedback loop of the op amp. The ΔG cell is set up to provide ac feedback only, so a separate dc feedback loop is provided by the two R_{dc} and C_{dc}. The values of R_{dc} will determine the dc bias at the output of the op amp. The output will bias to:

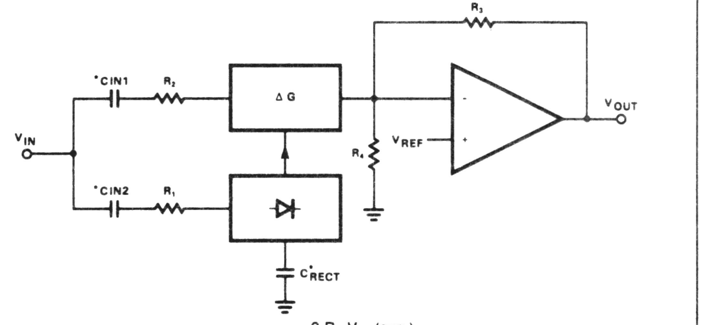
$$V_{out}\,dc = 1 + \frac{R_{dc1}+R_{dc2}}{R_4} V_{ref} = \left(1 + \frac{R_{dc\ tot}}{30K}\right) 1.8V$$

The output of the expandor will bias up to:

$$V_{out}\,dc = 1 + \frac{R_3}{R_4} V_{ref} = \left(1 + \frac{20K}{30K}\right) 1.8V = 3.0V$$

The output will bias to 3.0V when the internal resistors are used. External resistors may be placed in series with R_3, (which will affect the gain), or in parallel with R_4 to raise the dc bias to any desired value.

BASIC EXPANDOR



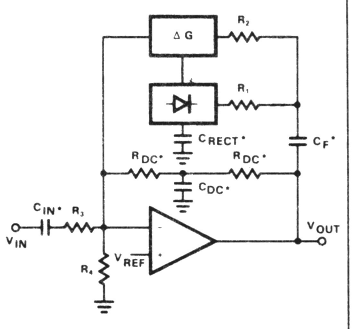
$$\text{GAIN} = \frac{2\,R_3\,V_{IN}\,(\text{avg.})}{R_1\,R_2\,I_B}$$

$I_B = 140\mu A$

*external components

Figure 3

BASIC COMPRESSOR



$$\text{GAIN} = \left(\frac{R_1 R_2 I_B}{2 R_3 V_{IN}\ (\text{avg.})}\right)^{1/2}$$

$I_B = 140\mu A$

*external components

Figure 4

CIRCUIT DETAILS-RECTIFIER

Figure 5 shows the concept behind the full wave averaging rectifier. The input current to the summing node of the op amp, V_{in}/R_1, is supplied by the output of the op amp. If we can mirror the op amp output current into a unipolar current, we will have an ideal rectifier. The output current is averaged by R_5, Cr, which set the averaging time constant, and then mirrored with a gain of 2 to become I_G, the gain control current.

RECTIFIER CONCEPT

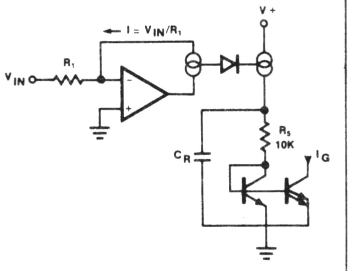
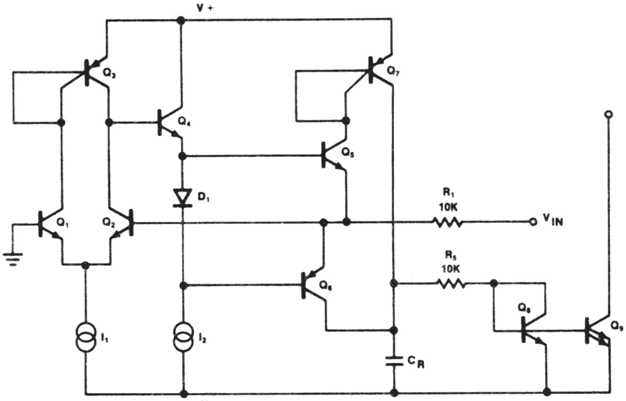


Figure 5

Figure 6 shows the rectifier circuit in more detail. The op amp is a one stage op amp, biased so that only one output device is on at a time. The non-inverting input, (the base of Q_1), which is shown grounded, is actually tied to the internal 1.8V V_{ref}. The inverting input is tied to the op amp output, (the emitters of Q_5 and Q_6), and the input summing resistor R_1. The single diode between the bases of Q_5 and Q_6 assures that only one device is on at a time. To detect the output current of the op amp, we simply use the collector currents of the output devices Q_5 and Q_6. Q_6 will conduct when the input swings positive and Q_5 conducts when the input swings negative. The collector currents will be in error by the α of Q_5 or Q_6 on negative or positive signal swings, respectively. IC's such as this have typical npn β's of 200 and pnp β's of 40. The α's of .995 and .975 will produce errors of .5% on negative swings and 2.5% on positive swings. The 1.5% average of these errors yields a mere .13dB gain error.

SIMPLIFIED RECTIFIER SCHEMATIC



$$I_G = 2\,\frac{V_{IN}\ \text{avg.}}{R1}$$

Figure 6

At very low input signal levels the bias current of Q_2, (typically 50nA), will become significant as it must be supplied by Q_5. Another low level error can be caused by dc coupling into the rectifier. If an offset voltage exists between the V_{in} input pin and the base of Q_2, an error current of V_{os}/R_1 will be generated. A mere 1mv of offset will cause an input current of 100na which will produce twice the error of the input bias current. For highest accuracy, the rectifier should be coupled into capacitively. At high input levels the β of the pnp Q_6 will begin to suffer, and there will be an increasing error until the circuit saturates. Saturation can be avoided by limiting the current into the rectifier input to 250μa. If necessary, an external resistor may be placed in series with R_1 to limit the current to this value. Figure 7 shows the rectifier accuracy vs input level at a frequency of 1kHz.

At very high frequencies, the response of the rectifier will fall off. The rolloff will be more pronounced at lower input levels due to the increasing amount of gain required to switch between Q_5 or Q_6 conducting. The rectifier frequency response for input levels of 0dBm, -20dBm, and -40dBm is shown in Figure 8. The response at all three levels is flat to well above the audio range.

RECTIFIER ACCURACY

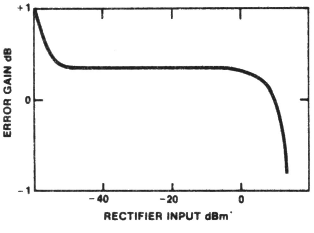


Figure 7

RECTIFIER FREQUENCY RESPONSE vs INPUT LEVEL

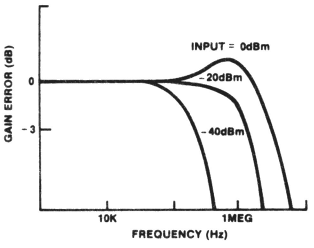


Figure 8

VARIABLE GAIN CELL

Figure 9 is a diagram of the variable gain cell. This is a linerarized two quadrant transconductance multiplier[1,2]. Q_1, Q_2 and the op amp provide a predistorted drive signal for the gain control pair, Q_3, Q_4. The gain is controlled by I_G and a current mirror provides the output current.

The op amp maintains the base and collector of Q_1 at ground potential (V_{ref}) by controlling the base of Q_2. The input current I_{in} ($= V_{in}/R_2$) is thus forced to flow through Q_1 along with the current I_1, so $I_{C1} = I_1 + I_{in}$. Since I_2 has been set at twice the value of I_1, the current through Q_2 is $I_2-(I_1+I_{in}) = I_1-I_{in} = I_{C2}$. The op amp has thus forced a linear current swing between Q_1 and Q_2, by providing the proper drive to the base of Q_2. This drive signal will be linear for small signals, but very non-linear for large signals, since it is compensating for the nonlinearity of the differential pair Q_1, Q_2 under large signal conditions.

The key to the circuit is that this same predistorted drive signal is applied to the gain control pair Q_3 and Q_4. When two differential pairs of transistors have the same signal applied, their collector current ratios will be identical, regardless of the magnitude of the currents. This gives us:

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{C4}}{I_{C3}} = \frac{I_1+I_{in}}{I_1-I_{in}}$$

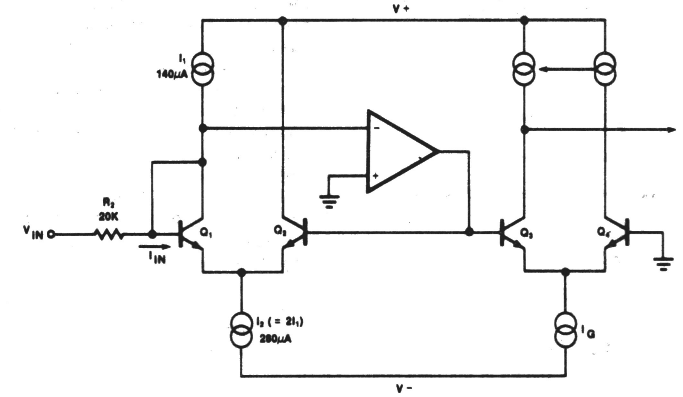
plus the relationships $I_G = I_{C3}+I_{C4}$ and $I_{out} = I_{C4}-I_{C3}$ will yield the multiplier transfer function,

$$I_{out} = \frac{I_G}{I_1} I_{in} = \frac{V_{in}}{R_2} \frac{I_G}{I_1}$$

this equation is linear and temperature insensitive, but it assumes ideal transistors.

If the transistors are not perfectly matched, a parabolic, non-linearity is generated, which results in 2nd harmonic distortion. Figure 10 gives an indication of the maginitude of the distortion caused by a given input level and offset voltage. The distortion is linearly proportional to the magnitude of the offset and the input level. Saturation of the gain cell occurs at a +8dBm level. At a nominal operating level of 0dBm, a 1mv offset will yield .34% of second harmonic distortion. Most circuits are somewhat better than this, which means our overall offsets are typically about $^1/_2$mv. The distortion is not affected by the magnitude of the gain control current, and it does not increase as the gain is changed. This second harmonic distortion could be eliminated by making perfect transistors, but since that would be difficult, we have had to resort to other methods. A trim pin has been provided to allow trimming of the internal offsets to zero, which effectively eliminated second harmonic distortion. Figure 11 shows the simple trim network required.

SIMPLIFIED ΔG CELL SCHEMATIC



$$I_{OUT} = \frac{I_G}{I_1} I_{IN} = \frac{I_G V_{IN}}{I_2 R_2}$$

Figure 9

ΔG CELL DISTORTION vs OFFSET VOLTAGE

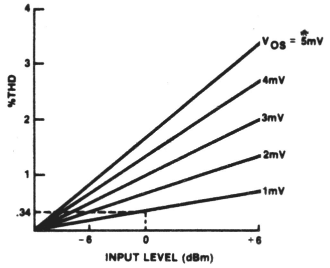


Figure 10

THD TRIM NETWORK

*IF TRIM NETWORK NOT USED, CONNECT CAPACITOR AS SHOWN.

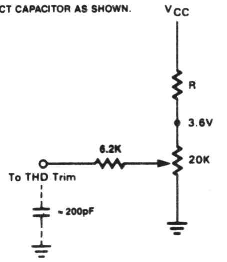


Figure 11

Figure 12 shows the noise performance of the ΔG cell. The maximum output level before clipping occurs in the gain cell is plotted along with the output noise in a 20kHz bandwidth. Note that the noise drops as the gain is reduced for the first 20dB of gain reduction. At high gains, the signal to noise ratio is 90dB, and the total dynamic range from maximum signal to minimum noise is 110dB.

Control signal feed-through is generated in the gain cell by imperfect device matching and mismatches in the current sources I_1 and I_2. When no input signal is present, changing I_G will cause a small output signal. The distortion trim is effective in nulling out any control signal feed-through, but in general, the null for minimum feed-through will be different than the null in distortion. The control signal feed-through can be trimmed independently of distortion by tying a current source to the ΔG input pin. This effectively trims I_1. Figure 13 shows such a trim network.

DYNAMIC RANGE OF NE570

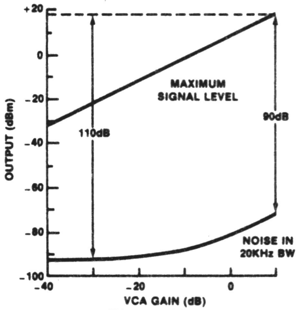


Figure 12

CONTROL SIGNAL FEEDTHRU TRIM

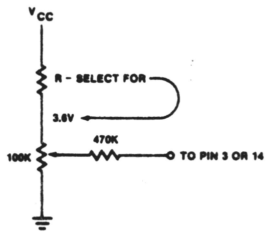


Figure 13

OPERATIONAL AMPLIFIER

The main op amp shown in the chip block diagram is equivalent to a 741 with a 1MHz bandwidth. Figure 14 shows the basic circuit. Split collectors are used in the input pair to reduce g_m, so that a small compensation capacitor of just 10pf may be used. The output stage, although capable of output currents in excess of 20ma., is biased for a low quiescent current to conserve power. When driving heavy loads, this leads to a small amount of crossover distortion.

RESISTORS

Inspection of the gain equations in Figure 3 and 4 will show that the basic compressor and expandor circuit gains may be set entirely by resistor ratios and the internal voltage reference. Thus, any form of resistors that match well would suffice for these simple hookups, and absolute accuracy and temperature coefficient would be of no importance. However, as one starts to modify the gain equation with external resistors, the internal resistor accuracy and tempco become very significant. Figure 15 shows the effects of temperature on the diffused resistors which are normally used in integrated circuits, and the ion implanted resistors which are used in this circuit. Over the critical 0°C to 70°C temperature range, there is a 10 to 1 improvement in drift from a 5% change for the diffused resistors, to a .5% change for the implemented resistors. The implanted resistors have another advantage in that they can be made 1/7 the size of the diffused resistors due to the higher resistivity. This saves a significant amount of chip area.

OPERATIONAL AMPLIFIER

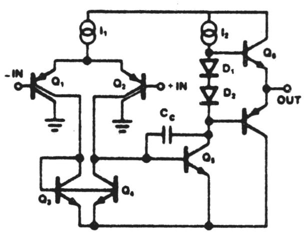


Figure 14

RESISTANCE vs TEMPERATURE

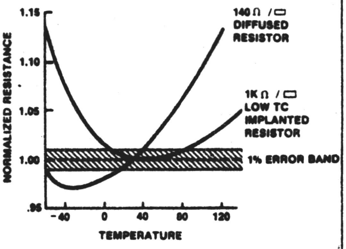


Figure 15

***For additional information, consult the Applications Section.**

PROGRAMMABLE ANALOG COMPANDOR

SA/NE572

DESCRIPTION

The NE572 is a dual channel, high performance gain control circuit in which either channel may be used for dynamic range compression or expansion. Each channel has a full wave rectifier to detect the average value of input signal; a linearized, temperature compensated variable gain cell (ΔG) and a dynamic time constant buffer. The buffer permits independent control of dynamic attack and recovery time with minimum external components and improved low frequency gain control ripple distortion over previous compandors.

The NE572 is intended for noise reduction in high performance audio systems. It can also be used in a wide range of communication systems and video recording applications.

FEATURES

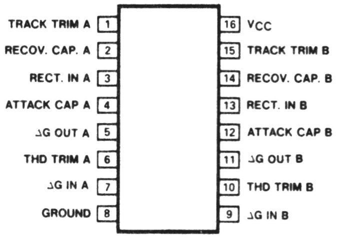
- **Independent control of attack and recovery time.**
- **Improved low frequency gain control ripple**
- **Complementary gain compression and expansion with external Op Amp**
- **Wide dynamic range—greater than 110dB**
- **Temperature compensated gain control**
- **Low distortion gain cell**
- **Low noise—6μV typical**
- **Wide supply voltage range—6V–22V**
- **System level adjustable with external components.**

APPLICATIONS

- **Dynamic noise reduction system**
- **Voltage control amplifier**
- **Stereo expandor**
- **Automatic level control**
- **High level limiter**
- **Low level noise gate**
- **State variable filter**

PIN CONFIGURATION

D, N PACKAGE


TRACK TRIM A 1
RECOV. CAP. A 2
RECT. IN A 3
ATTACK CAP A 4
ΔG OUT A 5
THD TRIM A 6
ΔG IN A 7
GROUND 8
16 VCC
15 TRACK TRIM B
14 RECOV. CAP. B
13 RECT. IN B
12 ATTACK CAP B
11 ΔG OUT B
10 THD TRIM B
9 ΔG IN B

(Top view)

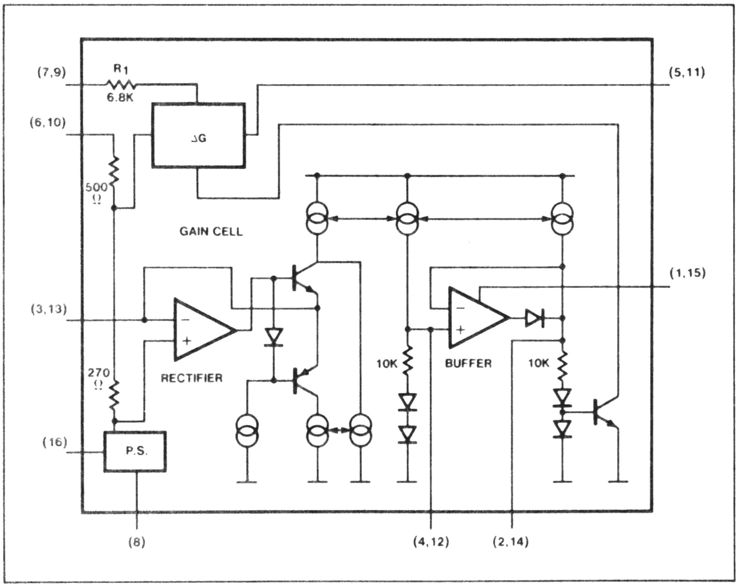
ORDER PART NO.

NE572N SA572N
SA572F NE572D SA572D

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	22	VDC
T_A	Operating temperature range	0 to 70	°C
P_D	Power dissipation	500	mW

BLOCK DIAGRAM


(7,9)
R1
6.8K
(6,10)
ΔG
500 Ω
GAIN CELL
(5,11)
(1,15)
(3,13)
RECTIFIER
10K
BUFFER
10K
270 Ω
(16)
P.S.
(8)
(4,12)
(2,14)

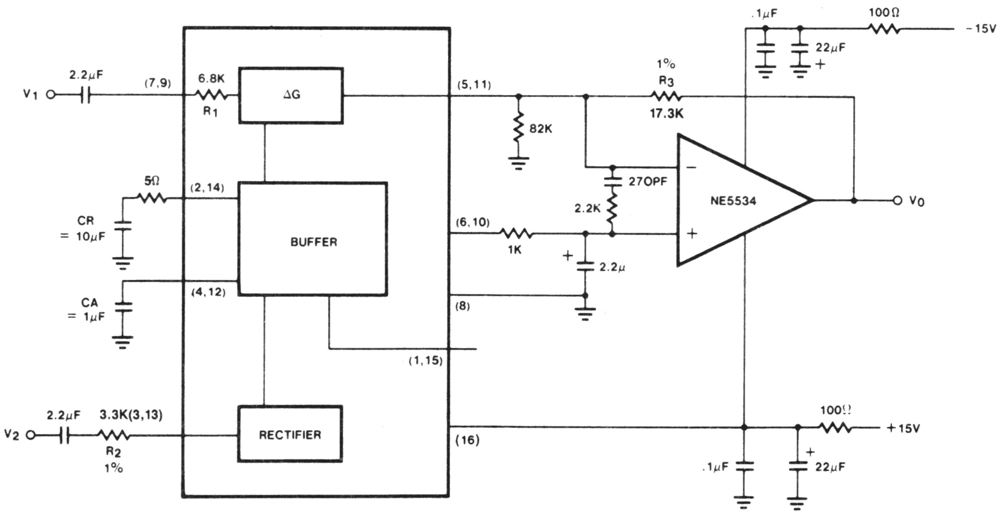
Note:
1. Supplied only in large SO (Small Outline) package.

ELECTRICAL CHARACTERISTICS

Standard Test Conditions (unless otherwise noted) V_{CC} = 15V TA = 25°C Expandor mode (see test circuit) Input signals at unity gain level (0dB) = 100mV RMS at 1KHz, $V_1 = V_2$, R_2 = 3.3K, R_3 = 17.3K

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		6		22	V_{DC}
I_{CC}	Supply current	No Signal			6	mA
	Internal voltage reference		2.3	2.5	2.7	V_{DC}
THD	(untrimmed)	1kHz C_A = 1.0μF		.2	1.0	%
THD	(trimmed)	1kHz C_R = 10μF		.05		%
THD	(trimmed)	100Hz		.25		%
	No signal output noise	Input to V_1 and V_2 grounded (20-20kHz)		6	25	uV
	DC level shift (untrimmed)	Input change from no signal to 100mV RMS		±20	±50	MV
	Unity gain level		−1	0	+1	dB
	Large signal distortion	$V_1 = V_2$ = 400mV		0.7	3.0	%
	Tracking error (measured relative to value at unity gain output) = $[V_O - V_O(\text{unity gain})]$ dB − V_2 (dBm)	Rectifier input V_2 = +6dB, V_1 = 0dB V_2 = −30dB, V_1 = 0dB		±.2 ±.5	−1.5 +.8	dB
	Channel crosstalk	200mV RMS into channel A, measured output on channel B	60			dB
	Power supply rejection ratio	120Hz		70		dB

TEST CIRCUIT


V1
2.2μF
(7,9)
6.8K
R1
ΔG
(5,11)
1%
R3
17.3K
82K
5Ω
(2,14)
CR
= 10μF
BUFFER
(6,10)
1K
270PF
2.2K
2.2μ
NE5534
VO
CA
= 1μF
(4,12)
(8)
(1,15)
.1μF
100Ω
−15V
22μF
V2
2.2μF
3.3K(3,13)
R2
1%
RECTIFIER
(16)
100Ω
+15V
.1μF
22μF

AUDIO SIGNAL PROCESSING IC COMBINES VCA AND FAST ATTACK-SLOW RECOVERY LEVEL SENSOR

In high performance audio gain control applications it is desirable to independently control the attack and recovery time of the gain control signal. This is true, for example, in compandor applications for noise reduction. In high end systems the input signal is usually split into two or more frequency bands to optimize the dynamic behavior for each band. This reduces low frequency distortion due to control signal ripple, phase distortion, high frequency channel overload and noise modulation. Because of the expense in hardware, multiple band signal processing up to now was limited to professional audio applications.

With the introduction of the Signetics NE572 this high performance noise reduction concept becomes feasible for consumer hi fi applications. The NE572 is a dual channel gain control IC. Each channel has a linearized, temperature compensated gain cell and an improved level sensor. In conjunction with an external low noise op amp for current to voltage conversion, the VCA features low distortion, low noise and wide dynamic range. The novel level sensor which provides gain control current for the VCA gives lower gain control ripple and independent control of fast attack, slow recovery dynamic response. An attack capacitor CA with an internal 10K resistor RA defines the attack time TA. The recovery time TR of a tone burst is defined by a recovery capacitor CR and an internal 10K resistor R_R. Typical attack time of 4MS for the high frequency spectrum and 40MS for the low frequency band can be obtained with .1μF and 1.0μF attack capacitors respectively. Recovery time of 200MS can be obtained with a 4.7μF external capacitor. With the recovery capacitor added in the level sensor, the gain control ripple for low frequency signals is much lower than that of a simple RC ripple filter. As a result the residual third harmonic distortion of low frequency signal in a two quad transconductance amplifier is greatly improved. With the 1.0μF attack capacitor and 4.7μF recovery capacitor for a 100HZ signal the third harmonic distortion is improved by more than 10db over the simple RC ripple filter with a single 1.0μF attack and recovery capacitor, while the attack time remains the same.

The NE572 is assembled in a standard 16 pin dual in line plastic package and in oversized SO (Small Outline) package. It operates over wide supply range from 6V to 22V. Supply current is less than 6mA. The NE572 is designed for consumer application over a temperature range 0-70°C. The SA572 is intended for applications from −40°C to +85°C.

NE572 BASIC APPLICATIONS

Description

The NE572 consists of two linearized, temperature compensated gain cells (ΔG) each with a full-wave rectifier and a buffer amplifier as shown in the block diagram. The two channels share a 2.5V common bias reference derived from the power supply but otherwise operate independently. Because of inherent low distortion, low noise and the capability to linearize large signals, a wide dynamic range can be obtained. The buffer amplifiers are provided to permit control of attack time and recovery time independent of each other. Partitioned as shown in the block diagram, the IC allows flexibility in the design of system levels that optimize DC shift, ripple distortion, tracking accuracy and noise floor for a wide range of application requirements.

Gain Cell

Figure 1 shows the circuit configuration of the gain cell. Bases of the differential pairs $Q_1 - Q_2$ and $Q_3 - Q_4$ are both tied to the output and inputs of OPA A_1. The negative feedback through Q_1 holds the V_{BE} of $Q_1 - Q_2$ and the V_{BE} of $Q_3 - Q_4$ equal. The following relationship can be derived from the transistor model equation in the forward active region.

$$\Delta V_{BE_{Q_3-Q_4}} = \Delta_{BE_{Q_1-Q_2}}$$

$$(V_{BE} = V_T\, l_n\, IC/IS)$$

$$V_T\, l_n\left(\frac{\frac{1}{2} I_G + \frac{1}{2} I_O}{I_S}\right) - V_T\, l_n\left(\frac{\frac{1}{2} I_G - \frac{1}{2} I_O}{I_S}\right)$$

$$= V_T\, l_n\left(\frac{I_1 + \text{lin}}{I_S}\right) - V_T\, l_n\left(\frac{I_2 - I_1 - \text{lin}}{I_S}\right) \quad \text{--(2)}$$

$$\text{where lin} = \frac{Vin}{R_1}$$

$$R_1 = 6.8K$$
$$I_1 = 140\mu A$$
$$I_2 = 280\mu A$$

I_O is the differential output current of the gain cell and I_G is the gain control current of the gain cell.

If all transistors Q_1 through Q_4 are of the same size, equation (2) can be simplfied to:

$$I_O = \frac{2}{I_2} \cdot \text{lin} \cdot I_G - \frac{1}{I_2}(I_2 - 2I_1) \cdot I_G \qquad (3)$$

The first term of eqn. (3) shows the multiplier relationship of a linearized two quadrant transconductance amplifier. The second term is the gain control feed through due to the mismatch of devices. In the design this

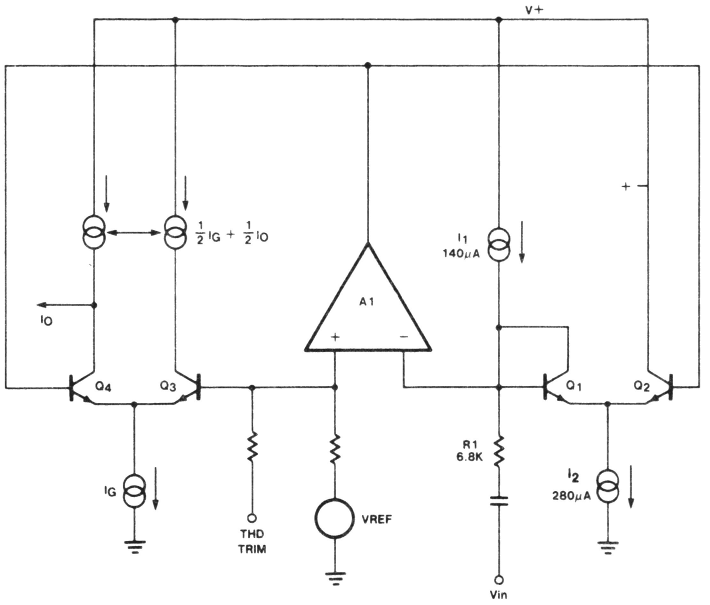


Figure 1

PROGRAMMABLE ANALOG COMPANDOR SA/NE572

has been minimized by large matched devices and careful layout. Offset voltage is caused by the device mismatch and it leads to even harmonic distortion. The offset voltage can be trimmed out by feeding a current source within ±25μA into the THD trim pin. The residual distortion is third harmonic distortion and is caused by gain control ripple. In a compandor system, available control of fast attack and slow recovery improves ripple distortion significantly. At the unity gain level of 100mV, the gain cell gives THD (total harmonic distortion) of .17% TYP. Output noise with no input signals is only 6μV in the audio spectrum (10HZ-20KHZ). The output current I_O must feed the virtual ground input of an operational amplifier with a resistor from output to inverting input. The non-inverting input of the operational amplifier has to be biased at VREF if the output current I_O is dc coupled.

Rectifier

The rectifier is a full-wave design as shown in Figure 2. The input voltage is converted to current through the input resistor R2 and turns on either Q5 or Q6 depending on the signal polarity. Deadband of the voltage to current converter is reduced by the loop gain of the gain block A2. If AC coupling is used, the rectifier error comes only from input bias current of gain block A2. The input bias current is typically about 70nA. Frequency response of the gain block A2 also causes second order error at high frequency. The collector current of Q6 is mirrored and summed at the collector of Q5 to form the full wave rectified output current I_R. The rectifier transfer function is

$$\frac{V_{IN}-V_{REF}}{R_2} \qquad (4)$$

If Vin is A.C. coupled, then the equation will be reduced to:

$$I_{RAC} = \frac{Vin\,(AVG)}{R_2}$$

The internal bias scheme limits the maximum output current I_R to be around 300μA. Within a ± 1dB error band the input range of the rectifier is about 52dB.

Buffer Amplifier

In audio systems, it is desirable to have fast attack time and slow recovery time for a tone burst input. The fast attack time reduces transient channel overload but also causes low frequency ripple distortion. The low frequency ripple distortion can be improved with the slow recovery time. If different attack times are implemented in corresponding frequency spectrums in a split band audio system, high quality performance can be achieved. The buffer amplifier is designed to make this feature available with minimum external components. Refer-

SIMPLIFIED RECTIFIER SCHEMATIC

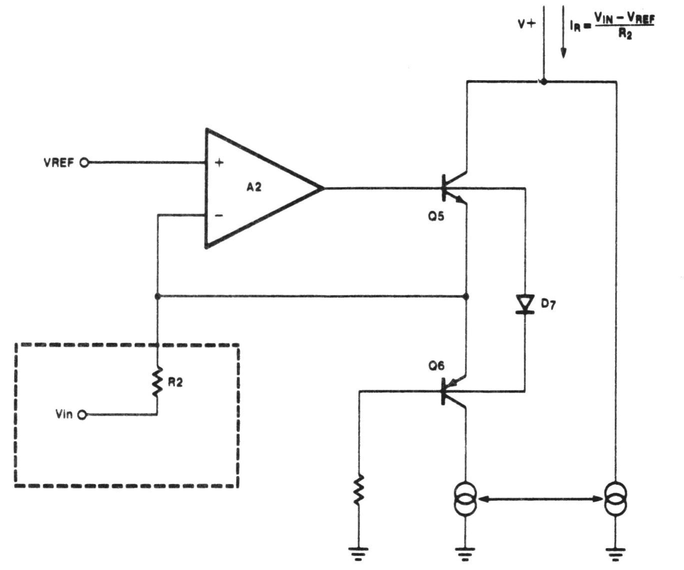


Figure 2

BUFFER AMPLIFIER SCHEMATIC

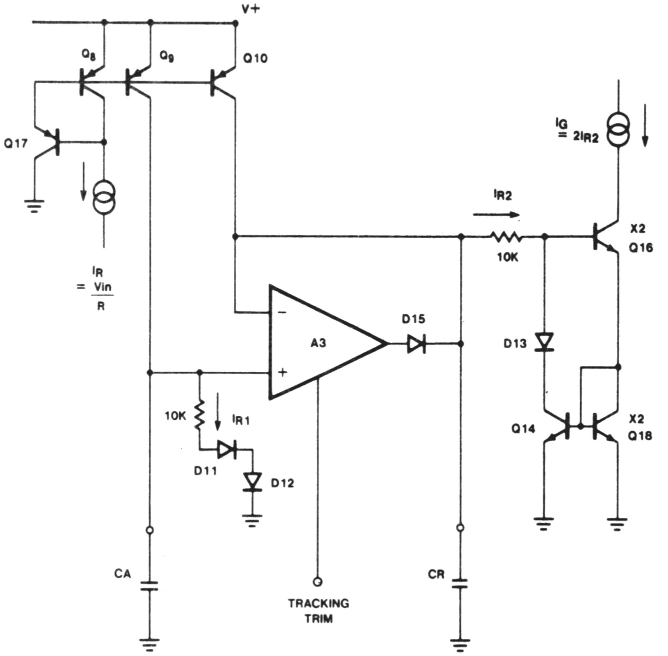


Figure 3

ring to Figure 3, the rectifier output current is mirrored into the input and output of the unipolar buffer amplifier A_3 through Q_8, Q_9 and Q_{10}. Diodes D_{11} and D_{12} improve tracking accuracy and provide common mode bias for A_3. For a positive going input signal, the buffer amplifier acts like a voltage follower. Therefore, the output impedance of A_3 makes the contribution of capacitor CR to attack time insignificant. Neglecting diode impedance the gain Ga(t) for ΔG can be expressed as follows.

$$Ga(t) = (Ga_{INT} - Ga_{FNL})\, e^{\frac{-t}{\tau A}} + Ga_{FNL}$$

Ga_{INT} = Initial Gain

$\tau A = R_A \cdot CA = 10K \cdot CA$ Ga_{FNL} = Final Gain

where τA is the attack time constant and RA is a 10K internal resistor. Diode D_{15} opens the feedback loop of A_3 for a negative going signal if the value of capacitor CR is larger than capacitor CA. The recovery time depends only on CR • R_R. If the diode impedance is assumed negligible, the dynamic gain G_R (t) for ΔG is expressed as follows.

$$G_R(t) = (G_{R\ INT} - G_{R\ FNL})\, e^{\frac{-t}{\tau R}} + G_{R\ FNL}$$

$$\tau R = R_R \cdot CR = 10K \cdot CR$$

where τR is the recovery time constant and R_R is a 10K internal resistor. The gain control current is mirrored to the gain cell through Q_{14}. The low level gain errors due to input bias current of A_2 and A_3 can be trimmed through the tracking trim PIN into A_3 with a current source of ±3μA.

Basic Expandor

Figure 4 shows an application of the circuit as a simple expandor. The gain expression of the system is given by

$$\frac{V_{OUT}}{V_{IN}} = \frac{2}{I_1} \bullet \frac{R_3 \bullet V_{IN}(AVG)}{R_2 \bullet R_1}\ (I_1 = 140\mu A) \qquad (5)$$

Both the resistors R_1 and R_2 are tied to internal summing nodes. R_1 is a 6.8K internal resistor. The maximum input current into the gain cell can be as large as 140μA. This corresponds to a voltage level of 140μA • 6.8K = 952mV peak. The input peak current into the rectifier is limited to 300μA by the internal bias system. Note that the value of R_1 can be increased to accommodate higher input level. R_2 and R_3 are external resistors. It is easy to adjust the ratio of R3/R2 for desirable system voltage and current levels. A small R2 results in higher gain control current and smaller static and dynamic tracking error. However, an impedance buffer A_1 may be necessary if the input is voltage drive with large source impedance.

The gain cell output current feeds the summing node of the external OPA A_2. R_3 and A_2 convert the gain cell output current to the output voltage. In high performance applications, A_2 has to be low noise, high speed and wide band so that the high performance output of the gain cell will not be degraded. The non-inverting input of A_2 can be biased at the low noise internal reference PIN 6 or 10. Resistor R_4 is used to biased up the output DC level of A_2 for maximum swing. The output DC level of A_2 is given by

$$V_{ODC} = V_{REF}\left(1 + \frac{R_3}{R_4}\right) - V_B \frac{R_3}{R_4} \qquad (6)$$

V_B can be tied to a regulated power supply for a dual supply system and be grounded for a single supply system. CA sets the attack time constant and CR sets the recovery time constant.

BASIC EXPANDOR SCHEMATIC

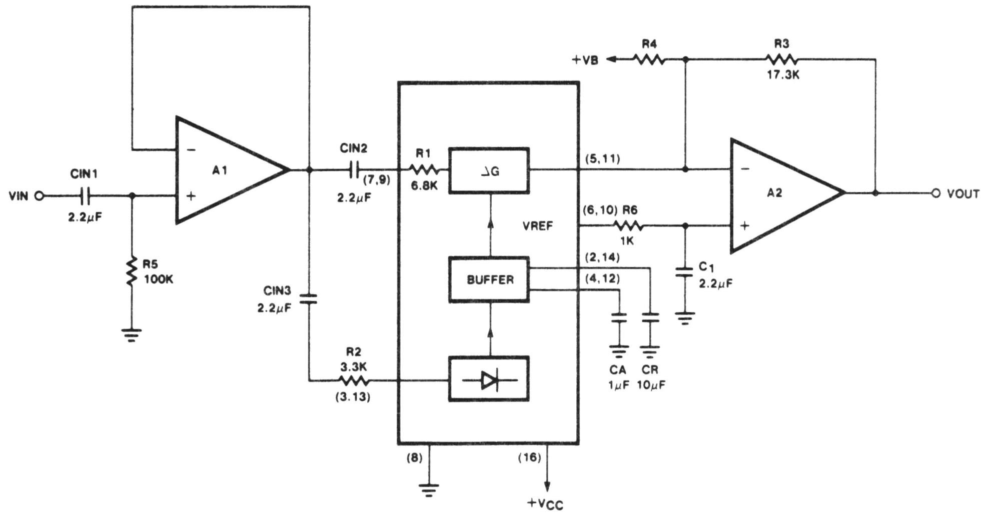


Figure 4

Basic Compressor

Figure 5 shows the hook-up of the circuit as a compressor. The IC is put in the feedback loop of the OPA A_1. The system gain expression is as follows:

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{I_1}{2} \cdot \frac{R_2 \cdot R_1}{R_3 \cdot V_{IN}\,(AVG)}\right)^{1/2} \qquad (7)$$

RDC1, RDC2, and CDC form a dc feedback for A_1. The output DC level of A_1 is given by

$$V_{ODC} = V_{REF}\left(1 + \frac{R_{DC1} + R_{DC2}}{R_4}\right) - V_B \cdot \left(\frac{R_{DC1} + R_{DC2}}{R_4}\right) \qquad (8)$$

The zener diodes D_1 and D_2 are used for channel overload protection.

Basic Compandor System

The above basic compressor and expandor can be applied to systems such as tape/disc noise reduction, digital audio, bucket brigade delay lines. Additional system design techniques such as bandlimiting, band splitting, pre-emphasis, de-emphasis and equalization are easy to incorporate. The IC is a versatile functional block to achieve a high performance audio system. Figure 6 shows the system level diagram for reference.

For additional information, refer to the Applications Section.

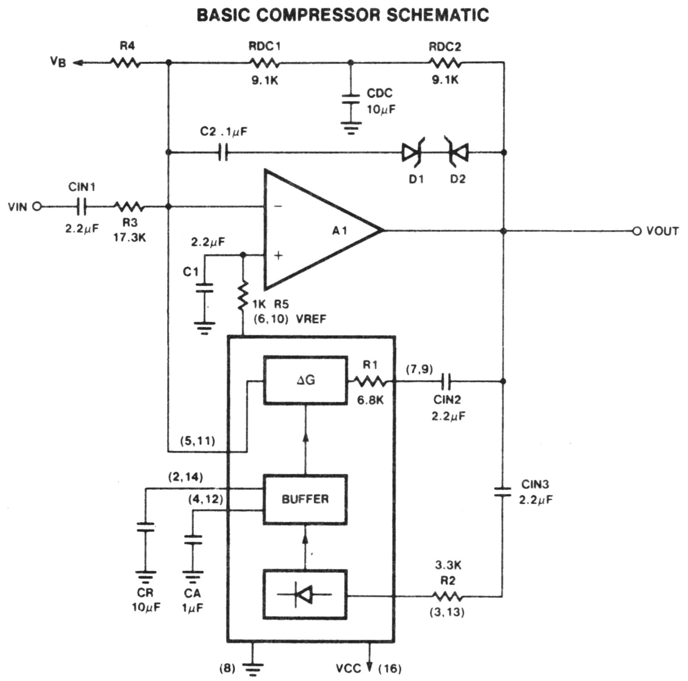

BASIC COMPRESSOR SCHEMATIC
VB
R4
RDC1
9.1K
RDC2
9.1K
CDC
10μF
C2 .1μF
D1
D2
CIN1
VIN
2.2μF
R3
17.3K
2.2μF
A1
VOUT
C1
1K R5
(6,10) VREF
ΔG
R1
6.8K
(7,9)
CIN2
2.2μF
(5,11)
(2,14)
(4,12)
BUFFER
CIN3
2.2μF
3.3K
R2
(3,13)
CR
10μF
CA
1μF
(8)
VCC
(16)

Figure 5

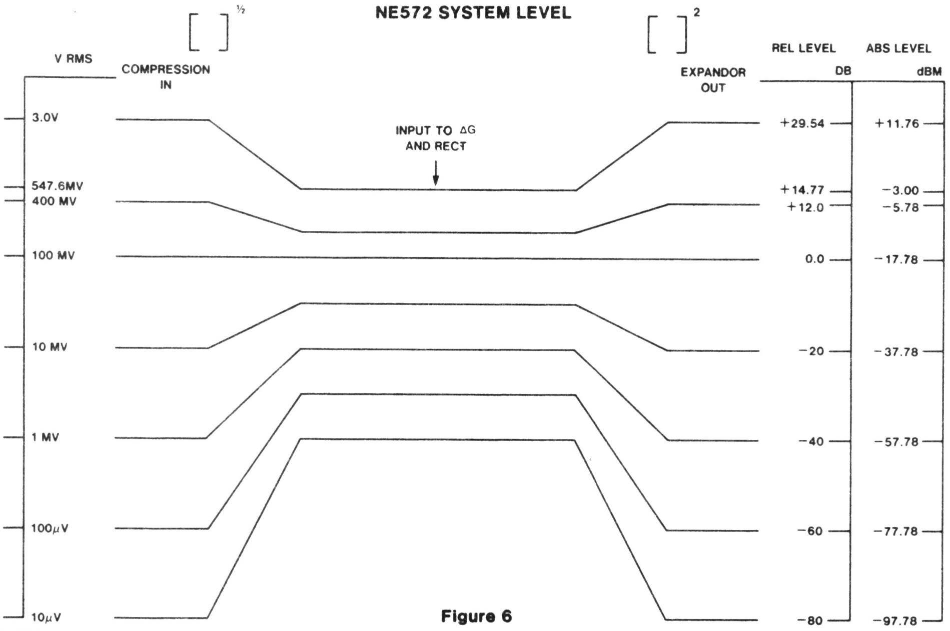


Figure 6

*For additional information, consult the Applications Section.

STEREO DEMODULATOR WITH BLEND

LM1870

DESCRIPTION

The LM1870 combination FM Stereo Demodulator and Blend Circuit is a PLL circuit with a D.C. control pin whose purpose is to reduce switching noise by decreasing separation under low signal amplitude conditions. The part is designed specifically for automobile applications where fluctuating signal strength can cause demodulation noise.

FEATURES

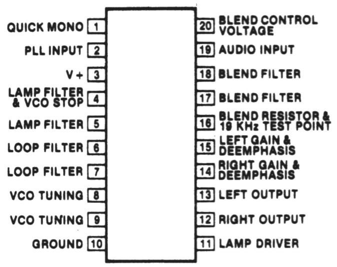
- **Stereo blend control**
- **Wide input dynamic range**
- **Low total harmonic distortion**
- **VCO disable function**
- **Monophonic override pin**
- **Supply range 7V-15V**

APPLICATIONS

- **Auto radios**
- **High fidelity tuners**
- **High performance portable radios**
- **Electronic tuned radios**

PIN CONFIGURATION

N PACKAGE

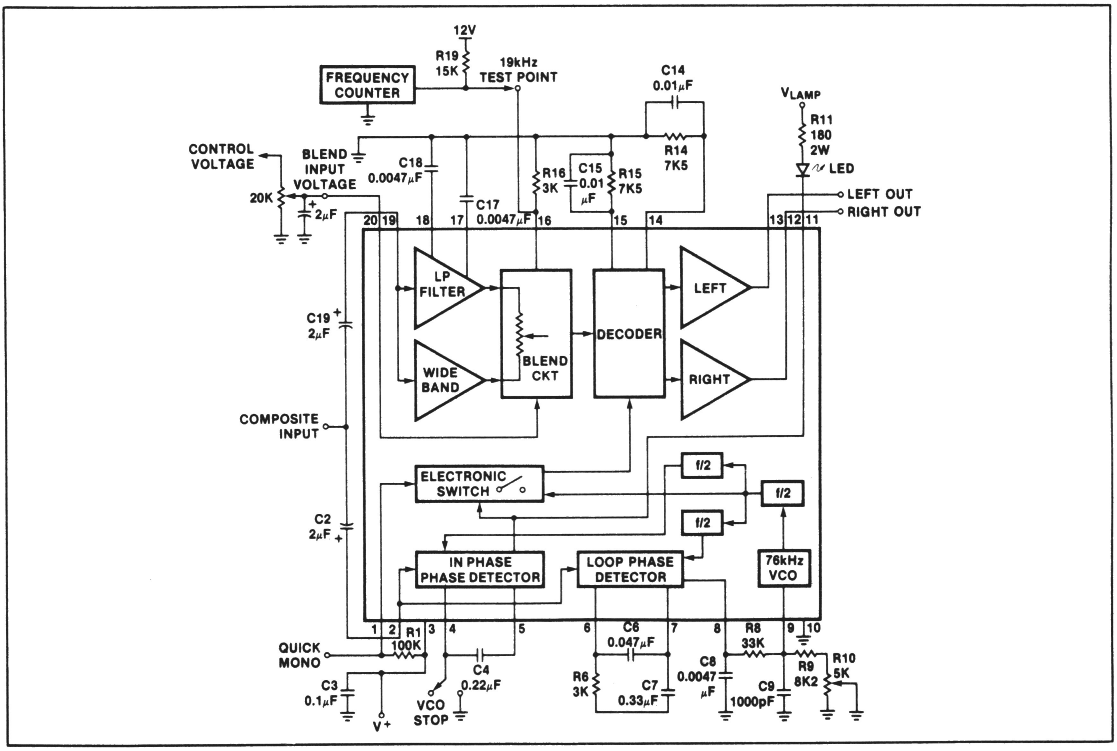

QUICK MONO 1
PLL INPUT 2
V+ 3
LAMP FILTER & VCO STOP 4
LAMP FILTER 5
LOOP FILTER 6
LOOP FILTER 7
VCO TUNING 8
VCO TUNING 9
GROUND 10
20 BLEND CONTROL VOLTAGE
19 AUDIO INPUT
18 BLEND FILTER
17 BLEND FILTER
16 BLEND RESISTOR & 19 KHz TEST POINT
15 LEFT GAIN & DEEMPHASIS
14 RIGHT GAIN & DEEMPHASIS
13 LEFT OUTPUT
12 RIGHT OUTPUT
11 LAMP DRIVER

TOP VIEW
ORDER NUMBER
LM1870N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage, pin 3	15	V
Lamp driver voltage, pin 11	18	V
Output voltage, pin 12, 13 supply off	7	V
Quick mono input (pin 20)	V + (pin 3)	
Blend input (pin 20)	15	V
Operating temperature range	0°C to + 70°C	
Power dissipation (note 1)	1	W
Storage temperature	− 65°C to + 125°C	
Lead temperature (soldering, 10 seconds)	300°C	

TYPICAL APPLICATION AND TEST CIRCUIT


12V
R19 15K
FREQUENCY COUNTER
19kHz TEST POINT
C14 0.01μF
R14 7K5
VLAMP
R11 180 2W
LED
LEFT OUT
RIGHT OUT
CONTROL VOLTAGE
BLEND INPUT VOLTAGE
20K
2μF
C18 0.0047μF
C17 0.0047μF
R16 3K
C15 0.01 μF
R15 7K5
20 19 18 17 16 15 14 13 12 11
LP FILTER
WIDE BAND
BLEND CKT
DECODER
LEFT
RIGHT
C19 2μF
COMPOSITE INPUT
ELECTRONIC SWITCH
f/2
f/2
f/2
76kHz VCO
C2 2μF
IN PHASE PHASE DETECTOR
LOOP PHASE DETECTOR
1 2 3 4 5 6 7 8 9 10
R1 100K
QUICK MONO
C3 0.1μF
V+
C4 0.22μF
VCO STOP
C6 0.047μF
R6 3K
C7 0.33μF
C8 0.0047 μF
R8 33K
C9 1000pF
R9 8K2
R10 5K

STEREO DEMODULATOR WITH BLEND

LM1870

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V^+ = 8V$ unless otherwise noted (Figure 1)

SYMBOL AND PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating supply voltage		7	8	15	V
Supply current			26	45	mA
Input DC voltage	Pin 19		4		V
Input DC voltage	Pin 2		1.8		V
Supply rejection		15	30		dB
Lamp leakage current	Lamp off, pin 11 = 16V		0.1	100	μA
Lamp saturation voltage	Lamp on, pin 11 @ 75mA		1.4	2.0	V
VCO stop voltage	Voltage @ pin 4 to stop VCO	0.2	0.4		V
VCO stop current	Pin 4 = 0.2V		– 30	– 100	μA
Blend input bias current			– 2	– 20	μA
Quick mono switch voltage			4		V
Quick mono bias current	Pin 1 = 8V		2		μA
Output leakage	Pin 12 or 13 = 6.5V, pin 3 = 0V		0.1	20	μA

AUDIO ELECTRICAL CHARACTERISTICS

SYMBOL AND PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Mono gain	1kHz	– 4	– 1	+ 2	dB
Mono THD	1kHz @ 200mVrms		0.05	0.25	%
Channel balance			± 0.4	± 1.5	dB
Gain shift	Mono to stereo		± 0.1	± 1.0	dB
Channel separation	Pin 20 ≥ 1.1V	30	45		dB
Output DC shift	Mono to stereo		± 15	± 100	mV
Input resistance	Pin 19	20	40		kΩ
Output resistance	Pin 12, 13		65	200	Ω
Ultrasonic rejection	19kHz + 38kHz		30		dB
SCA rejection	(Note 2)		70		dB
Signal to noise	1kHz @ 200mVrms MONO		68		dB

PLL ELECTRICAL CHARACTERISTICS

SYMBOL AND PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Lamp ON voltage	19kHz on pin 2		15	20	mV
Lamp OFF voltage	19kHz on pin 2	2.5	5		mV
Lamp hysteresis			10		dB
Capture range	25mVrms on pin 2	± 2	± 4	± 6	%
Hold in range	25mVrms on pin 2		± 12		%
Input resistance	Pin 2	8	14		kΩ

STEREO DEMODULATOR WITH BLEND LM1870

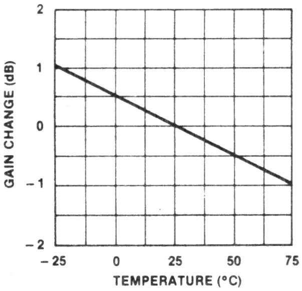
BLEND ELECTRICAL CHARACTERISTICS

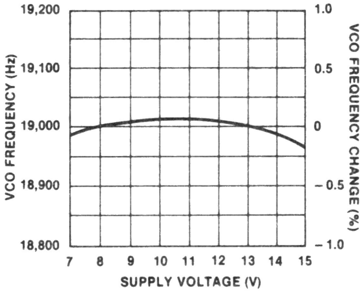
SYMBOL AND PARAMETER	TEST CONDITIONS (Pin 20 from 1.1V to 0.2V)	MIN	TYP	MAX	UNIT
Stereo gain change	1kHz L = − R input	− 25	− 35		dB
Mono gain change	1kHz L = R input 10kHz L = R input	− 1.5 − 8	− 0.5 − 14	0.5 − 20	dB dB
Output DC shift			± 40	± 100	mV

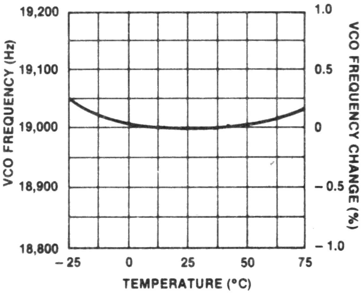
NOTES

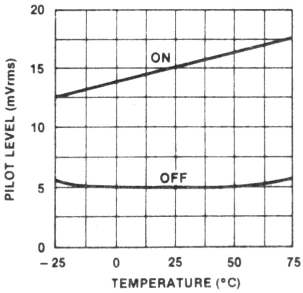
1. For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 125°C/W junction to ambient.
2. Input is 10% SCA (74.5kHz), 9% pilot and 1kHz left or right. Rejection is ratio of 1kHz output to 1.5kHz output.

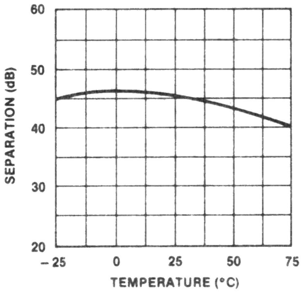
TYPICAL CHARACTERISTICS

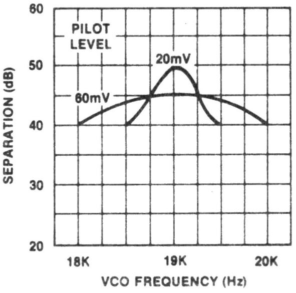

GAIN CHANGE vs TEMPERATURE

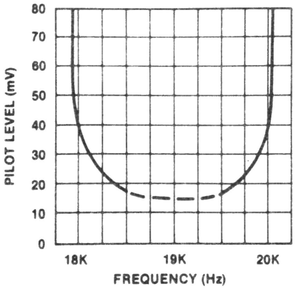

VCO SUPPLY SENSITIVITY

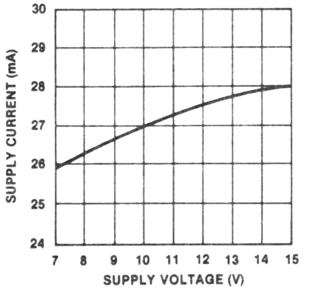

VCO TEMPERATURE STABILITY

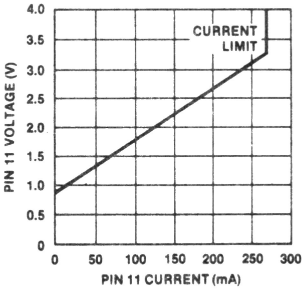

LAMP ON/OFF vs TEMPERATURE


SEPARATION vs TEMPERATURE

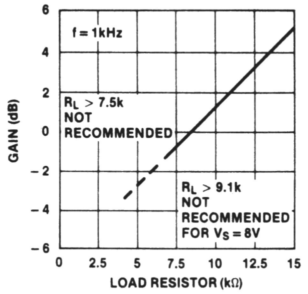

SEPARATION vs VCO TUNING


CAPTURE RANGE vs PILOT LEVEL

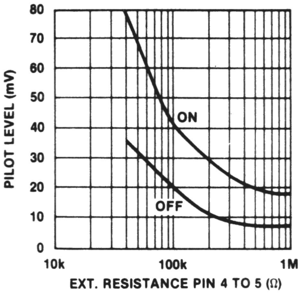

SUPPLY CURRENT vs SUPPLY VOLTAGE


LAMP DRIVER VOLTAGE vs CURRENT

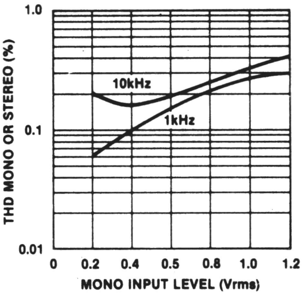
GAIN vs R_L (PIN 14, 15)



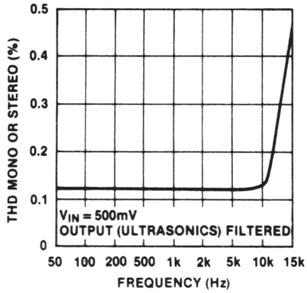
LAMP ON/OFF vs RESISTANCE PIN 4 TO 5



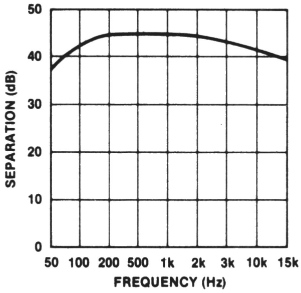
TOTAL HARMONIC DISTORTION vs INPUT LEVEL



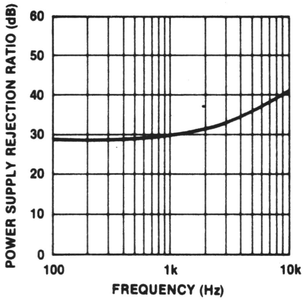
TOTAL HARMONIC DISTORTION vs FREQUENCY



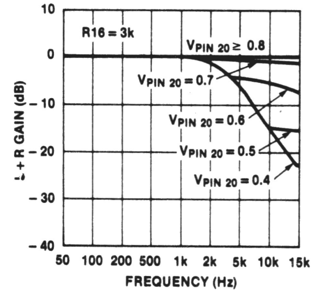
SEPARATION vs FREQUENCY



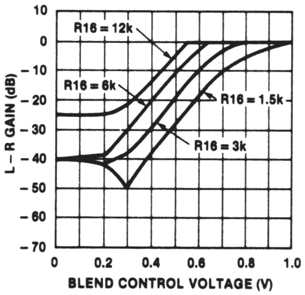
POWER SUPPLY REJECTION RATIO vs FREQUENCY



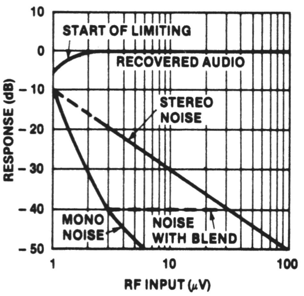
L + R FREQUENCY RESPONSE WITH BLEND CONTROL



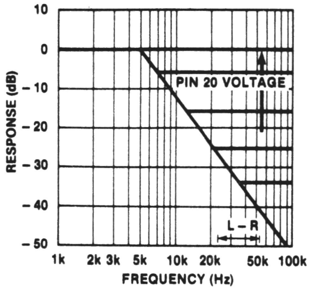
L – R GAIN vs BLEND CONTROL



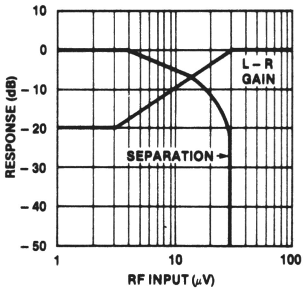
TYPICAL RADIO QUIETING CHARACTERISTIC



BLEND FILTER RESPONSE



L – R GAIN AND SEPARATION vs RF INPUT LEVEL WITH BLEND



DUAL LOW-NOISE PREAMP NE542

DESCRIPTION

The NE542 is a dual preamplifier for the amplification of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with individual internal power supply decoupler-regulator, providing 110dB supply rejection and 70dB channel separation. Other outstanding features include high gain (104dB), large output voltage swing (V_{CC} -2Vp-p), and internal compensation to 10dB. The NE542 operates from a single supply across the wide range of 9 to 24V.

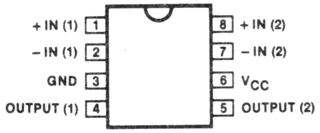
The NE542 is ideal for use in stereo phono, tape, or microphone preamps and other applications requiring low noise amplication of small signals.

FEATURES

- **Low noise—.7μV total input noise**
- **High gain—104dB open loop**
- **Single supply operation**
- **Wide supply range 9 to 24V**
- **Power supply rejection 110dB**
- **Large output voltage swing (V_{CC} -2V p-p)**
- **Wide bandwidth 15MHz unity gain**
- **Power bandwidth 100kHz (15V p-p)**
- **Internally compensated (stable at 10dB)**
- **Short circuit protected**
- **High slew rate 5V/μs**

PIN CONFIGURATION

N PACKAGE



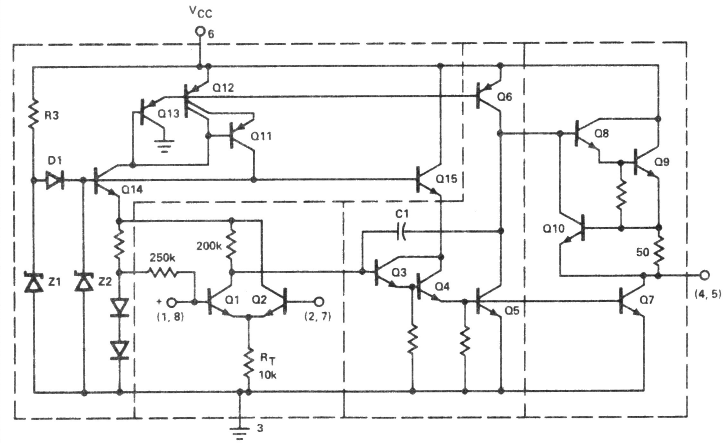
TOP VIEW

ORDER NUMBER
NE542N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	+24	V
Power dissipation	500	mW
Operating temperature range	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	+300	°C

EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = 14V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	NE542			UNIT
		Min	Typ	Max	
Supply voltage		9		24	V
Supply current	V_{CC} = 9 to 18V, $R_L = \infty$		9	15	mA
Input resistance					
Positive input			100		kΩ
Negative input			200		kΩ
Output resistance	Open loop		150		Ω

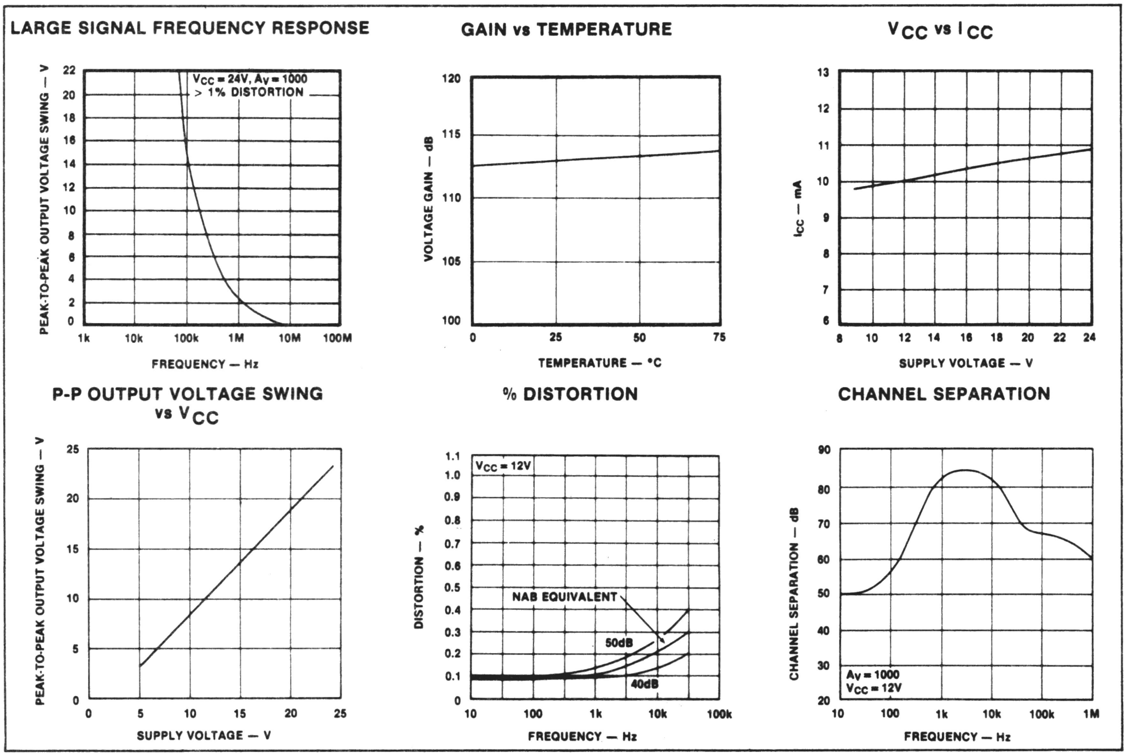
DUAL LOW-NOISE PREAMP

NE542

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 14V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	NE542			UNIT
		Min	Typ	Max	
Voltage gain	Open loop		160,000		V/V
Input current					
Negative input			.5		µA
Output current	Source	8	14		mA
	Sink (linear operation)	2	3		mA
Output voltage swing		V_{CC} -2.5	V_{CC} -2		V
Small signal bandwidth			15		MHz
Slew rate			5		V/µs
Power bandwidth	15V p-p		100		kHz
Maximum input voltage	Linear operation, <2.5% distortion			300	mVrms
Supply rejection ratio	f = 60, 120Hz		100		dB
	f = 1kHz		110		dB
Channel separation	f = 1kHz	40	70		dB
Total harmonic distortion	40 dB gain, f = 1kHz		.1	.3	%
Total equivalent input Noise	RS = 600Ω, 100 - 10,000Hz		.7	1.2	µVrms
Noise figure	RS = 50kΩ, 10 - 10,000Hz		1.2		dB
	RS = 20kΩ, 10 10,000Hz		1.2		dB
	RS = 10kΩ, 10 - 10,000Hz		1.5		dB
	RS = 5kΩ, 10 - 10,000Hz		2.4		dB

TYPICAL PERFORMANCE CHARACTERISTICS



LARGE SIGNAL FREQUENCY RESPONSE

GAIN vs TEMPERATURE

VCC vs ICC

P-P OUTPUT VOLTAGE SWING vs VCC

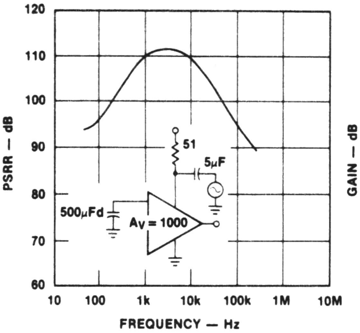
% DISTORTION

CHANNEL SEPARATION

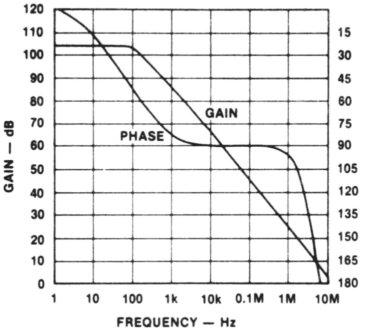
DUAL LOW-NOISE PREAMP NE542

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

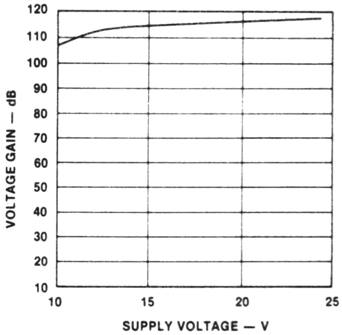
PSRR vs FREQUENCY



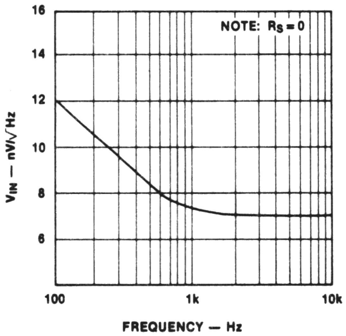
GAIN AND PHASE RESPONSE



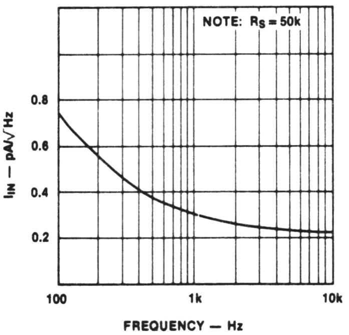
VOLTAGE GAIN vs SUPPLY VOLTAGE



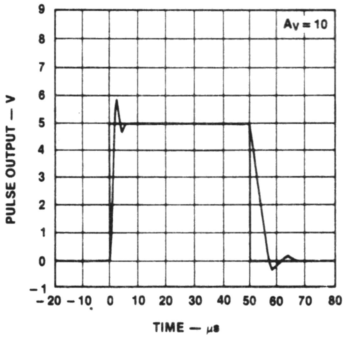
NOISE VOLTAGE vs FREQUENCY



NOISE CURRENT vs FREQUENCY

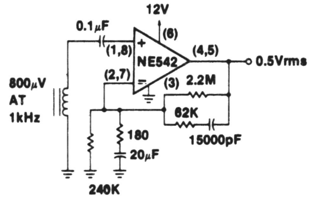


PULSE RESPONSE

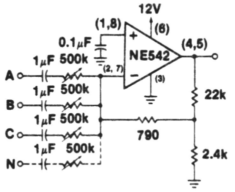


TYPICAL APPLICATIONS

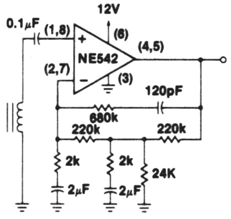
TYPICAL TAPE PLAYBACK AMPLIFIER


12V
0.1μF
(1,8)
(6)
NE542
(4,5)
0.5Vrms
(2,7)
(3)
2.2M
800μV
AT
1kHz
62K
15000pF
180
20μF
240K

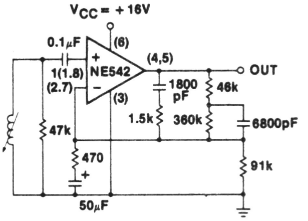
AUDIO MIXER


12V
(1,8)
(6)
0.1μF
(4,5)
1μF
500k
NE542
(2, 7)
(3)
A
B
C
N
22k
790
2.4k

TWO-POLE FAST TURN-ON NAB TAPE PREAMP


12V
0.1μF
(1,8)
(6)
NE542
(4,5)
(2,7)
(3)
120pF
680k
220k
220k
2k
2k
24K
2μF
2μF

RIAA MAGNETIC PHONO PREAMP


V_{CC} = +16V
0.1μF
(6)
1(1,8)
NE542
(4,5)
OUT
(2,7)
(3)
1800 pF
46k
1.5k
360k
6800pF
47k
470
50μF
91k

NOTE: All resistors values are typical and in ohms.

*For additional information, consult the Applications Section.

DOUBLE BALANCED MIXER AND OSCILLATOR SA/NE602

Preliminary

DESCRIPTION

The SA/NE602 is a monolithic Double Balanced Mixer with on-board oscillator and voltage regulator. The oscillator can be used as a buffer for external injection. The design is optimized for frequency conversion applications up to 200MHz and has excellent noise and 3rd order intermodulation performance. The SA/NE602 is available in a 8 lead dual in line plastic package and 8 lead SO (Surface mounted miniature package)

FEATURES

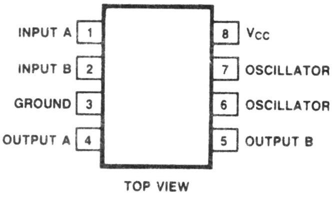
- **Low current consumption: 2.4mA typical**
- **High input and oscillator frequency operation up to 200MHz**
- **High third order intercept point: −15 dBm referred to matched input**
- **Excellent noise figure: 5.0dB typical at 45 MHz**
- **Low external count; suitable for crystal/ceramic filters**

APPLICATIONS

- **HF and VHF frequency conversion**
- **Cellular radio mixer/oscillator**
- **Communication receivers**
- **Instrumentation frequency converters**
- **VHF walkie talkie**

PIN CONFIGURATION

D, N PACKAGES


INPUT A
1
INPUT B
2
GROUND
3
OUTPUT A
4
8
Vcc
7
OSCILLATOR
6
OSCILLATOR
5
OUTPUT B
TOP VIEW

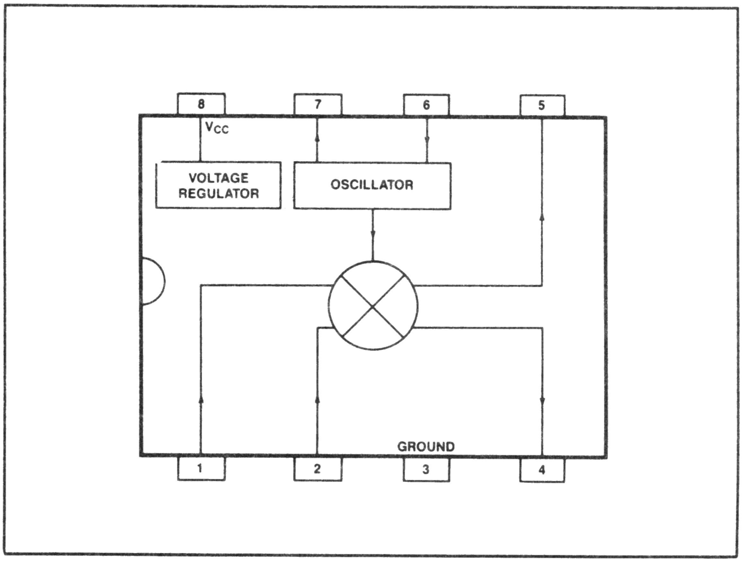
ORDER PART NUMBERS

NE602N	SA602N
NE602D	SA602D

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Maximum operating voltage	9	V
Storage temperature	−65 to +150	°C
Operating temperature NE602 SA602	 0 to +70 −40 to +85	 °C °C

BLOCK DIAGRAM


8
7
6
5
Vcc
VOLTAGE REGULATOR
OSCILLATOR
GROUND
1
2
3
4

DOUBLE BALANCED MIXER AND OSCILLATOR SA/NE602

Preliminary

DC ELECTRICAL CHARACTERISTICS: $T_A = 25°C$, $V_{CC} = 6V$.

SYMBOL AND PARAMETER	SA/NE602			UNIT
	Min	Typ	Max	
Power supply voltage range	4.5	—	8.0	V
D.C. current drain	—	2.4	2.7	mA
Input signal frequency	—	—	200	MHz
Oscillator frequency	—	—	200	MHz
Noise figure @ 45MHz	—	5.0	6	dB
Third order intercept point	—	−15	−17	dBm
Mixer input resistance	1.5	—	—	kΩ
Mixer input capacitance	—	3	3.5	pF
Mixer output resistance[1]	—	2 x 1.5	—	kΩ

NOTE:
1. Each output pin is internally connected to V_{CC} through a 1.5 (nominal) kΩ resistor.

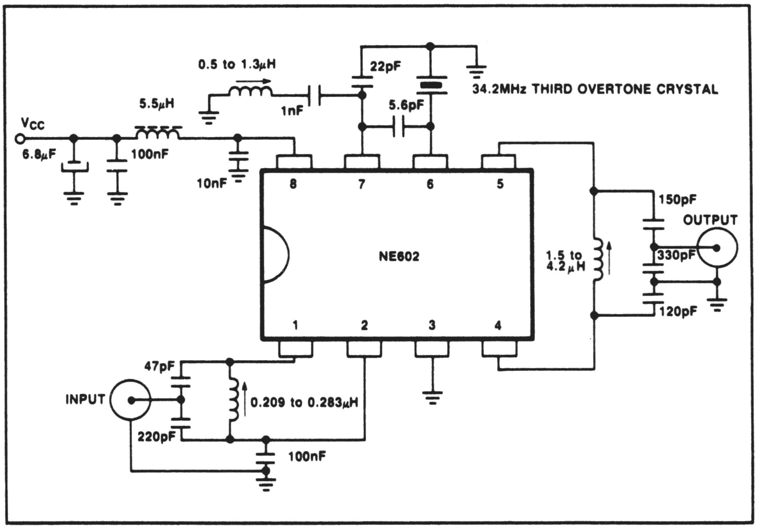
CIRCUIT DESCRIPTION

The NE602 utilizes an active double balanced mixer. The RF input port (pins 1 and 2) can be used in either a symmetrical or an asymmetrical configuration. The RF input port has a resistance of 1.5KΩ shunted by 3.0pF. In order to be used as an asymmetrical configuration, one of the two input pins (1 or 2) must be bypassed to ground with a capacitor. The RF input port does not need any external bias and should not be DC grounded. An external DC path between pins 1 and 2 is allowed.

The local oscillator is an emmitter-follower circuit and is capable of many types of oscillator configurations. Pin 6 (oscillator base) and pin 7 (oscillator emitter) do not need any external bias circuitry, but only pin 6 may have a DC path to V_{CC}. Pin 6 can be used for external oscillator or for frequency synthesizer injection.

The NE602 output pins can be used in a single-ended or push-pull configuration. There are internal 1.5KΩ resistors connected to V_{CC} for each output pin (4 and 5); therefore no external bias is needed. Pins 4 and/or 5 may have a DC path to V_{CC}.

TYPICAL APPLICATION



LOW POWER FM IF SYSTEM

SA/NE604

Preliminary

DESCRIPTION

The SA/NE604 is a monolithic low power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic signal strength indicator, and voltage regulator. The SA/NE604 is available in a 16 lead dual-in-line plastic package and 16 lead SO (surface mounted miniature package).

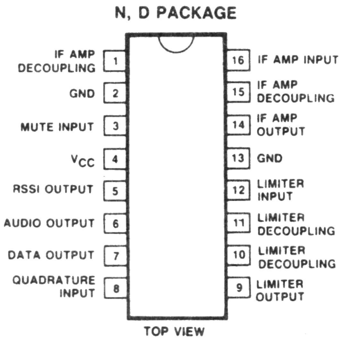
FEATURES

- Low power consumption: 2.3mA typical
- Logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB
- Separate data output
- Audio output with muting
- Low external count; suitable for crystal/ceramic filters
- Excellent sensitivity: 1.5μV across input pins (0.27 μV into 50Ω matching network) for 12dB SINAD (Signal to Noise and Distortion ratio) at 455kHz

APPLICATIONS

- Cellular Radio FM IF
- Communications receivers
- Intermediate frequency amplification and detection up to 10.7MHz
- RF level meter
- Spectrum analyzer

PIN CONFIGURATION


N, D PACKAGE
IF AMP DECOUPLING 1
GND 2
MUTE INPUT 3
VCC 4
RSSI OUTPUT 5
AUDIO OUTPUT 6
DATA OUTPUT 7
QUADRATURE INPUT 8
16 IF AMP INPUT
15 IF AMP DECOUPLING
14 IF AMP OUTPUT
13 GND
12 LIMITER INPUT
11 LIMITER DECOUPLING
10 LIMITER DECOUPLING
9 LIMITER OUTPUT
TOP VIEW

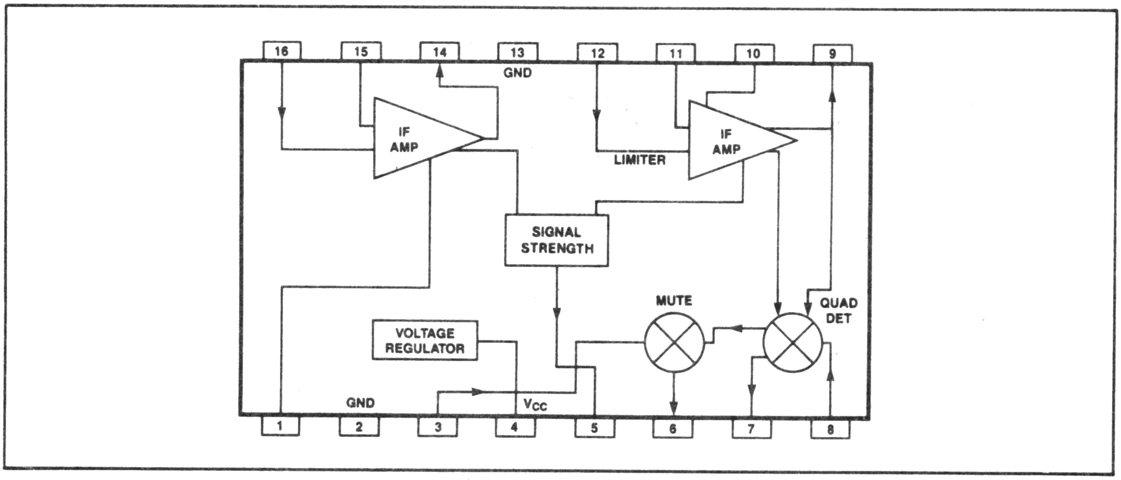
ORDER NUMBERS

NE604N, NE604D
SA604N, SA604D

ABSOLUTE MAXIMUM RATINGS

SYMBOL AND PARAMETER	RATING	UNIT
Maximum operating voltage	9	V
Storage temperature	−65 to +150	°C
Operating temperature		
NE604	0 to +70	°C
SA604	−40 to +85	°C

BLOCK DIAGRAM


16
15
14
13
GND
12
11
10
9
IF AMP
LIMITER
IF AMP
SIGNAL STRENGTH
MUTE
QUAD DET
VOLTAGE REGULATOR
GND
VCC
1
2
3
4
5
6
7
8

LOW POWER FM IF SYSTEM

SA/NE604

Preliminary

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = +6$ volts, unless otherwise stated.

SYMBOL AND PARAMETER	SA/NE604			UNITS
	Min	Typ	Max	
Power supply voltage range	4.5	-	8.0	V
D.C. current drain	-	2.3	2.7	mA
I.F. frequency	-	-	10.7	MHz
RSSI range	TBD	90	-	dB
RSSI accuracy	-	±1.5	-	dB
I.F. input impedance	1.5	-	-	kΩ
I.F. output impedance	1.0	-	-	kΩ
Limiter input impedance	1.5	-	-	kΩ
Quadrature detector data output impedance	50	-	-	kΩ
Muted audio out impedance	-	50	-	kΩ
Mute - switch input threshold (on)	1.7	-	-	V
(off)	-	-	1.0	V

CIRCUIT DESCRIPTION

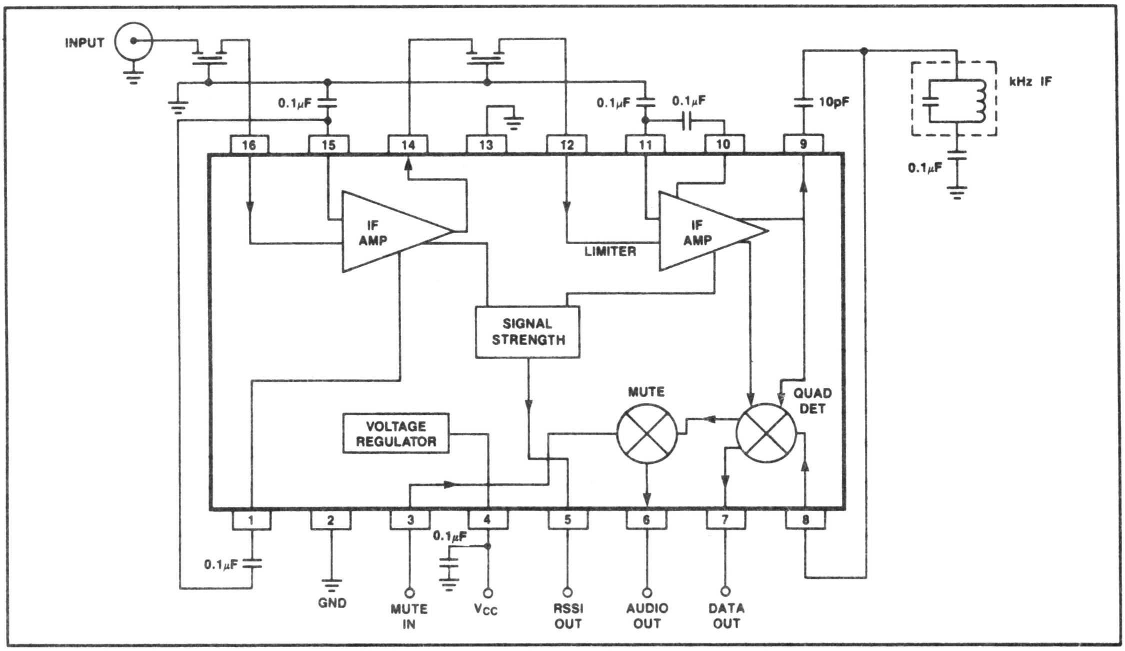
The SA/NE604's IF amplifier has a gain of 30dB, bandwidth of 15MHz, with an input impedance of 1.5KΩ and an output impedance of 1.0KΩ. The limiter has a gain of 60dB, bandwidth of 15MHz, and an input impedance of 1.5KΩ. An interstage filter between the IF Amplifier and Limiter is recommended to reduce wideband noise. The quadrature detector input (pin 8) impedance is 40KΩ.

The data (unmuted output) and audio (muted output) both have 50KΩ output impedance and their detected signals are 180 degrees out of phase with each other. The mute input (pin 3) has a very high impedance and is compatible with three and five volt CMOS and TTL levels. Little or no DC level shift occurs after muting when the quadrature detector is adjusted to the IF center frequency. Muting will attenuate the audio signal by more than 60dB and no voltage spikes will be generated by muting.

The logarithmic signal strength indicator is a current source output with maximum source current of 50 microamps. The signal strength indicator's transfer function is approximately 10 microamp per 20dB and is independent of IF frequency. The interstage filter must have a 6dB insertion loss to optimize slope linearity.

Pins 1, 16, 15, 14, 12, 11, 10, 9, and 8 do not need external bias and should not have a DC path.

TYPICAL APPLICATION



DOLBY NOISE REDUCTION CIRCUIT NE645/46

DESCRIPTION

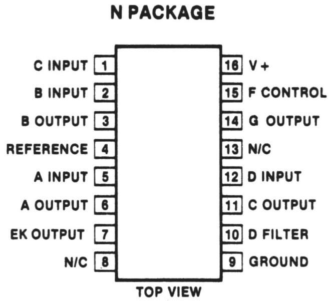
The NE645/646 is a monolithic audio noise reduction circuit designed as a direct replacement device for the NE645B/NE646B in Dolby* B-Type noise reduction systems. The NE645/646 is used to reduce the level of background noise introduced during recording and playback of audio signals on magnetic tape, and to improve the noise level in FM broadcast reception. This circuit is available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, California.

NOTE
*T.M. Dolby Laboratories Licensing Corporation.

FEATURES

- **Accurate record mode frequency response**
- **Excellent frequency response tracking with temperature and V_{CC} ±0.4 dB typical**
- **Excellent back-to-back dynamic response — D.C. shift less than 20 mV typical**
- **Improved stability of all op amps**
- **High reliability packaging**

PIN CONFIGURATION

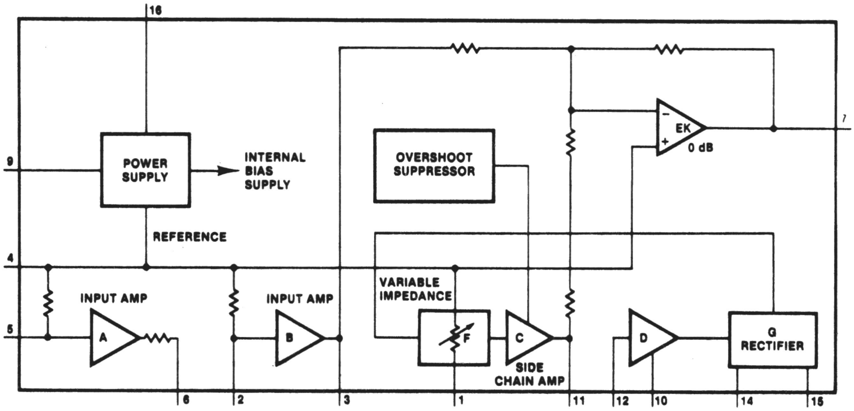

N PACKAGE
C INPUT 1
B INPUT 2
B OUTPUT 3
REFERENCE 4
A INPUT 5
A OUTPUT 6
EK OUTPUT 7
N/C 8
16 V+
15 F CONTROL
14 G OUTPUT
13 N/C
12 D INPUT
11 C OUTPUT
10 D FILTER
9 GROUND
TOP VIEW

ORDER NUMBERS
NE645N, NE646N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	24	V
Temperature range		
Operating	0 to +70	°C
Storage	−65 to +150	°C
Lead temperature (soldering, 60 sec)	+300	°C

BLOCK DIAGRAM


16
9
POWER SUPPLY
INTERNAL BIAS SUPPLY
REFERENCE
4
5
INPUT AMP
A
INPUT AMP
B
OVERSHOOT SUPPRESSOR
VARIABLE IMPEDANCE
F
C
SIDE CHAIN AMP
EK
0 dB
7
D
G RECTIFIER
6
2
3
1
11
12
10
14
15

ELECTRICAL CHARACTERISTICS

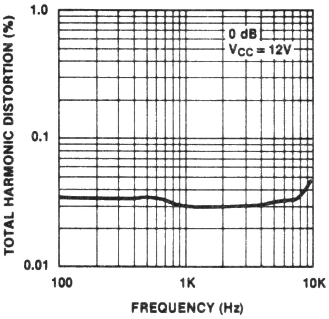
$V_{CC} = 12$ volts, f = 20 Hz to 20 kHz.
All levels referenced to 580 mVrms (0 dB) at Pin 3, $T_A = +25°C$
Unless otherwise noted.

PARAMETER	TEST CONDITIONS	NE645			NE646			UNIT
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage Range		8		20	8		20	V
Supply Current, I_{CC}	$V_{CC} = 12V$		16	24		16	24	mA
Voltage gain (Pins 5-3)	f = 1 kHz (Pins 6 and 2 connected)	24.5	26	27.5	24.5	26	27.5	dB
Voltage gain (Pins 3-7)	f = 1 kHz, 0 dB at pin 3, noise reduction out	−0.5	0	+0.5	−0.5	0	+0.5	dB
Distortion THD, 2nd and 3rd harmonic	f = 20 Hz − 10 kHz, 0dB		0.05	0.1		0.05	0.2	%
	f = 20 Hz − 10 kHz, +10 dB		0.15	0.3		0.2	0.5	%
Signal handling[1] ($V_{CC} = 12V$)	1% dist at 1 kHz	+12	+15		+12	+15		dB
Signal-to-noise ratio[2]	Record mode	67	72		64	72		dB
	Playback mode	77	82		74	82		dB
Record mode Frequency response (at pin 7) referenced to encode monitor point (pin 3)	f = 1.4kHz 0dB	−1	0	+1	−1.5	0	+1.5	dB
	−20dB	−16.6	−15.6	−14.6	−17.1	−15.6	−14.1	dB
	−30dB	−23.5	−22.5	−21.5	−24.0	−22.5	−21.0	dB
	f = 5kHz 0dB	−0.7	+0.3	+1.3	−1.2	+0.3	+1.8	dB
	−20dB	−17.8	−16.8	−15.8	−18.3	−16.8	−15.3	dB
	−30dB	−22.8	−21.8	−20.8	−23.3	−21.8	−20.3	dB
	−40dB	−30.2	−29.7	−28.7	−30.2	−29.7	−28.2	dB
	f = 20kHz 0dB	−0.3	+0.7	+1.7	−0.8	+0.7	+2.2	dB
	−20dB	−18.3	−17.3	−16.3	−18.8	−17.3	−15.8	dB
	−30dB	−24.5	−23.5	−22.5	−25.0	−23.5	−22.0	dB
Back-to-back frequency response	Using typical record mode frequency response test points	−1	0	+1	−1.5	0	+1.5	dB
Input resistance	Pin 5	35	50	65	35	50	65	kΩ
	Pin 2	3.1	4.2	5.3	3.1	4.2	5.3	kΩ
Output resistance	Pin 6	1.9	2.4	3.1	1.9	2.4	3.1	kΩ
	Pin 3		80	120		80	120	Ω
	Pin 7		80	120		80	120	Ω
Back-to-back frequency response shift Versus temperature	0°-70°C		±0.4			±0.4		dB
Versus supply voltage	8-20V		±0.4			±0.4		dB

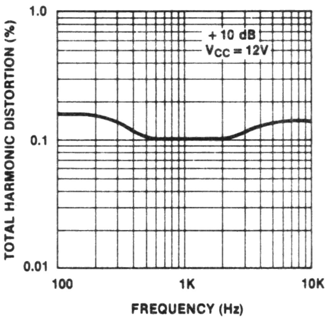
NOTES
1. See maximum signal handling versus supply voltage characteristics.
2. All noise levels are measured CCIR/ARM weighted using a 10K source with respect to Dolby level. See Dolby Laboratories Bulletin 19.

PERFORMANCE CHARACTERISTICS

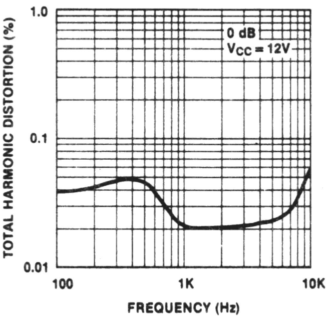
THD vs FREQUENCY RECORD MODE



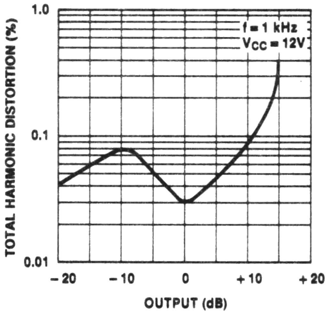
THD vs FREQUENCY RECORD MODE



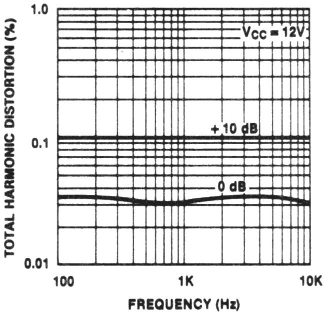
THD vs FREQUENCY PLAY MODE



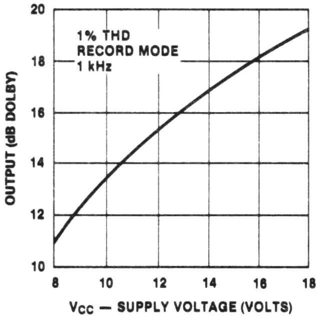
THD vs OUTPUT RECORD MODE



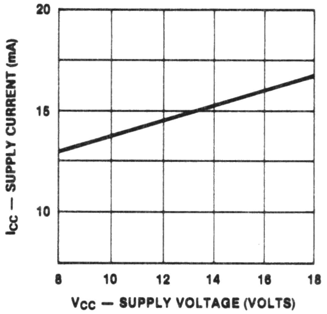
THD vs FREQUENCY NOISE REDUCTION (NR) OFF



MAXIMUM SIGNAL HANDLING vs SUPPLY VOLTAGE



SUPPLY CURRENT vs SUPPLY VOLTAGE



DOLBY NOISE REDUCTION CIRCUIT NE645/46

APPLICATION INFORMATION

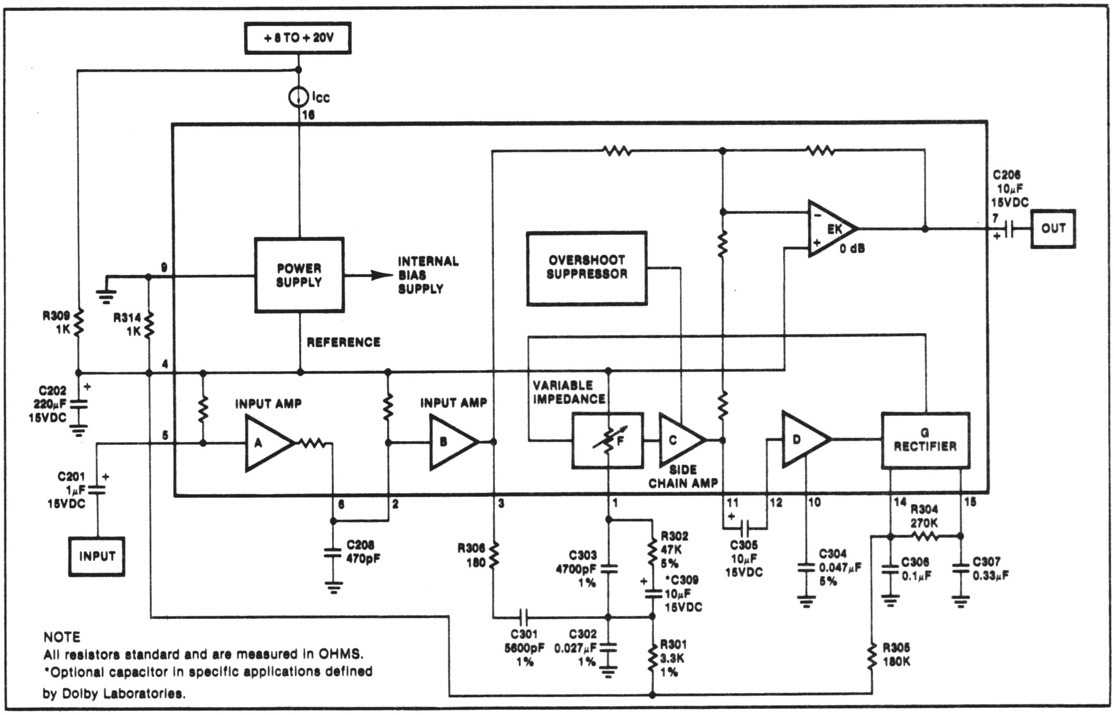
The NE645/646 is a direct replacement for the NE645B/646B. The NE645/646 incorporates improved design techniques to insure excellent performance required in Dolby B and C Type Audio Noise Reduction Systems. Critical component values are unchanged except for C309 on Pin 1 which is now an optional component in specific applications defined by Dolby Laboratories. All circuit parameters are guaranteed at 12V V_{CC}.

DOLBY ENCODER Output for constant level input (single tone frequency response)

Frequency (kHz)	Input Level (dB)								
	0 (Dolby Level)	-5	-10	-15	-20	-25	-30	-35	-40
0.1	0	0.1	0	0.1	0	0	0	0	0
0.14	0	0.2	0.2	0.2	0.2	0.2	0.1	0.2	0.1
0.2	0	0.3	0.4	0.5	0.5	0.6	0.6	0.5	0.5
0.3	0	0.3	0.6	1.1	1.3	1.3	1.3	1.3	1.3
0.4					2.0	2.1	2.2	2.3	2.1
0.5	0	0.3	0.8	1.8	2.6	2.9	2.9	3.0	2.9
0.6						3.6	3.7	3.8	3.7
0.7	0	0.4	0.9	2.1	3.5	4.3	4.4	4.5	4.4
0.8						4.8	5.0	5.3	5.1
0.9							5.6	5.8	5.6
1.0	0	0.4	1.0	2.3	4.2	5.7	6.1	6.3	6.2
1.2							6.9	7.1	7.1
1.4	0	0.3	0.9	2.3	4.4	6.6	7.5	7.7	7.7
2.0	0.1	0.4	0.9	2.2	4.3	7.0	8.5	8.9	8.9
3.0	0.2	0.6	0.9	1.9	3.9	6.6	8.8	9.7	9.7
5.0	0.3	0.6	1.0	1.7	3.2	5.4	8.2	10.0	10.3
7.0	0.3	0.6	1.0	1.7	2.8	4.7	7.3	9.7	10.4
10.0	0.4	0.7	1.1	1.7	2.6	4.2	6.5	9.1	10.4
14.0	0.5	0.8	1.1	1.8	2.7	4.4	6.5	8.7	10.3
20.0	0.7	0.7	1.2	1.9	2.7	4.4	6.5	8.7	10.3

NOTE
The figures given in this table are the average response of many of Dolby Laboratories' professional encoders, and are not intended to be taken as required consumer equipment performance characteristics. Thus, no inference should be drawn on the tolerances which licensees must retain in consumer equipment. The figures can, however, be used to plot typical characteristics.

TEST CIRCUIT NE645/646


+8 TO +20V
Icc
16
C206
10µF
15VDC
7
OUT
EK
0 dB
OVERSHOOT SUPPRESSOR
9
POWER SUPPLY
INTERNAL BIAS SUPPLY
R309
1K
R314
1K
REFERENCE
4
C202
220µF
15VDC
INPUT AMP
A
INPUT AMP
B
VARIABLE IMPEDANCE
F
C
SIDE CHAIN AMP
D
G
RECTIFIER
5
C201
1µF
15VDC
INPUT
6
2
C208
470pF
3
R306
180
1
C303
4700pF
1%
R302
47K
5%
*C309
10µF
15VDC
11
12
10
C305
10µF
15VDC
C304
0.047µF
5%
14
R304
270K
15
C306
0.1µF
C307
0.33µF
C301
5600pF
1%
C302
0.027µF
1%
R301
3.3K
1%
R305
180K

NOTE
All resistors standard and are measured in OHMS.
*Optional capacitor in specific applications defined by Dolby Laboratories.

LOW VOLTAGE DOLBY NOISE REDUCTION CIRCUIT NE648/49

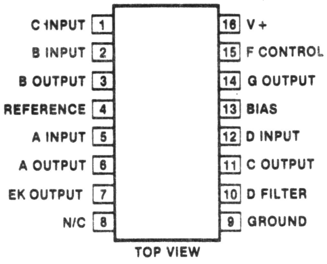
DESCRIPTION

The NE648/649 is an audio noise reduction circuit designed for use in low voltage entertainment systems. The circuit is used to reduce the level of background noise introduced during the recording and playback of audio signals on magnetic tape and improve the noise level in FM broadcast reception. The circuit is intended for use in automotive and portable cassette Dolby* B-Type noise reduction systems. This circuit is available only to licensees of Dolby Laboratories Licensing Corp., San Francisco.

NOTE
*T.M. Dolby Laboratories Licensing Corporation

PIN CONFIGURATION

N PACKAGE

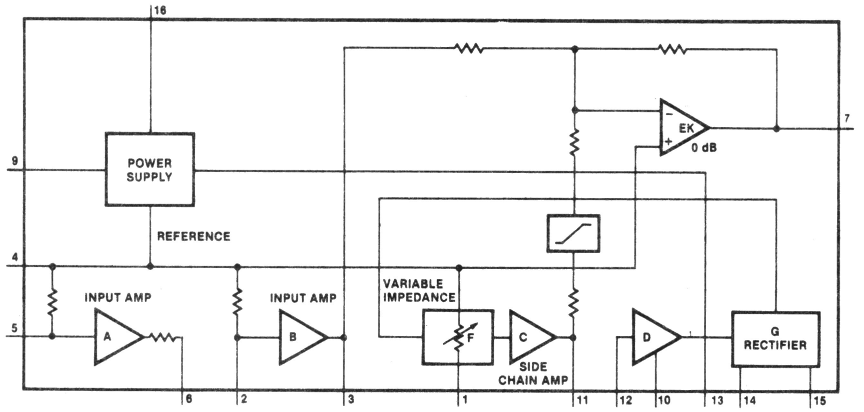

C INPUT 1
B INPUT 2
B OUTPUT 3
REFERENCE 4
A INPUT 5
A OUTPUT 6
EK OUTPUT 7
N/C 8
16 V+
15 F CONTROL
14 Q OUTPUT
13 BIAS
12 D INPUT
11 C OUTPUT
10 D FILTER
9 GROUND
TOP VIEW

ORDER NUMBERS
NE648N, NE649N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	16	V
Temperature range		
Operating	−40 to +85	°C
Storage	−65 to +150	°C
Lead temperature (soldering 60sec)	+300	°C

BLOCK DIAGRAM


16
9
POWER SUPPLY
REFERENCE
4
5
INPUT AMP
A
INPUT AMP
B
VARIABLE IMPEDANCE
F
C
SIDE CHAIN AMP
EK
0 dB
7
D
G RECTIFIER
6
2
3
1
11
12
10
13
14
15

LOW VOLTAGE DOLBY NOISE REDUCTION CIRCUIT NE648/49

DC ELECTRICAL CHARACTERISTICS $V_{CC}=9V$, f = 20Hz to 20kHz.

All levels referenced to 580mVrms (0dB) at pin 3, $T_A = +25°C$ unless otherwise noted.

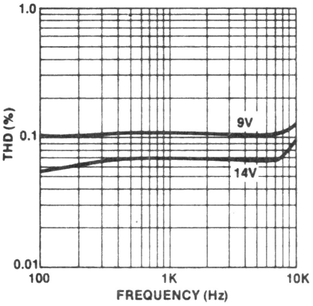
PARAMETER	TEST CONDITIONS	NE648			NE649			UNIT
		Min	Typ	Max	Min	Typ	Max	
Supply voltage range[3]		6	9	14	6	9	14	V
Minimum voltage supply for	f = 1.4kHz THD < 1%							
8dB headroom		6.5			6.5			V
10dB headroom		7.5			7.5			V
Supply Current, I_{CC}			11	18		11	18	mA
Supply Current,[1] I_{CC}				20			20	mA
Voltage gain (pins 5-3)	f = 1kHz (pins 6 and 2 connected)	24.5	26	27.5	24.5	26	27.5	dB
Voltage gain (pins 3-7)	f = 1kHz, 0dB at pin 3, noise reduction out	−0.5	0	+0.5	−0.5	0	+0.5	dB
Distortion	f = 20kHz to 10kHz, 0dB		0.05	0.1		0.05	0.2	%
	f = 20Hz to 10kHz, +10dB		0.2	0.3		0.2	0.5	%
Signal Handling (See Performance Characteristics)								
Signal-to-noise ratio[2]	Record (pins 6 and 2 connected)	67	72		64	72		dB
	Playback (pins 6 and 2 connected)	77	82		74	82		dB
Record mode frequency response (at pin 7) referenced to encode monitor point (pin 3)	f = 1.4kHz							
	0dB	−1	0	+1	−1.5	0	+1.5	dB
	−20dB	−16.6	−15.6	−14.6	−17.1	−15.6	−14.1	dB
	−30dB	−23.5	−22.5	−21.5	−24.0	−22.5	−21.0	dB
	f = 5kHz							
	0dB	−0.7	+0.3	+1.3	−1.2	+0.3	+1.8	dB
	−20dB	−17.8	−16.8	−15.8	−18.3	−16.8	−15.3	dB
	−30dB	−22.8	−21.8	−20.8	−23.3	−21.8	−20.3	dB
	−40dB	−30.2	−29.7	−28.7	−30.2	−29.7	−28.2	dB
	f = 20kHz							
	0dB	−0.3	+0.7	+1.7	−0.8	+0.7	+2.2	dB
	−20dB	−18.3	−17.3	−16.3	−18.8	−17.3	−15.8	dB
	−30dB	−24.5	−23.5	−22.5	−25.0	−23.5	−22.0	dB
Back-to-back frequency response	Using typical record mode response		±1.0			±1.5		dB
Input resistance	Pin 5	35	50	65	35	50	65	kΩ
	Pin 2	3.1	4.2	5.3	3.1	4.2	5.3	kΩ
Output resistance	Pin 6	1.9	2.4	3.1	1.9	2.4	3.1	kΩ
	Pin 3		80	120		80	120	Ω
	Pin 7		80	120		80	120	Ω
Record mode frequency response shift								
Versus temperature	0 to 70°C		±0.3					dB
	−40 to 85°C		±0.5					dB
Versus V_{CC}	6 to 14V		0.2					dB/V

NOTES

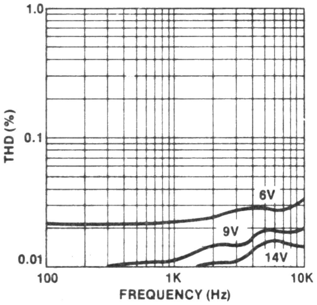
1. With electronic switching.
2. All noise levels are measured CCIR/ARM weighted using a 10K source with respect to Dolby level. See Dolby Laboratories Bulletin 19.
3. The circuit will function as low as $V_{CC} = 4.5V$ (i.e. output signal present). See graphs of I_{CC} and signal handling vs V_{CC}.

PERFORMANCE CHARACTERISTICS

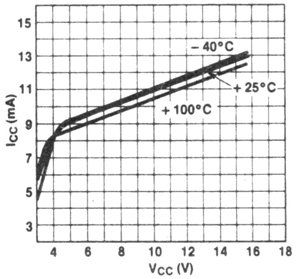
(+10dB) THD vs FREQUENCY



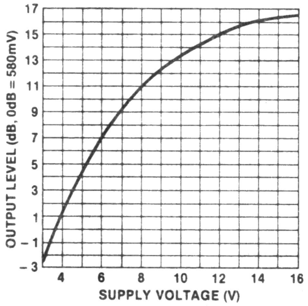
(0dB) THD vs FREQUENCY



CURRENT vs SUPPLY VOLTAGE



MAXIMUM SIGNAL HANDLING vs SUPPLY VOLTAGE FOR 1% THD (RECORD)



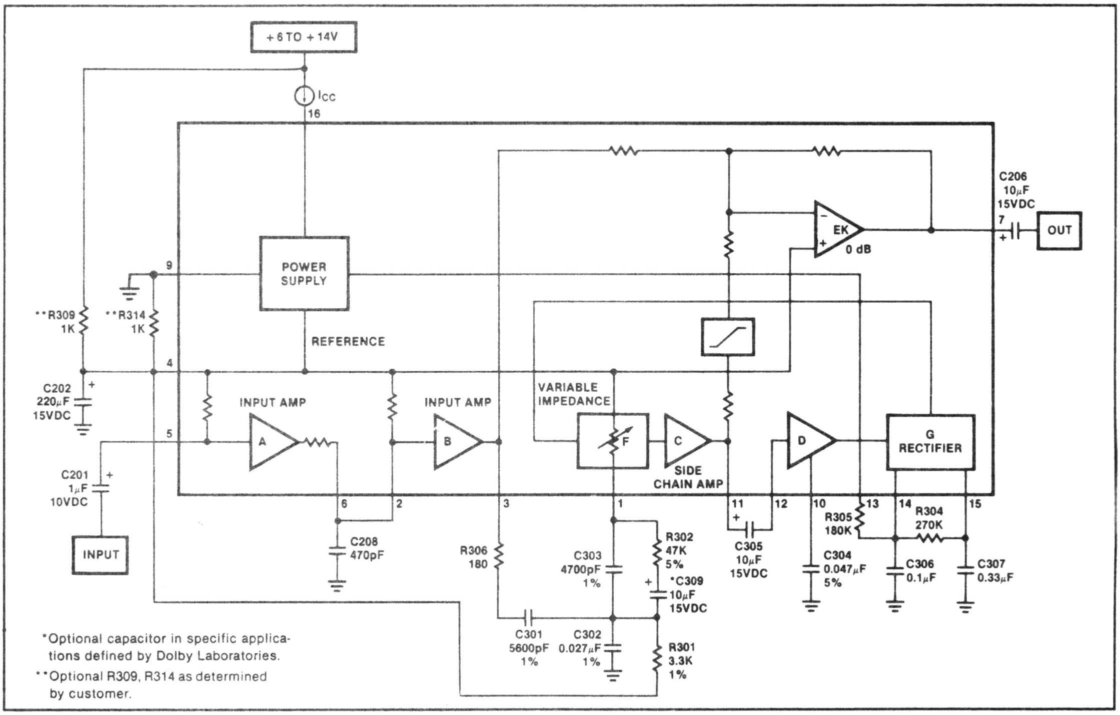
LOW VOLTAGE DOLBY NOISE REDUCTION CIRCUIT NE648/49

DOLBY ENCODER Output for constant level input (single tone frequency response)

Frequency (kHz)	Input Level (dB)								
	0 (Dolby Level)	-5	-10	-15	-20	-25	-30	-35	-40
0.1	0	0.1	0	0.1	0	0	0	0	0
0.14	0	0.2	0.2	0.2	0.2	0.2	0.1	0.2	0.1
0.2	0	0.3	0.4	0.5	0.5	0.6	0.6	0.5	0.5
0.3	0	0.3	0.6	1.1	1.3	1.3	1.3	1.3	1.3
0.4					2.0	2.1	2.2	2.3	2.1
0.5	0	0.3	0.8	1.8	2.6	2.9	2.9	3.0	2.9
0.6						3.6	3.7	3.8	3.7
0.7	0	0.4	0.9	2.1	3.5	4.3	4.4	4.5	4.4
0.8						4.8	5.0	5.3	5.1
0.9							5.6	5.8	5.6
1.0	0	0.4	1.0	2.3	4.2	5.7	6.1	6.3	6.2
1.2							6.9	7.1	7.1
1.4	0	0.3	0.9	2.3	4.4	6.6	7.5	7.7	7.7
2.0	0.1	0.4	0.9	2.2	4.3	7.0	8.5	8.9	8.9
3.0	0.2	0.6	0.9	1.9	3.9	6.6	8.8	9.7	9.7
5.0	0.3	0.6	1.0	1.7	3.2	5.4	8.2	10.0	10.3
7.0	0.3	0.6	1.0	1.7	2.8	4.7	7.3	9.7	10.4
10.0	0.4	0.7	1.1	1.7	2.6	4.2	6.5	9.1	10.4
14.0	0.5	0.8	1.1	1.8	2.7	4.4	6.5	8.7	10.3
20.0	0.7	0.7	1.2	1.9	2.7	4.4	6.5	8.7	10.3

NOTE
The figures given in this table are the average response of many of Dolby Laboratories' professional encoders, and are not intended to be taken as required consumer equipment performance characteristics. Thus, no inference should be drawn on the tolerances which licensees must retain in consumer equipment. The figures can, however, be used to plot typical characteristics.

TEST CIRCUIT NE648/49


+6 TO +14V
ICC
16
9
POWER SUPPLY
REFERENCE
**R309 1K
**R314 1K
4
C202 220µF 15VDC
5
C201 1µF 10VDC
INPUT
INPUT AMP
A
INPUT AMP
B
VARIABLE IMPEDANCE
F
C
SIDE CHAIN AMP
D
G RECTIFIER
EK
0 dB
C206 10µF 15VDC
7
OUT
6
2
3
1
11
12
10
13
14
15
C208 470pF
R306 180
C303 4700pF 1%
R302 47K 5%
*C309 10µF 15VDC
C301 5600pF 1%
C302 0.027µF 1%
R301 3.3K 1%
C305 10µF 15VDC
C304 0.047µF 5%
R305 180K
R304 270K
C306 0.1µF
C307 0.33µF

*Optional capacitor in specific applications defined by Dolby Laboratories.

**Optional R309, R314 as determined by customer.

DOLBY B TYPE NOISE REDUCTION CIRCUIT NE650

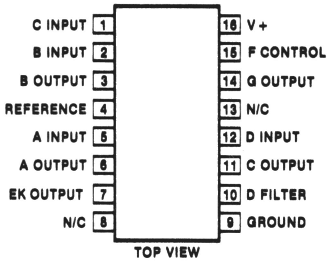
DESCRIPTION

The NE650 is a monolithic audio noise reduction circuit designed for use in Dolby* B Type noise reduction systems. The NE650 is used to reduce the level of background noise introduced during recording and playback of audio signals on magnetic tape. The NE650 features excellent dynamic characteristics over a wide range of operating conditions and is pin compatible with NE645/646. This circuit is available only to licensees of Dolby Laboratories Licensing Corp., San Francisco.

NOTE
*T.M. Dolby Laboratories Licensing Corporation.

PIN CONFIGURATION

N PACKAGE

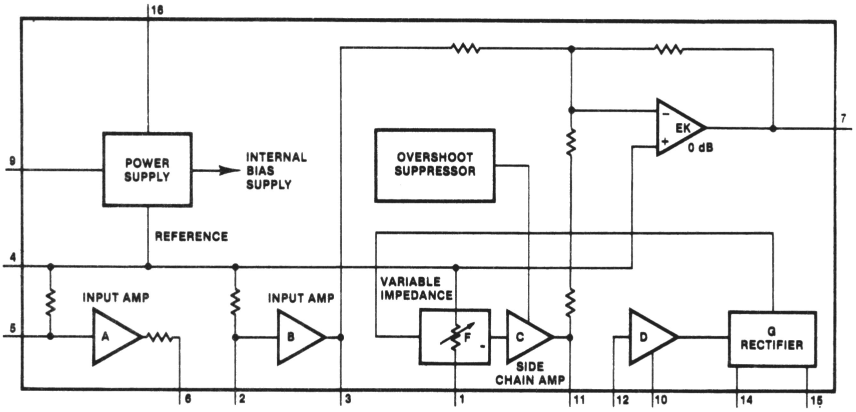

C INPUT 1
B INPUT 2
B OUTPUT 3
REFERENCE 4
A INPUT 5
A OUTPUT 6
EK OUTPUT 7
N/C 8
16 V+
15 F CONTROL
14 G OUTPUT
13 N/C
12 D INPUT
11 C OUTPUT
10 D FILTER
9 GROUND
TOP VIEW

ORDER NUMBER
NE650N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	24	V
Temperature range		
Operating	0 to +70	°C
Storage	−65 to +150	°C
Lead temperature (soldering 60sec)	+300	°C

BLOCK DIAGRAM


16
9
POWER SUPPLY
INTERNAL BIAS SUPPLY
REFERENCE
4
5
INPUT AMP
A
INPUT AMP
B
OVERSHOOT SUPPRESSOR
VARIABLE IMPEDANCE
F
C
SIDE CHAIN AMP
EK
0 dB
7
D
G RECTIFIER
6
2
3
1
11
12
10
14
15

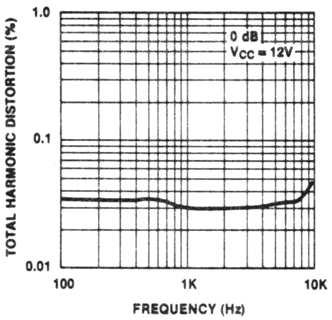
DC ELECTRICAL CHARACTERISTICS $V_{CC} = 12V$, f = 20Hz to 20kHz.
All levels referenced to 580mVrms (0dB) at pin 3, $T_A = +25°C$ unless otherwise noted.

PARAMETER	TEST CONDITIONS	NE650			UNIT
		Min	Typ	Max	
Supply voltage range		8		20	V
Supply current, I_{CC}	Electronic switching on		16	24	mA
Voltage gain (pins 5-3)	f = 1kHz (pins 6 and 2 connected)	25.5	26	26.5	dB
Voltage gain (pins 3-7)	f = kHz, 0dB at pin 3, noise reduction out	−0.5	0	+0.5	dB
Voltage gain (pins 2-3)	f = 1kHz		13		dB
Distortion	f = 20Hz to 10kHz, 0dB		0.05	0.1	%
THD; 2nd and 3rd harmonic	f = 20Hz to 10kHz, +10dB		0.15	0.3	%
Signal handling	1% distortion at 1kHz	+12	+15		dB
Signal-to-noise ratio*	Record mode	68	72		dB
	Playback mode	78	82		dB
Back-to-back frequency response	Using typical record mode response		±0.5		dB
Record mode frequency response (at pin 7) referenced to encode monitor point (pin 3)	f = 1.4kHz				
	0dB	−0.5	0	+0.5	dB
	−20dB	−16.1	−15.6	−15.1	dB
	−30dB	−23.5	−22.5	−21.5	dB
	f = 5kHz				
	0dB	−0.7	+0.3	+1.3	dB
	−20dB	−17.3	−16.8	−16.3	dB
	−30dB	−22.3	−21.8	−21.3	dB
	−40dB	−30.2	−29.7	−29.2	dB
	f = 20kHz				
	0dB	−0.3	+0.7	+1.7	dB
	−20dB	−18.3	−17.3	−16.3	dB
	−30dB	−24.5	−23.5	−22.5	dB
Input resistance	Pin 5	35	50	65	kΩ
	Pin 2	3.1	4.2	5.3	kΩ
Output resistance	Pin 6	1.9	2.4	3.1	kΩ
	Pin 3		80	120	Ω
	Pin 7		80	120	Ω
Back-to-back frequency response shift					
Versus T_A	0°C to −70°C		±0.4		dB
Versus V_{CC}	8 to 20V		±0.4		dB

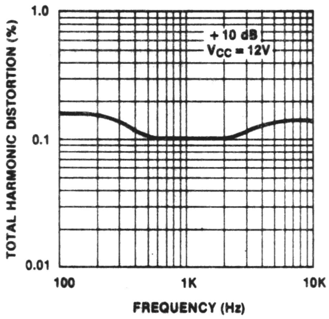
*All noise levels are measured CCIR/ARM weighted using a 10K source with respect to Dolby level. See Dolby Laboratories Bulletin 19.

PERFORMANCE CHARACTERISTICS

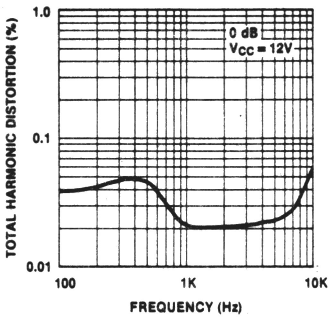
THD vs FREQUENCY RECORD MODE



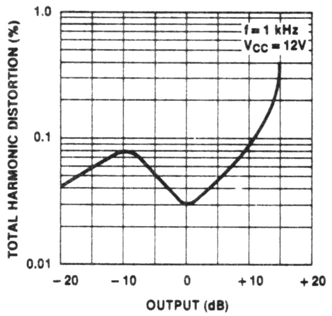
THD vs FREQUENCY RECORD MODE



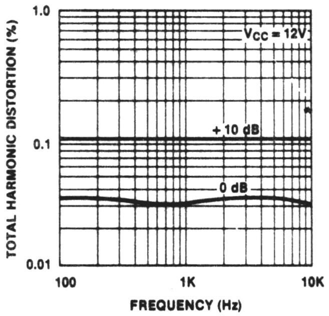
THD vs FREQUENCY PLAY MODE



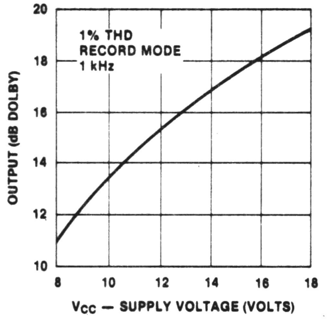
THD vs OUTPUT RECORD MODE



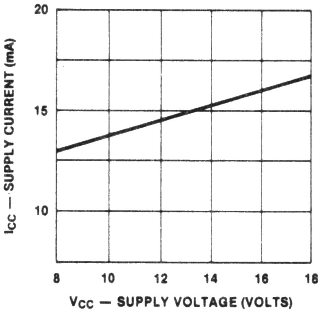
THD vs FREQUENCY
NOISE REDUCTION (NR) OFF



MAXIMUM SIGNAL HANDLING vs
SUPPLY VOLTAGE



SUPPLY CURRENT vs
SUPPLY VOLTAGE



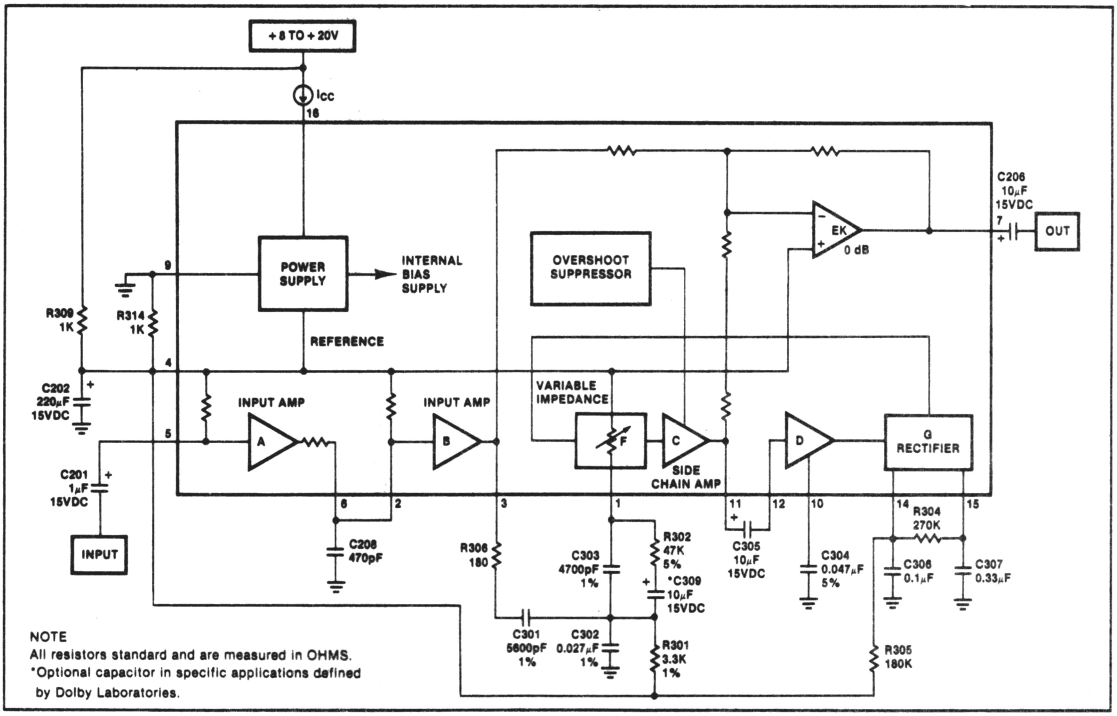
DOLBY B TYPE NOISE REDUCTION CIRCUIT NE650

DOLBY ENCODER Output for constant level input (single tone frequency response)

Frequency (kHz)	Input Level (dB)								
	0 (Dolby Level)	-5	-10	-15	-20	-25	-30	-35	-40
0.1	0	0.1	0	0.1	0	0	0	0	0
0.14	0	0.2	0.2	0.2	0.2	0.2	0.1	0.2	0.1
0.2	0	0.3	0.4	0.5	0.5	0.6	0.6	0.5	0.5
0.3	0	0.3	0.6	1.1	1.3	1.3	1.3	1.3	1.3
0.4					2.0	2.1	2.2	2.3	2.1
0.5	0	0.3	0.8	1.8	2.6	2.9	2.9	3.0	2.9
0.6						3.6	3.7	3.8	3.7
0.7	0	0.4	0.9	2.1	3.5	4.3	4.4	4.5	4.4
0.8						4.8	5.0	5.3	5.1
0.9							5.6	5.8	5.6
1.0	0	0.4	1.0	2.3	4.2	5.7	6.1	6.3	6.2
1.2							6.9	7.1	7.1
1.4	0	0.3	0.9	2.3	4.4	6.6	7.5	7.7	7.7
2.0	0.1	0.4	0.9	2.2	4.3	7.0	8.5	8.9	8.9
3.0	0.2	0.6	0.9	1.9	3.9	6.6	8.8	9.7	9.7
5.0	0.3	0.6	1.0	1.7	3.2	5.4	8.2	10.0	10.3
7.0	0.3	0.6	1.0	1.7	2.8	4.7	7.3	9.7	10.4
10.0	0.4	0.7	1.1	1.7	2.6	4.2	6.5	9.1	10.4
14.0	0.5	0.8	1.1	1.8	2.7	4.4	6.5	8.7	10.3
20.0	0.7	0.7	1.2	1.9	2.7	4.4	6.5	8.7	10.3

NOTE
The figures given in this table are the average response of many of Dolby Laboratories' professional encoders, and are not intended to be taken as required consumer equipment performance characteristics. Thus, no inference should be drawn on the tolerances which licensees must retain in consumer equipment. The figures can, however, be used to plot typical characteristics.

TEST CIRCUIT NE650


+8 TO +20V
Icc
16
POWER SUPPLY
INTERNAL BIAS SUPPLY
REFERENCE
OVERSHOOT SUPPRESSOR
EK
0 dB
C206 10μF 15VDC
7
OUT
9
R309 1K
R314 1K
4
C202 220μF 15VDC
5
C201 1μF 15VDC
INPUT
INPUT AMP
A
INPUT AMP
B
VARIABLE IMPEDANCE
F
C
SIDE CHAIN AMP
D
G RECTIFIER
6
2
3
1
11
12
10
14
15
C208 470pF
R306 180
C303 4700pF 1%
R302 47K 5%
*C309 10μF 15VDC
C305 10μF 15VDC
C304 0.047μF 5%
R304 270K
C306 0.1μF
C307 0.33μF
C301 5600pF 1%
C302 0.027μF 1%
R301 3.3K 1%
R305 180K

NOTE
All resistors standard and are measured in OHMS.
*Optional capacitor in specific applications defined by Dolby Laboratories.

DOLBY NOISE REDUCTION SYSTEM NE660

Preliminary

DESCRIPTION

The NE660 is a monolithic audio noise reduction circuit designed for low power supply voltage applications. It is used to reduce the level of background noise introduced during recording and playback of audio signals on magnetic tape. This circuit is available only to licensees of Dolby* Laboratories Licensing Corporation, San Francisco, California.

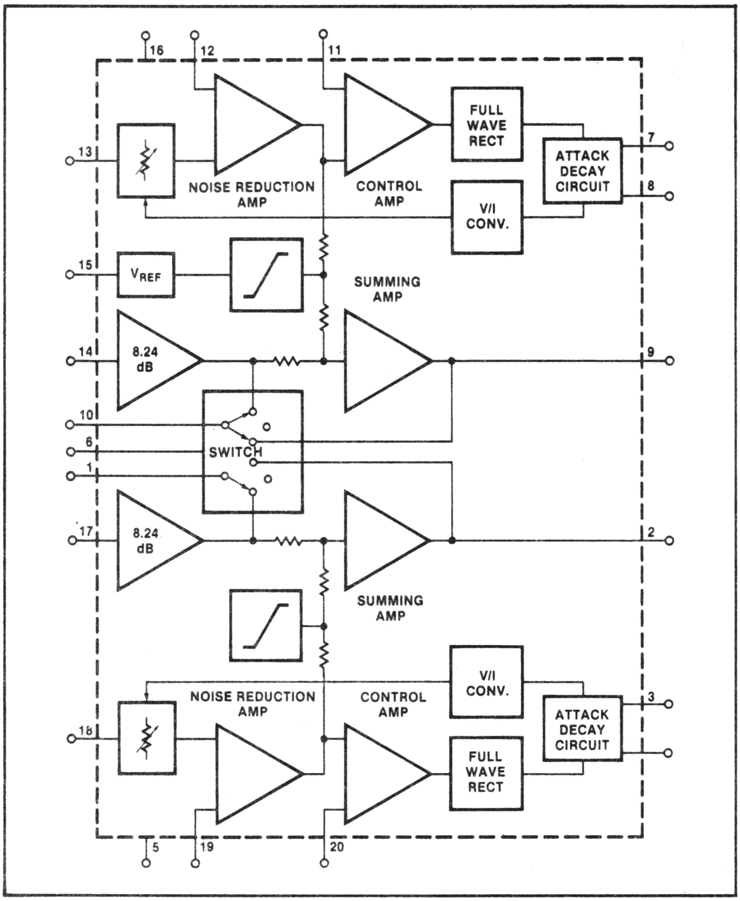
FEATURES

- **Low voltage operation**
- **Large headroom (17dB typical at 1.8V)**
- **Single or dual supply operation**
- **Excellent channel to channel matching**
- **Low noise**
- **Very low distortion**
- **Electronic Record/Play, on/off switch**
- **Minimum external part count**

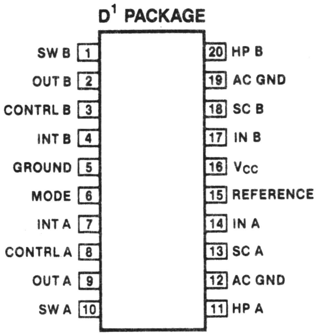
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	8	V
Temperature range		
Operating	−20 to +70	°C
Storage	−65 to +150	°C

BLOCK DIAGRAM


16
12
11
FULL WAVE RECT
ATTACK DECAY CIRCUIT
7
8
13
NOISE REDUCTION AMP
CONTROL AMP
V/I CONV.
15
V_{REF}
SUMMING AMP
14
8.24 dB
9
10
6
1
SWITCH
17
8.24 dB
2
SUMMING AMP
V/I CONV.
NOISE REDUCTION AMP
CONTROL AMP
3
ATTACK DECAY CIRCUIT
18
FULL WAVE RECT
5
19
20

PIN CONFIGURATION


D[1] PACKAGE
SW B 1
OUT B 2
CONTRL B 3
INT B 4
GROUND 5
MODE 6
INT A 7
CONTRL A 8
OUT A 9
SW A 10
20 HP B
19 AC GND
18 SC B
17 IN B
16 Vcc
15 REFERENCE
14 IN A
13 SC A
12 AC GND
11 HP A

TOP VIEW
ORDER NUMBER
NE660D[1]

1. Switch output channel B
2. Output channel B
3. Control voltage B
4. Integrating filter B
5. Ground
6. Mode
7. Integrating filter A
8. Control voltage A
9. Output channel A
10. Switch output channel A
11. High pass filter channel A
12. AC ground channel A
13. Side chain channel A
14. Input channel A
15. Reference
16. V_{CC}
17. Input channel B
18. Side chain channel B
19. AC ground channel B
20. High pass filter channel B

[1] SOL - Released in Large SO package only.
[2] SOL and non-standard pinout.
[3] SO and non-standard pinots.

---

*Available only to licensees of Dolby Laboratories Corporation, San Francisco, from whom licensing and application information must be obtained.
Dolby is a registered trademark of Dolby Laboratories Corporation, San Francisco, California.

DOLBY NOISE REDUCTION SYSTEM NE660

Preliminary

ELECTRICAL CHARACTERISTICS STANDARD CONDITIONS: $V_{CC} = 3V$, frequency range: 20Hz-20kHz, $T_A = 25°C$. All levels referenced to 77.5mV = 0dB at test point (T.P.) in test circuit of Fig. 1.

SYMBOL & PARAMETER	MODE	FREQ. Hz	TEST CONDITIONS	LIMITS			UNIT
				MIN	TYP	MAX	
Supply Voltage Range				1.8	3	7	V
Supply Current	Off		No input signal		6	9	mA
Voltage Gain	Off	1K	$20 \log \frac{V \text{ (Pin 2 or 9)}}{V \text{ (Pin 17 or 14)}}$	7.25	8.25	9.25	dB
Signal Handling at Output, Note 1	Off	1K	THD = 1%		20		dB
	R	1K	THD = 1%	18	22		dB
			$V_{CC} = 1.8V$, THD = 1%	12	17		dB
Distortion, Note 4	Off	1K	0dB		.02	.1	%
Distortion + Noise			+ 12dB		.03	.15	%
Distortion, Note 4	R	1K	0dB		.03	.25	%
Distortion + Noise			+ 12dB		.04	.2	%
Signal to Noise Ratio, Note 2	R		CCIR/ARM	64	69		dB
	P				80		dB
Frequency Response, Note 3	R	1K	T.P. Level = 0dB	− 1	0	+ 1	dB
		10K		− 1	+ .3	+ 1.5	dB
		2K	T.P. Level = − 25dB	− 19.5	− 18	− 16.5	dB
		10K	T.P. Level = − 30dB	− 25	− 23.5	− 22	dB
		5K	T.P. Level = − 40dB	− 30.2	− 29.7	− 28.7	dB
Channel to Channel Unbalance	R	2K	T.P. Level = − 20dB		.2	1.3	dB
Channel to Channel Crosstalk	R	2K	0dB in Channel "A"	50			dB
Ripple Rejection	R	50			48		dB
Input Resistance			No input termination	35	50	65	kOhm
Switching Thresholds (Relative to Voltage on Pin 15)	Off		Voltage at Pin 6	− .5		+ .5	V
	R			+ .8			V
	P					− .8	V
Maximum Frequency Response Shift vs. Temperature (Relative to $T_A = 25°C$)	R	20Hz to 20K	$-20 \leq T_A \leq 70°C$		± 1		dB
Maximum Frequency Response Shift vs. Supply Voltage (Relative to $V_{CC} = 3V$)	R	2K	T.P. Level = − 20dB $1.8 \leq V_{CC} \leq 7V$		± .2	± .6	dB

NOTES:

1. 12dB headroom guaranteed at 1.8V; however, system remains operational to $V_{CC} = 1.6V$.
2. See Dolby Laboratories bulletin No. 19.
3. In DC coupled configuration when Pins 12 and 19 are connected to Pin 15, the RECORD curves might read slightly different than in AC coupled mode (Fig. 1). The variation is typically .5dB at the worst case input level/frequency combination. A slight degradation of Channel to Channel Crosstalk will also occur. When device is intended for use in DC coupled configuration, factory test is to be requested accordingly.
4. 0dB distortion is specified with each harmonic measured in a 20Hz B.W. 12dB distortion is specified as the wideband (20Hz-20kHz) measurement of the harmonics plus noise.

DOLBY NOISE REDUCTION SYSTEM NE660

Preliminary

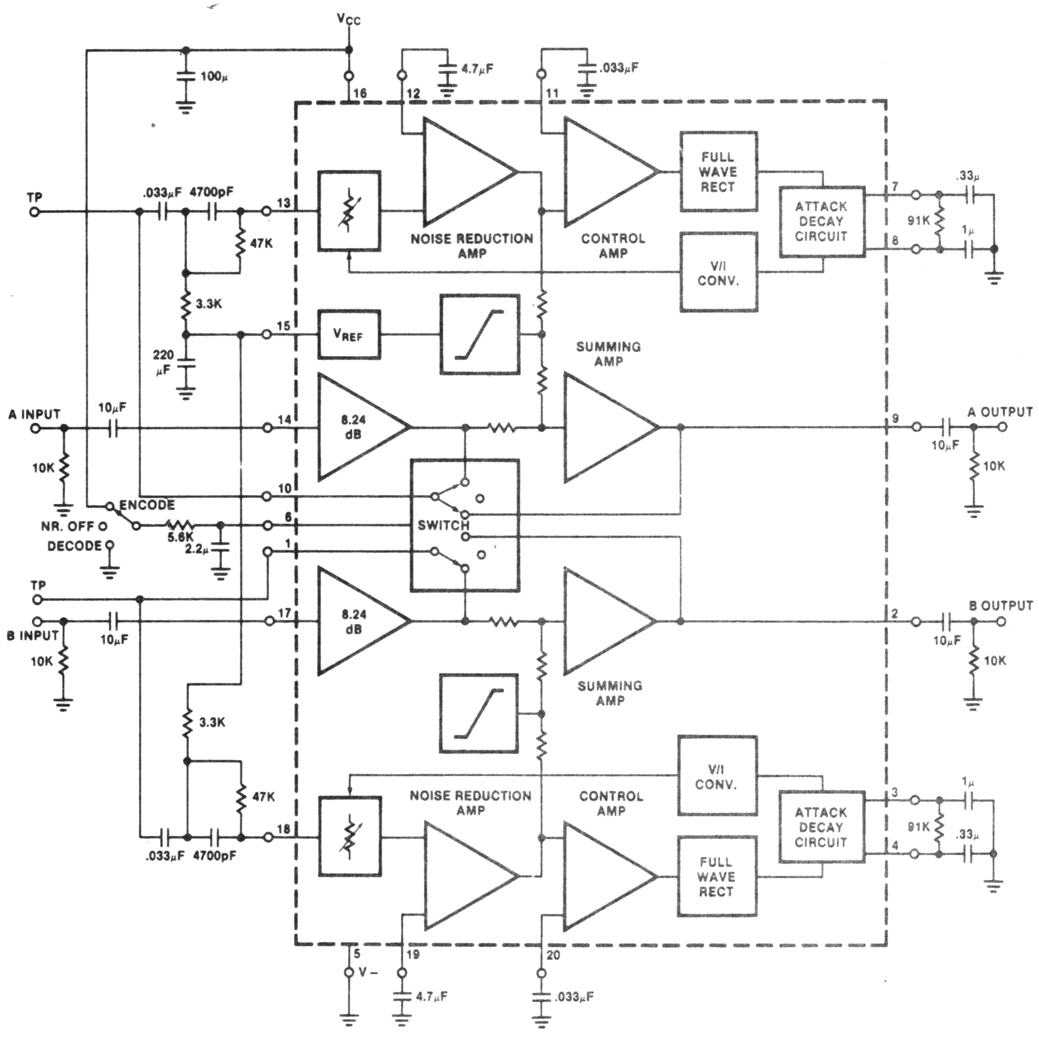

VCC
100μ
4.7μF
.033μF
16
12
11
TP
.033μF
4700pF
13
47K
3.3K
15
220 μF
A INPUT
10μF
14
10K
10
ENCODE
NR. OFF
6
5.6K
DECODE
2.2μ
1
TP
B INPUT
10μF
17
10K
3.3K
47K
18
.033μF
4700pF
NOISE REDUCTION AMP
CONTROL AMP
FULL WAVE RECT
ATTACK DECAY CIRCUIT
V/I CONV.
VREF
SUMMING AMP
8.24 dB
SWITCH
7
8
.33μ
91K
1μ
9
A OUTPUT
10μF
10K
2
B OUTPUT
10μF
10K
3
4
1μ
91K
.33μ
5
V−
19
4.7μF
20
.033μF

Figure 1. Test Circuit

Preliminary

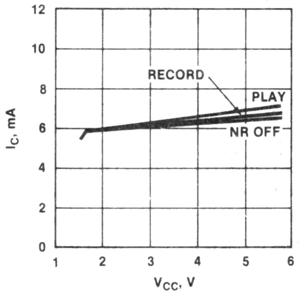


Figure 2. Supply Current vs. V_{CC}

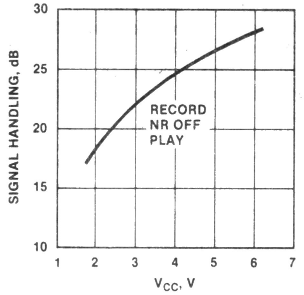


Figure 3. Signal Handling (THD — 1%)

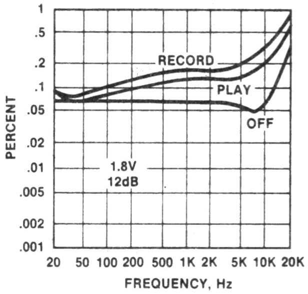


Figure 4. Distortion + Noise

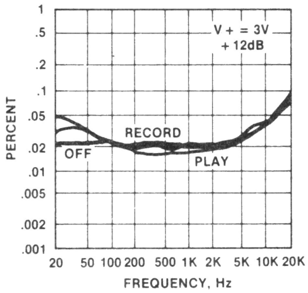


Figure 5. Harmonic Distortion + Noise

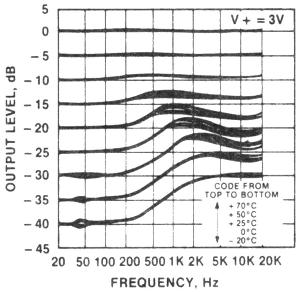


Figure 6. Encode Transfer Curve Shift With Temperature

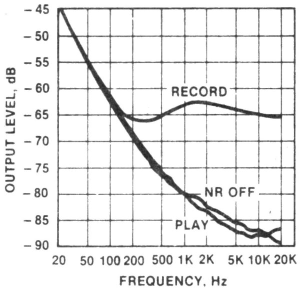


Figure 7. Crosstalk, $V_{CC} = 3V$

FM STEREO MULTIPLEX DECODER, PHASE LOCKED LOOP µA758

DESCRIPTION

The µA758 is a monolithic phase-locked loop FM stereo multiplex decoder. The device decodes an FM stereo multiplex signal into right and left audio channels while inherently suppressing SCA information when it is contained in the composite input signal. The device includes automatic mono-stereo mode switching and drive for an external lamp to indicate stereo mode operation.

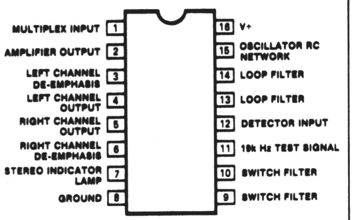
The µA758 operates over a large voltage range and requires a minimum number of external components. A simple setting of an external potentiometer adjusts the oscillator frequency. No coils are required.

FEATURES

- **45dB channel separation**
- **Automatic stereo/mono switching**
- **70dB SCA rejection**
- **10V to 16V supply range**
- **High impedance input—low impedance output**

PIN CONFIGURATION

N PACKAGE


MULTIPLEX INPUT 1
AMPLIFIER OUTPUT 2
LEFT CHANNEL DE-EMPHASIS 3
LEFT CHANNEL OUTPUT 4
RIGHT CHANNEL OUTPUT 5
RIGHT CHANNEL DE-EMPHASIS 6
STEREO INDICATOR LAMP 7
GROUND 8
16 V+
15 OSCILLATOR RC NETWORK
14 LOOP FILTER
13 LOOP FILTER
12 DETECTOR INPUT
11 19k Hz TEST SIGNAL
10 SWITCH FILTER
9 SWITCH FILTER

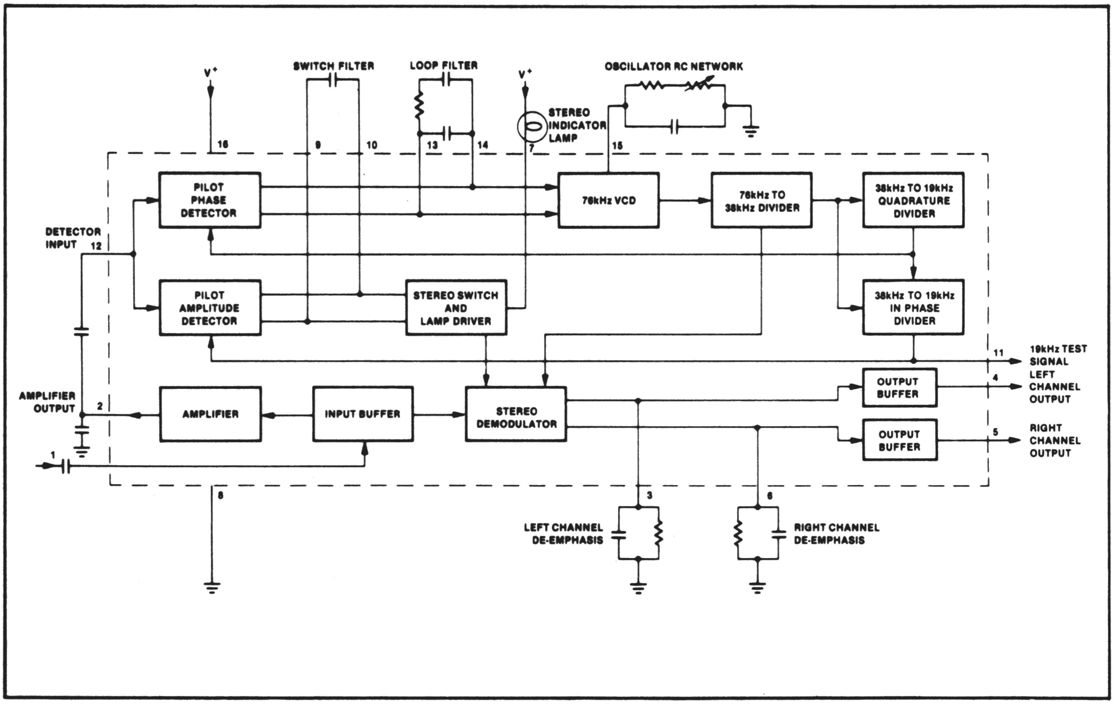
TOP VIEW

ORDER NUMBERS
µA758N

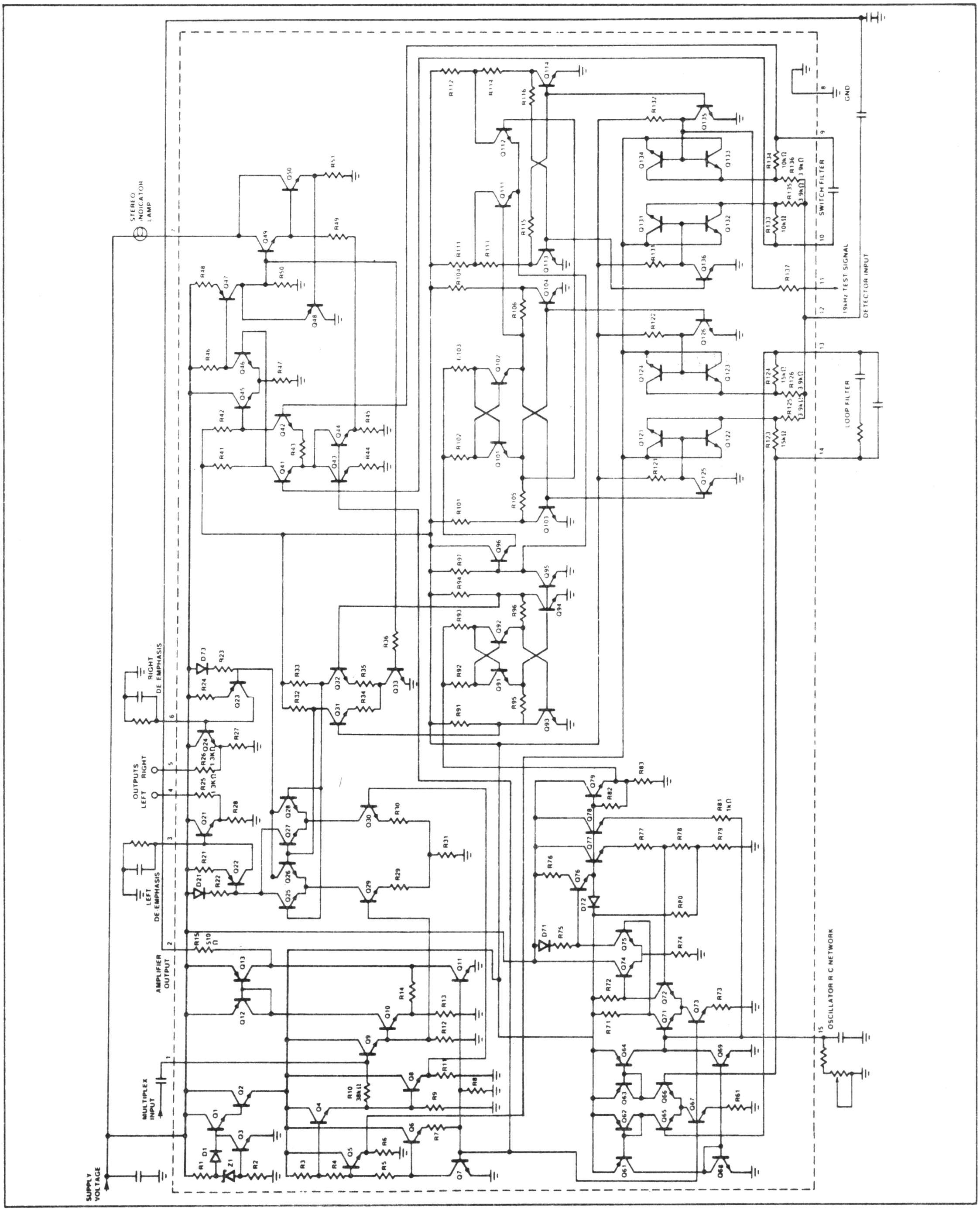
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	+18	V
Supply voltage (≤ 15 seconds)	+22	V
Voltage at lamp driver terminal (Lamp OFF)	+22	V
Internal power dissipation	730	mW
Operating temperature range	-40 to +85	°C
Storage temperature range	-55 to +125	°C
Lead temperature (60sec)	300	°C

BLOCK DIAGRAM


V+
SWITCH FILTER
LOOP FILTER
V+
OSCILLATOR RC NETWORK
STEREO INDICATOR LAMP
16
9
10
13
14
7
15
PILOT PHASE DETECTOR
76kHz VCO
76kHz TO 38kHz DIVIDER
38kHz TO 19kHz QUADRATURE DIVIDER
DETECTOR INPUT 12
PILOT AMPLITUDE DETECTOR
STEREO SWITCH AND LAMP DRIVER
38kHz TO 19kHz IN PHASE DIVIDER
11
19kHz TEST SIGNAL
AMPLIFIER OUTPUT 2
AMPLIFIER
INPUT BUFFER
STEREO DEMODULATOR
OUTPUT BUFFER
4
LEFT CHANNEL OUTPUT
OUTPUT BUFFER
5
RIGHT CHANNEL OUTPUT
1
8
3
6
LEFT CHANNEL DE-EMPHASIS
RIGHT CHANNEL DE-EMPHASIS

EQUIVALENT SCHEMATIC


SUPPLY VOLTAGE
MULTIPLEX INPUT
1
AMPLIFIER OUTPUT
2
LEFT DE EMPHASIS
3
OUTPUTS LEFT RIGHT
4
5
RIGHT DE EMPHASIS
6
STEREO INDICATOR LAMP
7
8
GND
9
SWITCH FILTER
10
19kHz TEST SIGNAL
11
DETECTOR INPUT
12
13
LOOP FILTER
14
15
OSCILLATOR R C NETWORK
R10 38kΩ
R15 510Ω
R25 1.3kΩ
R26 1.3kΩ
R81 1kΩ
R133 10kΩ
R134 10kΩ
R135 3.9kΩ
R136 3.9kΩ
R123 15kΩ
R124 15kΩ
R125 3.9kΩ
R126 3.9kΩ

FM STEREO MULTIPLEX DECODER, PHASE LOCKED LOOP μA758

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V+ = +12V$, 19kHz pilot level = 30mV_{RMS}, multiplex signal (L = R, pilot OFF) = 300mV_{RMS}, modulation frequency = 400Hz or 1Hz, test circuit 1, unless otherwise specified.

PARAMETER		TEST CONDITIONS	μA758			UNIT
			Min	Typ	Max	
I_{CC}	Supply current	Lamp OFF		31	38	mA
I_L	Maximum available lamp current		75	150		mA
V_7	Voltage at lamp driver terminal	Lamp = 50mA		1.3	1.8	V
r_i	Input resistance		20	35		kΩ
r_o	Output resistance		0.9	1.3	2.0	kΩ

AC ELECTRICAL CHARACTERISTICS

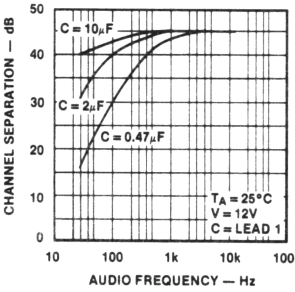
PARAMETER		TEST CONDITIONS	μA758			UNIT
			Min	Typ	Max	
$\Delta(V_4 \& V_5)$	DC voltage shift at either output terminal	Stereo to mono operation		30	150	mV
$P_{S.R.R.}$	Power supply ripple rejection	200Hz, 200mV_{RMS}	35			dB
SEP	Channel separation	100Hz		40		dB
		400Hz	30	45		dB
		10kHz		45		dB
BAL.	Channel balance			0.3	1.5	dB
A_V	Voltage gain	1kHz	0.5	0.9	1.4	V/V
	Pilot input level	Lamp turn-on		18	25	mV_{RMS}
		Lamp turn-off	2.0	7.0		mV_{RMS}
	Pilot input level hysteresis	Lamp turn-off to turn-on	3.0	7.0		dB
	Capture range		2.0	4.0	6.0	%
T.H.D.	Total harmonic distortion	Multiplex level = 600mV_{RMS} pilot OFF		0.4	1.0	%
	19kHz rejection		25	35		dB
	38kHz rejection		25	45		dB
	SCA rejection[1]			70		dB
VCO	Tuning resistance[2]		21.0	23.3	25.5	kΩ
VCO	Frequency drift	$0°C \le T_A \le 25°C$		+0.1	±2	%
		$25°C \le T_A \le 70°C$		-0.4	±2	%

NOTES

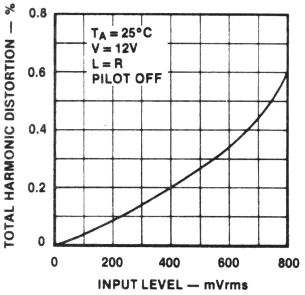
1. Measured with a stereo composite signal consistency of 80% stereo, 10% pilot and 10% SCA as defined in the FCC Rules on Broadcasting.
2. Total resistance from pin 15 to ground, in test circuit, required to set reference frequency at pin 11 to 19kHz ± 10hz.

TYPICAL PERFORMANCE CHARACTERISTICS

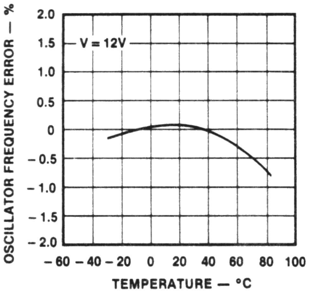
CHANNEL SEPARATION vs AUDIO FREQUENCY



HARMONIC DISTORTION vs INPUT LEVEL

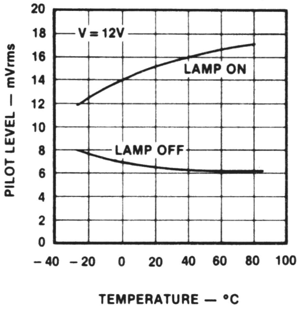


OSCILLATOR FREE RUNNING FREQUENCY ERROR vs AMBIENT TEMPERATURE

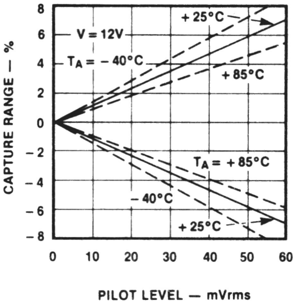


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

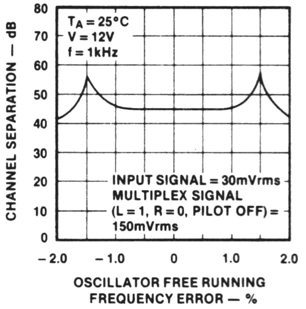
LAMP TURN ON & TURN OFF SENSITIVITY vs AMBIENT TEMPERATURE



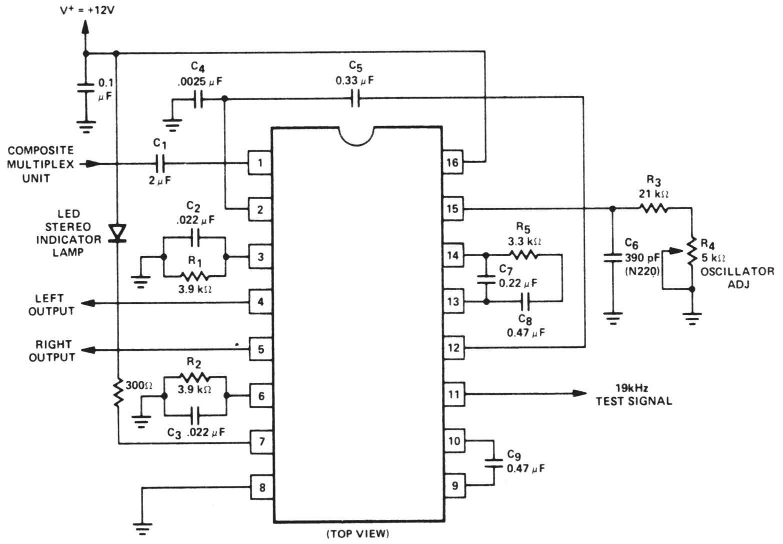
CAPTURE RANGES vs PILOT LEVEL



CHANNEL SEPARATION vs OSCILLATOR FREE RUNNING FREQUENCY ERROR



TEST CIRCUIT AND TYPICAL APPLICATION


V+ = +12V
0.1 μF
C_4 .0025 μF
C_5 0.33 μF
COMPOSITE MULTIPLEX UNIT
C_1 2 μF
LED STEREO INDICATOR LAMP
C_2 .022 μF
R_1 3.9 kΩ
LEFT OUTPUT
RIGHT OUTPUT
300Ω
R_2 3.9 kΩ
C_3 .022 μF
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
R_3 21 kΩ
R_5 3.3 kΩ
C_6 390 pF (N220)
R_4 5 kΩ OSCILLATOR ADJ
C_7 0.22 μF
C_8 0.47 μF
19kHz TEST SIGNAL
C_9 0.47 μF
(TOP VIEW)

NOTE

Tolerance on resistors is ±5% and tolerance on capacitors is ±20% unless otherwise specified. C_1 tolerance = +100%; −20%, C_6 tolerance = ±1% in test circuit and ±5% in typical applications, R_3 tolerance = ±1%, R_4 tolerance = ±10%, R_1 and R_2 tolerances = ±1% in test circuit and ±5% in typical application.

FM IF SYSTEM

CA3089

DESCRIPTION

CA3089 is a monolithic integrated circuit that provides all the functions of a comprehensive FM-IF system. Figure 6 is a block diagram showing the CA3089 features, which include a three-state FM-IF amplifier/limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The advanced circuit design of the IF system includes desirable features such as delayed AGC for the RF tuner, an AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power supply regulators maintain a nearly constant current drain over the voltage supply range of + 8 to + 18 volts.

The CA3089 is ideal for high-fidelity operation. Distortion in a CA3089 FM-IF system is primarily a function of the phase linearity characteristic of the outboard detector coil.

The CA3089 utilizes a 16-lead dual-in-line plastic package and can operate over the ambient temperature range of − 40°C to + 85°C.

FEATURES

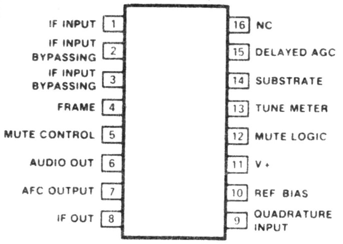
- **Exceptional limiting sensitivity: 10μV typ. at − 3dB point**
- **Low distortion: 0.1% typ. (with double-tuned coil)**
- **Single-coil tuning capability**
- **High recovered audio: 400mV typ.**
- **Provides specific signal for control of interchannel muting (squelch)**
- **Provides specific signal for direct drive of a tuning meter**
- **Provides delayed AGC voltage for RF amplifier**
- **Provides a specific circuit for flexible AFC**
- **Internal supply/voltage regulators**

APPLICATIONS

- **High-fidelity FM receivers**
- **Automotive FM receivers**
- **Communications FM receivers**

PIN CONFIGURATION

N PACKAGE

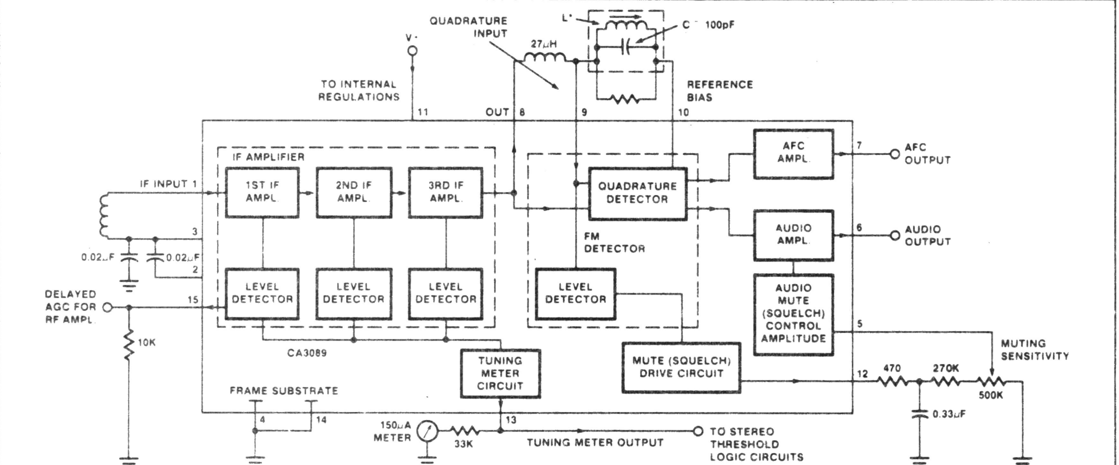

IF INPUT 1
IF INPUT BYPASSING 2
IF INPUT BYPASSING 3
FRAME 4
MUTE CONTROL 5
AUDIO OUT 6
AFC OUTPUT 7
IF OUT 8
16 NC
15 DELAYED AGC
14 SUBSTRATE
13 TUNE METER
12 MUTE LOGIC
11 V+
10 REF BIAS
9 QUADRATURE INPUT

TOP VIEW
ORDER NUMBER
CA3089N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
DC supply voltage:		
Between terminals 11 and 4	18	V
Between terminals 11 and 14	18	V
DC Current (out of terminal 15)	2	mA
Device dissipation:		
Up to T_A = 60°C	600	mW
Above T_A = 60°C	derate linearly 6.7	mW/°C
Ambient temperature range:		
Operating	−40 to +85	°C
Storage	−65 to +150	°C
Lead temperature (during soldering):		
At distance not less than 1/32" (0.79mm) from case for 10 seconds max	+265	°C

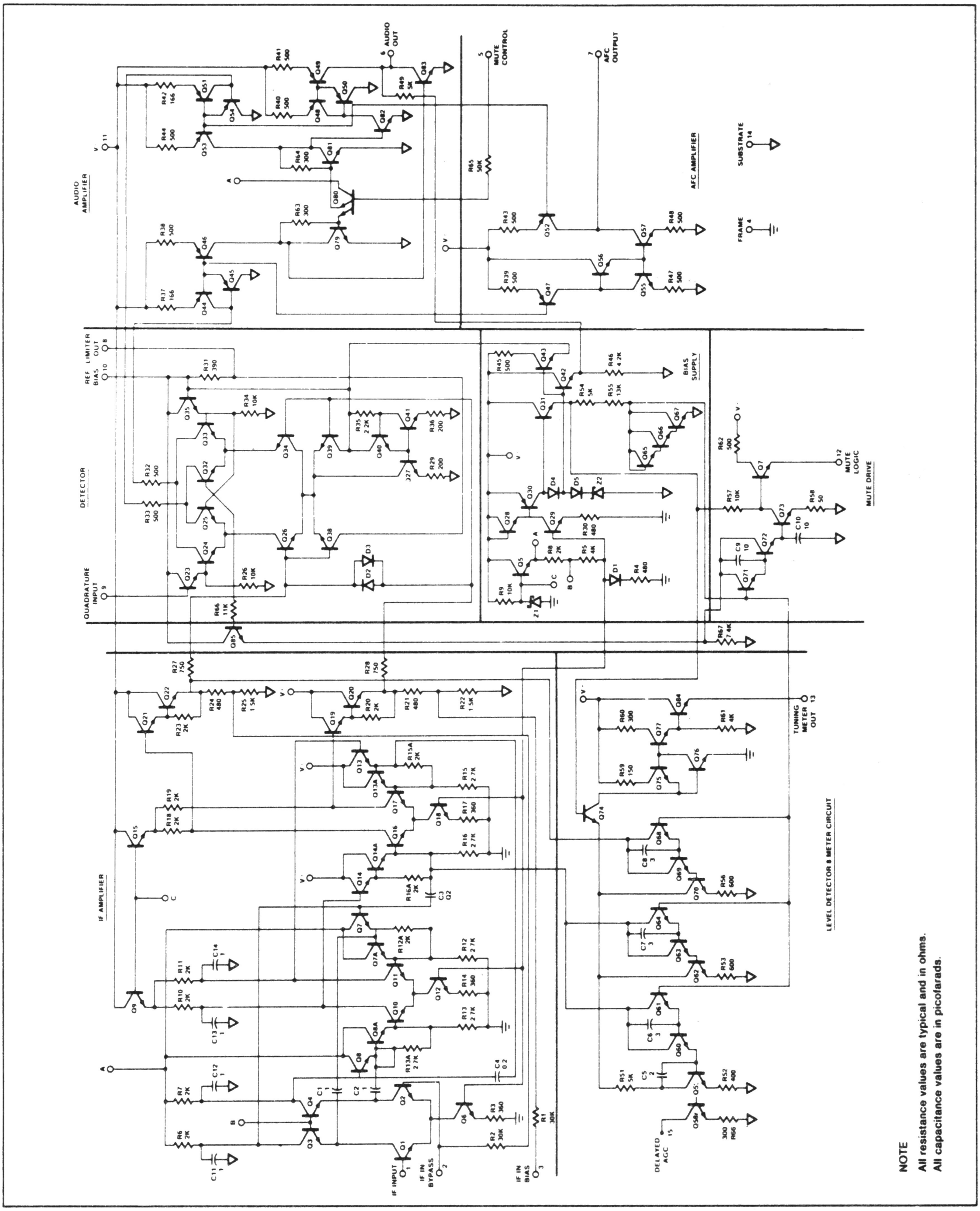
BLOCK DIAGRAM


QUADRATURE INPUT
V+
L*
C* 100pF
27μH
TO INTERNAL REGULATIONS
REFERENCE BIAS
11
OUT 8
9
10
IF AMPLIFIER
IF INPUT 1
1ST IF AMPL.
2ND IF AMPL.
3RD IF AMPL.
QUADRATURE DETECTOR
FM DETECTOR
AFC AMPL.
7
AFC OUTPUT
AUDIO AMPL.
6
AUDIO OUTPUT
3
0.02μF
0.02μF
2
DELAYED AGC FOR RF AMPL.
15
LEVEL DETECTOR
LEVEL DETECTOR
LEVEL DETECTOR
LEVEL DETECTOR
AUDIO MUTE (SQUELCH) CONTROL AMPLITUDE
5
10K
CA3089
TUNING METER CIRCUIT
MUTE (SQUELCH) DRIVE CIRCUIT
MUTING SENSITIVITY
12
470
270K
500K
FRAME SUBSTRATE
4
14
13
0.33μF
150μA METER
33K
TUNING METER OUTPUT
TO STEREO THRESHOLD LOGIC CIRCUITS

NOTE

All resistors values are typical and in ohms. $Q_0 \simeq 75$ (G.I. EX27825 or equivalent)
***L tunes with 100pF (C) at 10.7MHz**

EQUIVALENT SCHEMATIC


AUDIO AMPLIFIER
DETECTOR
IF AMPLIFIER
AFC AMPLIFIER
BIAS SUPPLY
MUTE DRIVE
LEVEL DETECTOR & METER CIRCUIT
6 AUDIO OUT
5 MUTE CONTROL
7 AFC OUTPUT
V+ 11
SUBSTRATE 14
FRAME 4
REF BIAS 10
LIMITER OUT 8
QUADRATURE INPUT 9
12 MUTE LOGIC
TUNING METER OUT 13
IF INPUT 1
IF IN BYPASS 2
IF IN BIAS 3
DELAYED AGC 15

NOTE
All resistance values are typical and in ohms.
All capacitance values are in picofarads.

FM IF SYSTEM

CA3089

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V^+ = 12V$ unless otherwise specified.

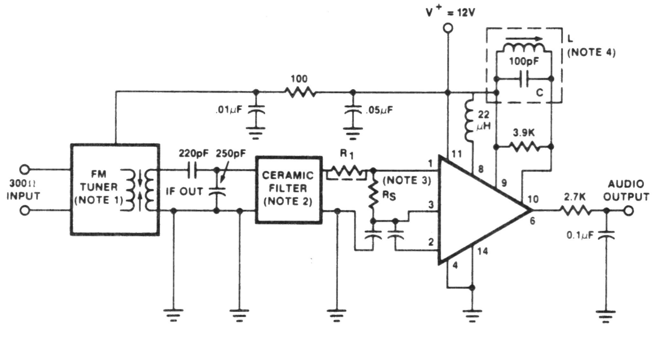
PARAMETER		TEST CONDITIONS	CA3089D2			UNIT
			Min	Typ	Max	
STATIC (DC) CHARACTERISTICS						
I_{11}	Quiescent circuit current	No signal input, non-muted	16	23	30	mA
DC Voltages:[4]						
V_1	Terminal 1 (IF input)	No signal input, non-muted	1.2	1.9	2.4	V
V_2	Terminal 2 (ac return to input)	No signal input, non-muted	1.2	1.9	2.4	V
V_3	Terminal 3 (dc bias to input)	No signal input, non-muted	1.2	1.9	2.4	V
V_6	Terminal 6 (audio output)	No signal input, non-muted	5.0	5.6	6.0	V
V_7	Terminal 7 (A.F.C.)	No signal input, non-muted	5.0	5.6	6.0	V
V_{10}	Terminal 10 (dc reference)	No signal input, non-muted	5.0	5.6	6.0	V
DYNAMIC CHARACTERISTICS						
$V_{I(lim)}$	Input limiting voltage (−3dB point)[3]			10	25	μV
	AMR AM Rejection (terminal 6)[4]	$V_{IN} = 0.1V$, $F_O = 10.7MHz$, $f_{mod} = 400Hz$, AM Mod = 30%	45	55		dB
V_O	Recovered audio voltage (terminal 6)[3]		400	500	600	mV
Total harmonic distortion:[1]						
THD	Single tuned (terminal 6)[3]			0.5	1.0	%
THD	Double tuned (terminal 6)[4]	$f_{mod} = 400Hz$, $V_{IN} = 0.1$		0.1		%
S+N/N	Signal plus noise to noise ratio (terminal 6)[3]	Deviation = ±75kHz $V_{IN} = 0.1V$	60	70		dB
MU_{IN}	Mute input (terminal 5)	$V_5 = 2.5V$	50	70		dB
MU_{OUT}	Mute output (terminal 12)	$V_{IN} = 50\mu V$			.5	V
		$V_{IN} = 0V$	4.0			V
MTR	Meter output (terminal 13)	$V_{IN} = 0.1V$	2.5	3.5		V
		$V_{IN} = 500\mu V$	1.0	1.5		V
		$V_{IN} = 0V$			.7	V
AGC	Delayed AGC (terminal 15)	$V_{IN} = .01V$			.5	V
		$V_{IN} = 10\mu V$	4.0	5.0		V
THD	Double tuned (terminal 6)[4]	$f_{mod} = 400Hz$ $V_{IN} = 0.1$		0.1		%

NOTES

1. THD characteristics and Audio Level are essentially a function of the phase and Q characteristics of the network connected between terminals 8,9, and 10.
2. Test circuit Figure 1.
3. Test circuit Figure 2.
4. Test circuit Figures 1 and 2.

TEST CIRCUITS

TYPICAL FM TUNER (With a single-tuned detector coil.)



NOTES

All resistors values are typical and in ohms.

1. Waller 4SN3FIC or equivalent
2. Murate SFG 10.7mA or equivalent
3. R_S will affect stability depending on circuit layout. To increase stability R_S is decreased. Range of R_S is 330 to 50Ω, $R_1 + R_S \leq 330\Omega$
4. L tunes with 100pF (C) at 10.7MHz
   Q_0 unloaded ≃ 75 (G.I. EX27825 or equivalent)

Performance data at f_o = 98MHz, f_{MOD} = 400Hz, deviation =

± 74kHz:

−3dB limiting sensitivity	2µV (antenna level)
20dB quieting sensitivity	1µV (antenna ievel)
30dB quieting sensitivity	1.5µV (antenna level)

Figure 3

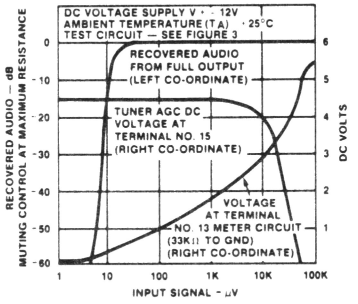
SYSTEM DESIGN CONSIDERATONS

The CA3089 is a very high gain device and therefore careful consideration must be given to the layout of external components to minimize feedback. The input bypass capacitors should be located close to the input terminals and the values should not be large nor should the capacitors be of the type which might introduce inductive reactance to the circuit. An example of good by-pass capacitors would be ceramic disc with values in the range of .01 to .05 microfarad.

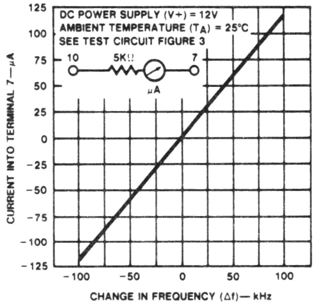
The input impedance of the CA3089 is approximately 10,000 ohms. It is *not* recommended to match this impedance. The value of the input termination resistor should be as low as possible without degrading system operation. The lower the value of this resistor the greater the system stability. An input terminating resistor between 50 and 100 ohms is recommended.

TYPICAL PERFORMANCE CHARACTERISTICS

MUTING ACTION, TUNER AGC
(Tuning meter output as a function of input signal voltage.)



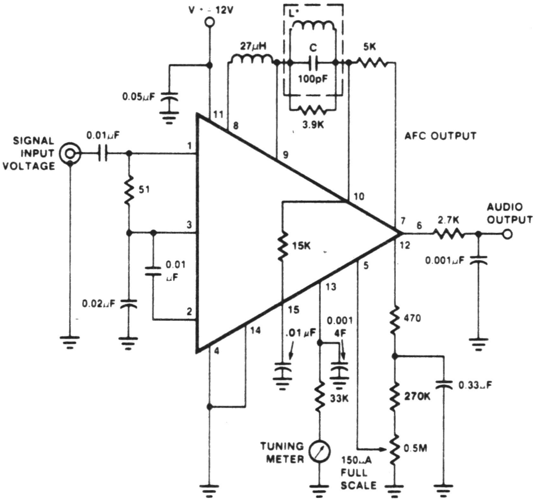
AFC CHARACTERISTICS
(Current at Term. 7 as a function of change in frequency.)



FM IF SYSTEM CA3089

TEST CIRCUITS

TEST CIRCUIT
(Using a single-tuned detector coil.)


V+ = 12V
L*
27µH
C
100pF
3.9K
5K
0.05µF
SIGNAL INPUT VOLTAGE
0.01µF
51
AFC OUTPUT
1
3
2
4
8
9
10
11
7
6
12
5
13
14
15
15K
0.01 µF
0.02µF
2.7K
AUDIO OUTPUT
0.001µF
.01µF
0.001 µF
470
270K
0.33µF
33K
TUNING METER
150µA FULL SCALE
0.5M

*NOTE

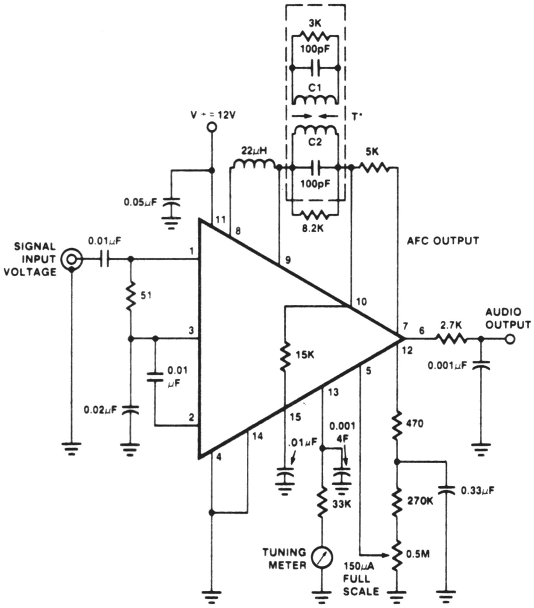
L tunes with 100pF (C) at 10.7MHz.

All resistors values are typical and in ohms.

Q_0 (unloaded) ≃ 75 (G.I. automatic mfg. div. EX27825 or equivalent).

Figure 1

TEST CIRCUIT
(Using a double-tuned detector coil.)


3K
100pF
C1
T*
C2
100pF
8.2K
V+ = 12V
22µH
5K
0.05µF
SIGNAL INPUT VOLTAGE
0.01µF
51
AFC OUTPUT
1
3
2
4
8
9
10
11
7
6
12
5
13
14
15
15K
0.01 µF
0.02µF
2.7K
AUDIO OUTPUT
0.001µF
.01µF
0.001 µF
470
270K
0.33µF
33K
TUNING METER
150µA FULL SCALE
0.5M

*NOTE

All resistors values are typical and in ohms.

T: Pri. – Q_o (unloaded) ≃ 75 (tunes with 100pF (C1) 20 † of 34e on 7/32" dia. form)
Sec. – Q_o (unloaded) ≃ 75 (tunes with 100pF (C2) 20 † of 34e on 7/32" dia. form)
kQ (percent of critical coupling) > 70%
(Adjusted for coil voltage V_C) = 150mV

Above values permit proper operation of mute (squelch) circuit "E" type slugs, spacing 4mm

Figure 2

BALANCED MODULATOR/DEMODULATOR MC1496/MC1596

DESCRIPTION

The MC1496 is a monolithic Double-Balanced Modulator/Demodulator designed for use where the output voltage is a product of an input voltage (signal) and a switched function (carrier). The MC1596 will operate over the full military temperature range of -55°C to +125°C. The MC 1496 is intended for applications within the range of 0°C to +70°C.

FEATURES

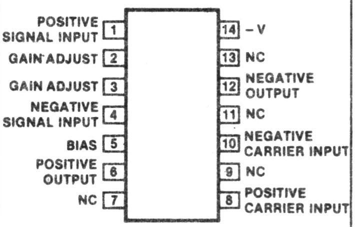
- **Excellent carrier suppression**
  - **65dB typ @ 0.5MHz**
  - **50dB typ @ 10MHz**
- **Adjustable gain and signal handling**
- **Balanced inputs and outputs**
- **High common-mode rejection—85dB typ**

APPLICATIONS

- **Suppressed carrier and amplitude modulation**
- **Synchronous detection**
- **FM detection**
- **Phase detection**
- **Sampling**
- **Single sideband**
- **Frequency doubling**

PIN CONFIGURATIONS

F, N PACKAGE



POSITIVE SIGNAL INPUT 1
GAIN ADJUST 2
GAIN ADJUST 3
NEGATIVE SIGNAL INPUT 4
BIAS 5
POSITIVE OUTPUT 6
NC 7
14 −V
13 NC
12 NEGATIVE OUTPUT
11 NC
10 NEGATIVE CARRIER INPUT
9 NC
8 POSITIVE CARRIER INPUT

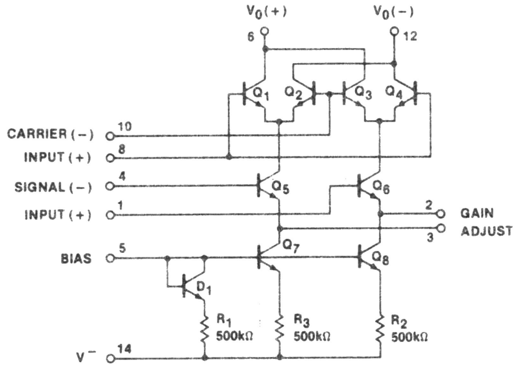
TOP VIEW

ORDER NUMBERS
MC1496F,N MC1596F

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Applied voltage	30	V
Differential input signal (V_8-V_{10})	±5.0	V
Differential input signal (V_4-V_1)	($5 \pm I_5 R_e$)	V
Input signal (V_2-V_1, V_3-V_4)	5.0	V
Bias current (I_5)	10	mA
Power dissipation (pkg. limitation)		
N package	900	mW
Operating temperature range		
MC1496	0 to +70	°C
MC1596	-55 to +125	°C
Storage temperature range	-65 to +150	°C

EQUIVALENT SCHEMATIC



V0(+)
6
V0(−)
12
Q1
Q2
Q3
Q4
CARRIER (−)
10
INPUT (+)
8
SIGNAL (−)
4
Q5
Q6
INPUT (+)
1
2
GAIN
ADJUST
3
BIAS
5
Q7
Q8
D1
R1 500kΩ
R3 500kΩ
R2 500kΩ
V−
14

BALANCED MODULATOR/DEMODULATOR MC1496/MC1596

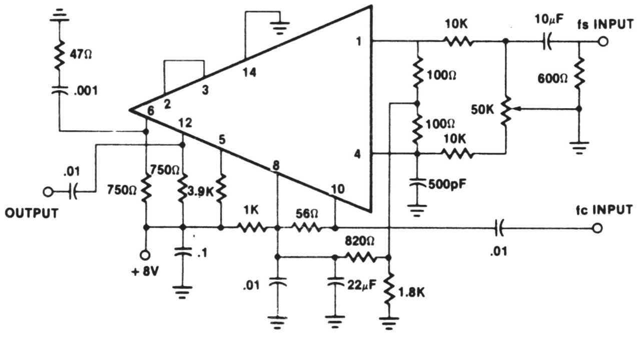
DC ELECTRICAL CHARACTERISTICS

$V^+ = +12Vdc$, $V^- = -8.0Vdc$, $I_5 = 1.0mAdc$, $R_L = 3.9k\Omega$, $R_e = 1.0k\Omega$, $T_A = 25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	MC1596			MC1496			UNIT
			Min	Typ	Max	Min	Typ	Max	
	Single-ended input impedance	Signal port, f = 5.0MHz							
R_{ip}	Parallel input resistance			200			200		kΩ
C_{ip}	Parallel input capacitance			2.0			2.0		pF
	Single-ended output impedance	f = 10MHz							
R_{op}	Parallel output resistance			40			40		kΩ
C_{op}	Parallel output capacitance			5.0			5.0		pF
	Input bias current								μA
I_{bS}	$I_{bS} = \frac{I_1 + I_4}{2}$			12	25		12	30	
I_{bC}	$I_{bS} = \frac{I_8 + I_{10}}{2}$			12	25		12	30	μA
	Input offset current								μA
I_{ioS}	$I_{ioS} = I_1 - I_4$			0.7	5.0		0.7	7.0	
I_{ioC}	$I_{ioC} = I_8 - I_{10}$			0.7	5.0		0.7	7.0	μA
T_{cIio}	Average temperature coefficient of input offset current			2.0			2.0		nA/°C
	Output offset current								
I_{oo}	$I_6 - I_{12}$			14	50		15	80	μA
T_{cIoo}	Average temperature coefficient of output offset current			90			90		nA/°C
V_o	Common-mode quiescent Output voltage (Pin 6 or Pin 12)			8.0			8.0		Vdc
	Power supply current								mAdc
I_{D+}	$I_6 + I_{12}$			2.0	3.0		2.0	4.0	
I_{D-}	I_{14}			3.0	4.0		3.0	5.0	
P_D	DC power dissipation			33			33		mW

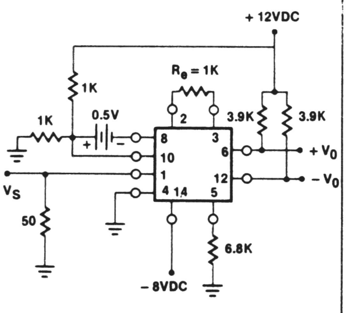
TEST CIRCUIT

CARRIER REJECTION AND SUPPRESSION


47Ω
.001
14
3
2
6
12
5
8
10
1
4
10K
10μF
fs INPUT
100Ω
600Ω
50K
100Ω
10K
500pF
.01
OUTPUT
750Ω
750Ω
3.9K
1K
56Ω
fc INPUT
820Ω
.01
+8V
.1
.01
22μF
1.8K

TEST CIRCUIT

SIGNAL GAIN AND OUTPUT SWING


+12VDC
1K
Re = 1K
1K
0.5V
2
3.9K
3.9K
8
3
6
10
1
12
4
14
5
+V0
−V0
VS
50
6.8K
−8VDC

BALANCED MODULATOR/DEMODULATOR MC1496/MC1596

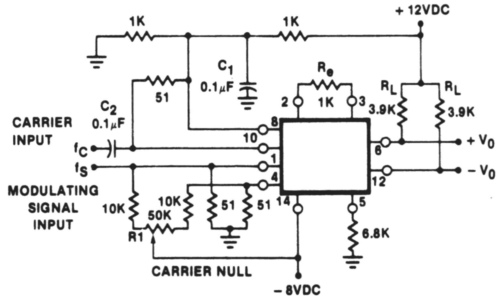
AC ELECTRICAL CHARACTERISTICS

$V^+ = +12$Vdc, $V^- = -9.0$Vdc, $I_5 = 1.0$mAdc, $R_L = 3.9k\Omega$, $R_e = 1.0k\Omega$, $T_A = +25°C$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	MC1596			MC1496			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CFT}	Carrier feedthrough	V_c = 60mVrms sinewave and offset adjusted to zero							
		f_C = 1.0kHz		40			40		μVrms
		f_C = 10MHz		140			140		
		V_c = 300mVp-p squarewave:							
		Offset adjusted to zero f_C = 1.0kHz		0.04	0.2		0.04	0.4	mVrms
		Offset not adjusted f_C = 1.0kHz		20	100		20	200	
V_{CS}	Carrier suppressions	f_S = 10kHz, 300mVrms sinewave							
		f_C = 500kHz, 60mVrms sinewave	50	65		40	65		dB
		f_C = 10MHz, 60mVrms sinewave		50			50		
BW_{3dB}	Transadmittance bandwidth (Magnitude) ($R_L = 50\Omega$)	Carrier input port, V_C = 60mVrms sinewave f_S = 1.0kHz, 300mVrms sinewave		300			300		MHz
		Signal input port, V_S = 300mVrms sinewave $\lvert V_C \rvert$ = 0.5Vdc		80			80		MHz
AV_S	Signal gain	V_S = 100mVrms; f = 1.0kHz $\lvert V_C \rvert$ = 0.5Vdc	2.5	3.5		2.5	3.5		V/V
CMV	Common-mode input swing	Signal port, f_s = 1.0kHz		5.0			5.0		Vp-p
ACM	Common-mode gain	Signal port, f_S = 1.0kHz $\lvert V_C \rvert$ = 0.5Vdc		-85			-85		dB
DV_{OUT}	Differential output voltage swing capability			8.0			8.0		Vp-p

TEST CIRCUIT

CARRIER REJECTION AND SUPPRESSION


+ 12VDC
1K
1K
C1
0.1μF
Re
1K
51
RL
3.9K
RL
3.9K
C2
0.1μF
CARRIER INPUT
fC
fS
MODULATING SIGNAL INPUT
2
3
8
10
1
4
6
12
14
5
+ V0
− V0
10K
10K
50K
51
51
R1
6.8K
CARRIER NULL
− 8VDC

*For additional information, consult the Applications Section.

HIGH SPEED FSK MODEM TRANSMITTER NE5080

DESCRIPTION

The NE5080 is the transmitter chip, of a two chip set, designed to be the heart of an FSK modem. (The NE5081 is the receiver chip.) The chips are compatible with the IEEE 802.4 standard for a "Single Channel Phase-Continuous-FSK Bus." The specifications shown in this data sheet are those guaranteed when the transmitter is tuned for the frequencies given in the 802 standard. However, both the NE5080 and the NE5081 may be used at other frequencies. The ratio of logic high to logic low frequencies remains fixed at 1.67 to 1.00 at any center frequency.

FEATURES

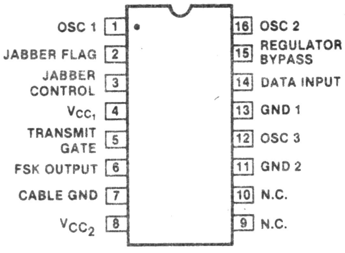
- **Meets IEEE 802.4 standard**
- **Data rates to several Megabaud**
- **Half or full duplex operation**
- **Jabber function on chip**

APPLICATIONS

- **Local Area Networks**
- **Point-to-point communications**
- **Factory automation**
- **Process control**
- **Office automation**

PIN CONFIGURATION

N PACKAGES


OSC 1
1
JABBER FLAG
2
JABBER CONTROL
3
V_{CC_1}
4
TRANSMIT GATE
5
FSK OUTPUT
6
CABLE GND
7
V_{CC_2}
8
16
OSC 2
15
REGULATOR BYPASS
14
DATA INPUT
13
GND 1
12
OSC 3
11
GND 2
10
N.C.
9
N.C.

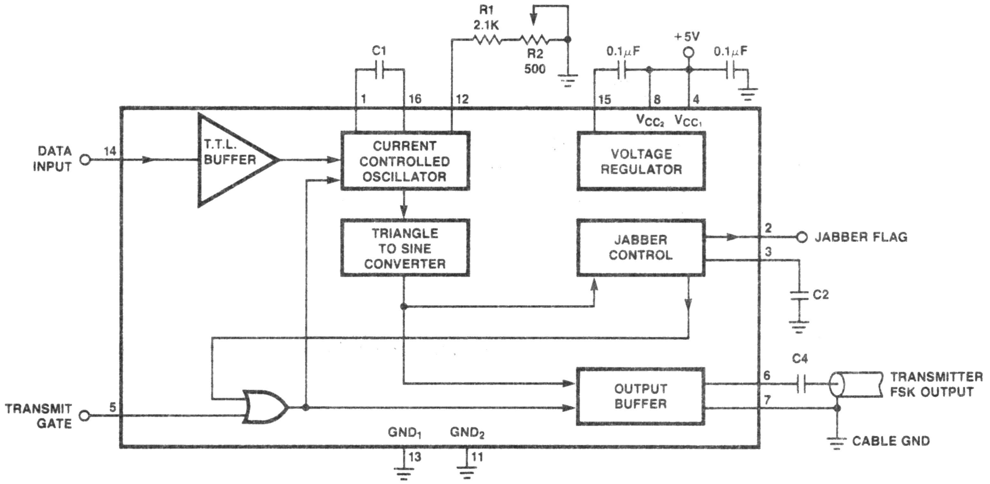
TOP VIEW

ORDER NUMBER
NE5080N

ABSOLUTE MAXIMUM RATINGS

SYMBOL & PARAMETER	RATING	UNIT
Supply Voltage V_{CC_1} V_{CC_2}	+6	V
Input Voltage Range (Data, Gate)	−0.3 to + V_{CC}	V
Power Dissipation	800	mW
Operating Temperature Range	0 to +70	°C
Max Junction Temperature	+150	°C
Storage Temperature Range	−65 to +150	°C
Lead Temperature (soldering, 10 sec)	300	°C

BLOCK DIAGRAM


R1
2.1K
R2
500
C1
+5V
0.1μF
0.1μF
1
16
12
15
8
4
V_{CC_2} V_{CC_1}
DATA INPUT
14
T.T.L. BUFFER
CURRENT CONTROLLED OSCILLATOR
VOLTAGE REGULATOR
TRIANGLE TO SINE CONVERTER
JABBER CONTROL
2
JABBER FLAG
3
C2
C4
6
7
OUTPUT BUFFER
TRANSMITTER FSK OUTPUT
CABLE GND
TRANSMIT GATE
5
GND_1
GND_2
13
11

HIGH SPEED FSK MODEM TRANSMITTER NE5080

GENERAL DESCRIPTION

The NE5080 is designed to transmit high frequency asynchronous data on coaxial cable, at rates from DC to 2 Megabaud (see note 1). The chip accepts serial data and transmits it as a periodic signal whose frequency depends on whether the data is high or low.

The device is meant to operate at a frequency of 6.25MHz for a logic high and 3.75MHz for a logic low (see note 2). The frequency is set up by external trimming components; however, the ratio of the high and low frequencies is set internally and cannot be altered.

The FSK output can be turned off by use of the transmit gate pin. When turned off, the transmitter has a high output impedance and the oscillator is disabled.

The length of time a transmitter can transmit can be controlled by the use of the Jabber control pin (see description of Jabber Control Pin).

Jabber Control Pin

During the time the transmitter is transmitting, this pin sources a current. This current can be used to set the maximum time that the transmitter can be on. There are three options that can be used:

1. Use the current to charge a capacitor. When the voltage across the cap gets to approx. 1.4V the transmitter will turn off. A logic low applied to pin 3 will reset the Jabber function; an open collector output should be used for this purpose. A logic high applied to the pin will disable the transmitter.
2. Use to externally sense the current and have external circuitry to control the length of time the transmitter is on.
3. The pin can be tied to ground and is then not active. Transmission is then controlled solely by the signal at the transmit gate pin.

Jabber Flag Pin

This pin will go to a logic high when the Jabber Control pin is used to shut off the transmitter. It will latch and can be reset by applying a logic low to the Jabber Control pin.

NE5080 PIN FUNCTION

PIN	FUNCTION
1	**OSC 1**—one end of an external capacitor used to set the carrier frequency
2	**JABBER FLAG**—this pin goes to a logic high if the transmitter attempts to transmit for a longer time than allowed by the Jabber control function
3	**JABBER CONTROL**—used to control transmit time. See note on Jabber function
4	V_{CC_1}—voltage supply
5	**TRANSMIT GATE**—a logic low on this pin will enable the transmitter; a logic high will disable it
6	**TRANSMITTER FSK OUTPUT**
7	**CABLE GROUND**—the shield of the coax cable should be connected to this pin and to Pin 11
8	V_{CC_2}—Connect to pin 4 close to device
9	**No Connection**
10	**No Connection**
11	**GROUND 2**—connect to Analog ground close to device
12	**OSC 3**—a variable resistor between this point and ground is used to set the carrier frequencies.
13	**GROUND 1**—connect to Analog ground close to device
14	**DATA INPUT**
15	**REGULATOR BYPASS**—a bypass capacitor between this pin and V_{CC_1} is required for the internal voltage regulator function
16	**OSC 2**—one end of a capacitor that is between pin 1 and pin 16 and is used to set the carrier frequency

Notes:

1. The NE5080 is capable of transmitting up to 1 Megabaud of differential Manchester code at a center frequency of 5MHz.
2. Although the chip is designed to meet the requirements of IEEE standard 802.4 (Token-Passing Single Channel Phase-Continuous-FSK Bus), it can be used at other frequencies. See "Determining Component Values."

ELECTRICAL CHARACTERISTICS $V_{CC_{1,2}}$ = 4.75-5.25V T_A = 0°C to +70°C

PARAMETER	SYMBOL	TEST CONDITIONS	NE5080			UNIT
			Min.	Typ.	Max.	
Output Frequency (Logic High)	F_1	Data Input ≥2.0V (See Note 1)	6.17	6.25	6.33	MHz
Output Frequency (Logic Low)	F_0	Data Input ≤0.8V (See Note 1)	3.67	3.75	3.83	MHz
Output Amplitude	V_0	Data Input ≥2.0V or ≤0.8V Output Load = 37.5Ω	0.5		1.0	V_{RMS}
Output Impedance (gated off)	R_{off}	Transmit gate ≥2.0V	100			KΩ
Output Impedance (gated on)	R_{on}	Transmit gate ≤0.8V			37.5	Ω
Output Capacitance	C_0	Transmit gate ≥2.0V or ≤0.8V			10	pF
Feed through	V_F	Transmit gate ≥2.0V 2.0MHz sq. wave (TTL Levels) Input			1	mV_{RMS}
Jabber Current	I_J	Transmit gate ≤0.8V Input ≥2.0V or ≤0.8V		1.25		μA
Supply Current	I_{CC}	V_{CC_1} connected to V_{CC_2}		75	100	mA
LOGIC LEVELS						
Data Input						
Logic High	V_{IH}	Input high voltage	2.0			Volts
Logic Low	V_{IL}	Input low voltage			0.8	Volts
Input Current	I_{IH}	Vin = 2.4V			40	μA
Input Current	I_{IL}	Vin = 0.4V			− 1.6	mA
Transmit Gate						
Logic High	V_{IH}	Input high voltage	2.0			Volts
Logic Low	V_{IL}	Input low voltage			0.8	Volts
Input Current	I_{IH}	VG = 2.4V			40	μA
Input Current	I_{IL}	VG = 0.4V			− 1.6	mA
Jabber Flag						
Logic High	V_{OH}	IOH = −400μA	2.4			Volts
Logic Low	V_{OL}	IOL = 4.0mA			0.4	Volts
Jabber Control						
Logic High	V_{IH}	Input high voltage	2.0			Volts
Logic Low	V_{IL}	Input low voltage			0.8	Volts

NOTE

(1) Tuned per instructions in Applications section.

AC ELECTRICAL CHARACTERISTICS

SYMBOL & PARAMETER	TO	FROM	TEST CONDITIONS	NE5080			UNIT
				Min.	Typ.	Max.	
Set Up Time — T_S	Data In	Gate On	Figure 1	2	0.1		μS
Delay Time — T_A	Output Freq. Change	Data Transition	Figure 2			150	nS
Delay Time — T_B	Output Disabled	Gate Off	Figure 3		0.4	2	μS
Delay Time — T_C	Output Disabled	Jabber Control	Figure 4			100	nS
Delay Time — T_D	Jabber Flag	Jabber Control	Figure 5			100	nS
Jabber Control Reset Pulse Width (Logic Low)				100			nS

TIMING DIAGRAMS

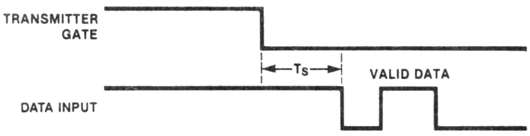

TRANSMITTER GATE
DATA INPUT
T_S
VALID DATA

Figure 1. Set-up Time, T_S

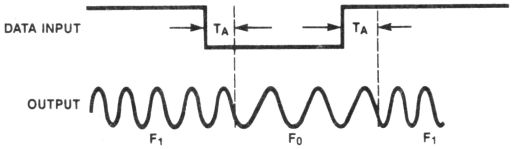

DATA INPUT
T_A
T_A
OUTPUT
F_1
F_0
F_1

Figure 2. Delay Time, T_A

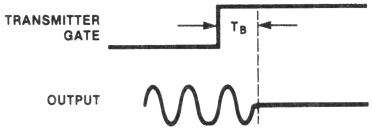

TRANSMITTER GATE
T_B
OUTPUT

Figure 3. Delay Time, T_B

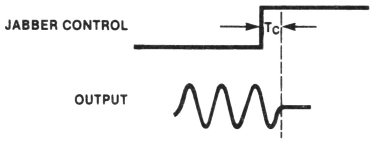

JABBER CONTROL
T_C
OUTPUT

Figure 4. Delay Time, T_C

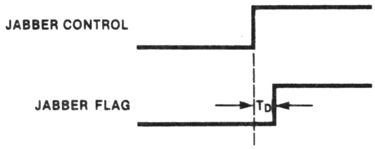

JABBER CONTROL
JABBER FLAG
T_D

Figure 5. Delay Time, T_D

HIGH SPEED FSK MODEM RECEIVER

NE5081

DESCRIPTION

The NE5081 is the receiver chip of a two chip set designed to operate as an FSK modem (the NE5080 is the transmitter chip). The chips are compatible with the IEEE 802.4 standard for a "Single Channel Phase-Continuous-FSK Bus." The specifications given in this data sheet are those guaranteed when the receiver is tuned to the frequencies in the 802 standard. However, the receiver will work at other frequencies.

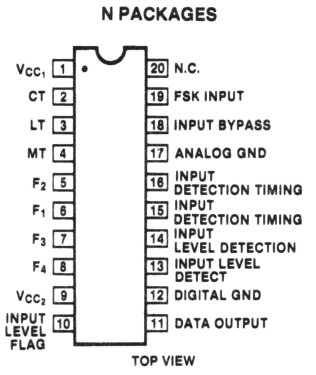
FEATURES

- **Meets IEEE 802.4 standard**
- **Data rates to several Megabaud**
- **Half or full duplex operation**
- **Low bit rate error (10^{-12} typical)**

APPLICATIONS

- **Local Area Networks**
- **Point-to-point communications**
- **Factory automation**
- **Process control**
- **Office automation**

PIN CONFIGURATION


N PACKAGES
V_{CC_1} 1
CT 2
LT 3
MT 4
F_2 5
F_1 6
F_3 7
F_4 8
V_{CC_2} 9
INPUT LEVEL FLAG 10
20 N.C.
19 FSK INPUT
18 INPUT BYPASS
17 ANALOG GND
16 INPUT DETECTION TIMING
15 INPUT DETECTION TIMING
14 INPUT LEVEL DETECTION
13 INPUT LEVEL DETECT
12 DIGITAL GND
11 DATA OUTPUT
TOP VIEW

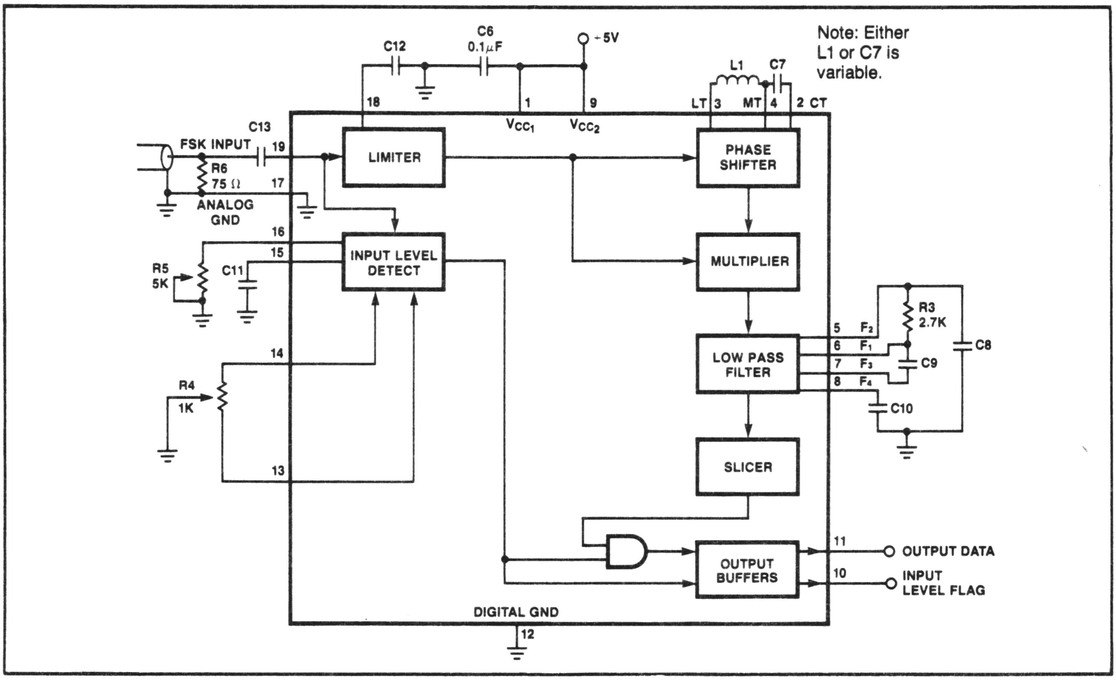
ORDER NUMBER

NE5081N

ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$

SYMBOL & PARAMETER	RATING	UNIT
Supply Voltage V_{CC_1} V_{CC_2}	+6	Volts
Input Voltage Range	−0.3 to $+V_{CC}$	Volts
Output (Data, Level Detect) Max Sink Current	20	mA
Power Dissipation	800	mW
Operating Temperature Range	0 to +70	°C
Storage Temperature Range	−65 to +150	°C
Lead Temperature (soldering, 10 sec)	300	°C
Max Differential Voltage between Analog and Digital Grounds	100	mV

BLOCK DIAGRAM


C12
C6
0.1μF
+5V
18
1
9
V_{CC_1}
V_{CC_2}
L1
C7
LT 3
MT 4
2 CT
C13
FSK INPUT
19
R6
75 Ω
17
ANALOG GND
LIMITER
PHASE SHIFTER
16
15
R5
5K
C11
INPUT LEVEL DETECT
MULTIPLIER
R3
2.7K
C8
5 F_2
6 F_1
7 F_3
8 F_4
C9
C10
LOW PASS FILTER
14
R4
1K
13
SLICER
OUTPUT BUFFERS
11
OUTPUT DATA
10
INPUT LEVEL FLAG
DIGITAL GND
12

Note: Either L1 or C7 is variable.

HIGH SPEED FSK MODEM RECEIVER NE5081

GENERAL DESCRIPTION

The NE5081 will accept an FSK encoded signal and provide the demodulated digital data at the output. It is optimized to work at frequencies specified in IEEE 802.4 (Token-Passing Single Channel Phase-Continuous FSK Bus) i.e., 3.75MHz and 6.25MHz. However, it will work at other frequencies (see note 1).

Its normal acceptable input signal level range is from 16mV RMS to 1V RMS. (This can be adjusted, see note 2 below.)

The receiver will yield an undetected "Bit Error Rate" of 10^{-9} or lower when receiving signals with a 20dB signal-to-noise ratio. It has a maximum output Jitter of ±40nSec (see definition of "Jitter" note 3).

Notes:

1. The receiver can be tuned to accept different frequencies by adjustment of the LC circuit shown in Fig. 7. However, the external components have been optimized for 3.75MHz and 6.25MHz. See "Determining Component Values" for use at other frequencies.
2. Input Level Detect
   This is a method of turning off the output of the receiver when the input signal falls below an acceptable level. This level is adjustable within the range given in the electrical specification section. The purpose of this function is to minimize the effect of noise on receiver performance and to indicate when there is an acceptable signal present at the input. All specifications given in this data sheet are with the input level detection set at 16mV RMS.
3. Jitter Definition
   This is a measure of the ability of the receiver to accurately reproduce the timing of its FSK coded digital input. The spec indicates the error band in the timing of a logic level change.

NE5081 PIN FUNCTION

PIN	FUNCTION
1	V_{CC_1}—should be connected to the 5 volt supply and pin 9
2	**CT**—one end of an external capacitor that is used to tune the receiver
3	**LT**—one end of an inductor that is used to tune the receiver
4	**MT**—the junction of the capacitor and inductor used for tuning the receiver
5	**F2** } Pins 5, 6, 7, 8 are used for a low pass filter to remove carrier harmonics from the data output
6	**F1**
7	**F3**
8	**F4**
9	V_{CC_2}—connect to Pin 1 (see Pin 1 function) close to the device
10	**INPUT LEVEL FLAG**—this pin is used to indicate when there is a signal at the input that is greater than the level set by the input level detection circuitry. A logic high indicates an input greater than the set level
11	**DATA OUTPUT**—supplies T^2L level data that corresponds to the FSK input received
12	**DIGITAL GROUND**—should be connected to digital ground
13 and 14	**INPUT LEVEL DETECT**—These pins are used to set the level of input signal that the device will accept as valid
15	**INPUT DETECTION TIMING**—an external capacitor between this pin and ground is used to determine the time from carrier turn-off to output disable
16	**INPUT DETECTION TIMING**—same as pin 15, except that a resistor goes between this pin and ground. The values of the C and R depend on the carrier frequency. The values given in this data sheet are for a 5MHz carrier center frequency
17	**ANALOG GROUND**—connect to analog ground close to the device
18	**INPUT BYPASS**—A capacitor between this pin and ground is used to bypass the input bias circuitry
19	**INPUT**—the FSK signal from the cable goes to this pin
20	**NO CONNECTION**

ELECTRICAL CHARACTERISTICS

$V_{CC_{1,2}}$ = 4.75 - 5.25V. External LC circuit tuned to 5MHz. Input level detect set at 16mV Rms, T_A = 0°C to +70°C.

PARAMETER	SYMBOL	TEST CONDITIONS	NE5081			UNIT
			Min.	Typ.	Max.	
Logic Low Frequency	F_0	External LC tuned to 5MHz	3.67	3.75	3.83	MHz
Logic High Frequency	F_1	External LC tuned to 5MHz	6.17	6.25	6.33	MHz
Minimum Input Detect Level	IN_{DL}	Minimum input level that is detected as carrier. See Note 2 in General Description	5		50	mV RMS
LOGIC LEVELS:						
Data Output	V_{OL}	$I_{OL} = 4.0mA$ $V_{IN} > 16mV$ RMS $Freq = F_0$			0.4	Volts
Data Output	V_{OH}	$I_{OH} = -400\mu A$ $V_{IN} > 16mV$ RMS $Freq = F_1$	2.4			Volts
Data Output	V_{OH}	$I_{OH} = -400\mu A$ $V_{IN} < 5mV$ RMS $Freq = F_0$	2.4			Volts
Input Detect Flag	V_{OL}	$I_{OL} = 4.0mA$ $V_{IN} = 0V$ RMS			0.4	Volts
	V_{OH}	$I_{OH} = -400\mu A$ $V_{IN} > 16mV$	2.4			Volts
Supply Current	I_{CC}	$V_{CC} = 5.25V$ (V_{CC_1} connected to V_{CC_2}) $V_{IN} = 1.0V$ RMS $Freq = F_1$ or F_0			50	mA
Bit Error Rate	B.E.R	Input Signal > 16mV RMS. maximum in-band noise = 1.6mV RMS		10^{-12}	10^{-9}	

AC ELECTRICAL CHARACTERISTICS

SYMBOL & PARAMETER	TO	FROM	TEST CONDITIONS	NE5081			UNIT
				Min.	Typ.	Max.	
Delay Time T_B	Input Level Detect Flag	Input On	Figure 1		0.05	1	μS
Delay Time T_C	Input Level Detect Flag	Input Off	Figure 1	.5	1.5	2.5	μS
Delay Time T_D	Output Enabled	Input On	Figure 2			2	μS
Delay Time T_E	Output Disabled	Input Off	Figure 2	.5	1.5	2.5	μS
Required Delay	Carrier Turn Off	Valid Data End		2			μS

TIMING DIAGRAMS

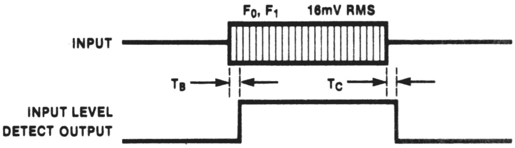

F_0, F_1
16mV RMS
INPUT
T_B
T_C
INPUT LEVEL
DETECT OUTPUT

Figure 1. Delay Time, T_B, T_C

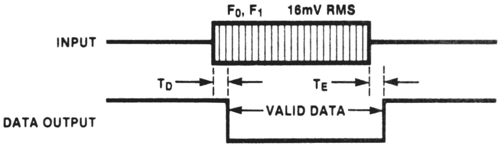

F_0, F_1
16mV RMS
INPUT
T_D
T_E
VALID DATA
DATA OUTPUT

Figure 2. Delay Time, T_D, T_E

PHASE-LOCKED LOOPS—SYMBOLS AND DEFINITIONS

Absolute Maximum Rating

Operating safe zones exceeding these limits could cause permanent damage to the device and are not meant to imply that devices can operate at these limits.

Capture Range ($2f_c$, $2\omega_c$)\**

Although the loop will remain in lock throughout its lock range, it may not be able to acquire lock at the tracking range extremes because of the selectivity afforded by the low-pass filter. The capture range also is centered at f_o' with the equal deviations called the *Lock-in* or *Pull-in Ranges.* The capture range can never exceed the lock range.

Closed Loop Gain (CLG)

The output signal frequency and phase can be determined from a product of the CLG and the input signal where the CLG is given by

$$CLG = \frac{K_v}{1 + K_v} \qquad \text{(Equation 1.4)}$$

Damping Factor (ζ)

The standard damping constant of a second order feedback system. For the PLL, ζ refers to the ability of the loop to respond quickly to an input frequency step without excessive overshoot.

Free-Running Frequency (f_o', ω_O')

Also called the *center frequency*, this is the frequency at which the loop VCO operates when not locked to an input signal. The "prime" superscripts are used to distinguish the free-running frequency from f_o' and ω_o' which are used for the general oscillator frequency. (Many references use f_o' and ω_o' for both the free-running and general oscillator frequency and leave the proper choice for the reader to infer from the context). the appropriate units for f_o' and ω_o' are Hz and radians per second respectively.

Lock Range ($2f_L$, $2\omega_L$)\*

The range of frequencies over which the loop will remain in lock. Normally the lock range is centered at the free-running frequency unless there is some nonlinearity in the system which limits the frequency deviation on one side of f_o'. The deviations from f_o' are referred to as the *Tracking Range* or *Hold-in Range.* (See figure 1.6.) The tracking range is therefore one-half of the lock range.

Lock-Up Time (t_L)***

The transient time required for a free-running loop to lock. This time depends principally upon the bandwidth selectivity designed into the loop with the low-pass filter. The lock-up time is inversely proportional to the selectivity bandwidth. Also, lock-up time exhibits a statistical spreading due to random initial phase relationships between the input and oscillator phases.

Loop Gain (K_v)

The product of K_d, K_o, and the low-pass filters gain at dc. K_d is evaluated at the appropriate input signal level and K_o at the appropriate ω_o'. K_v has units of $(sec)^{-1}$.

Loop Noise Bandwidth (B_L)

A loop property relating ω_n and τ which describes the effective bandwidth of the received signal. Noise and signal components outside this bandwidth are greatly attenuated.

Natural Frequency (ω_n)

The characteristic frequency of the loop, determined mathematically by the final pole positions in the complex plane or determined experimentally as the modulation frequency for which an underdamped loop gives the maximum frequency deviation from f_o' and at which the phase error swing is the greatest.

Package Type Designation

See full package designations in Appendix.

Phase Comparator Conversion Gain (K_d)

The conversion constant relating the phase comparators output voltage to the phase difference between input and VCO signals when the loop is locked. At low input signal levels, K_d is also a function of signal amplitude. K_d has units of volts per radian (V/rad).

Power Dissipation

The power that the device can safely handle at 25°C. The dissipation must be derated as indicated for the individual package type.

T_A

Ambient temperature range. Range of the surrounding environment of the operating device.

T_J

Junction Temperature. The maximum temperature of the device. 150°C is standard for silicon devices.

T_{SOLD}

Soldering Temperature. The temperature which can be applied to the lead frame of the device for short periods of time (normally specified for a duration of 10 sec).

T_{STG}

Storage temperature range. Temperature range that the device can be stored in a non-operating condition.

Truth Tables

0 is logic level low
1 is logic level high
X — don't care condition — has no effect under circuit conditions listed.

*Also called Synchronization Range.
**Also called Acquisition Range.
***Also called Acquisition Time.

PHASE LOCKED LOOP SE/NE564

DESCRIPTION

The NE564 is a versatile, high guaranteed frequency Phase Locked Loop designed for operation up to 50MHz. As shown in the block diagram, the NE564 consists of a VCO, limiter, phase comparator, and post detection processor.

APPLICATIONS

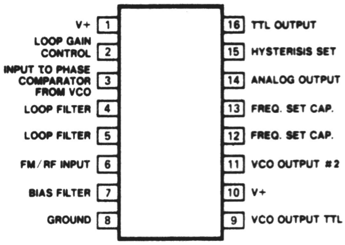
- **High speed modems**
- **FSK receivers and transmitters**
- **Frequency synthesizers**
- **Signal generators**
- **Various satcom/TV systems**

FEATURES

- **Operation with single 5V supply**
- **TTL compatible inputs and outputs**
- **Guaranteed operation to 50MHz**
- **External loop gain control**
- **Reduced carrier feedthrough**
- **No elaborate filtering needed in FSK applications**
- **Can be used as a modulator**
- **Variable loop gain (Externally Controlled)**

PIN CONFIGURATION

D, I, N PACKAGE


V+ 1
LOOP GAIN CONTROL 2
INPUT TO PHASE COMPARATOR FROM VCO 3
LOOP FILTER 4
LOOP FILTER 5
FM/RF INPUT 6
BIAS FILTER 7
GROUND 8
16 TTL OUTPUT
15 HYSTERISIS SET
14 ANALOG OUTPUT
13 FREQ. SET CAP.
12 FREQ. SET CAP.
11 VCO OUTPUT #2
10 V+
9 VCO OUTPUT TTL

TOP VIEW

ORDER NUMBERS

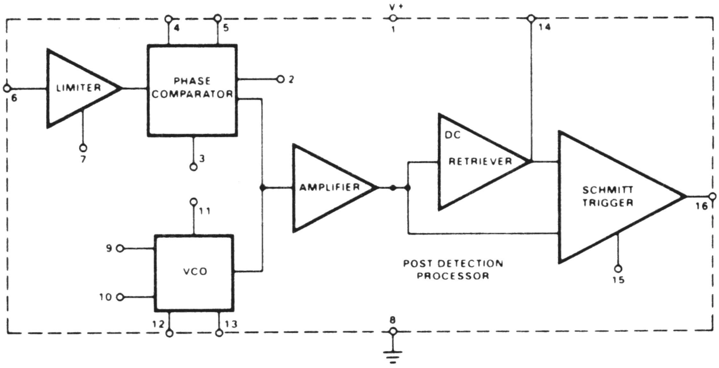
NE/SE564I NE/SE564N
NE564D

ABSOLUTE MAXIMUM RATINGS

PARAMETER			RATING	UNIT
V+	Supply voltage			V
	Pin 1		14	
	Pin 10		6	
P_D	Power dissipation		600	mW
T_A	Operating temperature	NE	0 to 70	°C
	Operating temperature	SE	−55 to +125	
t_{stg}	Storage temperature		−65 to 150	°C

NOTE:
Operation above 5 volts will require heatsinking of the case.

BLOCK DIAGRAM

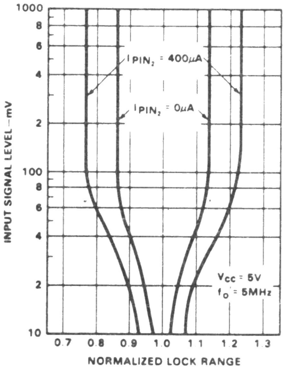

V+
1
4
5
14
LIMITER
PHASE COMPARATOR
2
6
7
3
AMPLIFIER
DC RETRIEVER
SCHMITT TRIGGER
16
11
9
VCO
10
12
13
POST DETECTION PROCESSOR
15
8

ELECTRICAL CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25°C$, $f_o = 5MHz$, $I_B = 400\mu A$ unless otherwise specified

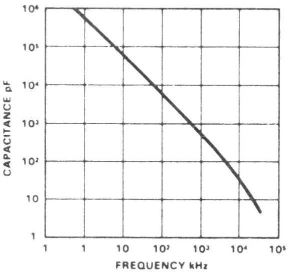
PARAMETER	TEST CONDITIONS	SE564			NE564			UNIT
		Min	Typ	Max	Min	Typ	Max	
Maximum VCO frequency	$C_1 = 0$ (stray)	50	65		45	60		MHz
Lock range	Input ≥ 200mVrms $T_A = 25°C$	40	70		40	70		% of f_o
	= 125°C	20	30					
	= −55°C	50	80					
	= 0°C					70		
	= 70°C					40		
Capture range	Input ≥ 200mVrms, $R_2 = 27\Omega$	20	30		20	30		% of f_o
VCO frequency drift with temperature	$f_o = 5MHz$, $T_A = -55°C$ to 125°C		400	1000				PPM/°C
	= 0°C to 70°C					400	1250	
	$f_o = 500KHz$, $T_A = -55°C$ to 125°C		250	500				
	= 0°C to 70°C					400	850	
VCO free running frequency	$C_1 = 91pF$ $R_C = 100\Omega$ "Internal"	4	5	6	3.5	5	6.5	MHz
VCO frequency change with supply voltage	$V_{CC} = 4.5V$ to 5.5V		3	8		3	8	% of f_o
Demodulated output voltage	Modulation frequency: 1KHz $f_o = 5MHz$, input deviation:							
	2% T = 25°C	16	28		16	28		mVrms
	1% T = 25°C	8	14		8	14		mVrms
	= 0°C					13		mVrms
	= −55°C	6	10					mVrms
	= 70°C					15		mVrms
	= 125°C	12	16					mVrms
Distortion	Deviation: 1% to 8%		1			1		%
Signal to noise ratio	Std. condition, 1% to 10% dev.		40			40		dB
AM rejection	Std. condition, 30% AM		35			35		dB
Demodulated Output at operating voltage	Modulation frequency: 1KHz $f_o = 5MHz$, input deviation: 1%							
	$V_{CC} = 4.5V$	7	12		7	12		mVrms
	$V_{CC} = 5.5V$	8	14		8	14		mVrms
Supply current	$V_{CC} = 5V$ I_1, I_{10}		45	60		45	60	mA
Output								
"1" output leakage current	$V_{OUT} = 5V$, Pin 16, 9		1	20		1	20	µA
"0" output voltage	$I_{OUT} = 2mA$, Pin 16, 9		0.3	0.6		0.3	0.6	V
	$I_{OUT} = 6mA$, Pin 16, 9		0.4	0.8		0.4	0.8	V

TYPICAL PERFORMANCE CHARACTERISTICS

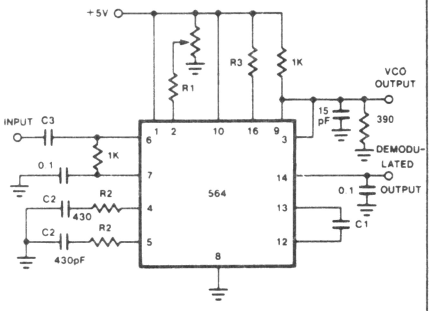
LOCK RANGE vs SIGNAL INPUT



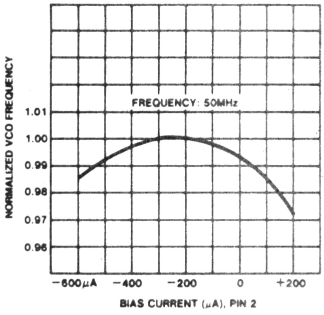
VCO CAPACITOR vs FREQUENCY



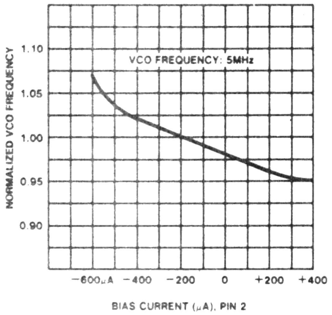
SE/NE 564 TEST CIRCUIT



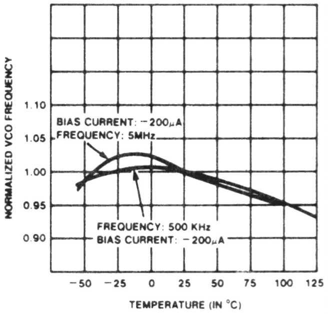
TYPICAL NORMALIZED VCO FREQUENCY AS A FUNCTION OF PIN 2 BIAS CURRENT



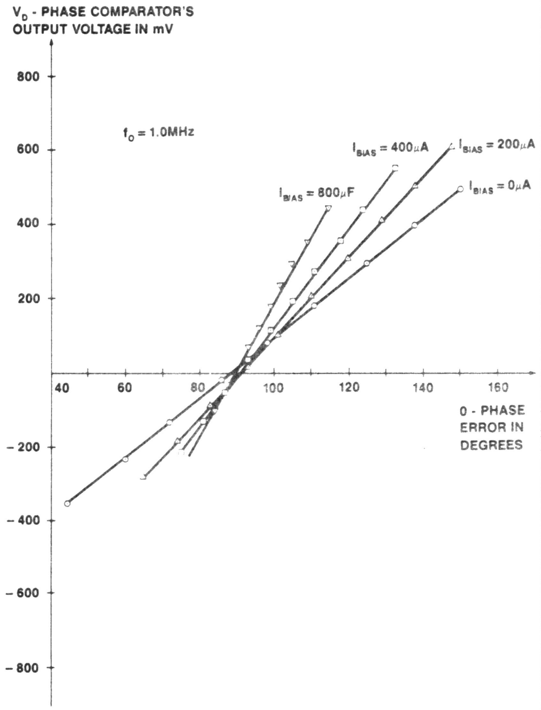
TYPICAL NORMALIZED VCO FREQUENCY AS A FUNCTION OF PIN 2 BIAS CURRENT



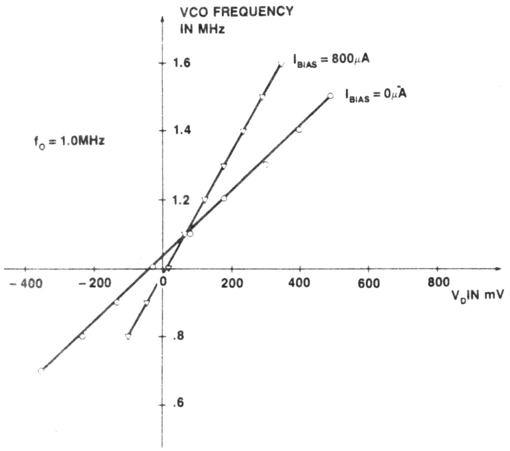
NORMALIZED VCO FREQUENCY AS A FUNCTION OF TEMPERATURE



VARIATION OF THE PHASE COMPARATOR'S OUTPUT VOLTAGE VERSUS PHASE ERROR AND BIAS CURRENT (K_D)



VCO OUTPUT FREQUENCY AS A FUNCTION OF INPUT VOLTAGE AND BIAS CURRENT (K_O)



PHASE LOCKED LOOP SE/NE564

FUNCTIONAL DESCRIPTION (figure 1)

The NE564 is a monolithic phase locked loop with a post detection processor. The use of Schottky clamped transistors and optimized device geometries extends the frequency of operation to greater than 50MHz. In addition to the classical PLL applications, the NE564 can be used as a modulator with a controllable frequency deviation.

The output voltage of the PLL can be written as shown in the following equation:

$$V_O = \frac{(f_{in} - f_o)}{K_{VCO}} \qquad \text{Equation 1}$$

K_{VCO} = conversion gain of the VCO
f_{in} = frequency of the input signal
f_o = free running frequency of the VCO

The process of recovering FSK signals involves the conversion of the PLL output into logic compatible signals. For high data rates, a considerable amount of carrier will be present at the output of the PLL due to the wideband nature of the loop filter. To avoid the use of complicated filters, a comparator with hysteresis or Schmitt trigger is required. With the conversion gain of the VCO fixed, the output voltage as given by Equation 1 varies according to the frequency deviation of f_{in} from f_O. Since this differs from system to system, it is necessary that the hysteresis of the Schmitt trigger be capable of being changed, so that it can be optimized for a particular system. This is accomplished in the 564 by varying the voltage at pin 15 which results in a change of the hysteresis of the Schmitt trigger.

For FSK signals, an important factor to be considered is the drift in the free running frequency of the VCO itself. If this changes due to temperature, according to Equation 1 it will lead to a change in the dc levels of the PLL output, and consequently to errors in the digital output signal. This is especially true for narrow band signals where the deviation in f_{in} itself may be less than the change in f_O due to temperature. This effect can be eliminated if the dc or average value of the signal is retrieved and used as the reference to the comparator. In this manner, variations in the dc levels of the PLL output do not affect the FSK output.

VCO Section

Due to its inherent high frequency performance, an emitter coupled oscillator is used in the VCO. In the circuit, shown in the equivalent schematic, transistors Q_{21} and Q_{23} with current sources $Q_{25} - Q_{26}$ form the basic oscillator. The approximate free running frequency of the oscillator is shown in the following equation:

$$f_o \simeq \frac{1}{22\, R_C\, (C_1 + C_S)} \qquad \text{Equation 2}$$

R_C = R_{19} = R_{20} = 100Ω (INTERNAL)
C_1 = external frequency setting capacitor
C_S = stray capacitance

Variation of V_d (phase detector output voltage) changes the frequency of the oscillator. As indicated by Equation 2, the frequency of the oscillator has a negative

EQUIVALENT SCHEMATIC

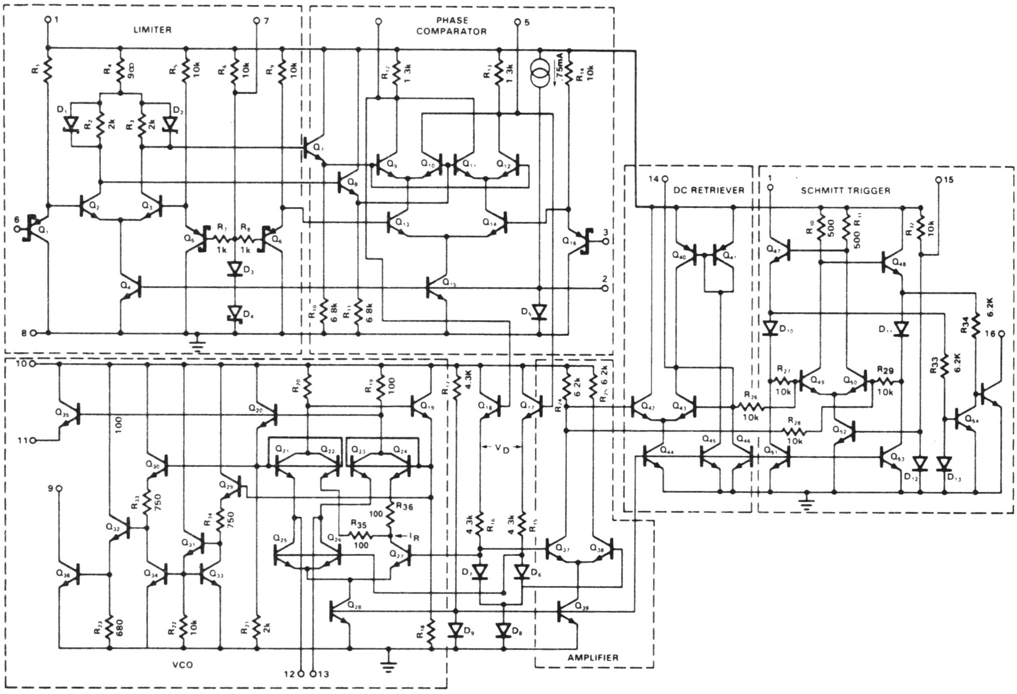


Figure 1

temperature coefficient due to the positive temperature coefficient of the monolithic resistor. To compensate for this, a current I_R with negative temperature coefficient is introduced to achieve a low frequency drift with temperature.

Phase Comparator Section

The phase comparator consists of a double balanced modulator with a limiter amplifier to improve AM rejection. Schottky clamped vertical PNPs are used to obtain TTL level inputs. The loop gain can be varied by changing the current in Q_4 and Q_{15} which effectively changes the gain of the differential amplifiers. This can be accomplished by introducing a current at pin 2.

Post Detection Processor Section

The post detection processor consists of a unity gain transconductance amplifier and comparator. The amplifier can be used as a dc retriever for demodulation of FSK signals, and as a post detection filter for linear FM demodulation. The comparator has adjustable hysteresis so that phase jitter in the output signal can be eliminated.

As shown in the equivalent schematic, the dc retriever is formed by the transductance amplifier $Q_{42}-Q_{43}$ together with an external capacitor which is connected at the amplifier output (pin 14). This forms an integrator whose output voltage is shown in the following equation:

$$V_O = \frac{g_m}{C_2} \int V_{in} dt \qquad \text{Equation 3}$$

g_m = transconductance of the amplifier
C_2 = capacitor at the output (pin 14)
V_{in} = signal voltage at amplifier input

With proper selection of C_2, the integrator time constant can be varied so that the output voltage is the dc or average value of the input signal for use in FSK, or as a post detection filter in linear demodulation.

The comparator with hysteresis is made up of $Q_{49}-Q_{50}$ with positive feedback being provided by Q_{47}-Q_{48}. The hysteresis is varied by changing the current in Q_{52} with a resulting variation in the loop gain of the comparator. This method of hysteresis control, which is a dc control, provides symmetric variation around the nominal value.

Design Formula

The free running frequency of the VCO is shown by the following equation:

$$f_o = \frac{1}{25 R_C (C_1 + C_S)} \qquad \text{Equation 4}$$

R_C = 100Ω
C_1 = external cap in farads
C_S = stray capacitance

FM DEMODULATOR AT 5V

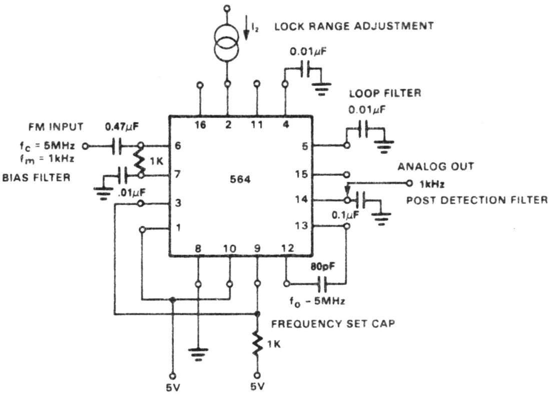

I₂ LOCK RANGE ADJUSTMENT
0.01μF
LOOP FILTER
0.01μF
FM INPUT
0.47μF
fc = 5MHz
fm = 1kHz
1K
BIAS FILTER
.01μF
16
2
11
4
6
5
7
564
15
3
14
1
13
8
10
9
12
ANALOG OUT
1kHz
POST DETECTION FILTER
0.1μF
80pF
fo - 5MHz
FREQUENCY SET CAP
1K
5V
5V

Figure 2

FM DEMODULATOR AT 12V

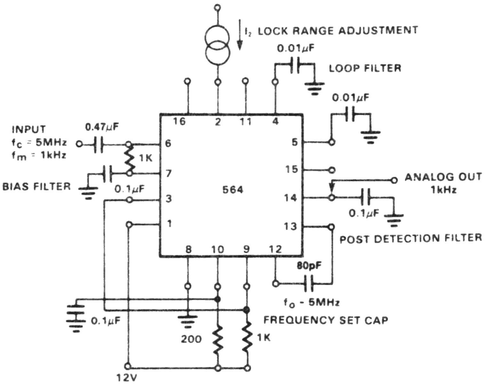

I₂ LOCK RANGE ADJUSTMENT
0.01μF
LOOP FILTER
0.01μF
INPUT
0.47μF
fc = 5MHz
fm = 1kHz
1K
BIAS FILTER
0.1μF
16
2
11
4
6
5
7
15
564
3
14
1
13
8
10
9
12
ANALOG OUT
1kHz
0.1μF
POST DETECTION FILTER
80pF
fo - 5MHz
FREQUENCY SET CAP
0.1μF
200
1K
12V

Figure 3

MODULATOR

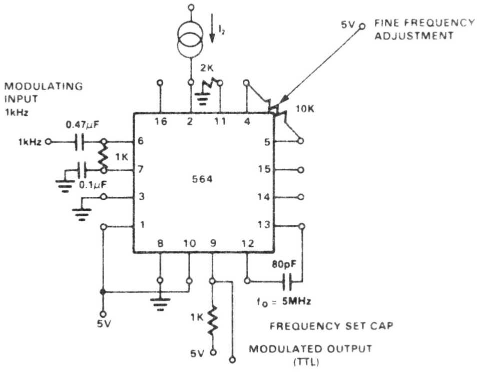

I₂
5V
FINE FREQUENCY ADJUSTMENT
2K
10K
MODULATING INPUT
1kHz
0.47μF
1kHz
1K
0.1μF
16
2
11
4
6
5
7
564
15
3
14
1
13
8
10
9
12
80pF
fo = 5MHz
5V
1K
FREQUENCY SET CAP
5V
MODULATED OUTPUT
(TTL)

Figure 4

The loop filter diagram shown is explained by the following equation:

$$F(s) = \frac{1}{1 + sRC_3} \text{ (First Order)} \qquad \text{Equation 5}$$

$R = R_{12} = R_{13} = 1.3k\Omega$ (INTERNAL)*

By adding capacitors to pins 4 and 5, a pole is added to the loop transfer function at

$$\omega = \frac{1}{RC_3}.$$

*Refer to Figure 1.

APPLICATIONS

FM DEMODULATOR

The NE564 can be used as an FM demodulator. The connections for operation at 5V and 12V are shown in figures 2 and 3 respectively. The input signal is ac coupled with the output signal being extracted at pin 14. Loop filtering is provided by the capacitors at pins 4 and 5 with additional filtering being provided by the capacitor at pin 14. Since the conversion gain of the VCO is not very high, to obtain sufficient demodulated output signal the frequency deviation in the input signal should be 1% or higher.

MODULATION TECHNIQUES

The NE564 phase locked loop can be modulated at either the loop filter ports (pins 4 and 5) or the input port (pin 6) as shown in figure 4. The approximate modulation frequency can be determined from the frequency conversion gain curve shown in figure 5. This curve will be appropriate for signals injected into pins 4 and 5 as shown in figure 4.

FSK Demodulation

The 564 PLL is particularly attractive for FSK demodulation since it contains an internal voltage comparator and VCO which have TTL compatible inputs and outputs, and it can operate from a single 5 volt power supply. Demodulated dc voltages associated with the mark and space frequencies are recovered with a single external capacitor in a dc retriever without utilizing extensive filtering networks. An internal comparator, acting as a Schmitt trigger with an adjustable hysteresis, shapes the demodulated voltages into compatible TTL output levels. The high frequency design of the 564 enables it to demodulate FSK at high data rates in excess of 1.0M baud.

Figure 5 shows a high-frequency FSK decoder designed for input frequency deviations of ± 1.0MHz centered around a free-running frequency of 10.8MHz. The value of the timing capacitance required was estimated from figure 8 to be approximately 40pF. A trimmer capacitor was added to fine tune f_o' to 10.8MHz.

The lock range graph indicates that the ± 1.0MHz frequency deviations will be within the lock range for input signal levels greater than approximately 50mV with zero pin 2 bias current. While strictly this figure is appropriate only for 5MHz, it can be used as a guide for lock range estimates at other f_o' frequencies.

The hysteresis was adjusted experimentally via the 10kΩ potentiometer and 2kΩ bias arrangement to give the waveshape shown in figure 7 for 20K, 500K, 2M baud rates with square wave FSK modulation. Note the magnitude and phase relationships of the phase comparators output voltages with respect to each other and to the FSK output. The high frequency sum components of the input and VCO frequency also are visible as noise on the phase comparators outputs.

10.8MHz FSK DECODER USING THE 564

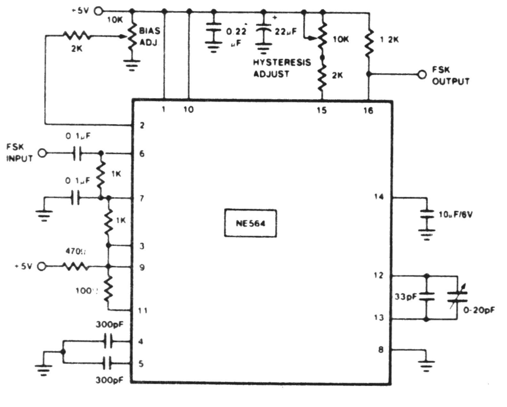
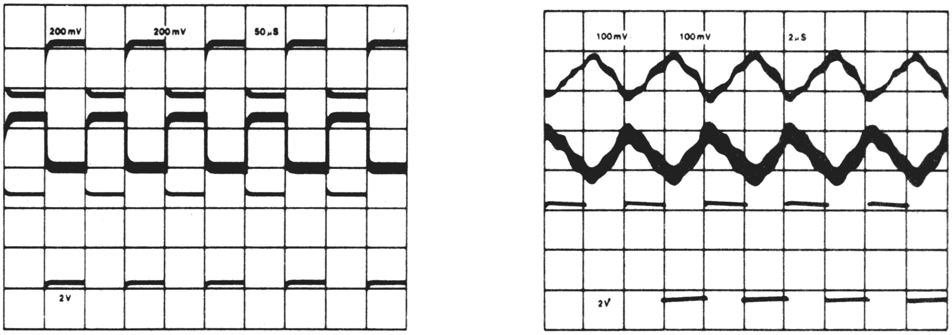
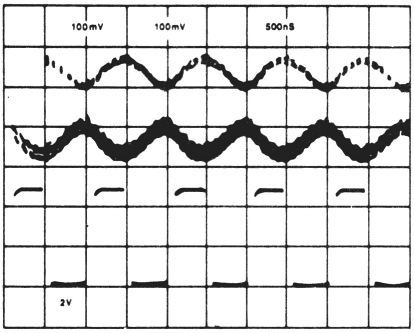


Figure 5

PHASE COMPARATOR (PINS 4 AND 5) AND FSK (PIN 16) OUTPUTS FOR DATA RATES OF



(a) 20K BAUD (b) 500K BAUD



NOTE
Top trace-pin 4
Center trace-pin 5
Bottom trace-pin 16

(c) 2.0M BAUD

Figure 6

OUTLINE OF SETUP PROCEDURE

1. Determine operating frequency of the VCO – .
   If ÷ N in feedback loop, then
   $f_o = N \times f_{in}$.
2. Calculate value of the VCO frequency set capacitor:
   $$C_O \simeq \frac{1}{2500\, f_o}$$
3. Set I_2 (current sinking into Pin 2) for $\cong 100\mu A$. After operation is obtained, this value may be adjusted for best dynamic behavior.
4. Check VCO output frequency with digital counter at Pin 9 of device (loop open, VCO to ϕ det.). Adjust C_O trim or frequency adj. Pin 4-5 for exact center frequency if needed.
5. Close loop and inject input signal to Pin 6. Monitor Pin 3 and 6 with two channel scope. Lock should occur with $\Delta\phi_{3-6}$ equal to 90° (phase error).
6. If pulsed burst or ramp frequency is used for input signal, special loop filter design may be required in place of simple single capacitor filter on Pin 4 and 5. (See PLL application section in Analog Manual.)
7. The input signal to Pin 6 and the VCO feedback signal to Pin 3 must have a duty cycle of 50% for proper operation of the phase detector. Due to the nature of a balanced mixer if signals are not 50% in duty cycle, D.C. offsets will occur in the loop which tend to create an artificial or biased VCO offset.
8. For multiplier circuits where phase jitter is a problem, loop filter capacitors may be increased to a value of 10-50μF on Pin 4, 5. Also careful supply decoupling may be necessary. This includes the counter chain V_{CC} lines.

NE564 PHASE LOCKED FREQUENCY MULTIPLIER WITH VCXO

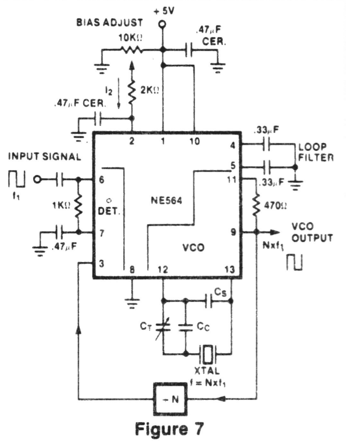


Figure 7

*For additional information, consult the Applications Section.

PHASE LOCKED LOOP SE/NE565

DESCRIPTION

The SE/NE565 Phase-Locked Loop (PLL) is a self-contained, adaptable filter and demodulator for the frequency range from 0.001Hz to 500kHz. The circuit comprises a voltage-controlled oscillator of exceptional stability and linearity, a phase comparator, an amplifier and a low-pass filter as shown in the block diagram. The center frequency of the PLL is determined by the free-running frequency of the VCO; this frequency can be adjusted externally with a resistor or a capacitor. The low-pass filter, which determines the capture characteristics of the loop, is formed by an internal resistor and an external capacitor.

FEATURES

- **Highly stable center frequency (200ppm/°C typ.)**
- **Wide operating voltage range (±6 to ±12 volts)**
- **Highly linear demodulated output (0.2% typ.)**
- **Center frequency programming by means of a resistor or capacitor, voltage or current**
- **TTL and DTL compatible square-wave output; loop can be opened to insert digital frequency divider**
- **Highly linear triangle wave output**
- **Reference output for connection of comparator in frequency discriminator**
- **Bandwidth adjustable from < ±1% to > ±60%**
- **Frequency adjustable over 10 to 1 range with same capacitor**

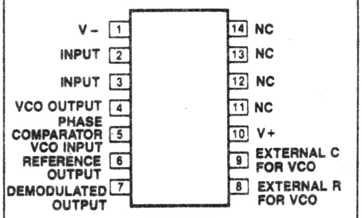
APPLICATIONS

- **Frequency shift keying**
- **Modems**
- **Telemetry receivers**
- **Tone decoders**
- **SCA receivers**
- **Wideband FM discriminators**
- **Data synchronizers**
- **Tracking filters**
- **Signal restoration**
- **Frequency multiplication & division**

NOTES:
1. SOL — Released in large SO package only.
2. SOL *and* non-standard pinout.
3. SO *and* non-standard pinout.

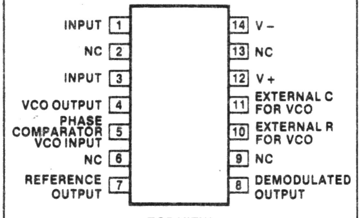
PIN CONFIGURATIONS

F,N PACKAGE


V- 1
INPUT 2
INPUT 3
VCO OUTPUT 4
PHASE COMPARATOR VCO INPUT 5
REFERENCE OUTPUT 6
DEMODULATED OUTPUT 7
14 NC
13 NC
12 NC
11 NC
10 V+
9 EXTERNAL C FOR VCO
8 EXTERNAL R FOR VCO

TOP VIEW
ORDER NUMBER
SE/NE565F,N

D³ PACKAGE

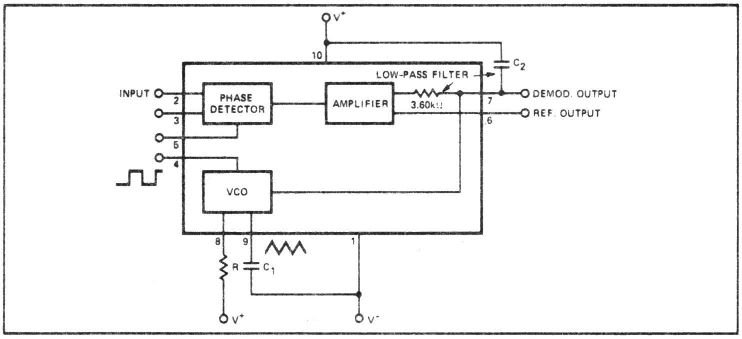

INPUT 1
NC 2
INPUT 3
VCO OUTPUT 4
PHASE COMPARATOR VCO INPUT 5
NC 6
REFERENCE OUTPUT 7
14 V-
13 NC
12 V+
11 EXTERNAL C FOR VCO
10 EXTERNAL R FOR VCO
9 NC
8 DEMODULATED OUTPUT

TOP VIEW
ORDER NUMBER
NE565D

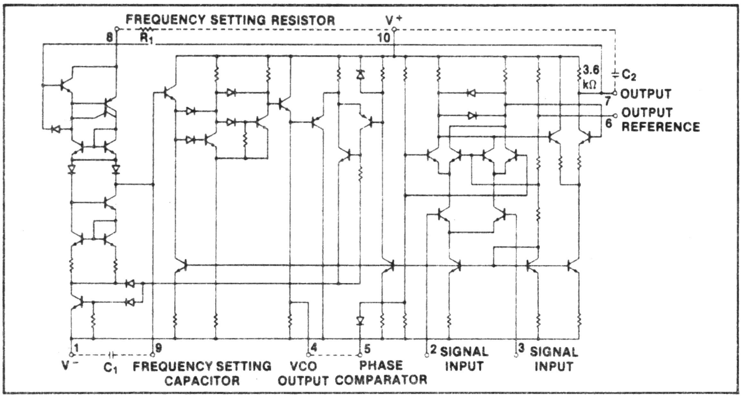
ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$ unless otherwise specified.

PARAMETER	RATING	UNIT
Maximum operating voltage	26	V
Input voltage	3	Vp-p
Storage temperature	-65 to +150	°C
Operating temperature range		
NE565	0 to +70	°C
SE565	-55 to +125	°C
Power dissipation	300	mW

BLOCK DIAGRAM


V+
10
C2
LOW-PASS FILTER
INPUT
2
3
5
4
PHASE DETECTOR
AMPLIFIER
3.60kΩ
7
DEMOD. OUTPUT
6
REF. OUTPUT
VCO
8
9
1
R
C1
V+
V-

EQUIVALENT SCHEMATIC


FREQUENCY SETTING RESISTOR
V+
8
R1
10
3.6 kΩ
C2
7 OUTPUT
OUTPUT 6 REFERENCE
1
V-
C1
9
FREQUENCY SETTING CAPACITOR
4
VCO OUTPUT
5
PHASE COMPARATOR
2 SIGNAL INPUT
3 SIGNAL INPUT

PHASE LOCKED LOOP

SE/NE565

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = ±6V$ unless otherwise specified.

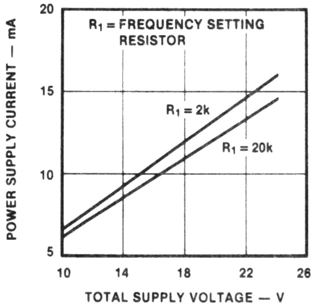
PARAMETER	TEST CONDITIONS	SE565			NE565			UNIT
		Min	Typ	Max	Min	Typ	Max	
SUPPLY REQUIREMENTS								
Supply voltage		± 6		±12	±6		±12	V
Supply current			8	12.5		8	12.5	mA
INPUT CHARACTERISTICS								
Input impedance[1]		7	10		5	10		kΩ
Input level required for tracking	f_o = 50kHz, ±10% frequency deviation	10			10			mVrms
VCO CHARACTERISTICS								
Center frequency								
Maximum value		300	500			500		kHz
Distribution[2]	Distribution taken about f_o = 50kHz, R_1 = 5.0kΩ, C_1 = 1200pF	-10	0	+10	-30	0	+30	%
Drift with temperature	f_o = 50kHz		200			300		ppm/°C
Drift with supply voltage	f_o = 50kHz, V_{CC} = ±6 to ±7 volts		0.1	1.0		0.2	1.5	%/V
Triangle wave								
Output voltage level		1.9	2.4	3	1.9	2.4	3	Vp-p
Linearity			0.2			0.5		%
Square wave								
Logical "1" output voltage	f_o = 50kHz	+4.9	+5.2		+4.9	+5.2		V
Logical "0" output voltage	f_o = 50kHz		-0.2	+0.2		-0.2	+0.2	V
Duty cycle	f_o = 50kHz	45	50	55	40	50	60	%
Rise time			20	100		20		ns
Fall time			50	200		50		ns
Output current (sink)		0.6	1		0.6	1		mA
Output current (source)		5	10		5	10		mA
DEMODULATED OUTPUT CHARACTERISTICS								
Output voltage level	Measured at pin 7	4.25	4.5	4.75	4.0	4.5	5.0	V
Maximum voltage swing[3]			2			2		Vp-p
Output voltage swing	±10% frequency deviation	250	300		200	300		mVp-p
Total harmonic distortion			0.2	0.75		0.4	1.5	%
Output impedance[4]			3.6			3.6		kΩ
Offset voltage (V6-V7)			30	100		50	200	mV
Offset voltage vs temperature (drift)			50			100		μV/°C
AM rejection		30	40			40		dB

NOTES

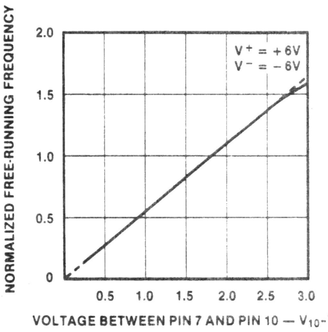
1. Both input terminals (pins 2 and 3) must receive identical dc bias. This bias may range from 0 volts to -4 volts.
2. The external resistance for frequency adjustment (R1) must have a value between 2kΩ and 20kΩ.
3. Output voltage swings negative as input frequency increases.
4. Output not buffered.

TYPICAL PERFORMANCE CHARACTERISTICS

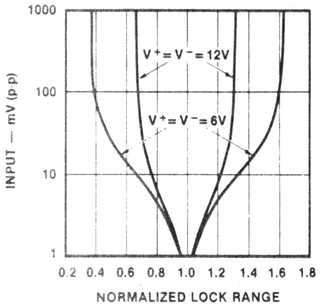
POWER SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



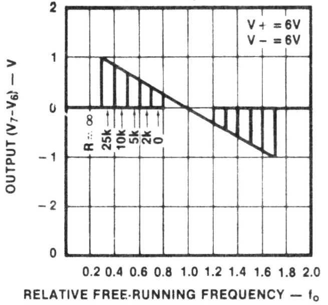
VCO CONVERSION GAIN



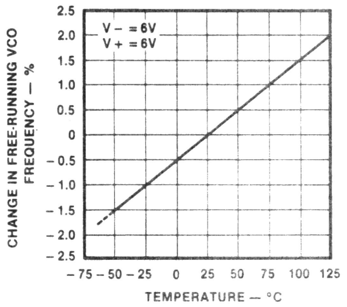
LOCK RANGE AS A FUNCTION OF INPUT VOLTAGE



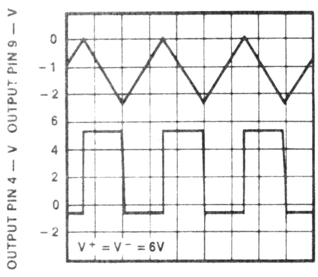
LOCK RANGE AS A FUNCTION OF GAIN SETTING RESISTANCE (PIN 6-7)



CHANGE IN FREE-RNNING VCO FREQUENCY AS A FUNCTION OF TEMPERATURE



VCO OUTPUT WAVEFORM



DESIGN FORMULAS (See Figure 1)

Free-running frequency of VCO: $f_o \approx \frac{1.2}{4R_1C_1}$ in Hz

Lock-range: $f_L = \pm \frac{8f_o}{V_{CC}}$ in Hz

Capture-range: $f_C \approx \pm \frac{1}{2\pi}\sqrt{\frac{2\pi f_L}{\tau}}$

where $\tau = (3.6\text{X}10^3)\ \text{X}\ C_2$

TYPICAL APPLICATIONS

FM Demodulation

The 565 Phase Locked Loop is a general purpose circuit designed for highly linear FM demodulation. During lock, the average dc level of the phase comparator output signal is directly proportional to the frequency of the input signal. As the input frequency shifts, it is this output signal which causes the VCO to shift its frequency to match that of the input. Consequently, the linearity of the phase comparator output with frequency is determined by the voltage-to-frequency transfer function of the VCO.

Because of its unique and highly linear VCO, the 565 PLL can lock to and track an input signal over a very wide bandwidth (typically ±60%) with very high linearity (typically, within 0.5%).

A typical connection diagram is shown in Figure 1. The VCO free-running frequency is given approximately by

$f_o \approx \frac{1.2}{4R_1C_1}$ and should be adjusted to be at the center of the input signal frequency range, C1 can be any value, but R1 should be within the range of 2000 to 20,000 ohms with an optimum value on the order of 4000 ohms. The source can be direct coupled if the dc resistances seen from pins 2 and 3 are equal and there is no DC voltage difference between the pins. A short between pins 4 and 5 connects the VCO to the phase comparator. Pin 6 provides a DC reference voltage that is close to the DC potential of the demodulated output (pin 7). Thus, if a resistance is connected between pins 6 and 7, the gain of the output stage can be reduced with little change in the DC voltage level at the output. This allows the lock range to be decreased with little change in the free-running frequency. In this manner the lock range can be decreased from ± 60% of f_o to approximately ± 20% of f_o (at ± 6V).

A small capacitor (typically 0.001μF) should be connected between pins 7 and 8 to eliminate possible oscillation in the control current source.

A single-pole loop filter is formed by the capacitor C2, connected between pin 7 and the positive supply, and an internal resistance of approximately 3600 ohms.

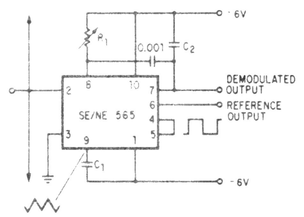


Figure 1

Frequency Shift Keying (FSK)

FSK refers to data transmission by means of a carrier which is shifted between two preset frequencies. This frequency shift is usually accomplished by driving a VCO with the binary data signal so that the two resulting frequencies correspond to the "0" and "1" states (commonly called space and mark) of the binary data signal.

A simple scheme using the 565 to receive FSK signals of 1070Hz and 1270Hz is shown in Figure 2. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output.

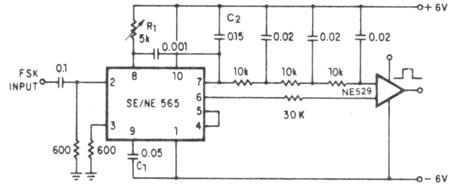


Figure 2

The loop filter capacitor C2 is chosen smaller than usual to eliminate overshoot on the output pulse, and a three-stage RC ladder filter is used to remove the carrier component from the output. The band edge of the ladder filter is chosen to be approximately half way between the maximum keying rate (in this case 300 baud or 150Hz) and twice the input frequency (approximately 2200Hz). The output signal can now be made logic compatible by connecting a voltage comparator between the output and pin 6 of the loop. The free-running frequency is adjusted with R1 so as to result in a slightly-positive voltage at the output with $f_{IN} = 1070Hz$.

The input connection is typical for cases where a dc voltage is present at the source and therefore a direct connection is not desirable. Both input terminals are returned to ground with identical resistors (in this case, the values are chosen to effect a 600-ohm input impedance).

Frequency Multiplication

There are two methods by which frequency multiplication can be achieved using the 565:

1. Locking to a harmonic of the input signal.
2. Inclusion of a digital frequency divider or counter in the loop between the VCO and phase comparator.

The first method is the simplest, and can be achieved by setting the free-running frequency of the VCO to a multiple of the input frequency. A limitation of this scheme is that the lock range decreases as successively higher and weaker harmonics are used for locking. If the input frequency is to be constant with little tracking required, the loop can generally be locked to any one of the first 5 harmonics. For higher orders of multiplication, or for cases where a large lock range is desired, the second scheme is more desirable. An example of this might be a case where the input signal varies over a wide frequency range and a large multiple of the input frequency is required.

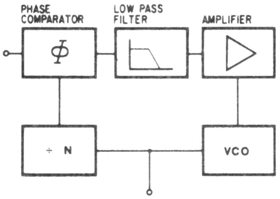


Figure 3

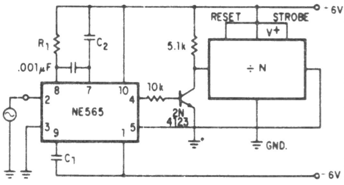


Figure 4

A block diagram of the second scheme is shown in Figure 3. Here the loop is broken between the VCO and the phase comparator, and a frequency divider is inserted. The fundamental of the divided VCO frequency is locked to the input frequency in this case, so that the VCO is actually running at a multiple of the input frequency. The amount of multiplication is determined by the frequency divider. A typical connection scheme is shown in Figure 4. To set up the circuit, the frequency limits of the input signal must be determined. The free-running frequency of the VCO is then adjusted by means of R1 and C1 (as discussed under FM demodulation) so that the output frequency of the divider is midway between the input frequency limits. The filter capacitor, C2, should be large enough to eliminate variations in the demodulated output voltage (at pin 7), in order to stabilize the VCO frequency. The output can now be taken as the VCO squarewave output, and its fundamental will be the desired multiple of the input frequency (f_{IN}) as long as the loop is in lock.

SCA (Background Music) Decoder

Some FM stations are authorized by the FCC to broadcast uninterrupted background music for commerical use. To do this a frequency modulated subcarrier of 67kHz is used. The frequency is chosen so as not to interfere with the normal stereo or monaural program; in addition, the level of the subcarrier is only 10% of the amplitude of the combined signal.

The SCA signal can be filtered out and demodulated with the NE565 Phase Locked Loop without the use of any resonant circuits. A connection diagram is shown in Figure 5. This circuit also serves as an example of operation from a single power supply.

A resistive voltage divider is used to establish a bias voltage for the input (pins 2 and 3). The demodulated (multiplex) FM signal is fed to the input through a two-stage high-pass filter, both to effect capacitive coupling and to attenuate the strong signal of the regular channel. A total signal amplitude, between 80mV and 300mV, is required at the input. Its source should have an impedance of less than 10,000 ohms.

The Phase Locked Loop is tuned to 67kHz with a 5000 ohm potentiometer; only approximate tuning is required, since the loop will seek the signal.

The demodulated output (pin 7) passes through a three-stage low-pass filter to provide de-emphasis and attenuate the high-frequency noise which often accompanies SCA transmission. Note that no capacitor is provided directly at pin 7; thus, the circuit is operating as a first-order loop. The demodulated output signal is in the order of 50mV and the frequency response extends to 7kHz.

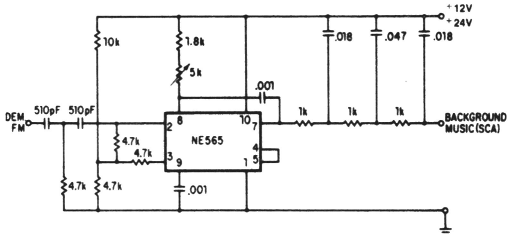

+12V
+24V
.018
.047
.018
10k
1.8k
5k
.001
DEM FM
510pF
510pF
8
10
7
2
NE565
4.7k
4.7k
3
9
4
5
1
1k
1k
1k
BACKGROUND MUSIC (SCA)
4.7k
4.7k
.001

Figure 5

***For additional information, consult the Applications Section.**

FUNCTION GENERATOR

SE/NE566

DESCRIPTION

The SE/NE 566 Function Generator is a voltage controlled oscillator of exceptional linearity with buffered square wave and triangle wave outputs. The frequency of oscillation is determined by an external resistor and capacitor and the voltage applied to the control terminal. The oscillator can be programmed over a ten to one frequency range by proper selection of an external resistance and modulated over a ten to one range by the control voltage, with exceptional linearity.

FEATURES

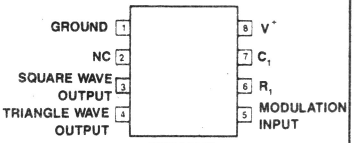
- **Wide range of operating voltage (up to 24 volts) (single or dual)**
- **High linearity of modulation**
- **Highly stable center frequency (200 ppm/°C typical)**
- **Highly linear triangle wave output**
- **Frequency programming by means of a resistor or capacitor, voltage or current**
- **Frequency adjustable over 10 to 1 range with same capacitor**

APPLICATIONS

- **Tone generators**
- **Frequency shift keying**
- **FM modulators**
- **Clock generators**
- **Signal generators**
- **Function generators**

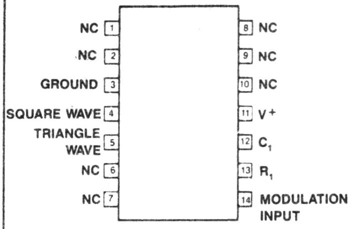
PIN CONFIGURATIONS

D, N PACKAGE


GROUND 1
NC 2
SQUARE WAVE OUTPUT 3
TRIANGLE WAVE OUTPUT 4
8 V+
7 C1
6 R1
5 MODULATION INPUT

TOP VIEW
ORDER NUMBERS
SE/NE566N NE566D

F PACKAGE

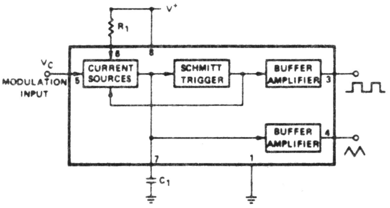

NC 1
NC 2
GROUND 3
SQUARE WAVE 4
TRIANGLE WAVE 5
NC 6
NC 7
8 NC
9 NC
10 NC
11 V+
12 C1
13 R1
14 MODULATION INPUT

TOP VIEW
ORDER NUMBERS
SE/NE566F

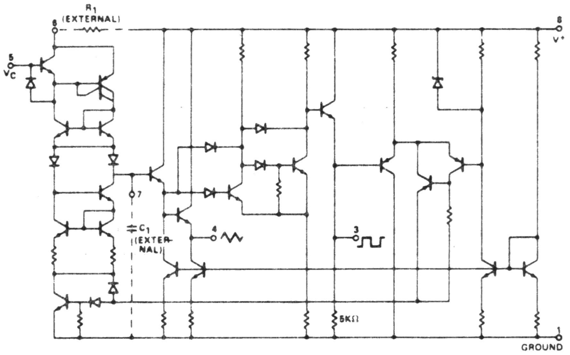
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Maximum operating voltage	26	V
Input voltage	3	V_{P-P}
Storage temperature	-65 to +150	°C
Operating temperature range		
NE566	0 to +70	°C
SE566	-55 to +125	°C
Power dissipation	300	mW

BLOCK DIAGRAM


V+
R1
8
8
VC
MODULATION INPUT
5
CURRENT SOURCES
SCHMITT TRIGGER
BUFFER AMPLIFIER
3
BUFFER AMPLIFIER
4
7
1
C1

EQUIVALENT SCHEMATIC


R1 (EXTERNAL)
8
5
VC
8
V+
7
C1 (EXTERNAL)
4
3
5KΩ
1
GROUND

FUNCTION GENERATOR SE/NE566

ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = \pm 6V$ unless otherwise specified.

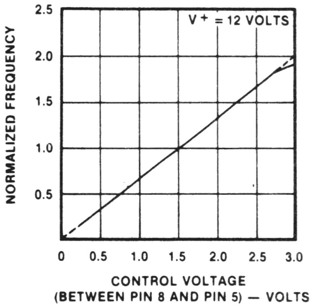
PARAMETER	SE566			NE566			UNIT
	Min	Typ	Max	Min	Typ	Max	
GENERAL							
Operating temperature range	-55		125	0		70	°C
Operating supply voltage	±6		±12	±6		±12	V
Operating supply current		7	12.5		7	12.5	mA
VCO[1]							
Maximum operating frequency		1			1		MHz
Frequency drift with temperature		200			300		ppm/°C
Frequency drift with supply voltage		.1	1		.2	2	%/V
Control terminal input impedance[2]		1			1		MΩ
FM distortion (±10% deviation)		0.2	0.75		0.4	1.5	%
Maximum sweep rate		1			1		MHz
Sweep range		10:1			10:1		
OUTPUT							
Triangle wave output							
Impedance		50			50		Ω
Voltage	1.9	2.4		1.9	2.4		Vpp
Linearity		0.2			0.5		%
Square wave input							
Impedance		50			50		Ω
Voltage	5	5.4		5	5.4		Vpp
Duty Cycle	45	50	55	40	50	60	%
Rise time		20			20		ns
Fall Time		50			50		ns

NOTES

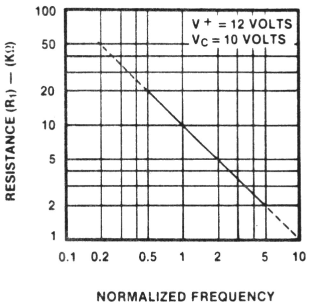
1. The external resistance for frequency adjustment (R_1) must have a value between 2kΩ and 20KΩ.
2. The bias voltage (V_C) applied to the control terminal (pin 5) should be in the range $3/4V^+ \le V_C \le V^+$

TYPICAL PERFORMANCE CHARACTERISTICS

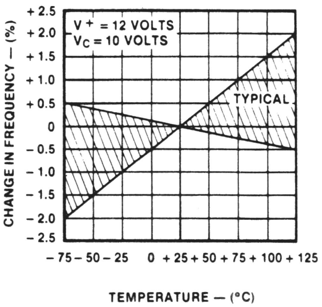
NORMALIZED FREQUENCY AS A FUNCTION OF CONTROL VOLTAGE



NORMALIZED FREQUENCY AS A FUNCTION OF RESISTANCE (R1)



CHANGE IN FREQUENCY AS A FUNCTION OF TEMPERATURE



LOW POWER DUAL OPERATIONAL AMPLIFIERS SA/SE/NE532/LM158/258/358

DESCRIPTION

The 532/358 consists of two independent, high gain, internally frequency compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages. Operation from dual power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

FEATURES

- **Internally frequency compensated for unity gain**
- **Large dc voltage gain—(100dB)**
- **Wide bandwidth (unity gain)—1MHz (temperature compensated)**
- **Wide power supply range single supply—(3Vdc to 30Vdc) or dual supplies—(±1.5Vdc to ±15Vdc)**
- **Very low supply current drain (400μA)—essentially independent of supply voltage (1mW/op amp at +5Vdc)**
- **Low input biasing current—(45nA dc temperature compensated)**
- **Low input offset voltage—(2mVdc) and offset current—(5nA dc)**
- **Differential input voltage range equal to the power supply voltage**
- **Large output voltage—(0Vdc to V+—-1.5Vdc swing)**
- **SE532 MIL-STD-883A,B,C available**

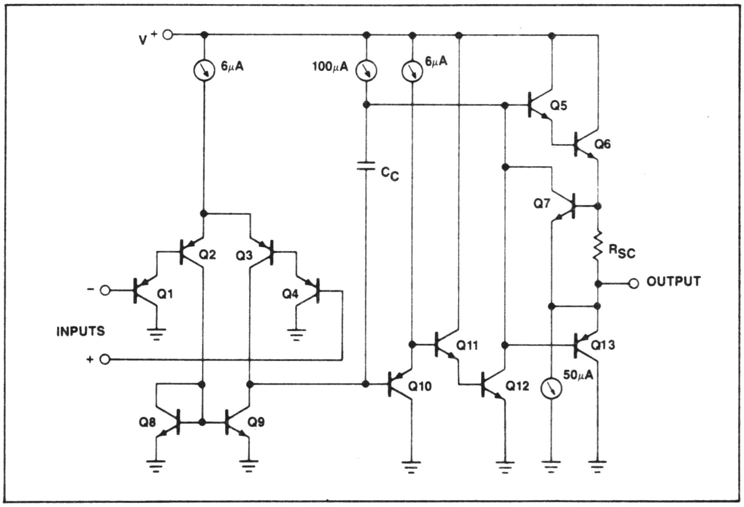
UNIQUE FEATURES

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage. The unity gain cross frequency is temperature compensated. The input bias current is also temperature compensated.

ABSOLUTE MAXIMUM RATINGS

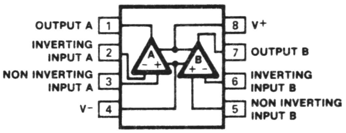
PARAMETER	RATING	UNIT
Supply voltage, V+	32 or ±16	Vdc
Differential input voltage	32	Vdc
Input voltage	-0.3 to +32	Vdc
Power dissipation[1]		
FE package	900	mW
H package	680	mW
N package	500	mW
Output short-circuit to GND[5]		
V+ < 15 Vdc and T_A = 25°C	Continuous	
Operating temperature range		
NE532/LM358	0 to +70	°C
LM258	-25 to +85	°C
SA532N	-40 to +85	°C
SE532/LM158	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 10sec)	300	°C

EQUIVALENT CIRCUIT


V+
6μA
100μA
6μA
Q5
Q6
CC
Q7
RSC
OUTPUT
Q2
Q3
Q1
Q4
INPUTS
-
+
Q11
Q13
Q10
Q12
50μA
Q8
Q9

PIN CONFIGURATIONS

D,FE,N PACKAGE

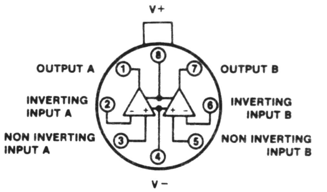

OUTPUT A 1
INVERTING INPUT A 2
NON INVERTING INPUT A 3
V- 4
8 V+
7 OUTPUT B
6 INVERTING INPUT B
5 NON INVERTING INPUT B
A
B

TOP VIEW

ORDER NUMBERS

LM158N, FE	NE532D, N, FE
LM258N, FE	SA532FE, N
LM358D, N, FE	SE532N, FE

H PACKAGE*


V+
8
OUTPUT A 1
OUTPUT B 7
INVERTING INPUT A 2
INVERTING INPUT B 6
NON INVERTING INPUT A 3
NON INVERTING INPUT B 5
4
V-

ORDER NUMBERS

LM158/258/358H
NE/SE532H

*Metal cans (H) not recommended for new designs

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, V+ = +5V unless otherwise specified.

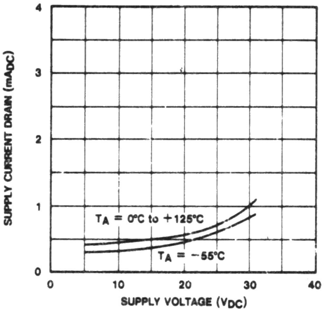
PARAMETER	TEST CONDITIONS	SE532, LM158/258			NE/SA532/LM358			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS} Offset voltage[1]	$R_S \leq 0\Omega$		±2	±5		±2	±7	mV
	$R_S \leq 0\Omega$, over temp.			±7			±9	mV
V_{OS} Drift	$R_S = 0\Omega$, over temp.		7			7		μV/°C
I_{OS} Offset current	$I_{IN}(+) - I_{IN}(-)$		±3	±30		±5	±50	nA
	Over temp.			±100			±150	nA
I_{OS} Drift	Over temp.		10			10		pA/°C
I_{BIAS} Input current[2]	$I_{IN}(+)$ or $I_{IN}(-)$		45	150		45	250	nA
	Over temp., $I_{IN}(+)$ or $I_{IN}(-)$		40	300		40	500	nA
I_B Drift	Over temp		50			50		pA/°C
V_{CM} Common mode voltage range[3]	V+ = 30V	0		V+ −1.5	0		V+ −1.5	V
	Over temp., V+ = 30V	0		V+ −2.0	0		V+ −2.0	V
C_{MRR} Common mode rejection ratio	V+ = 30V	70	85		65	70		dB
V_{OUT} Output voltage swing (V_{OH})	$R_L \geq 2k\Omega$, V+ = 30V, over temp.	26			26			V
	$R_L \geq 10k\Omega$, V+ = 30V, over temp.	27	28		27	28		V
V_{OUT} Output voltage swing (V_{OL})	$R_L \leq 10k\Omega$, over temp.		5	20		5	20	mV
I_{CC} Supply current	$R_L = \infty$, V+ = 30V		1.0	2.0		1.0	2.0	mA
	$R_L = \infty$ on all amplifiers, over temp.		0.5	1.2		0.5	1.2	mA
A_{VOL} Large signal voltage gain	$R_L \geq 2k\Omega$, V_{OUT} ± 10V, V+ = 15V	50	100		25	100		V/mV
	(for large V_O swing) over temp.	25			15			V/mV
PSRR Supply voltage rejection ratio	$R_S \leq 0\Omega$	65	100		65	100		dB
Amplifier-to-amplifier coupling[4]	f = 1kHz to 20kHz (input referred)		−120			−120		dB
Output current Source	V_{IN+} = +1Vdc, V_{IN-} = 0Vdc, V+ = 15Vdc	20	40		20	40		mA
	V_{IN+} = +1Vdc, V_{IN-} = 0Vdc, V+ = 15Vdc, over temp.	10	20		10	20		mA
Sink	V_{IN-} = +1Vdc, V_{IN+} = 0Vdc, V+ = 15Vdc	10	20		10	20		mA
	V_{IN-} = +1Vdc, V_{IN+} = 0Vdc, V+ = 15Vdc, over temp.	5	8		5	8		mA
	V_{IN+} = 0V, V_{IN-} = +1Vdc, V_O = 200mV	12	50		12	50		μA
I_{SC} Short circuit current[5]			40	60		40	60	mA
Differential input voltage[6]				V+			V+	V
GBW Unity gain bandwidth	T_A = 25°C		1			1		MHz
S.R. Slew rate	T_A = 25°C		0.3			0.3		V/μs
Noise Input Noise Voltage	T_A = 25°C, f = 1kHz		40			40		nV/√Hz

NOTES

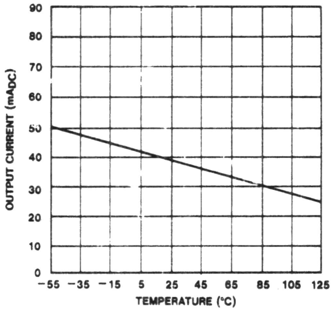
1. $V_O \cong 1.4V$, $R_S = 0\Omega$ with V+ from 5V to 30V; and over the full input common-mode range (0V to V+ − 1.5V).
2. The direction of the input current is out of the IC due to the pnp input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ − 1.5V, but either or both inputs can go to +32V without damage.
4. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance coupling increases at higher frequencies.
5. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of +15Vdc, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ − 1.5V, buteither or both inputs can go to +32Vdc without damage.
7. For operating at high temperatures, all devices must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient.

TYPICAL PERFORMANCE CHARACTERISTICS

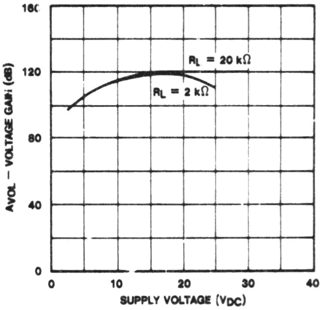
SUPPLY CURRENT



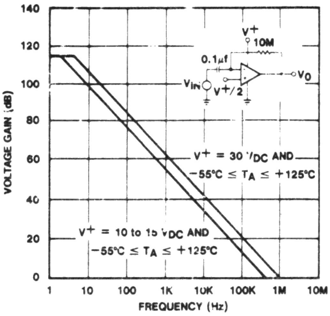
CURRENT LIMITING



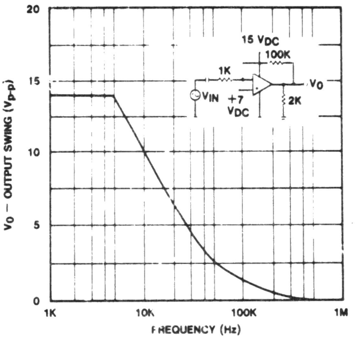
VOLTAGE GAIN



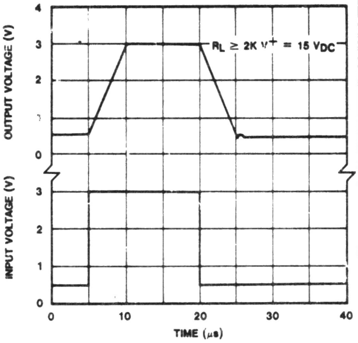
OPEN LOOP FREQUENCY RESPONSE



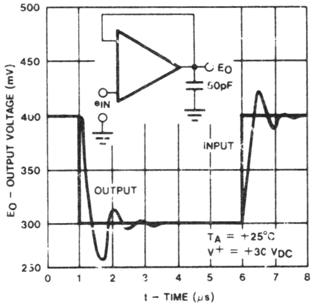
LARGE SIGNAL FREQUENCY RESPONSE



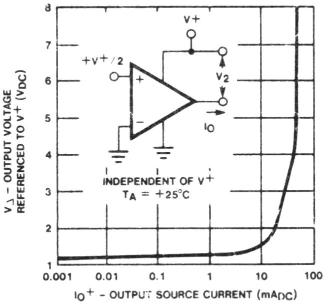
VOLTAGE FOLLOWER PULSE RESPONSE



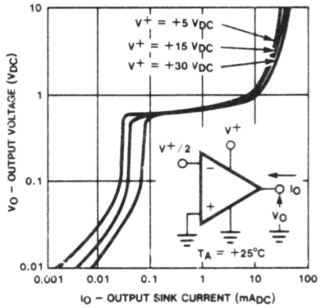
VOLTAGE FOLLOWER PULSE RESPONSE (SMALL SIGNAL)



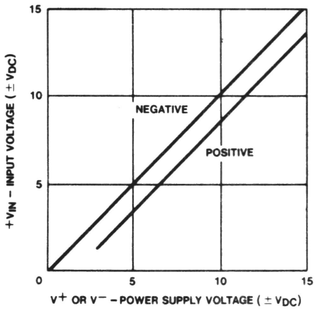
OUTPUT CHARACTERISTICS CURRENT SOURCING

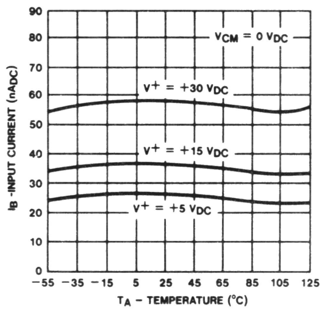


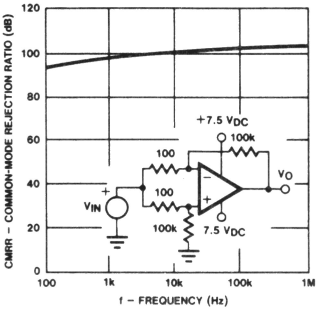
OUTPUT CHARACTERISTICS CURRENT SINKING



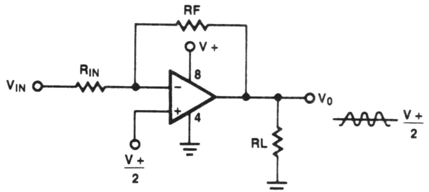
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

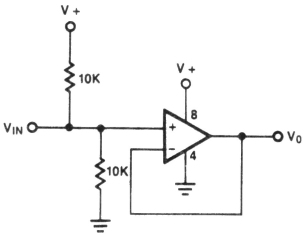

INPUT VOLTAGE RANGE

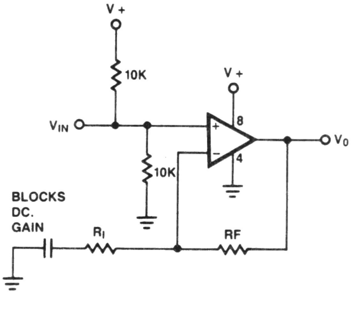

INPUT CURRENT


COMMON MODE REJECTION RATIO

TYPICAL APPLICATIONS


SINGLE SUPPLY INVERTING AMPLIFIER
RF
V+
RIN
VIN
8
4
V0
RL
V+/2
V+/2


INPUT BIASING *VOLTAGE FOLLOWER
V+
10K
V+
VIN
8
4
10K
V0


NON-INVERTING AMPLIFIER
V+
10K
V+
VIN
8
4
V0
10K
BLOCKS DC. GAIN
RI
RF

GENERAL PURPOSE OPERATIONAL AMPLIFIER MC/SA1458/MC1558

DESCRIPTION

The MC1458 is a high performance operational amplifier with high open loop gain, internal compensation, high common mode range and exceptional temperature stability. The MC1458 is short-circuit protected and allows for nulling of offset voltage.

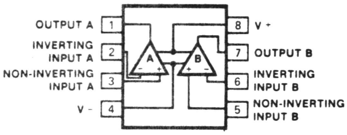
The MC1458/SA1458/MC1558 consists of a pair of 741 operational amplifiers on a single chip.

FEATURES

- **Internal frequency compensation**
- **Short circuit protection**
- **Excellent temperature stability**
- **High input voltage range**
- **No latch-up**
- **1558/1458 are 2 "op amps" in space of one 741 package**
- **MC1558 MIL-STD-883A,B,C available**

PIN CONFIGURATIONS

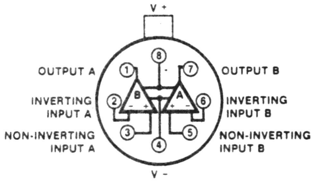
D,N, PACKAGE


OUTPUT A
1
INVERTING INPUT A
2
NON-INVERTING INPUT A
3
V-
4
5
NON-INVERTING INPUT B
6
INVERTING INPUT B
7
OUTPUT B
8
V+
A
B

TOP VIEW

ORDER NUMBERS
MC1458N
MC1558N
SA1458N

H PACKAGE*


V+
8
OUTPUT A
1
7
OUTPUT B
INVERTING INPUT A
2
B
A
6
INVERTING INPUT B
NON-INVERTING INPUT A
3
4
5
NON-INVERTING INPUT B
V-

ORDER NUMBERS
MC1458H
MC1558H

*Metal cans (H) not recommended for new designs

ABSOLUTE MAXIMUM RATINGS

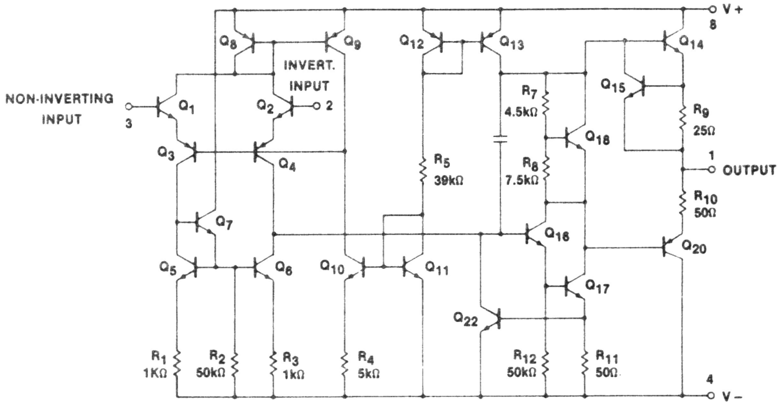
PARAMETER	RATING	UNIT
Supply voltage		
MC1458	±18	V
SA1458	±18	V
MC1558	±22	V
Internal power dissipation		
N package	500	mW
H package[1]	800	mW
F,FE package	1000	mW
Differential input voltage	±30	V
Input voltage[2]	±15	V
Output short-circuit duration	Continuous	
Operating temperature range		
MC1458	0 to +70	°C
SA1458	-40 to +85	°C
MC1558	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 60sec)	300	°C

NOTES

1. Ratings based on thermal resistances, junction to ambient, of 240°C/W, 150°C/W, 110°C/W for N, H, F and FE packages respectively, and a maximum junction temperature of 150°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

EQUIVALENT SCHEMATIC

AMPLIFIER "A" OF MC1458, SA1458, MC1558


V+
8
Q8
Q9
Q12
Q13
Q14
INVERT. INPUT
2
NON-INVERTING INPUT
3
Q1
Q2
R7 4.5kΩ
Q15
R9 25Ω
Q18
Q3
Q4
R5 39kΩ
R8 7.5kΩ
1
OUTPUT
R10 50Ω
Q7
Q16
Q20
Q5
Q6
Q10
Q11
Q17
Q22
R1 1KΩ
R2 50kΩ
R3 1kΩ
R4 5kΩ
R12 50kΩ
R11 50Ω
4
V-

GENERAL PURPOSE OPERATIONAL AMPLIFIER MC/SA1458/MC1558

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MC1558			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage	$R_S = 10k\Omega$		1.0	5.0	mV
		$R_S = 10k\Omega$, over temperature			6.0	mV
ΔV_{OS}	Offset voltage	Over temperature		10		μV/°C
I_{OS}	Offset current			20	200	nA
		Over temperature			500	nA
ΔI_{OS}	Offset current	Over temperature		0.10		nA/°C
I_{BIAS}	Input bias current			80	500	nA
		Over temperature			1500	nA
ΔI_B	Bias current	Over temperature		1.0		nA/°C
V_{OUT}	Output voltage swing	$R_L = 10k\Omega$, over temperature	± 12	± 14		V
		$R_L = 2k\Omega$, over temperature	± 10	± 13		V
A_{VOL}	Large signal voltage gain	$R_L = 2k\Omega$, $V_O = \pm 10V$	50	100		V/mV
		$R_L = 2k\Omega$, $V_O = \pm 10V$, over temperature	20			V/mV
	Offset voltage adjustment range			± 30		mV
PSRR	Supply voltage rejection ratio	$R_S \leq 10k\Omega$		30	150	μV/V
CMRR	Common mode rejection ratio		70	90		dB
I_{CC}	Supply current			2.3	5.0	mA
V_{IN}	Input voltage range		± 12	± 13		V
P_d	Power consumption			70	150	mW
	Channel separation			120		dB
R_{OUT}	Output resistance			75		Ω
I_{SC}	Output short-circuit current		10	26	60	mA

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$, $V_{CC} = \pm 15V$, unless otherwise specified.[1]

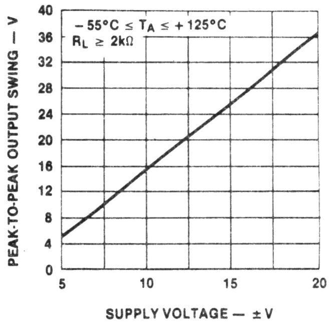
PARAMETER		TEST CONDITIONS	MC1458			SA1458			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S = 10k\Omega$		2.0	6.0		2.0	6.0	mV
		$R_S = 10k\Omega$, over temp.			7.5			7.5	mV
ΔV_{OS}	Offset voltage	Over temperature		12			12		μV/°C
I_{OS}	Offset current			20	200		20	200	nA
		Over temperature			300			500	nA
ΔI_{OS}	Offset current	Over temperature		0.10			0.10		nA/°C
I_{BIAS}	Input bias current			80	500		80	500	nA
		Over temperature			800			1500	nA
ΔI_B	Bias current	Over temperature		1.0			1.0		nA/°C
V_{OUT}	Output voltage swing	$R_L = 10k\Omega$	± 12	± 14		± 12	± 14		V
		$R_L = 2k\Omega$, over temp.	± 10	± 13		± 10	± 13		V
A_{VOL}	Large signal voltage gain	$R_L = 2k\Omega$, $V_O = \pm 10V$	25	200		20	200		V/mV
		$R_L = 2k\Omega$, $V_O = \pm 10V$, Over temperature	15			15			V/mV
	Offset voltage adjustment range			± 30			± 30		mV
PSRR	Supply voltage rejection ratio	$R_S \leq 10k\Omega$		30	150		30	150	μV/V
CMRR	Common mode rejection ratio		70	90		70	90		dB
I_{CC}	Supply current			2.3	5.6		2.3	5.6	mA
V_{IN}	Input voltage range		± 12	± 13		± 12	± 13		V
R_{IN}	Input resistance								MΩ
P_d	Power consumption			70	170		70	170	mW
	Channel separation			120			120		dB
I_{SC}	Output short-circuit current			25			25		mA

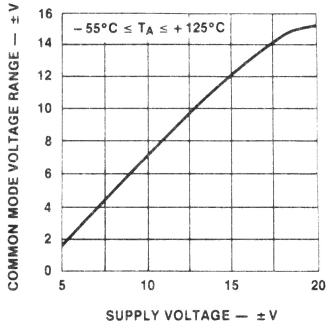
GENERAL PURPOSE OPERATIONAL AMPLIFIER MC/SA1458/MC1558

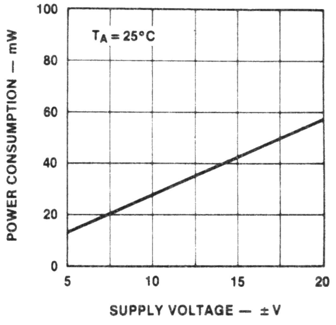
AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.

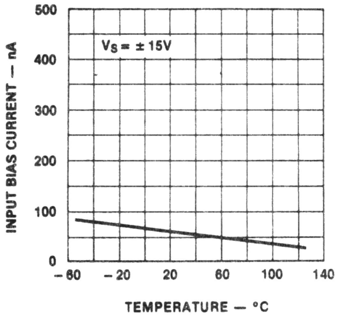
PARAMETER	TEST CONDITIONS	MC1458, SA1458, MC1558			UNIT
		Min	Typ	Max	
Parallel input resistance	Open loop, f = 20Hz	0.3			MΩ
Common mode input impedance	f = 20Hz		200		MΩ
Equivalent input noise voltage	$A_V = 100$, $R_S = 10k\Omega$, $B_W = 1.0kHz$, f = 1.0kHz		30		nV √Hz
Power bandwidth	$A_V = 1$, $R_L = 2.0k\Omega$, THD ≤ 5%, $V_{OUT} = 20Vp\text{-}p$		14		kHz
Phase margin			65		degrees
Gain margin			11		dB
Unity gain crossover frequency	Open loop		1.0		MHz
Transient response unity gain	$V_{IN} = 20mV$, $R_L = 2k\Omega$, $C_L \leq 100pF$				
Rise time			0.3		μs
Overshoot			5.0		%
Slew rate	C ≤ 100pF, $R_L \geq 2k$, $V_{IN} = \pm 10V$		0.8		V/μs

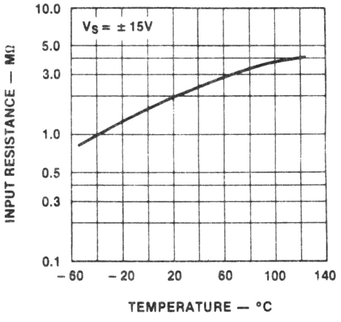
TYPICAL PERFORMANCE CHARACTERISTICS

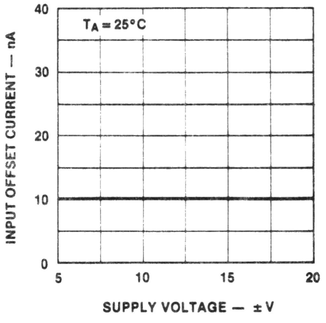

OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE


INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE


POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE

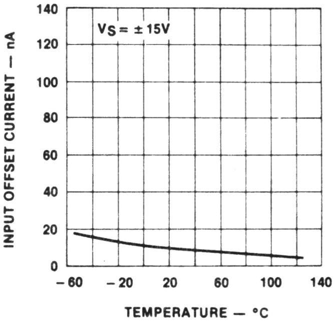

INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE


INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

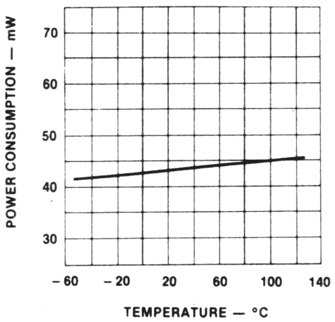

INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

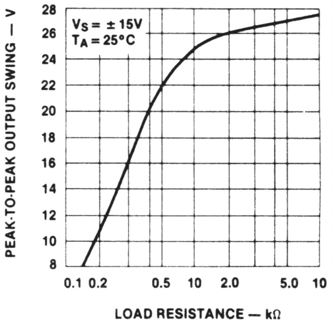
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



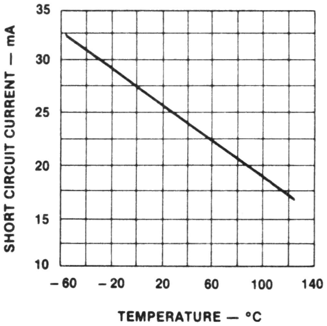
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



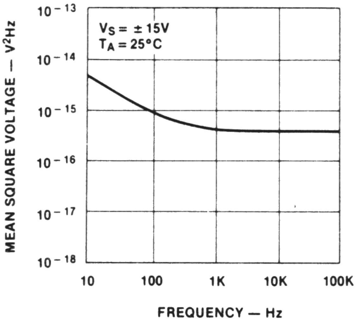
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



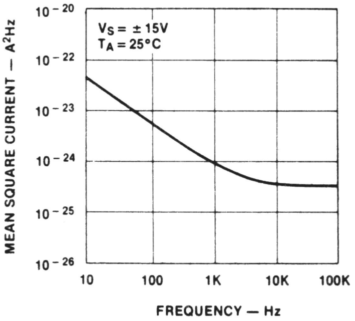
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



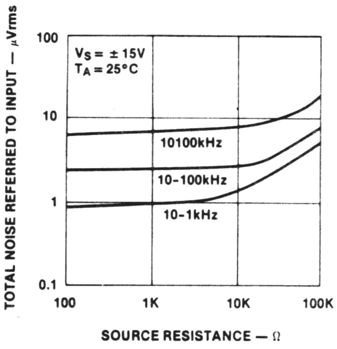
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



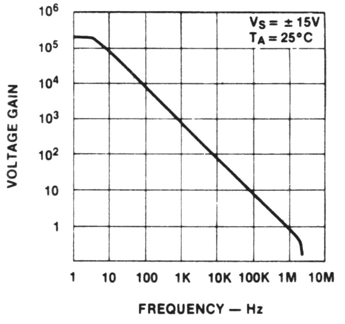
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



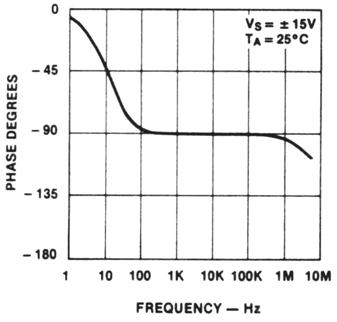
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

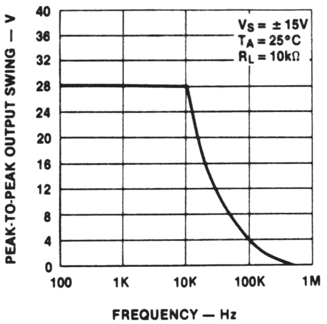


OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY

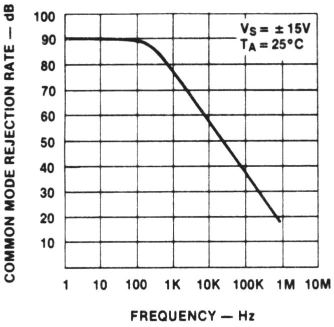


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

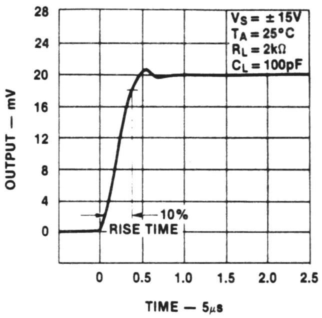
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



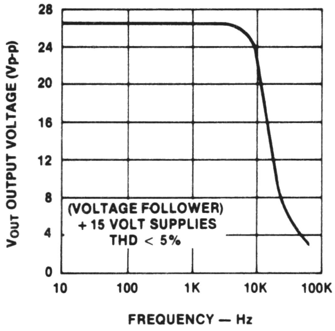
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



TRANSIENT RESPONSE



POWER BANDWIDTH (Large Signal Swing vs Frequency)



QUAD LOW POWER OPERATIONAL AMPLIFIERS MC3303/3403/3503

DESCRIPTION

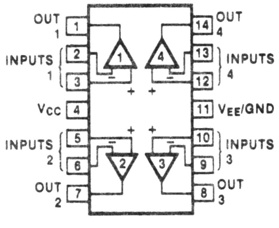
The MC3403 is a quad operational amplifier with true differential inputs. The device has electrical characteristics similar to the popular μA741. However, the MC3403 has several distinct advantages over standard operational amplifier types in single supply applications. The MC3403 can operate at supply voltages as low as 3.0V or as high as 32V. The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

FEATURES

- **Short circuit protected outputs**
- **Class AB output stage for minimal crossover distortion**
- **True differential input stage**
- **Single supply operation: 3.0 to 32V**
- **Split supply operation: ± 1.5 to ± 16V**
- **Low input bias currents: 500nA max**
- **Four amplifiers per package**
- **Internally compensated**

PIN CONFIGURATION

D, F, N PACKAGES


OUT 1
1
INPUTS 1
2
3
VCC
4
INPUTS 2
5
6
OUT 2
7
14
OUT 4
13
12
INPUTS 4
11
VEE/GND
10
9
INPUTS 3
8
OUT 3
1
2
3
4

TOP VIEW

ORDER NUMBERS

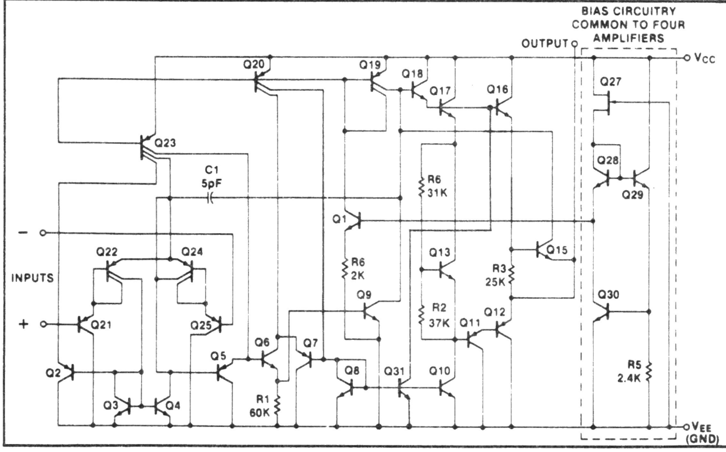
MC3303F	MC3403D	MC3503F
MC3303N	MC3403F	
	MC3403N	

ABSOLUTE MAXIMUM RATINGS

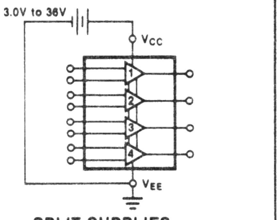
SYMBOL AND PARAMETER		RATING	UNIT
	Power supply voltages (3)		
V_{CC}	Single supply	36	Vdc
V_{CC}	Split supplies	+ 18	Vdc
V_{EE}		− 18	Vdc
V_{IDR}	Input differential voltage range[1]	± 36	Vdc
V_{ICR}	Input common mode voltage range[1,2]	± 18	Vdc
T_{stg}	Storage temperature range		
	Ceramic package	− 65 to + 150	°C
	Plastic package	− 55 to + 125	°C
T_A	Operating ambient temperature range		
	MC3503	− 55 to + 125	°C
	MC3403	0 to + 70	°C
	MC3303	− 40 to + 85	°C
T_J	Junction temperature		
	Ceramic package	175	°C
	Plastic package	150	°C

NOTES
1. Split power supplies.
2. For supply voltages less than ± 15V, the absolute maximum input voltage is equal to the supply voltage.
3. Device not functional for single supply >32V or split supply> ± 16V

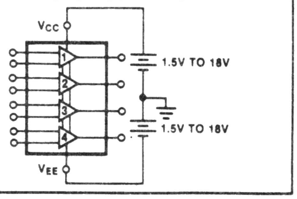
CIRCUIT SCHEMATIC (1/4 Shown)


BIAS CIRCUITRY COMMON TO FOUR AMPLIFIERS
OUTPUT
VCC
Q20
Q19
Q18
Q17
Q16
Q27
Q23
C1 5pF
R6 31K
Q28
Q29
Q1
−
INPUTS
+
Q22
Q24
Q21
Q25
R6 2K
Q13
R3 25K
Q15
Q9
R2 37K
Q11
Q12
Q30
Q6
Q7
Q5
Q2
Q8
Q31
Q10
R5 2.4K
Q3
Q4
R1 60K
VEE (GND)

SINGLE SUPPLY


3.0V to 36V
VCC
1
2
3
4
VEE

SPLIT SUPPLIES


VCC
1
2
3
4
1.5V TO 18V
1.5V TO 18V
VEE

QUAD LOW POWER OPERATIONAL AMPLIFIERS MC3303/3403/3503

ELECTRICAL CHARACTERISTICS (V_{CC} = + 15V, V_{EE} = − 15V for MC3503, MC3403; V_{CC} = + 14V, V_{EE} = GND for MC3303. T_A = 25°C unless otherwise noted)

SYMBOL AND PARAMETER		TEST CONDITIONS	MC3503			MC3403			MC3303			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input offset voltage		—	2.0	5.0	—	2.0	10	—	2.0	8.0	mV
		$T_A = T_{HIGH}$ to T_{LOW}	—	—	6.0	—	—	12	—	—	10	
I_{IO}	Input offset current		—	10	50	—	10	50	—	30	75	nA
		$T_A = T_{HIGH}$ to T_{LOW}	—	—	200—	—	200—	—	250			
A_{VOL}	Large signal open-loop voltage gain	$V_o = \pm 10V$, R_L = 2.0kΩ	50	200	—	20	200	—	20	200	—	V/mV
		$T_A = T_{HIGH}$ to T_{LOW}	25	300	—	15	—	—	15	—	—	
I_{IB}	Input bias current		—	− 30	− 500	—	− 30	− 500	—	− 30	− 500	nA
		$T_A = T_{HIGH}$ to T_{LOW}	—	− 40	− 1200	—	—	− 800	—	—	− 1000	
z_o	Output impedance	f = 20Hz	—	75	—	—	75	—	—	75	—	Ω
z_i	Input impedance	f = 20Hz	0.3	1.0	—	0.3	1.0	—	0.3	1.0	—	MΩ
V_{OR}	Output voltage range	R_L = 10kΩ	± 12	± 13.5	—	± 12	± 13.5	—	+ 12	+ 12.5	—	V
		R_L = 2.0kΩ	± 10	± 13	—	± 10	± 13	—	+ 10	+ 12	—	
		R_L = 2.0kΩ, $T_A = T_{HIGH}$ to T_{LOW}	± 10	—	—	± 10	—	—	+ 10	—	—	
V_{ICR}	Input common mode voltage range		+ 13V $- V_{EE}$	+ 13.5V $- V_{EE}$	—	+ 13V $- V_{EE}$	+ 13.5V $- V_{EE}$	—	+ 12V $- V_{EE}$	+ 12.5V $- V_{EE}$	—	V
CMRR	Common mode rejection ratio	$R_S \le$ 10kΩ	70	90	—	70	90	—	70	90	—	dB
I_{CC}, I_{EE}	Power supply current (V_o = 0)	$R_L = \infty$	—	2.5	4.0	—	2.5	7.0	—	2.5	7.0	mA
$\Delta I_B/\Delta T$		$T_A = T_{HIGH}$ to T_{LOW}		3.5	5		3.5	7		3.5	7	mA
$I_{OS\pm}$	Individual output short circuit current[2]		± 10	± 30	± 45	± 10	± 20	± 45	± 10	± 30	± 45	mA
PSRR +	Positive power supply rejection ratio		—	30	150	—	30	150	—	30	150	μV/V
PSRR −	Negative power supply rejection ratio		—	30	150	—	30	150	—	—	—	μV/V
$\Delta I_B/\Delta T$		$T_A = T_{HIGH}$ to T_{LOW}		50			50			50		pA/°C
$\Delta I_{IO}/\Delta T$	Average temperature coeficient of input offset current	$T_A = T_{HIGH}$ to T_{LOW}	—	50	—	—	50	—	—	50	—	pA/°C
$\Delta V_{IO}/\Delta T$	Average temperature coefficient of input offset voltage	$T_A = T_{HIGH}$ to T_{LOW}	—	10	—	—	10	—	—	10	—	μV/°C
BW_P	Power bandwidth	A_v = 1, R_L = 2.0kΩ, V_o = 20V(p-p) THD = 5%	—	9.0	—	—	9.0	—	—	9.0	—	kHz
BW	Small signal bandwidth	A_v = 1, R_L = 10kΩ, V_o = 50mV	—	1.0	—	—	1.0	—	—	1.0	—	MHz
SR	Slew rate	A_v = 1, V_i = −10V to + 10V	—	0.6	—	—	0.6	—	—	0.6	—	V/μs
t_{TLH}	Rise time	A_v = 1, R_L = 10kΩ, V_o = 50mV	—	0.35	—	—	0.35	—	—	0.35	—	μs
t_{THL}	Fall time	A_v = 1, R_L = 10kΩ, V_o = 50mV	—	0.35	—	—	0.35	—	—	0.35	—	μs
OS	Overshoot	A_v = 1, R_L = 10kΩ, V_o = 50mV	—	20	—	—	20	—	—	20	—	%
ϕm	Phase margin	A_v = 1, R_L = 2.0kΩ, C_L = 200pF	—	50	—	—	50	—	—	50	—	°
—	Crossover distortion	V_{IN} = 30mV(p-p), V_{OUT} = 2.0V(p-p), f = 10kHz	—	1.0	—	—	1.0	—	—	1.0	—	%

NOTES:
1. T_{HIGH} = 125°C for MC3503, 70°C for MC3303. T_{LOW} = − 55°C for MC3503, 0°C for MC3403, − 40°C for MC3303.
2. Not to exceed maximum package power dissipation.

QUAD LOW POWER OPERATIONAL AMPLIFIERS MC3303/3403/3503

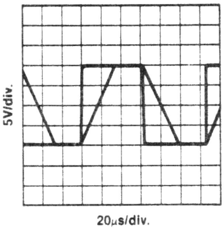
ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0V$, $V_E = GND$, $T_A = 25°C$ unless otherwise noted.)

SYMBOL AND PARAMETER		TEST CONDITIONS	MC3503			MC3403			MC3303			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input offset voltage		—	2.0	5.0	—	2.0	10	—	—	10	mV
I_{IO}	Input offset current		—	30	50	—	30	50	—	—	75	nA
I_{IB}	Input bias current		—	−200	−500	—	−200	−500	—	—	−500	nA
A_{VOL}	Large signal open-loop voltage gain	$R_L = 2.0kΩ$	10	200	—	10	200	—	10	200	—	V/mV
PSRR	Power supply rejection ratio		—	—	150	—	—	150	—	—	150	µV/V
V_{OR}	Output voltage range(3)	$R_L = 10kΩ$, $V_{CC} = 5.0V$	3.3	3.5	—	3.3	3.5	—	3.3	3.5	—	Vp-p
		$R_L = 10kΩ$, $5.0V \le V_{CC} \le 30V$	$V_{CC} - 1.7$	$V_{CC} - 1.5$	—	$V_{CC} - 1.7$	$V_{CC} - 1.5$	—	$V_{CC} - 1.7$	$V_{CC} - 1.5$	—	
I_{CC}	Power supply current		—	2.5	4.0	—	2.5	7.0	—	2.5	7.0	mA
—	Channel separation	f = 1.0kHz to 20kHz (input referenced)	—	−120	—	—	−120	—	—	−120	—	dB

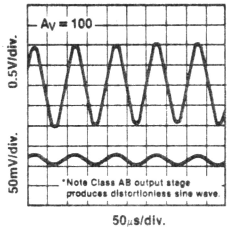
NOTE
3. Output will swing to ground.

TYPICAL PERFORMANCE CURVES

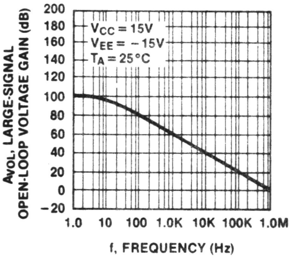
INVERTER PULSE RESPONSE



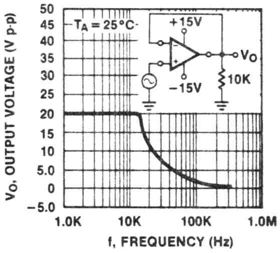
SINE WAVE RESPONSE



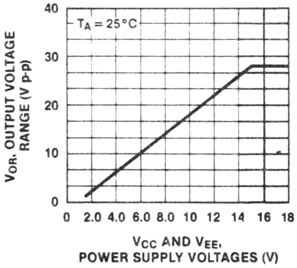
OPEN LOOP FREQUENCY RESPONSE



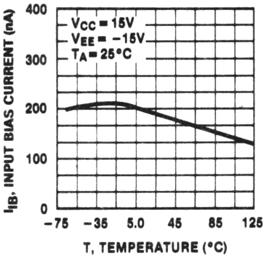
POWER BANDWIDTH

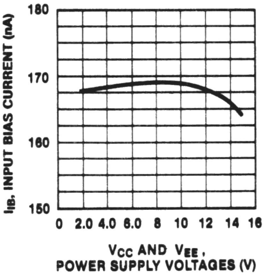


OUTPUT SWING vs SUPPLY VOLTAGE



TYPICAL PERFORMANCE CURVES (Continued)


INPUT BIAS CURRENT vs TEMPERATURE


INPUT BIAS CURRENT vs SUPPLY VOLTAGE

*For additional information, consult the Applications Section.

DUAL GENERAL-PURPOSE OPERATIONAL AMPLIFIER

SA/SE/NE4558

DESCRIPTION

The 4558 is a dual operational amplifier internally compensated. The use of planar epitaxial process for silicon chip construction gives the IC unique performance characteristics.

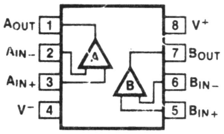
Excellent channel separation allows the use of a dual device in a single amp application, providing the highest packaging density. The SA/SE/NE4558 is a pin for pin replacement for the RC/RM/RV4558.

FEATURES

- **2MHz unity gain bandwidth guaranteed**
- **Supply voltage ±22V for SE4558 and ±18V for NE4558**
- **Short circuit protection**
- **No frequency compensation required**
- **No latch-up**
- **Large common mode and differential voltage ranges**
- **Low power consumption**

PIN CONFIGURATION

D, FE, N PACKAGES



TOP VIEW

ORDER NUMBERS

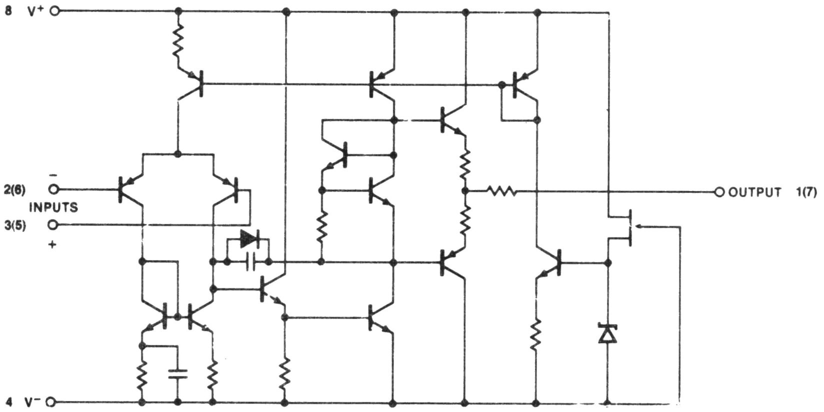
NE4558D	SA4558FE
NE4558FE	SE4558FE
NE4558N	SA4558N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
SE4558:	±22	V
NE4558, SA4558:	±18	V
Internal power dissipation (Note 1)	500	mW
Differential input voltage	±30	V
Input voltage (Note 2)	±15	V
Storage temperature range	−65 to +150	°C
Operating temperature range		
SE4558:	−55 to +125	°C
SA4558:	−40 to +85	°C
NE4558:	0 to +70	°C
Lead temperature (soldering, 60s)	300	°C
Output short circuit duration (Note 3)	Indefinite	

NOTES
1. Rating applies for case temperatures to +125°C; derate linearly at 5.6 mw/°C for ambient temperatures above +75°C for SE4558.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground on one amp only. Rating applies to +125°C case temperature or +75°C ambient temperature for NE4558 and to +85°C ambient temperature for SA4558.

EQUIVALENT SCHEMATIC



DUAL GENERAL-PURPOSE OPERATIONAL AMPLIFIER SA/SE/NE4558

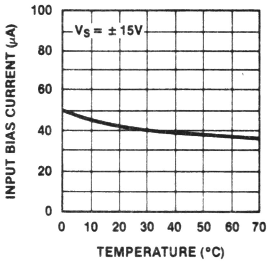
ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 15V$, $T_A = 25°C$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE4558			SA/NE4558			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage	$R_S \leq 10k\Omega$		1.0	5.0		2.0	6.0	mV
$\Delta V_{os}/\Delta T$	Over temp.		4			4		μV/°C
Input offset current			50	200		30	200	nA
$\Delta I_{os}/\Delta T$	Over temp.		20			20		pA/°C
Input bias current			40	500		200	500	nA
$\Delta I_B/\Delta T$	Over temp.		40			40		pA/°C
Input resistance		0.3	1.0		0.3	1.0		MΩ
Large signal voltage gain	$R_L \geq 2K\Omega$ $V_{OUT} = \pm 10V$	50,000	300,000		20,000	300,000		V/V
Output voltage swing	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	± 12 ± 10	± 14 ± 13		± 12 ± 10	± 14 ± 13		V
Input voltage range		± 12	± 13		± 12	± 13	V	
Common mode rejection ratio	$R_S \leq 10k\Omega$	70	100		70	100		dB
Supply voltage rejection ratio	$R_S \leq 10k\Omega$		10	150		10	150	μV/V
Power consumption (all amplifiers)	$R_L = •$		100	170		100	170	mW
Transient response (unity gain)	$V_{IN} = 20mV$ $R_L = 2K\Omega$ $C_L \leq 100pF$							
Risetime			100			100		ns
Overshoot			15.0			15.0		%
Slew rate (unity gain)	$R_L \geq 2k\Omega$		1.0			1.0		V/μs
Channel separation (gain = 100)	f = 10kHz $R_S = 1k\Omega$		90			90		dB
Unity gain bandwidth (gain = 1)		2.5	3.0		2.0	3.0		MHz
θ_M phase margin	$T_A = 25°C$		45			45		Degree
Input noise voltage	f = 1kc		25			25		nv/$\sqrt{Hz}$
I_{SC} short circuit	$T_A = 25°C$	5	25	50	5	25	50	mA
The following specifications apply for $-55°C \leq T_A \leq +125°C$ for SE4558; $0°C \leq T_A \leq +70°C$ for NE4558; $-40°C \leq T_A \leq +85°C$ for SA4558								
Input offset voltage	$R_S \leq 10k\Omega$			6.0			7.5	mV
Input offset current				500			300/500*	nA
Input bias current				1500			800/1500*	nA
Large signal voltage gain	$R_L \geq 2k\Omega$ $V_{OUT} = \pm 10$	25,000			15,000			
Output voltage swing	$R_L \geq 2k\Omega$	± 10			± 10			V
Power consumption	$V_S = \pm 15V$ $T_A = HIGH$ $T_A = LOW$		90 120	150 200		90 120	150 200	mW

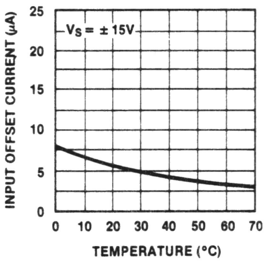
*SA4558

TYPICAL PERFORMANCE CURVES

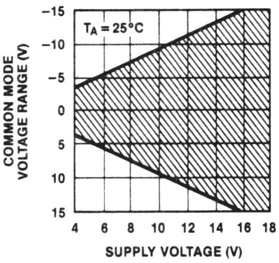
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



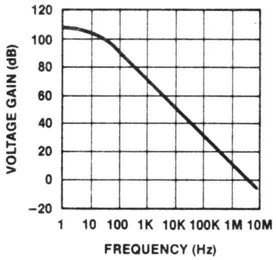
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



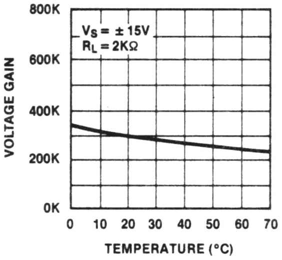
COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



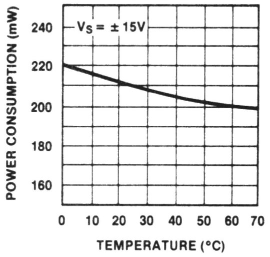
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



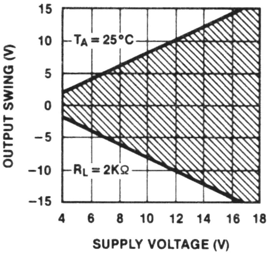
OPEN LOOP GAIN AS A FUNCTION OF TEMPERATURE



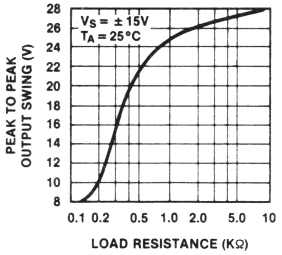
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



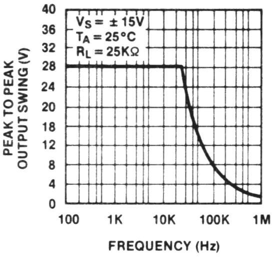
TYPICAL OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



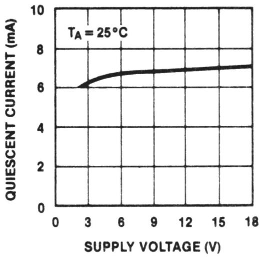
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

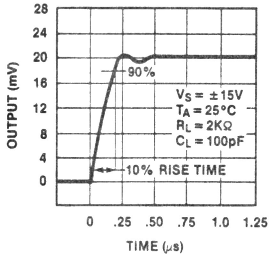


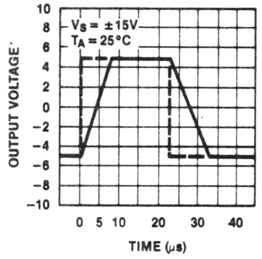
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

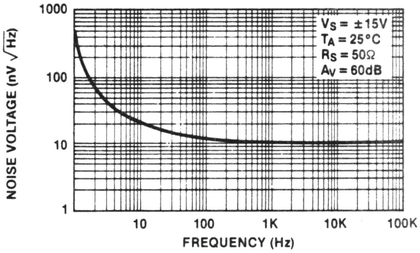


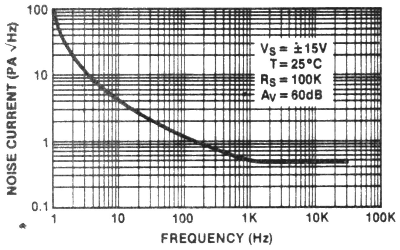
TYPICAL PERFORMANCE CURVES (Continued)

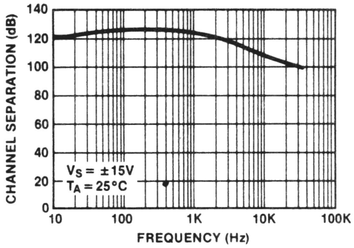

QUIESCENT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

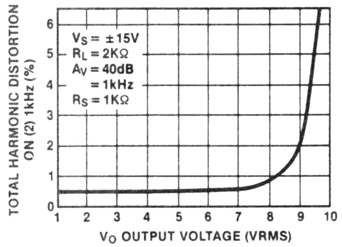

TRANSIENT RESPONSE

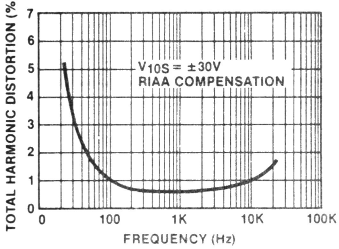

VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE


INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY


INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY


CHANNEL SEPARATION


TOTAL HARMONIC DISTORTION vs OUTPUT VOLTAGE


DISTORTION vs FREQUENCY V_O = 1vrms

HIGH SLEW RATE OPERATIONAL AMPLIFIER SE/NE530

DESCRIPTION

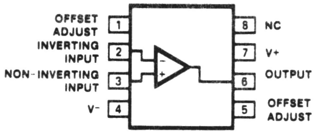
The 530 is a new generation operational amplifier featuring a high slew rate combined with improved input characteristics. Internally compensated, the SE530 guarantees slew rates of 25V/μs with 2mV maximum offset voltage. Industry standard pinout and internal compensation allow the user to upgrade system performance by directly replacing general purpose amplifiers such as the 741 and LF356 types.

FEATURES

- **Gain bandwidth product—3MHz**
- **35V/μs slew rate (Gain = -1)**
- **Internal frequency compensation**
- **Low input offset voltage 2mV max**
- **Low input bias current-60nA max**
- **Short circuit protection**
- **Offset null capability**
- **Large common mode and differential voltage ranges**

PIN CONFIGURATIONS

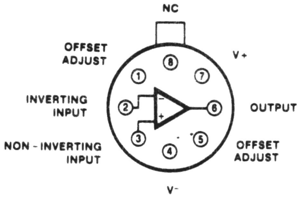
FE,N PACKAGE


OFFSET ADJUST
1
INVERTING INPUT
2
NON-INVERTING INPUT
3
V-
4
8
NC
7
V+
6
OUTPUT
5
OFFSET ADJUST
-
+

TOP VIEW

ORDER NUMBERS
NE530FE, NE530N
SE530FE, SE530N

H PACKAGE*


NC
OFFSET ADJUST
V+
8
1
7
INVERTING INPUT
2
6
OUTPUT
3
5
4
NON-INVERTING INPUT
OFFSET ADJUST
-
+
V-

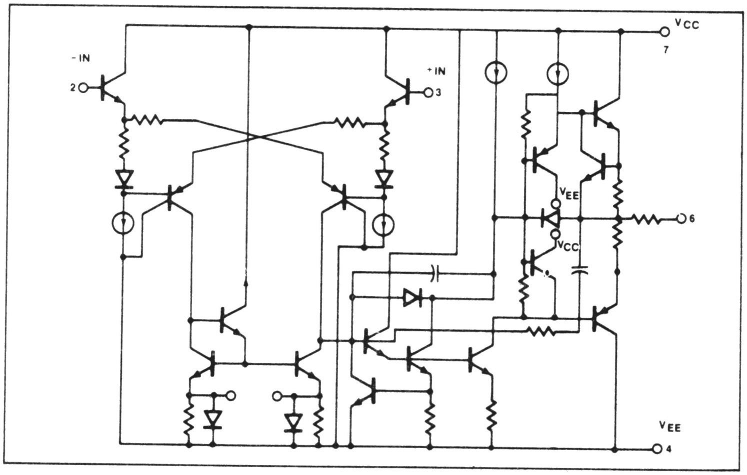
ORDER NUMBERS
NE530H SE530H

*Metal cans (H) not recommended for new designs.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
SE530	±22	V
NE530	±18	V
Internal power dissipation		
N Package	500	mW
H Package	800	mW
FE Package	1000	mW
Differential input voltage	±30	V
Input voltage	±15	V
Operating temperature range		
SE530	-55 to +125	°C
NE530	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature range (Solder, 60sec)	300	°C*
Output short circuit	Indefinite	

EQUIVALENT SCHEMATIC EACH AMPLIFIER


-IN
2
+IN
3
VCC
7
VEE
VCC
6
VEE
4

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = \pm 15V$ unless otherwise specified.[1]

PARAMETER		TEST CONDITIONS	SE530			NE530			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S \leq 10k\Omega$ Over temperature		0.7	4.0 5.0		2.0	6.0 7.0	mV mV
ΔV_{OS}	Temperature coefficient of input offset voltage	Over temperature		3	15		6		μV/°C
I_{OS}	Input offset current	 Over temperature		5	20 40		15	40 80	nA nA
ΔI_{OS}	Input offset current	Over temperature		25			40		pA/°C
I_B	Input bias current	 Over temperature		45	80 200		65	150 200	nA nA
ΔI_B	Input current	Over temperature		50			80		pA/°C
R_{IN}	Input resistance		3	10		1	6		MΩ
V_{CM}	input common mode voltage range		± 12	± 13		± 12	± 13		V
A_{VOL}	Large signal voltage gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$ Over temperature	50 25	200		50 25	200		V/mV V/mV
V_{OUT}	Output voltage swing	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	± 12 ± 10	± 14 ± 13		± 12 ± 10	± 14 ± 13		V V
I_{SC}	Output short circuit current		10	25	50	10	25	50	mA
R_{OUT}	Output resistance			100			100		Ω
I_{CC}	Supply current	Each amplifier Over temperature		2.0 2.2	3.0 3.6		2.0 2.2	3.0	mA mA
CMRR	Common mode rejection ratio	$R_S \leq 10k\Omega$ Over temperature	70	90		70	90		dB
PSRR	Power supply rejection ratio	$R_S \leq 10k\Omega$ Over temperature		30	150		30	150	μV/V

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = \pm 15V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE530/5530			NE530/5530			UNIT
		Min	Typ	Max	Min	Typ	Max	
Transient Response								
Small signal rise time			.06			.06		μs
Small signal overshoot			13			13		%
Settling time	TO 0.1% (10V step)		0.9			0.9		μs
Slew rate	±15V supply, $V_O = \pm 10V$, $R_L \geq 2k\Omega$							
Unity gain inverting		25	35		20	35		V/μs
Unity gain non-inverting		18	25		12	25		V/μs
Power bandwidth	5% THD, $V_O = \pm 10V$, $R_L \geq 2k\Omega$	360	500		280	500		kHz
Small signal bandwidth	Open loop		3			3		MHz
Input noise voltage	f = 1kHz		30			30		$nV/\sqrt{Hz}$

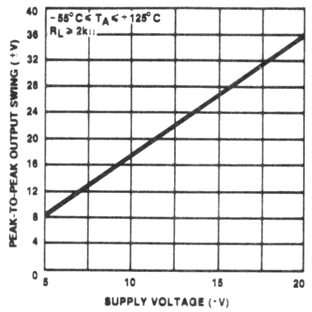
NOTE

1. Operating temperature range for the SE530 is − 55°C to + 125°C
Operating temperature range for the NE530 is 0°C to + 70°C.

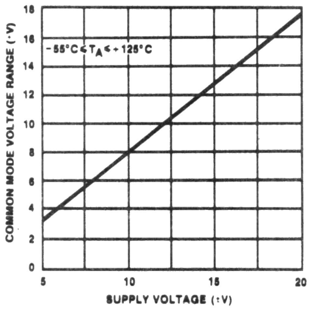
HIGH SLEW RATE OPERATIONAL AMPLIFIER SE/NE530

TYPICAL PERFORMANCE CHARACTERISTICS

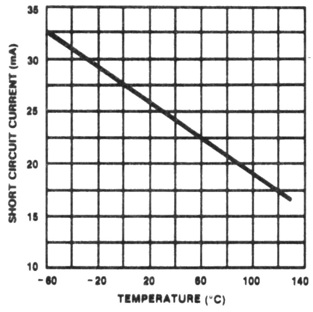
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



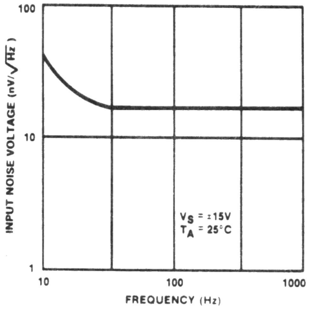
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



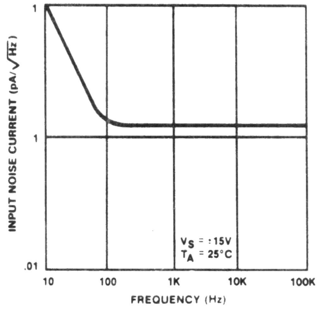
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



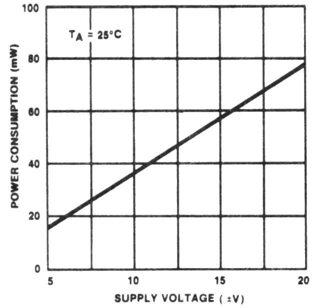
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



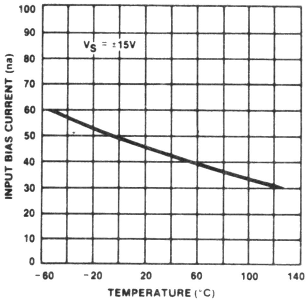
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



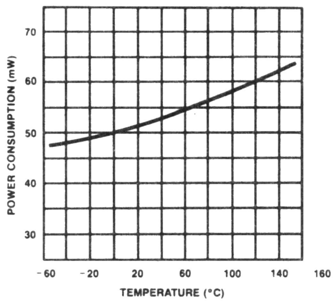
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE (EACH AMPLIFIER)



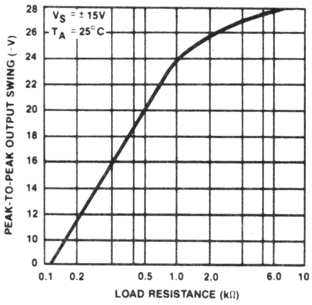
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE (EACH AMPLIFIER)



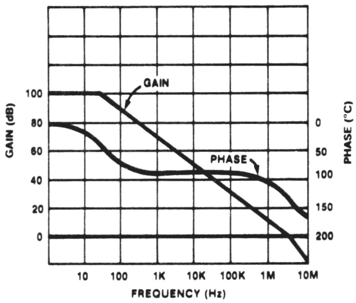
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



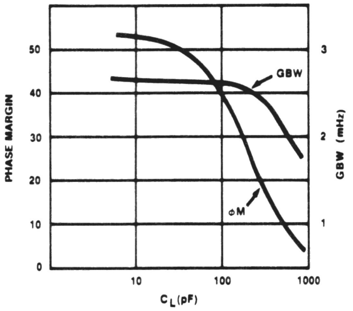
HIGH SLEW RATE OPERATIONAL AMPLIFIER SE/NE530

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

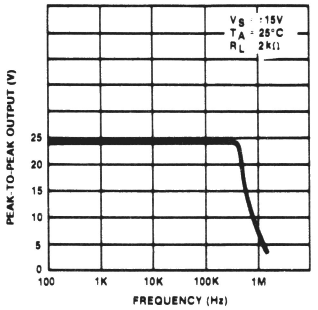
NE530 OPEN-LOOP GAIN AND PHASE vs FREQUENCY



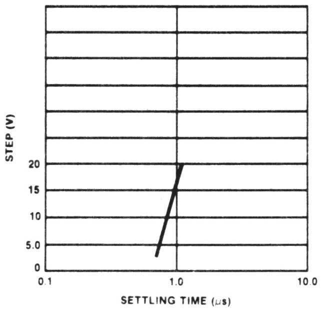
GAIN-BANDWIDTH PRODUCT AND PHASE MARGIN vs LOAD CAPACITANCE



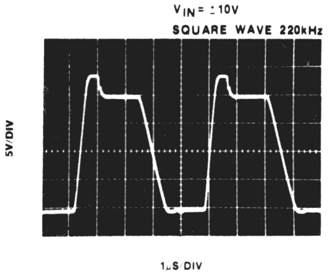
POWER BANDWIDTH



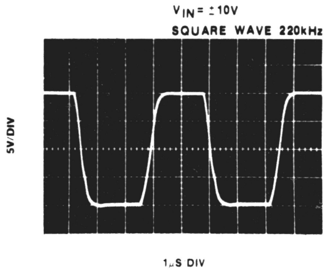
INPUT VOLTAGE STEP vs SETTLING TIME TO 10mV



SLEW RATE—VOLTAGE FOLLOWER

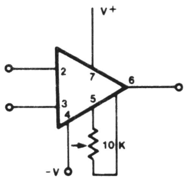


SLEW RATE (-1 AMPLIFIER)



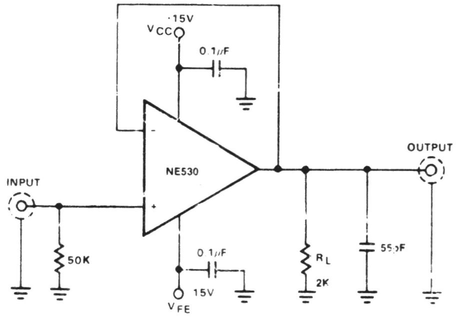
TYPICAL CIRCUIT CONNECTION

OFFSET ADJUST CIRCUIT



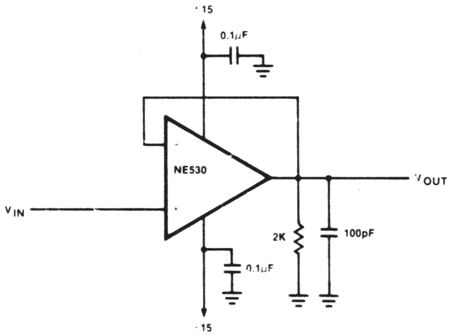
TEST LOAD CIRCUITS

SLEW RATE AND SETTLING TIME

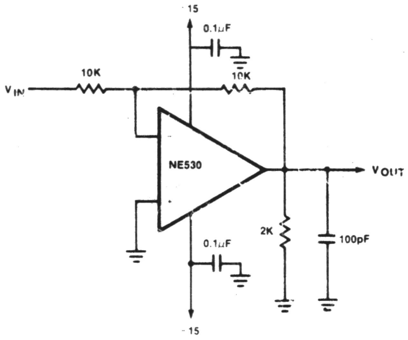

+15V
VCC
0.1μF
NE530
INPUT
OUTPUT
50K
0.1μF
-15V
VEE
RL
2K
55pF

Pins not shown are not connected.
All resistor values are typical and in ohms.

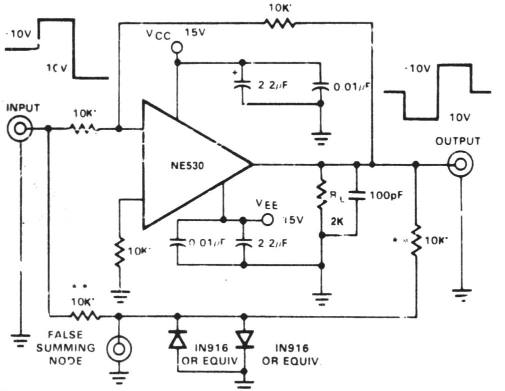
HIGH SLEW RATE—VOLTAGE FOLLOWER


+15
0.1μF
NE530
VIN
VOUT
2K
100pF
0.1μF
-15

HIGH SLEW RATE—INVERTING AMPLIFIER


+15
0.1μF
VIN
10K
10K
NE530
VOUT
2K
100pF
0.1μF
-15

TESTING SLEW RATE AND SETTLING TIME

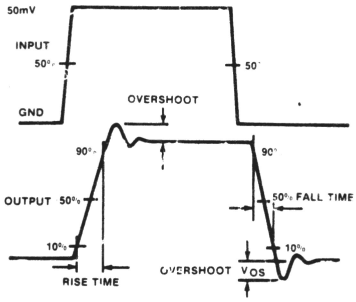

10K*
+10V
-10V
VCC 15V
2.2μF
0.01μF
+10V
-10V
INPUT
10K*
NE530
OUTPUT
RL
2K
100pF
VEE
-15V
0.01μF
2.2μF
10K*
**
10K*
**
10K*
FALSE SUMMING NODE
IN916 OR EQUIV
IN916 OR EQUIV

Pins not shown are not connected.
All resistor values are typical and in ohms.

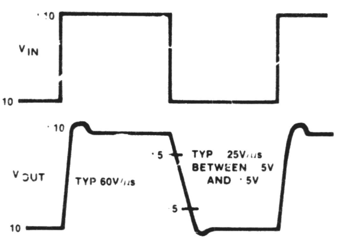
*Match to within 0.01%.
**Open for slew rate.

VOLTAGE WAVEFORMS

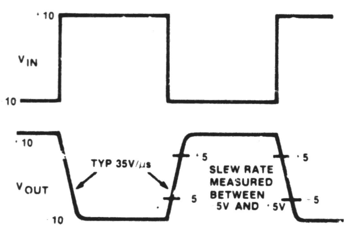
SMALL SIGNAL TRANSIENT RESPONSE DEFINITIONS


50mV
INPUT
50%
50%
GND
OVERSHOOT
90%
90%
OUTPUT 50%
50% FALL TIME
10%
10%
RISE TIME
OVERSHOOT VOS

SLEW RATE—VOLTAGE FOLLOWER



SLEW RATE—INVERTING AMPLIFIER



HIGH SLEW RATE OPERATIONAL AMPLIFIER SE/NE531

DESCRIPTION

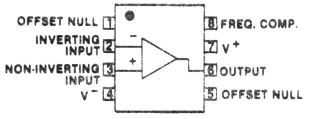
The 531 is a fast slewing high performance operational amplifier which retains dc performance equal to the best general purpose types while providing far superior large signal ac performance. A unique input stage design allows the amplifier to have a large signal response nearly identical to its small signal response. The amplifier is compensated for truly negligible overshoot with a single capacitor. In applications where fast settling and superior large signal bandwidths are required, the amplifier out performs conventional designs which have much better small signal response. Also, because the small signal response is not extended, no special precautions need be taken with circuit board layout to achieve stability. The high gain, simple compensation and excellent stability of this amplifier allow its use in a wide variety of instrumentation applications.

FEATURES

- **35V/μsec slew rate at unity gain**
- **Pin for pin replacement for μA709, μA748 or LM101**
- **Compensated with a single capacitor**
- **Same low drift offset null circuitry as μA741**
- **Small signal bandwidth 1MHz**
- **Large signal bandwidth 500KHz**
- **True op amp dc characteristics make the 531 the ideal answer to all slew rate limited operational amplifier applications.**

PIN CONFIGURATIONS

N,FE PACKAGE

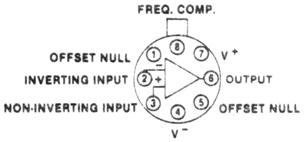

OFFSET NULL 1
INVERTING INPUT 2
NON-INVERTING INPUT 3
V⁻ 4
8 FREQ. COMP.
7 V⁺
6 OUTPUT
5 OFFSET NULL
−
+

TOP VIEW

ORDER NUMBERS

NE531N	SE531N
NE531FE	SE531FE

H PACKAGE*

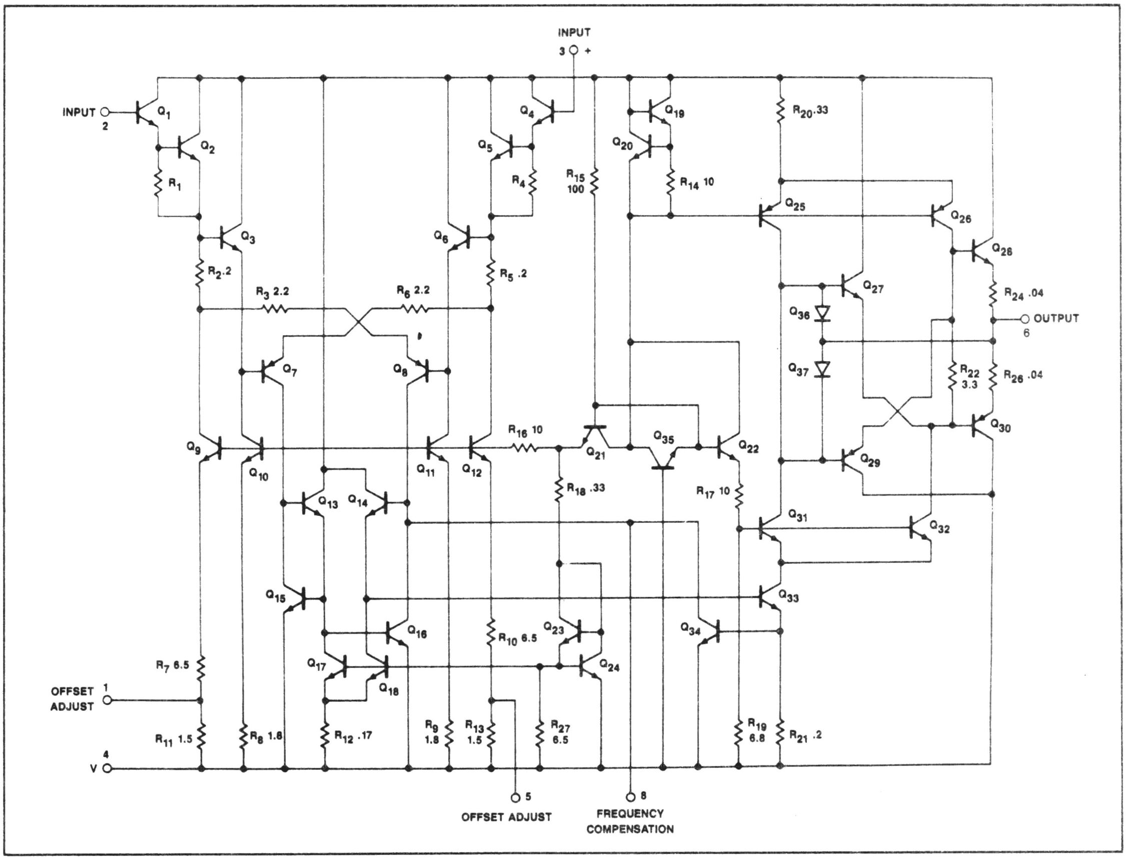

FREQ. COMP.
OFFSET NULL
INVERTING INPUT
NON-INVERTING INPUT
V⁺
OUTPUT
OFFSET NULL
V⁻
1
2
3
4
5
6
7
8
−
+

ORDER NUMBERS

NE531H/SE531H

*Metal cans (H) not recommended for new designs

EQUIVALENT SCHEMATIC


INPUT 3 +
INPUT 2
Q1
Q2
R1
Q3
R2 .2
R3 2.2
R6 2.2
Q4
Q5
R4
Q6
R5 .2
R15 100
Q19
Q20
R14 10
R20 .33
Q25
Q26
Q28
R24 .04
OUTPUT 6
Q27
Q36
Q37
R22 3.3
R26 .04
Q30
Q29
Q7
Q8
Q9
Q10
Q11
Q12
R16 10
Q21
Q35
Q22
R18 .33
R17 10
Q13
Q14
Q31
Q32
Q15
Q33
Q16
R10 6.5
Q23
Q24
Q34
Q17
Q18
R7 6.5
OFFSET ADJUST 1
R11 1.5
R8 1.8
R12 .17
R9 1.8
R13 1.5
R27 6.5
R19 6.8
R21 .2
4 V⁻
5 OFFSET ADJUST
8 FREQUENCY COMPENSATION

HIGH SLEW RATE OPERATIONAL AMPLIFIER SE/NE531

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	±22	V
Internal power dissipation[1]	300	mW
Differential input voltage	±15	V
Common mode input voltage[2]	±15	V
Voltage between offset null and V-	±0.5	V
Operating temperature range		
NE531	0 to +70	°C
SE531	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60 sec)	300	°C
Output short circuit duration[3]	indefinite	

NOTES

1. Rating applies for case temperature to 125°C, derate linearly at 6.5mW/°C for ambient temperatures above +75°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or to +75°C ambient temperature.

DC ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE531[1]			NE531			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS} Offset voltage	$R_S \le 10k\Omega$, $T_A = 25°C$		2.0	5.0		2.0	6.0	mV
	$R_S \le 10k\Omega$, over temp			6.0			7.5	mV
ΔV_{OS}	Over temp		10			10		μV/°C
I_{OS} Offset current	$T_A = 25°C$		30	200		50	200	nA
	$T_A = HIGH$			200			200	nA
	$T_A = LOW$			500			300	nA
ΔI_{OS}	Over temp		0.4			0.4		nA/°C
I_{BIAS} Input current	$T_A = 25°C$		300	500		400	1500	nA
	$T_A = HIGH$			500			1500	nA
	$T_A = LOW$			1500			2000	nA
ΔI_B	Over temp		2			2		nA/°C
V_{CM} Common mode voltage range	$T_A = 25°C$	± 10			± 10			V
CMRR Common mode rejection ratio	$T_A = 25°C$, $R_S \le 10k\Omega$				70	100		dB
	Over temp $R_S \le 10k\Omega$	70	90					dB
R_{IN} Input resistance	$T_A = 25°C$		20			20		MΩ
V_{OUT} Output voltage swing	$R_L \ge 10k\Omega$, over temp	± 10	± 13		± 10	± 13		V
I_{CC} Supply current	$T_A = 25°C$			7.0			10	mA
	T_{MAX}			7.0			10	mA
P_D Power consumption	$T_A = 25°C$			210			300	mW
PSRR Power supply rejection ratio	$R_S \le 10k\Omega$, $T_A = 25°C$					10	150	μV/V
	$R_S \le 10k\Omega$, over temp		10	150				μV/V
R_{OUT} Output resistance	$T_A = 25°C$		75			75		Ω
A_{VOL} Large signal voltage gain	$T_A = 25°C$, $R_L \ge 10k\Omega$, $V_{OUT} = \pm 10V$	50	100		20	60		V/mV
	$R_L \ge 10k\Omega$, $V_{OUT} = \pm 10V$, over temp	25			15			V/mV
V_{INN} Input noise voltage	25°C, f = 1kHz		20			20		nV/√Hz
I_{SC}	25°C	5	15	45	5	15	45	mA

NOTE:

1. Temperature range:

   SE531 $-55°C \le T_A \le 125°C$

   NE531 $0°C \le T_A \le 70°C$

HIGH SLEW RATE OPERATIONAL AMPLIFIER SE/NE531

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

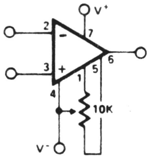
PARAMETER	TEST CONDITIONS	NE531			SE531			UNIT
		Min	Typ	Max	Min	Typ	Max	
Full power bandwidth			500			500		kHz
Settling time (1%) (.1%)	$A_V = +1$, $V_{IN} = \pm 10V$		1.5 2.5			1.5 2.5		μs μs
Large signal overshoot	$A_V = +1$, $V_{IN} = \pm 10V$		2			2		%
Small signal overshoot	$A_V = +1$, $V_{IN} = 400mV$		5			5		%
Small signal risetime	$A_V = +1$, $V_{IN} = 400mV$		300			300		ns
Slew rate	$A_V = 100$		35			35		V/μs
	$A_V = 10$		35			35		V/μs
	$A_V = 1$ (noninverting)		30		20	30		V/μs
	$A_V = 1$ (inverting)		35		25	35		V/μs

NOTE

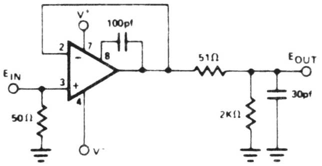
1. All AC testing is performed in the transient response test circuit.

TEST LOAD CIRCUITS

OFFSET NULL CIRCUIT

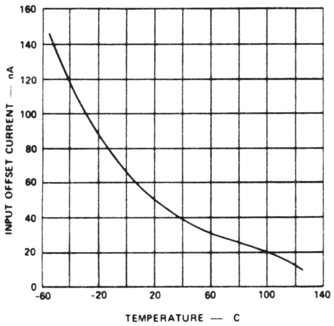


TRANSIENT RESPONSE CIRCUIT

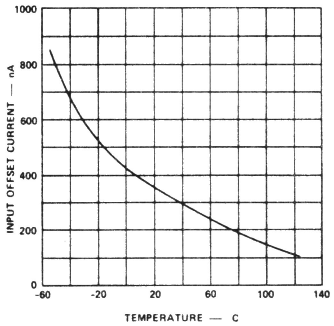


TYPICAL PERFORMANCE CHARACTERISTICS ($V_S = \pm 15V$, $T_A = +25°C$, unless otherwise specified.)

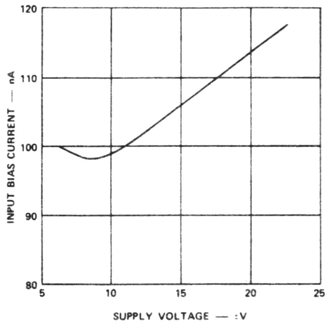
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

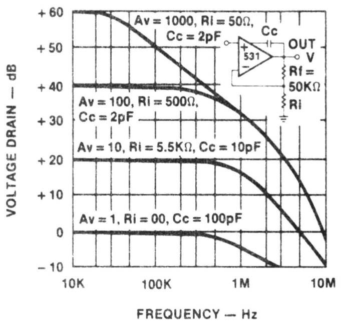


INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

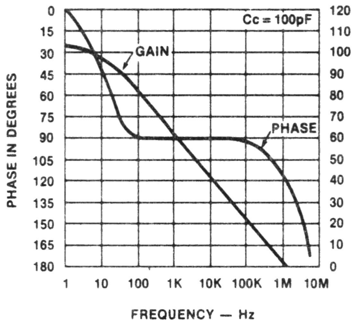


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

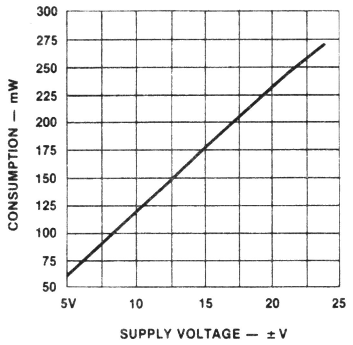
CLOSED LOOP NON-INVERTING VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



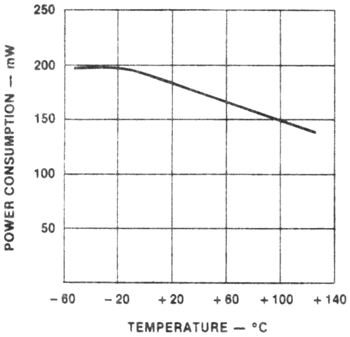
OPEN LOOP PHASE RESPONSE AND VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



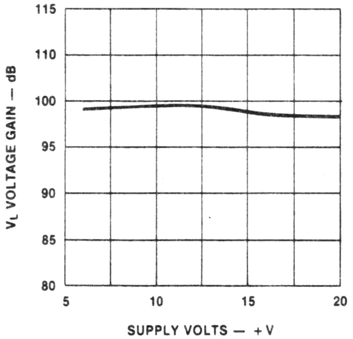
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



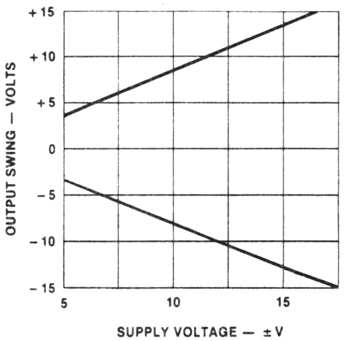
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



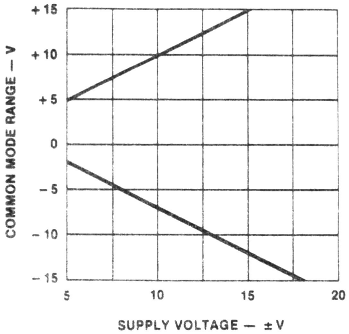
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



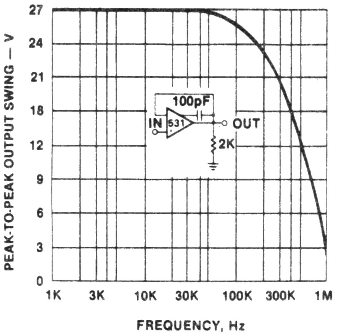
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



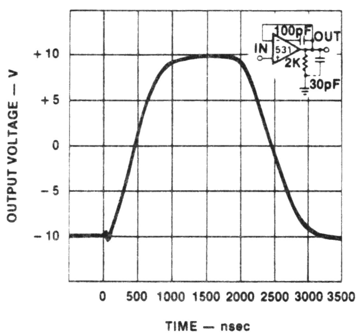
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

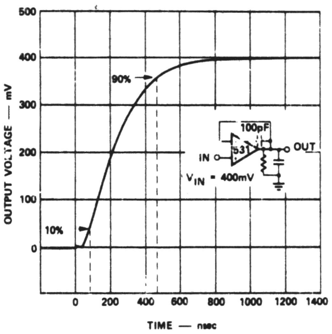


VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE

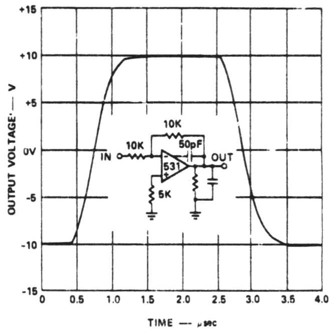


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

VOLTAGE FOLLOWER TRANSIENT RESPONSE

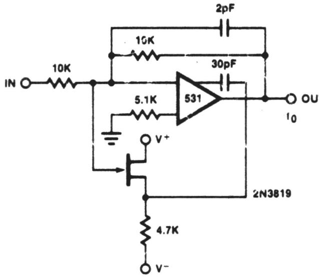


UNITY GAIN INVERTING AMPLIFIER LARGE SIGNAL RESPONSE

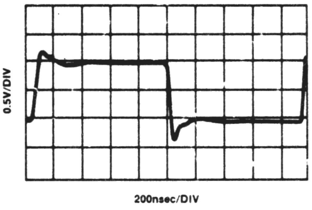


TYPICAL APPLICATIONS

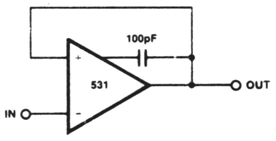
HIGH SPEED INVERTER (10MHz BANDWIDTH)


2pF
10K
10K
30pF
IN
531
OUT
I_0
5.1K
V+
2N3819
4.7K
V−

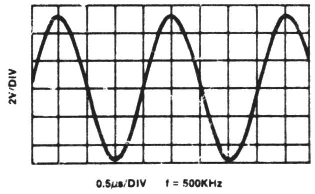
PULSE RESPONSE HIGH SPEED INVERTER



FAST SETTLING VOLTAGE FOLLOWER


100pF
+
531
−
IN
OUT

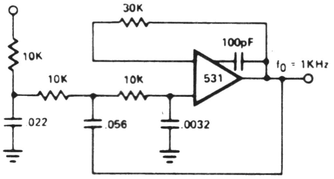
LARGE SIGNAL RESPONSE VOLTAGE FOLLOWER



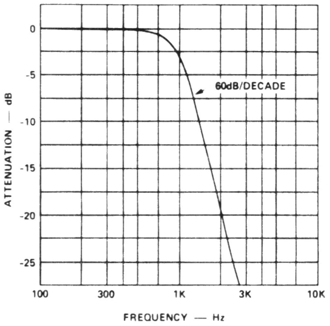
HIGH SLEW RATE OPERATIONAL AMPLIFIER SE/NE531

TYPICAL APPLICATIONS (Cont'd)

THREE POLE ACTIVE LOW PASS FILTER BUTTERWORTH MAXIMALLY FLAT RESPONSE*


30K
100pF
10K
10K
10K
531
f_0 = 1KHz
.022
.056
.0032

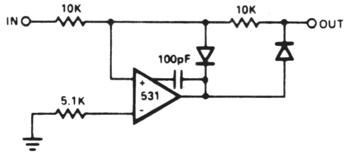
RESPONSE OF 3-POLE ACTIVE BUTTERWORTH MAXIMALLY FLAT FILTER



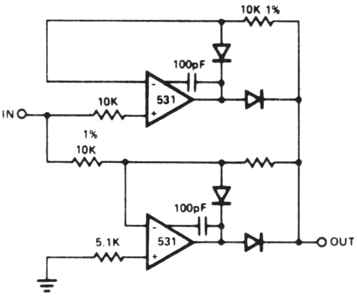
*Reference—EDN Dec. 15, 1970
Simplify 3-Pole Active Filter Design
A. Paul Brokow

PRECISION RECTIFIERS

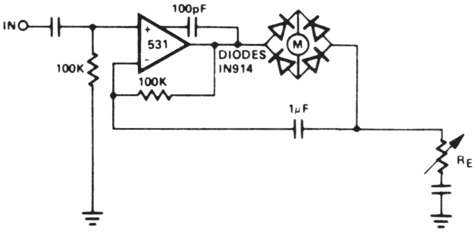
(a) HALF WAVE


IN
10K
10K
OUT
100pF
531
5.1K

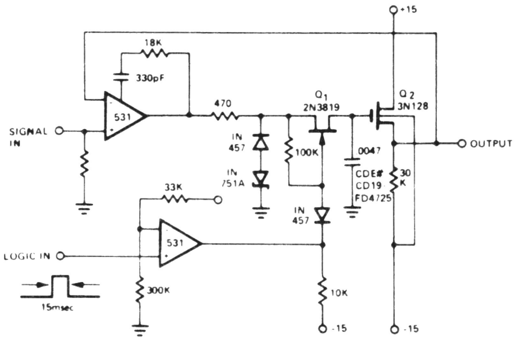
(b) FULL WAVE


10K 1%
100pF
531
IN
10K
1%
10K
100pF
531
5.1K
OUT

AC MILLIVOLTMETER


IN
100pF
531
M
DIODES
IN914
100K
100K
1µF
R_E

SAMPLE AND HOLD


+15
18K
330pF
531
SIGNAL IN
470
Q_1
2N3819
Q_2
3N128
OUTPUT
IN 457
IN 751A
100K
.0047
CDE#
CD19
FD4725
30 K
33K
IN 457
531
LOGIC IN
15msec
300K
10K
-15
-15

CYCLIC A TO D CONVERTER

One interesting, but, much ignored A/D converter is the cyclic converter. This consists of a chain of identical stages, each of which senses the polarity of the input. The stage then subtracts V_{ref} from the input and doubles the remainder if the polarity was correct. In Figure 1 the signal is full wave rectified and the remainder of $V_{in} - V_{ref}$ is doubled. A chain of these stages gives the gray code equivalent of the input voltage in digitized form related to the magnitude of V_{ref}. Possessing high potential accuracy, the circuit using NE531 devices settles in 5μs.

TRIANGLE AND SQUARE WAVE GENERATOR

The circuit in Figure 2 will generate precision triangle and square waves. The output amplitude of the square wave is set by the output swing of the op amp A-1 and R1/R2 sets the triangle amplitude. The frequency of oscillation in either case is

$$f = \frac{1}{4RC} \bullet \frac{R2}{R1} \qquad (3\text{-}23)$$

The square wave will maintain 50% duty cycle even if the amplitude of the oscillation is not symmetrical.

The use of the NE531 in this circuit will allow good square waves to be generated to quite high frequencies. Since the amplifier A1 runs open loop, there is no need for compensation. The triangle-generating amplifier must be compensated. The NE5535 device can be used as well, except for the lower frequency response.

CYCLIC A TO D CONVERTER

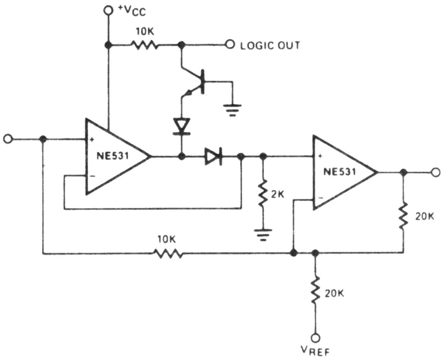


Figure 1a

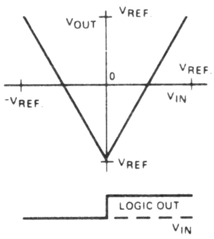


Figure 1b

TRIANGLE AND SQUARE WAVE GENERATOR

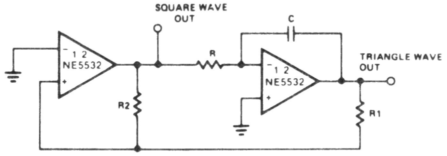


Figure 2

HIGH SLEW RATE OP AMP SE/NE538

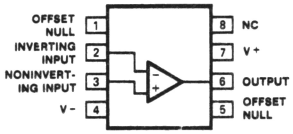
DESCRIPTION

The SE/NE538 is a new generation operational amplifier featuring high slew rates combined with improved input characteristics. Internally compensated for gains of 5 or larger, the SE538 offers guaranteed minimum slew rates of 40V/μs or larger. Featuring 2mV max input offset voltage, the 538 is a single amplifier. Industry standard pin out and internal compensation allow the user to upgrade system performance by directly replacing general purpose amplifiers, such as 748, 101A and 741.

FEATURES

- **2mV input offset voltage**
- **80nA max input offset current**
- **Short circuit protected**
- **Offset null capability**
- **Large common mode and differential voltage ranges**
- **60V/μs slew rate (gain of +5, −4 min)**
- **6MHz gain bandwidth product (gain +5, −4 minimum)**
- **Internal frequency compensation (gain of +5, −4 minimum)**
- **Pin out: 538 same as 741 (single)**

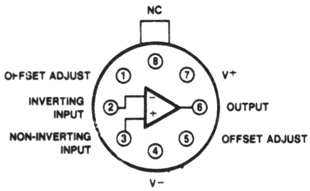
FE,N PACKAGE



TOP VIEW

ORDER NUMBERS
SE538N, FE NE538N, FE

H PACKAGE*



ORDER NUMBERS
SE538H NE538H

ABSOLUTE MAXIMUM RATINGS[1,2,3]

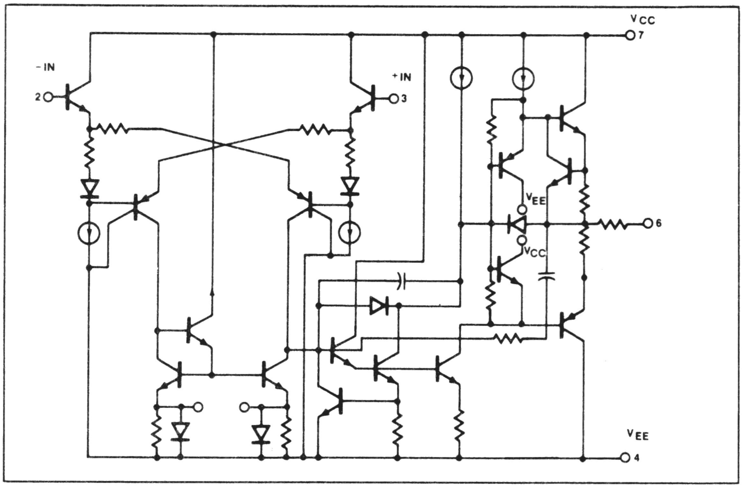
PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		
	SE military grade	±22	V
	NE commercial grade	±18	V
P_D	Internal power dissipation FE package	1000	mW
P_D	Internal power dissipation[1] N package	500	mW
P_D	Internal power dissipation[1] H package	800	mW
	Differential input voltage	±30	V
	Input voltage[2]	±15	V
	Operating temperature range		
	SE military grade	-55 to +125	°C
	NE commercial grade	0 to 70	°C
	Output short circuit[3]	indefinite	
	Storage temperature range	-65 to +150	°C
	Lead temperature (solder, 60sec.)	300	°C

NOTES

1. Rating applies for thermal resistances of 240°C/W and 150°C/W junction to ambient for N and H packages. Maximum chip temperature is 150°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

HIGH SLEW RATE OP AMP SE/NE538

EQUIVALENT SCHEMATIC (EACH AMPLIFIER)



DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SE538			NE538			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S \leq 10k\Omega$		0.7	4.0		2.0	6.0	mV
		$R_S \leq 10k\Omega$, over temp.			5.0			7.0	mV
ΔV_{OS}	Input offset voltage drift	$R_S = 0\Omega$, over temp.		4.0			6.0		μV/°C
I_{OS}	Input offset current			5	20		15	40	nA
		Over temp.			40			80	nA
ΔI_{OS}	Input offset current	Over temp		25			40		pA/°C
I_B	Input current			45	80		65	150	nA
		Over temp.			200			200	nA
ΔI_B	Input current	Over temp.		50			80		pA/°C
V_{CM}	Input common mode voltage range		± 12	± 13		± 12	± 13		V
CMRR	Common mode rejection ratio	$R_S \leq 10k\Omega$, over temp.	70	90		70	90		dB
PSRR	Power supply rejection	$R_S \leq 10k\Omega$, over temp.		30	150		30	150	μV/V
R_{IN}	Input resistance		3	10		1	6		MΩ
A_{VOL}	Large signal voltage gain	$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	50	200		50	200		V/mV
		Over temp., $R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	25			25			V/mV
V_{OUT}	Output voltage	Over temp., $R_L \geq 2k\Omega$	± 10	± 13		± 10	± 13		V
		Over temp., $R_L \geq 10k\Omega$	± 12	± 14		± 12	± 14		V
I_{CC}	Supply current	Per amplifier		2	3		2	3	mA
		Over temp., per amplifier		2.2	3.6		2.2	3.6	mA
P_D	Power dissipation	Per amplifier		60	90		60	90	mW
		Over temp., per amplifier		66	108		66	108	mW
I_{SC}	Output short circuit current		10	25	50	10	25	50	mA
R_{OUT}	Output resistance			100			100		Ω

NOTE

Temperature Range

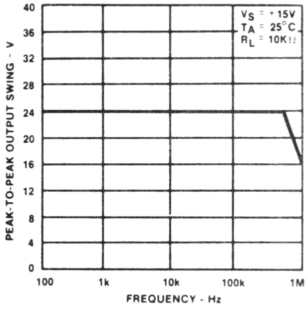
SE Types $-55°C \leq T_A \leq 125°C$

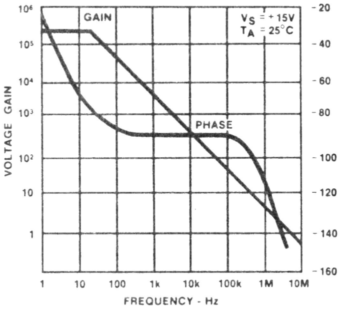
NE Types $0°C \leq T_A \leq 70°C$

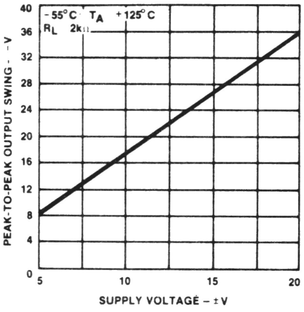
AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

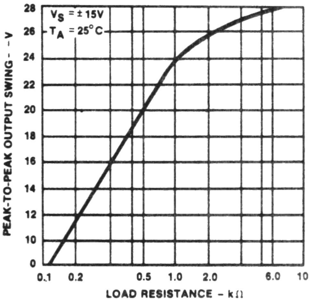
PARAMETER	TEST CONDITIONS	SE538/SE5538			SE538/NE5538			UNIT
		Min	Typ	Max	Min	Typ	Max	
Gain bandwidth product (Gain +5, -4 minimum)			6			6		MHz
Transient response								
Small signal rise time			0.25			0.25		μs
Small signal overshoot			6			6		%
Settling time	To 0.1%		1.2			1.2		μs
Slew rate	Minimum gain = 5 Noninverting $R_L \geq 2k\Omega$	40	60			60		V/μs
Input noise voltage	$f = 1kHz, T_A = 25°C$		30			30		nV/$\sqrt{Hz}$

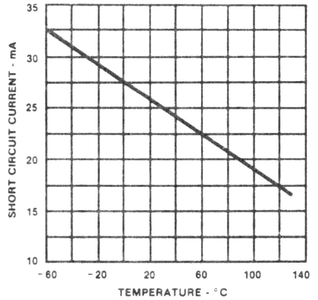
TYPICAL PERFORMANCE CHARACTERISTICS

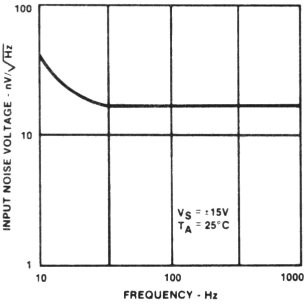

OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY


OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY


OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE


OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE


OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE


INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY

LOW POWER DUAL OPERATIONAL AMPLIFIERS SA/SE/NE532/LM158/258/358

DESCRIPTION

The 532/358 consists of two independent, high gain, internally frequency compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages. Operation from dual power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

FEATURES

- **Internally frequency compensated for unity gain**
- **Large dc voltage gain—(100dB)**
- **Wide bandwidth (unity gain)—1MHz (temperature compensated)**
- **Wide power supply range**
  single supply—(3Vdc to 30Vdc)
  or dual supplies—(±1.5Vdc to ±15Vdc)
- **Very low supply current drain (400μA)—essentially independent of supply voltage (1mW/op amp at +5Vdc)**
- **Low input biasing current—(45nA dc temperature compensated)**
- **Low input offset voltage—(2mVdc) and offset current—(5nA dc)**
- **Differential input voltage range equal to the power supply voltage**
- **Large output voltage—(0Vdc to V+—-1.5Vdc swing)**
- **SE532 MIL-STD-883A,B,C available**

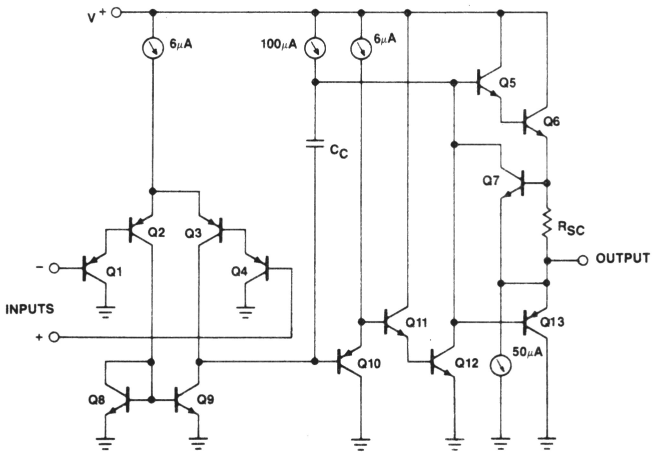
UNIQUE FEATURES

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage. The unity gain cross frequency is temperature compensated. The input bias current is also temperature compensated.

ABSOLUTE MAXIMUM RATINGS

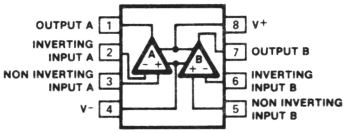
PARAMETER	RATING	UNIT
Supply voltage, V+	32 or ±16	Vdc
Differential input voltage	32	Vdc
Input voltage	-0.3 to +32	Vdc
Power dissipation[1]		
FE package	900	mW
H package	680	mW
N package	500	mW
Output short-circuit to GND[5]		
V+ < 15 Vdc and T_A = 25°C	Continuous	
Operating temperature range		
NE532/LM358	0 to +70	°C
LM258	-25 to +85	°C
SA532N	-40 to +85	°C
SE532/LM158	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 10sec)	300	°C

EQUIVALENT CIRCUIT


V+
6μA
100μA
6μA
Q5
Q6
CC
Q7
RSC
OUTPUT
Q2
Q3
Q1
Q4
INPUTS
-
+
Q11
Q13
50μA
Q10
Q12
Q8
Q9

PIN CONFIGURATIONS

D,FE,N PACKAGE

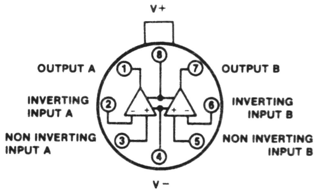

OUTPUT A
1
INVERTING INPUT A
2
NON INVERTING INPUT A
3
V-
4
8
V+
7
OUTPUT B
6
INVERTING INPUT B
5
NON INVERTING INPUT B
A
B

TOP VIEW

ORDER NUMBERS

LM158N, FE
LM258N, FE
LM358D, N, FE
NE532D, N, FE
SA532FE, N
SE532N, FE

H PACKAGE*


V+
OUTPUT A
①
⑧
⑦
OUTPUT B
INVERTING INPUT A
②
⑥
INVERTING INPUT B
NON INVERTING INPUT A
③
⑤
NON INVERTING INPUT B
④
V-

ORDER NUMBERS

LM158/258/358H
NE/SE532H

*Metal cans (H) not recommended for new designs

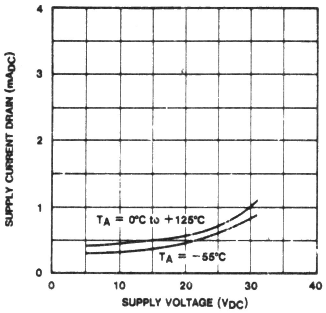
DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V+ = +5V$ unless otherwise specified.

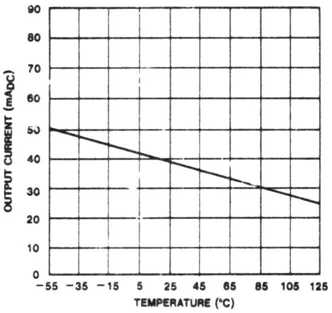
PARAMETER	TEST CONDITIONS	SE532, LM158/258			NE/SA532/LM358			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS} Offset voltage[1]	$R_S \le 0\Omega$ $R_S \le 0\Omega$, over temp.		±2	±5 ±7		±2	±7 ±9	mV mV
V_{OS} Drift	$R_S = 0\Omega$, over temp.		7			7		μV/°C
I_{OS} Offset current	$I_{IN}(+) - I_{IN}(-)$ Over temp.		±3	±30 ±100		±5	±50 ±150	nA nA
I_{OS} Drift	Over temp.		10			10		pA/°C
I_{BIAS} Input current[2]	$I_{IN}(+)$ or $I_{IN}(-)$ Over temp., $I_{IN}(+)$ or $I_{IN}(-)$		45 40	150 300		45 40	250 500	nA nA
I_B Drift	Over temp		50			50		pA/°C
V_{CM} Common mode voltage range[3]	$V+ = 30V$ Over temp., $V+ = 30V$	0 0		$V+ - 1.5$ $V+ - 2.0$	0 0		$V+ - 1.5$ $V+ - 2.0$	V V
C_{MRR} Common mode rejection ratio	$V+ = 30V$	70	85		65	70		dB
V_{OUT} Output voltage swing (V_{OH})	$R_L \ge 2k\Omega$, $V+ = 30V$, over temp.	26			26			V
	$R_L \ge 10k\Omega$, $V+ = 30V$, over temp.	27	28		27	28		V
V_{OUT} Output voltage swing (V_{OL})	$R_L \le 10k\Omega$, over temp.		5	20		5	20	mV
I_{CC} Supply current	$R_L = \infty$, $V+ = 30V$		1.0	2.0		1.0	2.0	mA
	$R_L = \infty$ on all amplifiers, over temp.		0.5	1.2		0.5	1.2	mA
A_{VOL} Large signal voltage gain	$R_L \ge 2k\Omega$, $V_{OUT} \pm 10V$, $V+ = 15V$ (for large V_O swing) over temp.	50 25	100		25 15	100		V/mV V/mV
PSRR Supply voltage rejection ratio	$R_S \le 0\Omega$	65	100		65	100		dB
Amplifier-to-amplifier coupling[4]	f = 1kHz to 20kHz (input referred)		−120			−120		dB
Output current Source	$V_{IN+} = +1Vdc$, $V_{IN-} = 0Vdc$, $V+ = 15Vdc$	20	40		20	40		mA
	$V_{IN+} = +1Vdc$, $V_{IN-} = 0Vdc$, $V+ = 15Vdc$, over temp.	10	20		10	20		mA
Sink	$V_{IN-} = +1Vdc$, $V_{IN+} = 0Vdc$, $V+ = 15Vdc$	10	20		10	20		mA
	$V_{IN-} = +1Vdc$, $V_{IN+} = 0Vdc$, $V+ = 15Vdc$, over temp.	5	8		5	8		mA
	$V_{IN+} = 0V$, $V_{IN-} = +1Vdc$, $V_O = 200mV$	12	50		12	50		μA
I_{SC} Short circuit current[5]			40	60		40	60	mA
Differential input voltage[6]				V+			V+	V
GBW Unity gain bandwidth	$T_A = 25°C$		1			1		MHz
S.R. Slew rate	$T_A = 25°C$		0.3			0.3		V/μs
Noise Input Noise Voltage	$T_A = 25°C$, f = 1kHz		40			40		nV/√Hz

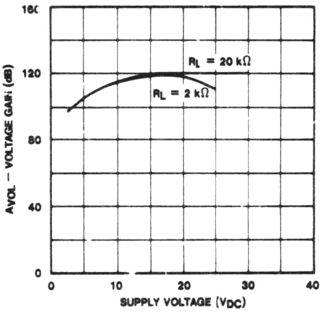
NOTES

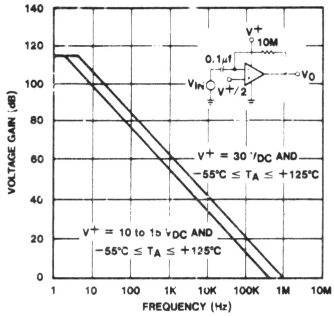
1. $V_O \cong 1.4V$, $R_S = 0\Omega$ with V+ from 5V to 30V; and over the full input common-mode range (0V to V+ − 1.5V).
2. The direction of the input current is out of the IC due to the pnp input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ − 1.5V, but either or both inputs can go to +32V without damage.
4. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance coupling increases at higher frequencies.
5. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of +15Vdc, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V+ − 1.5V, buteither or both inputs can go to +32Vdc without damage.
7. For operating at high temperatures, all devices must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient.

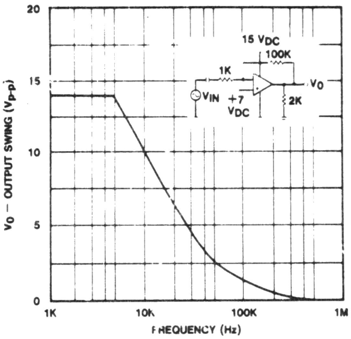
TYPICAL PERFORMANCE CHARACTERISTICS

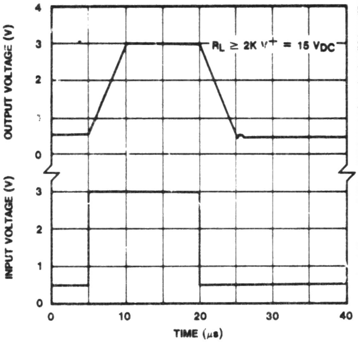

SUPPLY CURRENT

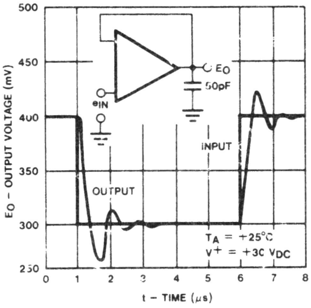

CURRENT LIMITING

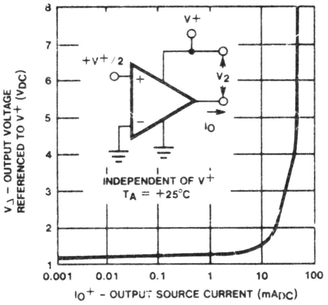

VOLTAGE GAIN

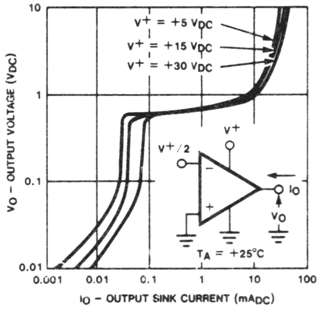

OPEN LOOP FREQUENCY RESPONSE


LARGE SIGNAL FREQUENCY RESPONSE


VOLTAGE FOLLOWER PULSE RESPONSE

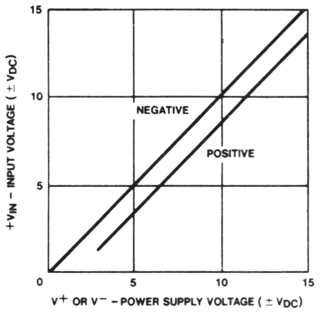

VOLTAGE FOLLOWER PULSE RESPONSE (SMALL SIGNAL)


OUTPUT CHARACTERISTICS CURRENT SOURCING

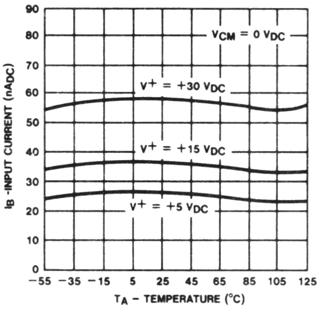

OUTPUT CHARACTERISTICS CURRENT SINKING

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

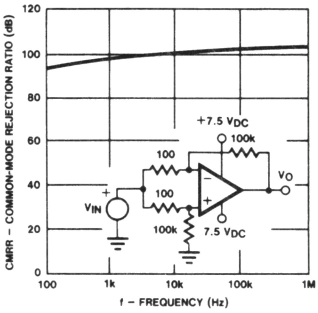
INPUT VOLTAGE RANGE



INPUT CURRENT

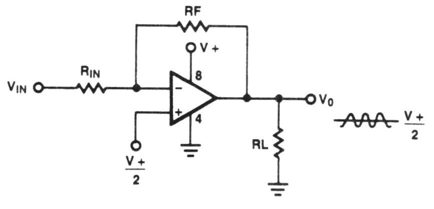


COMMON MODE REJECTION RATIO

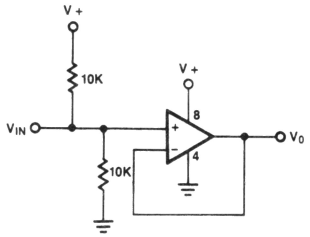


TYPICAL APPLICATIONS

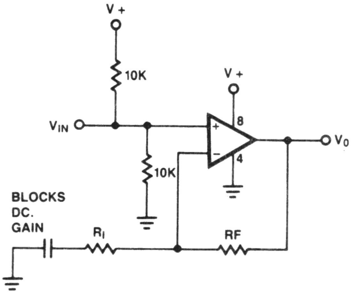
SINGLE SUPPLY INVERTING AMPLIFIER


RF
V+
R_IN
V_IN
8
4
V_O
RL
V+/2
V+/2

INPUT BIASING *VOLTAGE FOLLOWER


V+
10K
V+
V_IN
8
4
V_O
10K

NON-INVERTING AMPLIFIER


V+
10K
V+
V_IN
8
4
V_O
10K
BLOCKS DC. GAIN
R_I
RF

GENERAL PURPOSE OPERATIONAL AMPLIFIER MC/SA1458/MC1558

DESCRIPTION

The MC1458 is a high performance operational amplifier with high open loop gain, internal compensation, high common mode range and exceptional temperature stability. The MC1458 is short-circuit protected and allows for nulling of offset voltage.

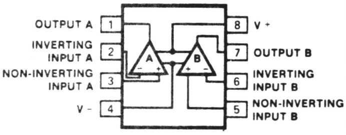
The MC1458/SA1458/MC1558 consists of a pair of 741 operational amplifiers on a single chip.

FEATURES

- **Internal frequency compensation**
- **Short circuit protection**
- **Excellent temperature stability**
- **High input voltage range**
- **No latch-up**
- **1558/1458 are 2 "op amps" in space of one 741 package**
- **MC1558 MIL-STD-883A,B,C available**

PIN CONFIGURATIONS

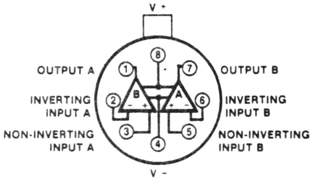
D,N, PACKAGE


OUTPUT A 1
INVERTING INPUT A 2
NON-INVERTING INPUT A 3
V- 4
8 V+
7 OUTPUT B
6 INVERTING INPUT B
5 NON-INVERTING INPUT B
A
B

TOP VIEW

ORDER NUMBERS
MC1458N
MC1558N
SA1458N

H PACKAGE*


V+
8
OUTPUT A 1
7 OUTPUT B
INVERTING INPUT A 2
6 INVERTING INPUT B
NON-INVERTING INPUT A 3
5 NON-INVERTING INPUT B
4
V-
A
B

ORDER NUMBERS
MC1458H
MC1558H

*Metal cans (H) not recommended for new designs

ABSOLUTE MAXIMUM RATINGS

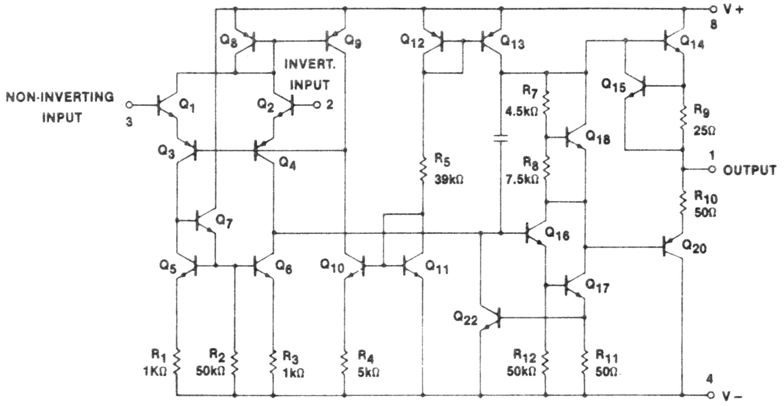
PARAMETER	RATING	UNIT
Supply voltage		
MC1458	±18	V
SA1458	±18	V
MC1558	±22	V
Internal power dissipation		
N package	500	mW
H package[1]	800	mW
F,FE package	1000	mW
Differential input voltage	±30	V
Input voltage[2]	±15	V
Output short-circuit duration	Continuous	
Operating temperature range		
MC1458	0 to +70	°C
SA1458	-40 to +85	°C
MC1558	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 60sec)	300	°C

NOTES

1. Ratings based on thermal resistances, junction to ambient, of 240°C/W, 150°C/W, 110°C/W for N, H, F and FE packages respectively, and a maximum junction temperature of 150°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

EQUIVALENT SCHEMATIC

AMPLIFIER "A" OF MC1458, SA1458, MC1558


V+
8
Q8
Q9
Q12
Q13
Q14
INVERT. INPUT
NON-INVERTING INPUT
3
Q1
Q2
2
R7 4.5kΩ
Q15
R9 25Ω
Q18
Q3
Q4
R5 39kΩ
R8 7.5kΩ
1
OUTPUT
R10 50Ω
Q7
Q16
Q20
Q5
Q6
Q10
Q11
Q17
Q22
R1 1KΩ
R2 50kΩ
R3 1kΩ
R4 5kΩ
R12 50kΩ
R11 50Ω
4
V-

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MC1558			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage	$R_S = 10k\Omega$		1.0	5.0	mV
		$R_S = 10k\Omega$, over temperature			6.0	mV
ΔV_{OS}	Offset voltage	Over temperature		10		µV/°C
I_{OS}	Offset current			20	200	nA
		Over temperature			500	nA
ΔI_{OS}	Offset current	Over temperature		0.10		nA/°C
I_{BIAS}	Input bias current			80	500	nA
		Over temperature			1500	nA
ΔI_B	Bias current	Over temperature		1.0		nA/°C
V_{OUT}	Output voltage swing	$R_L = 10k\Omega$, over temperature	± 12	± 14		V
		$R_L = 2k\Omega$, over temperature	± 10	± 13		V
A_{VOL}	Large signal voltage gain	$R_L = 2k\Omega$, $V_O = \pm 10V$	50	100		V/mV
		$R_L = 2k\Omega$, $V_O = \pm 10V$, over temperature	20			V/mV
	Offset voltage adjustment range			± 30		mV
PSRR	Supply voltage rejection ratio	$R_S \leq 10k\Omega$		30	150	µV/V
CMRR	Common mode rejection ratio		70	90		dB
I_{CC}	Supply current			2.3	5.0	mA
V_{IN}	Input voltage range		± 12	± 13		V
P_d	Power consumption			70	150	mW
	Channel separation			120		dB
R_{OUT}	Output resistance			75		Ω
I_{SC}	Output short-circuit current		10	26	60	mA

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$, $V_{CC} = \pm 15V$, unless otherwise specified.[1]

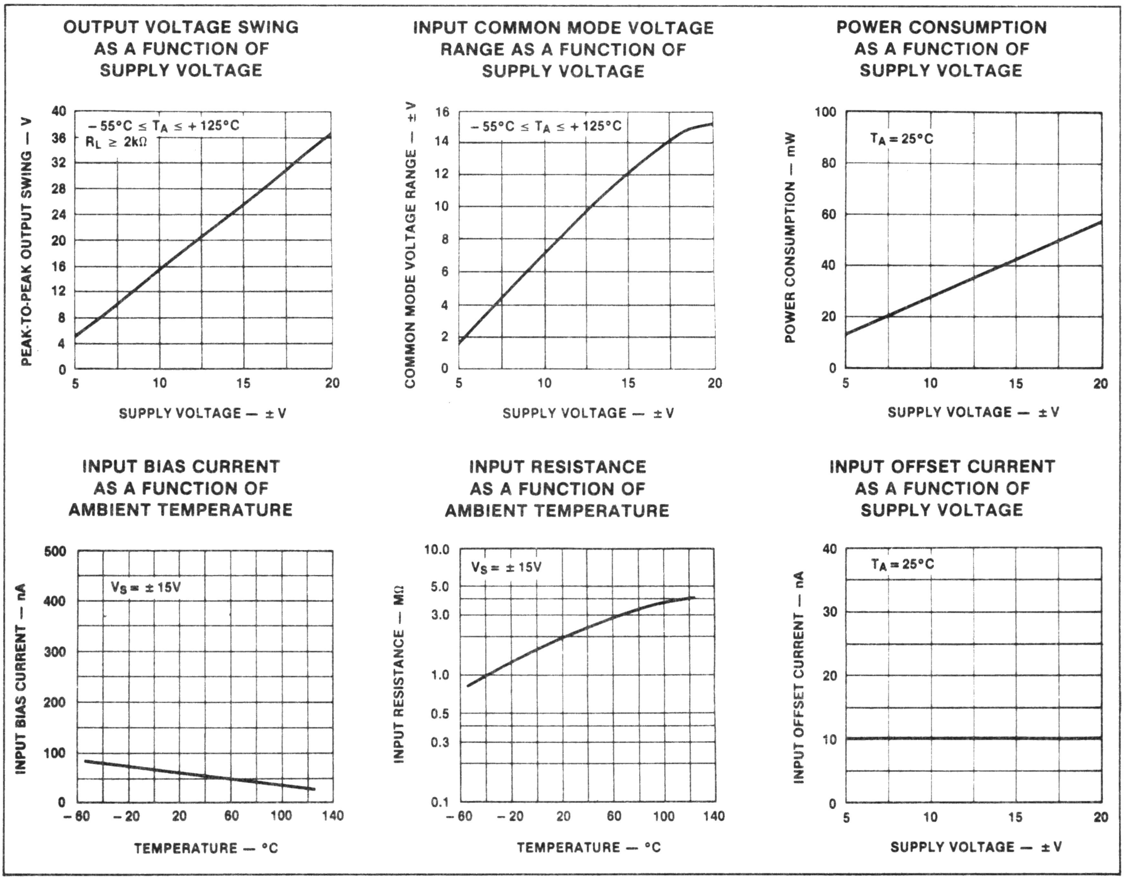
PARAMETER		TEST CONDITIONS	MC1458			SA1458			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S = 10k\Omega$		2.0	6.0		2.0	6.0	mV
		$R_S = 10k\Omega$, over temp.			7.5			7.5	mV
ΔV_{OS}	Offset voltage	Over temperature		12			12		µV/°C
I_{OS}	Offset current			20	200		20	200	nA
		Over temperature			300			500	nA
ΔI_{OS}	Offset current	Over temperature		0.10			0.10		nA/°C
I_{BIAS}	Input bias current			80	500		80	500	nA
		Over temperature			800			1500	nA
ΔI_B	Bias current	Over temperature		1.0			1.0		nA/°C
V_{OUT}	Output voltage swing	$R_L = 10k\Omega$	± 12	± 14		± 12	± 14		V
		$R_L = 2k\Omega$, over temp.	± 10	± 13		± 10	± 13		V
A_{VOL}	Large signal voltage gain	$R_L = 2k\Omega$, $V_O = \pm 10V$	25	200		20	200		V/mV
		$R_L = 2k\Omega$, $V_O = \pm 10V$, Over temperature	15			15			V/mV
	Offset voltage adjustment range			± 30			± 30		mV
PSRR	Supply voltage rejection ratio	$R_S \leq 10k\Omega$		30	150		30	150	µV/V
CMRR	Common mode rejection ratio		70	90		70	90		dB
I_{CC}	Supply current			2.3	5.6		2.3	5.6	mA
V_{IN}	Input voltage range		± 12	± 13		± 12	± 13		V
R_{IN}	Input resistance								MΩ
P_d	Power consumption			70	170		70	170	mW
	Channel separation			120			120		dB
I_{SC}	Output short-circuit current			25			25		mA

GENERAL PURPOSE OPERATIONAL AMPLIFIER MC/SA1458/MC1558

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.

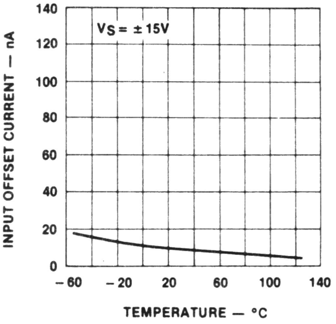
PARAMETER	TEST CONDITIONS	MC1458, SA1458, MC1558			UNIT
		Min	Typ	Max	
Parallel input resistance	Open loop, f = 20Hz	0.3			MΩ
Common mode input impedance	f = 20Hz		200		MΩ
Equivalent input noise voltage	$A_V = 100$, $R_S = 10k\Omega$, $B_W = 1.0kHz$, f = 1.0kHz		30		nV √Hz
Power bandwidth	$A_V = 1$, $R_L = 2.0k\Omega$, THD ≤ 5%, $V_{OUT} = 20Vp\text{-}p$		14		kHz
Phase margin			65		degrees
Gain margin			11		dB
Unity gain crossover frequency	Open loop		1.0		MHz
Transient response unity gain Rise time Overshoot Slew rate	$V_{IN} = 20mV$, $R_L = 2k\Omega$, $C_L \leq 100pF$ $C \leq 100pF$, $R_L \geq 2k$, $V_{IN} = \pm 10V$		 0.3 5.0 0.8		 μs % V/μs

TYPICAL PERFORMANCE CHARACTERISTICS

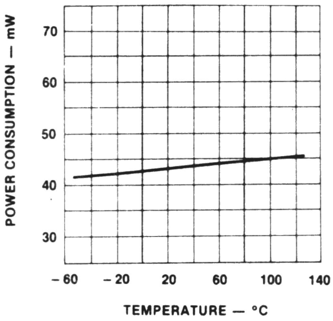


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

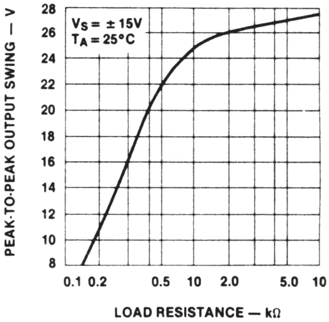
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



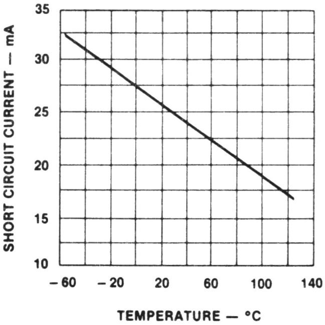
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



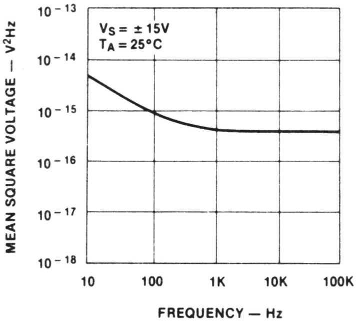
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



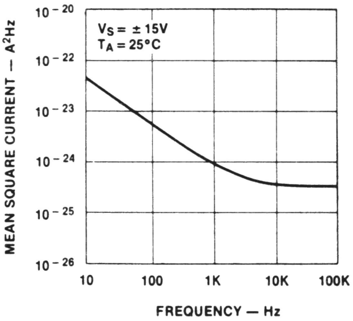
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



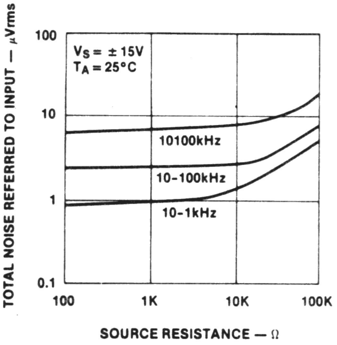
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



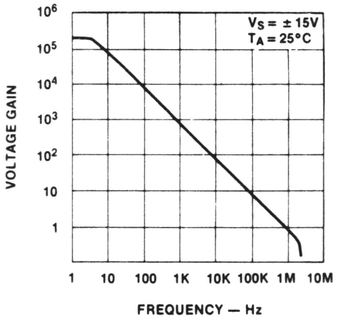
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



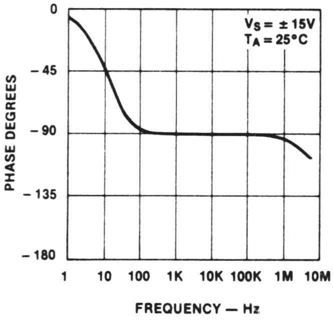
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

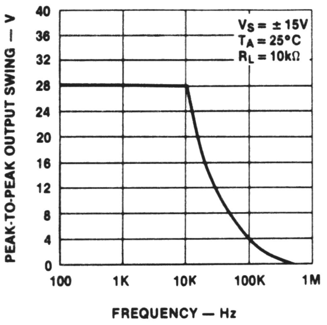


OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY

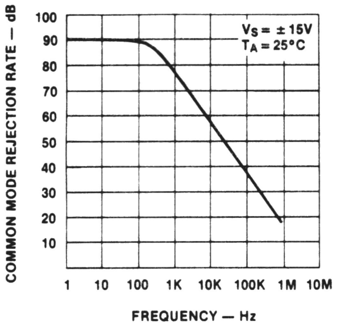


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

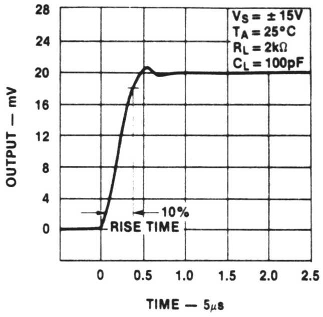
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



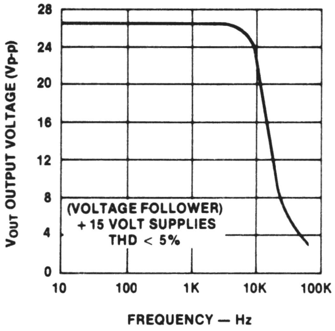
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



TRANSIENT RESPONSE



POWER BANDWIDTH (Large Signal Swing vs Frequency)



QUAD LOW POWER OPERATIONAL AMPLIFIERS MC3303/3403/3503

DESCRIPTION

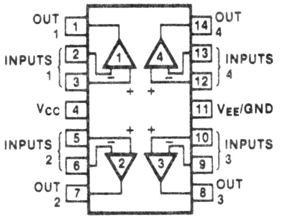
The MC3403 is a quad operational amplifier with true differential inputs. The device has electrical characteristics similar to the popular μA741. However, the MC3403 has several distinct advantages over standard operational amplifier types in single supply applications. The MC3403 can operate at supply voltages as low as 3.0V or as high as 32V. The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

FEATURES

- **Short circuit protected outputs**
- **Class AB output stage for minimal crossover distortion**
- **True differential input stage**
- **Single supply operation: 3.0 to 32V**
- **Split supply operation: ± 1.5 to ± 16V**
- **Low input bias currents: 500nA max**
- **Four amplifiers per package**
- **Internally compensated**

PIN CONFIGURATION

D, F, N PACKAGES


OUT 1
1
INPUTS 1
2
3
Vcc
4
INPUTS 2
5
6
OUT 2
7
OUT 4
14
13
INPUTS 4
12
VEE/GND
11
10
INPUTS 3
9
OUT 3
8
1
2
3
4

TOP VIEW

ORDER NUMBERS

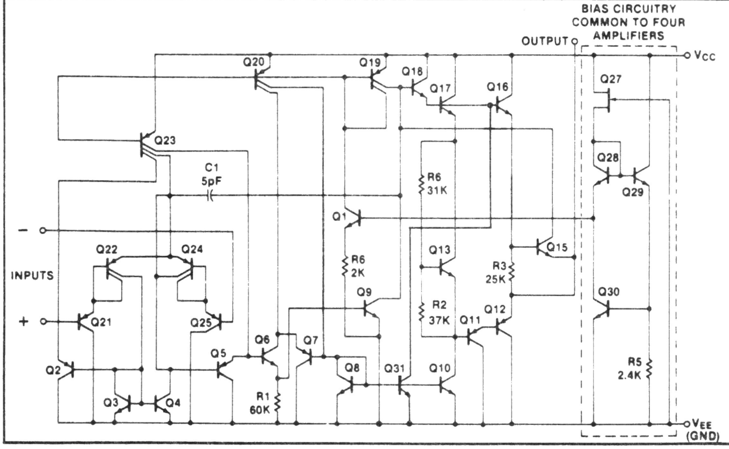
MC3303F
MC3303N
MC3403D
MC3403F
MC3403N
MC3503F

ABSOLUTE MAXIMUM RATINGS

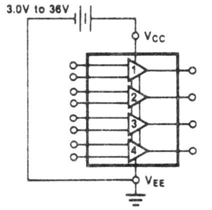
SYMBOL AND PARAMETER		RATING	UNIT
	Power supply voltages (3)		
V_{CC}	Single supply	36	Vdc
V_{CC}	Split supplies	+ 18	Vdc
V_{EE}		– 18	Vdc
V_{IDR}	Input differential voltage range(1)	± 36	Vdc
V_{ICR}	Input common mode voltage range(1,2)	± 18	Vdc
T_{stg}	Storage temperature range		
	Ceramic package	– 65 to + 150	°C
	Plastic package	– 55 to + 125	°C
T_A	Operating ambient temperature range		
	MC3503	– 55 to + 125	°C
	MC3403	0 to + 70	°C
	MC3303	– 40 to + 85	°C
T_J	Junction temperature		
	Ceramic package	175	°C
	Plastic package	150	°C

NOTES
1. Split power supplies.
2. For supply voltages less than ± 15V, the absolute maximum input voltage is equal to the supply voltage.
3. Device not functional for single supply >32V or split supply> ± 16V

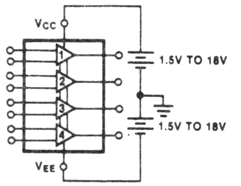
CIRCUIT SCHEMATIC (1/4 Shown)


BIAS CIRCUITRY COMMON TO FOUR AMPLIFIERS
OUTPUT
Vcc
Q20
Q19
Q18
Q17
Q16
Q27
Q23
C1 5pF
R6 31K
Q28
Q29
Q1
−
INPUTS
+
Q22
Q24
Q21
Q25
Q13
Q15
R6 2K
R3 25K
Q9
Q30
R2 37K
Q11
Q12
Q6
Q7
Q5
Q2
Q8
Q31
Q10
R5 2.4K
Q3
Q4
R1 60K
VEE (GND)

SINGLE SUPPLY


3.0V to 36V
Vcc
1
2
3
4
VEE

SPLIT SUPPLIES


Vcc
1
2
3
4
1.5V TO 18V
1.5V TO 18V
VEE

QUAD LOW POWER OPERATIONAL AMPLIFIERS MC3303/3403/3503

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15V$, $V_{EE} = -15V$ for MC3503, MC3403; $V_{CC} = +14V$, $V_{EE} = GND$ for MC3303. $T_A = 25°C$ unless otherwise noted)

SYMBOL AND PARAMETER		TEST CONDITIONS	MC3503			MC3403			MC3303			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input offset voltage	 $T_A = T_{HIGH}$ to T_{LOW}	— —	2.0 —	5.0 6.0	— —	2.0 —	10 12	— —	2.0 —	8.0 10	mV
I_{IO}	Input offset current	 $T_A = T_{HIGH}$ to T_{LOW}	— —	10 —	50 200—	— —	10 200—	50 —	— 250	30	75	nA
A_{VOL}	Large signal open-loop voltage gain	$V_o = \pm 10V$, $R_L = 2.0k\Omega$ $T_A = T_{HIGH}$ to T_{LOW}	50 25	200 300	— —	20 15	200 —	— —	20 15	200 —	— —	V/mV
I_{IB}	Input bias current	 $T_A = T_{HIGH}$ to T_{LOW}	— —	−30 −40	−500 −1200	— —	−30 —	−500 −800	— —	−30 —	−500 −1000	nA
z_o	Output impedance	f = 20Hz	—	75	—	—	75	—	—	75	—	Ω
z_i	Input impedance	f = 20Hz	0.3	1.0	—	0.3	1.0	—	0.3	1.0	—	MΩ
V_{OR}	Output voltage range	$R_L = 10k\Omega$ $R_L = 2.0k\Omega$ $R_L = 2.0k\Omega$, $T_A = T_{HIGH}$ to T_{LOW}	±12 ±10 ±10	±13.5 ±13 —	— — —	±12 ±10 ±10	±13.5 ±13 —	— — —	+12 +10 +10	+12.5 +12 —	— — —	V
V_{ICR}	Input common mode voltage range		$+13V - V_{EE}$	$+13.5V - V_{EE}$	—	$+13V - V_{EE}$	$+13.5V - V_{EE}$	—	$+12V - V_{EE}$	$+12.5V - V_{EE}$	—	V
CMRR	Common mode rejection ratio	$R_S \leq 10k\Omega$	70	90	—	70	90	—	70	90	—	dB
I_{CC}, I_{EE}	Power supply current ($V_o = 0$)	$R_L = \infty$	—	2.5	4.0	—	2.5	7.0	—	2.5	7.0	mA
$\Delta I_B/\Delta T$		$T_A = T_{HIGH}$ to T_{LOW}		3.5	5		3.5	7		3.5	7	mA
$I_{OS\pm}$	Individual output short circuit current[2]		±10	±30	±45	±10	±20	±45	±10	±30	±45	mA
PSRR+	Positive power supply rejection ratio		—	30	150	—	30	150	—	30	150	μV/V
PSRR−	Negative power supply rejection ratio		—	30	150	—	30	150	—	—	—	μV/V
$\Delta I_B/\Delta T$		$T_A = T_{HIGH}$ to T_{LOW}		50			50			50		pA/°C
$\Delta I_{IO}/\Delta T$	Average temperature coeficient of input offset current	$T_A = T_{HIGH}$ to T_{LOW}	—	50	—	—	50	—	—	50	—	pA/°C
$\Delta V_{IO}/\Delta T$	Average temperature coefficient of input offset voltage	$T_A = T_{HIGH}$ to T_{LOW}	—	10	—	—	10	—	—	10	—	μV/°C
BW_P	Power bandwidth	$A_v = 1$, $R_L = 2.0k\Omega$, $V_o = 20V(p\text{-}p)$ THD = 5%	—	9.0	—	—	9.0	—	—	9.0	—	kHz
BW	Small signal bandwidth	$A_v = 1$, $R_L = 10k\Omega$, $V_o = 50mV$	—	1.0	—	—	1.0	—	—	1.0	—	MHz
SR	Slew rate	$A_v = 1$, $V_i = -10V$ to $+10V$	—	0.6	—	—	0.6	—	—	0.6	—	V/μs
t_{TLH}	Rise time	$A_v = 1$, $R_L = 10k\Omega$, $V_o = 50mV$	—	0.35	—	—	0.35	—	—	0.35	—	μs
t_{THL}	Fall time	$A_v = 1$, $R_L = 10k\Omega$, $V_o = 50mV$	—	0.35	—	—	0.35	—	—	0.35	—	μs
OS	Overshoot	$A_v = 1$, $R_L = 10k\Omega$, $V_o = 50mV$	—	20	—	—	20	—	—	20	—	%
ϕm	Phase margin	$A_v = 1$, $R_L = 2.0k\Omega$, $C_L = 200pF$	—	50	—	—	50	—	—	50	—	°
—	Crossover distortion	$V_{IN} = 30mV(p\text{-}p)$, $V_{OUT} = 2.0V(p\text{-}p)$, f = 10kHz	—	1.0	—	—	1.0	—	—	1.0	—	%

NOTES:

1. T_{HIGH} = 125°C for MC3503, 70°C for MC3303. T_{LOW} = −55°C for MC3503, 0°C for MC3403, −40°C for MC3303.
2. Not to exceed maximum package power dissipation.

QUAD LOW POWER OPERATIONAL AMPLIFIERS MC3303/3403/3503

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0V$, $V_E = GND$, $T_A = 25°C$ unless otherwise noted.)

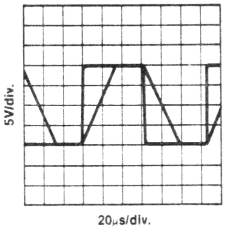
SYMBOL AND PARAMETER		TEST CONDITIONS	MC3503			MC3403			MC3303			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input offset voltage		—	2.0	5.0	—	2.0	10	—	—	10	mV
I_{IO}	Input offset current		—	30	50	—	30	50	—	—	75	nA
I_{IB}	Input bias current		—	−200	−500	—	−200	−500	—	—	−500	nA
A_{VOL}	Large signal open-loop voltage gain	$R_L = 2.0kΩ$	10	200	—	10	200	—	10	200	—	V/mV
PSRR	Power supply rejection ratio		—	—	150	—	—	150	—	—	150	μV/V
V_{OR}	Output voltage range[3]	$R_L = 10kΩ$, $V_{CC} = 5.0V$	3.3	3.5	—	3.3	3.5	—	3.3	3.5	—	Vp-p
		$R_L = 10kΩ$, $5.0V \leq V_{CC} \leq 30V$	$V_{CC} - 1.7$	$V_{CC} - 1.5$	—	$V_{CC} - 1.7$	$V_{CC} - 1.5$	—	$V_{CC} - 1.7$	$V_{CC} - 1.5$	—	
I_{CC}	Power supply current		—	2.5	4.0	—	2.5	7.0	—	2.5	7.0	mA
—	Channel separation	f = 1.0kHz to 20kHz (input referenced)	—	−120	—	—	−120	—	—	−120	—	dB

NOTE

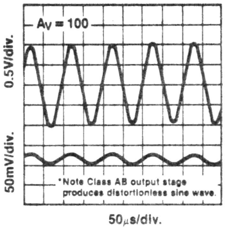
[3] Output will swing to ground.

TYPICAL PERFORMANCE CURVES

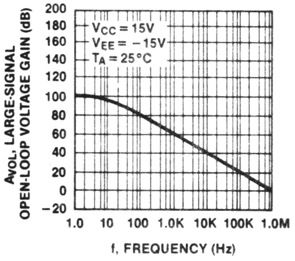
INVERTER PULSE RESPONSE



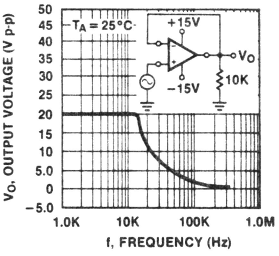
SINE WAVE RESPONSE



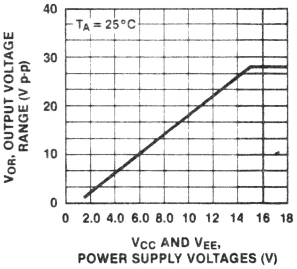
OPEN LOOP FREQUENCY RESPONSE



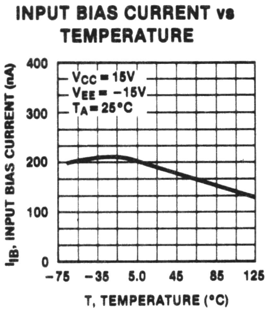
POWER BANDWIDTH

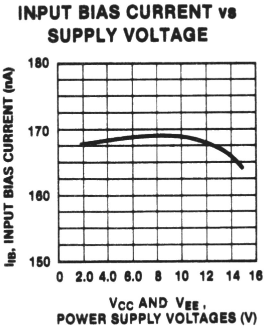


OUTPUT SWING vs SUPPLY VOLTAGE



TYPICAL PERFORMANCE CURVES (Continued)





*For additional information, consult the Applications Section.

DUAL GENERAL-PURPOSE OPERATIONAL AMPLIFIER SA/SE/NE4558

DESCRIPTION

The 4558 is a dual operational amplifier internally compensated. The use of planar epitaxial process for silicon chip construction gives the IC unique performance characteristics.

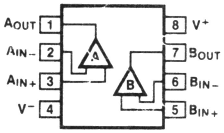
Excellent channel separation allows the use of a dual device in a single amp application, providing the highest packaging density. The SA/SE/NE4558 is a pin for pin replacement for the RC/RM/RV4558.

FEATURES

- **2MHz unity gain bandwidth guaranteed**
- **Supply voltage ±22V for SE4558 and ±18V for NE4558**
- **Short circuit protection**
- **No frequency compensation required**
- **No latch-up**
- **Large common mode and differential voltage ranges**
- **Low power consumption**

PIN CONFIGURATION

D, FE, N PACKAGES



TOP VIEW

ORDER NUMBERS

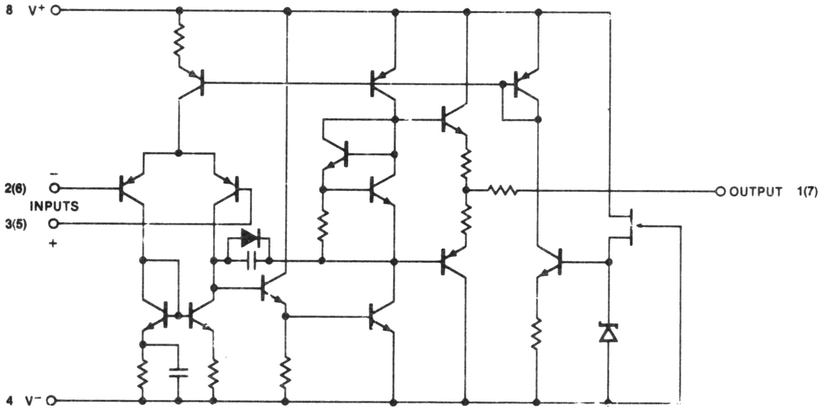
NE4558D
NE4558FE
NE4558N
SA4558FE
SE4558FE
SA4558N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
SE4558:	±22	V
NE4558, SA4558:	±18	V
Internal power dissipation (Note 1)	500	mW
Differential input voltage	±30	V
Input voltage (Note 2)	±15	V
Storage temperature range	−65 to +150	°C
Operating temperature range		
SE4558:	−55 to +125	°C
SA4558:	−40 to +85	°C
NE4558:	0 to +70	°C
Lead temperature (soldering, 60s)	300	°C
Output short circuit duration (Note 3)	Indefinite	

NOTES
1. Rating applies for case temperatures to +125°C; derate linearly at 5.6 mw/°C for ambient temperatures above +75°C for SE4558.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground on one amp only. Rating applies to +125°C case temperature or +75°C ambient temperature for NE4558 and to +85°C ambient temperature for SA4558.

EQUIVALENT SCHEMATIC



DUAL GENERAL-PURPOSE OPERATIONAL AMPLIFIER SA/SE/NE4558

ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 15V$, $T_A = 25°C$ unless otherwise specified.

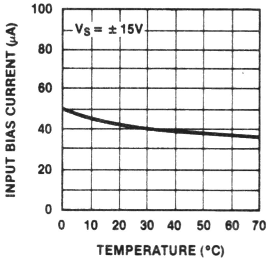
PARAMETER	TEST CONDITIONS	SE4558			SA/NE4558			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage	$R_S \leq 10k\Omega$		1.0	5.0		2.0	6.0	mV
$\Delta V_{os}/\Delta T$	Over temp.		4			4		μV/°C
Input offset current			50	200		30	200	nA
$\Delta I_{os}/\Delta T$	Over temp.		20			20		pA/°C
Input bias current			40	500		200	500	nA
$\Delta I_B/\Delta T$	Over temp.		40			40		pA/°C
Input resistance		0.3	1.0		0.3	1.0		MΩ
Large signal voltage gain	$R_L \geq 2K\Omega$ $V_{OUT} = \pm 10V$	50,000	300,000		20,000	300,000		V/V
Output voltage swing	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	± 12 ± 10	± 14 ± 13		± 12 ± 10	± 14 ± 13		V
Input voltage range		± 12	± 13		± 12	± 13	V	
Common mode rejection ratio	$R_S \leq 10k\Omega$	70	100		70	100		dB
Supply voltage rejection ratio	$R_S \leq 10k\Omega$		10	150		10	150	μV/V
Power consumption (all amplifiers)	R_L = •		100	170		100	170	mW
Transient response (unity gain)	$V_{IN} = 20mV$ $R_L = 2K\Omega$ $C_L \leq 100pF$							
Risetime			100			100		ns
Overshoot			15.0			15.0		%
Slew rate (unity gain)	$R_L \geq 2k\Omega$		1.0			1.0		V/μs
Channel separation (gain = 100)	f = 10kHz $R_S = 1k\Omega$		90			90		dB
Unity gain bandwidth (gain = 1)		2.5	3.0		2.0	3.0		MHz
θ_M phase margin	$T_A = 25°C$		45			45		Degree
Input noise voltage	f = 1kc		25			25		nv/$\sqrt{Hz}$
I_{SC} short circuit	$T_A = 25°C$	5	25	50	5	25	50	mA
The following specifications apply for $-55°C \leq T_A \leq +125°C$ for SE4558; $0°C \leq T_A \leq +70°C$ for NE4558; $-40°C \leq T_A \leq +85°C$ for SA4558								
Input offset voltage	$R_S \leq 10k\Omega$			6.0			7.5	mV
Input offset current				500			300/500*	nA
Input bias current				1500			800/1500*	nA
Large signal voltage gain	$R_L \geq 2k\Omega$ $V_{OUT} = \pm 10$	25,000			15,000			
Output voltage swing	$R_L \geq 2k\Omega$	± 10			± 10			V
Power consumption	$V_S = \pm 15V$ T_A = HIGH T_A = LOW		90 120	150 200		90 120	150 200	mW

*SA4558

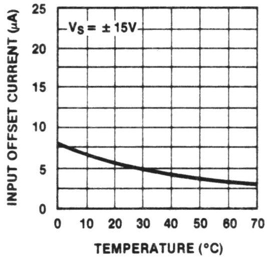
DUAL GENERAL-PURPOSE OPERATIONAL AMPLIFIER SA/SE/NE4558

TYPICAL PERFORMANCE CURVES

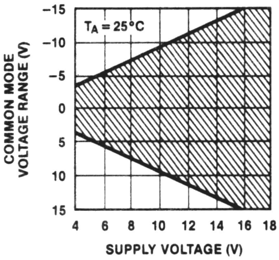
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



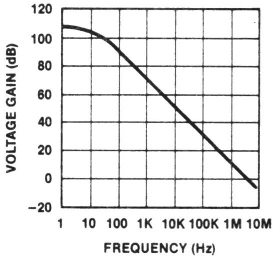
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



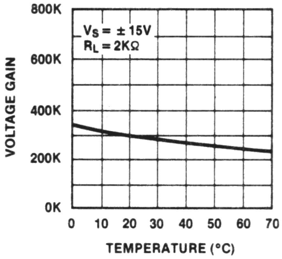
COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



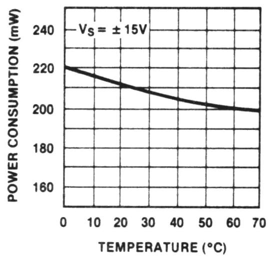
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



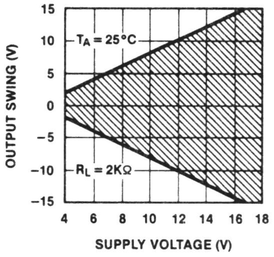
OPEN LOOP GAIN AS A FUNCTION OF TEMPERATURE



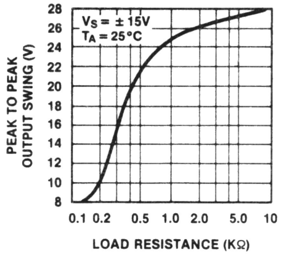
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



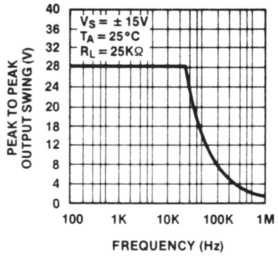
TYPICAL OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

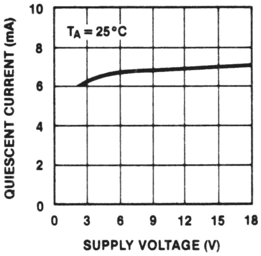


OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

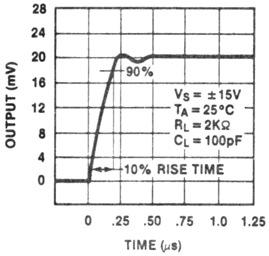


TYPICAL PERFORMANCE CURVES (Continued)

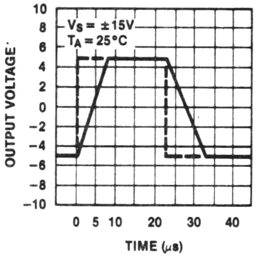
QUIESCENT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



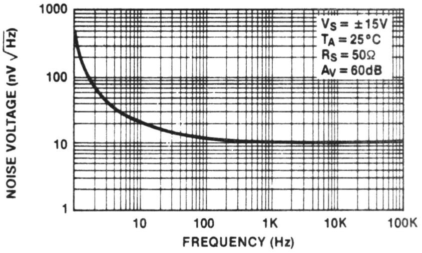
TRANSIENT RESPONSE



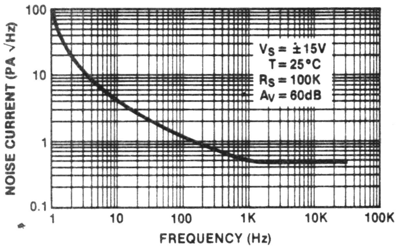
VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE



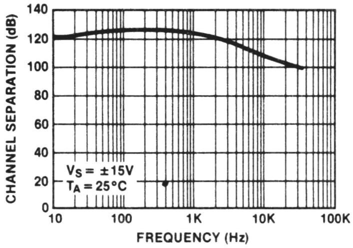
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



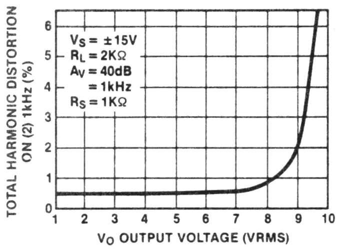
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



CHANNEL SEPARATION

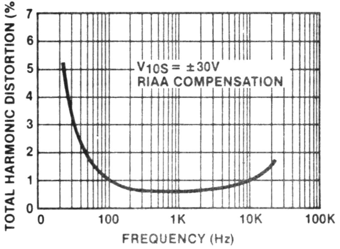


TOTAL HARMONIC DISTORTION vs OUTPUT VOLTAGE



DISTORTION vs FREQUENCY

V$_O$ = 1vrms



HIGH SLEW RATE OPERATIONAL AMPLIFIER SE/NE530

DESCRIPTION

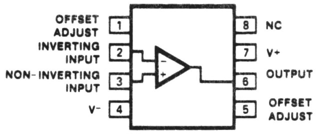
The 530 is a new generation operational amplifier featuring a high slew rate combined with improved input characteristics. Internally compensated, the SE530 guarantees slew rates of 25V/µs with 2mV maximum offset voltage. Industry standard pinout and internal compensation allow the user to upgrade system performance by directly replacing general purpose amplifiers such as the 741 and LF356 types.

FEATURES

- **Gain bandwidth product—3MHz**
- **35V/µs slew rate (Gain = -1)**
- **Internal frequency compensation**
- **Low input offset voltage 2mV max**
- **Low input bias current-60nA max**
- **Short circuit protection**
- **Offset null capability**
- **Large common mode and differential voltage ranges**

PIN CONFIGURATIONS

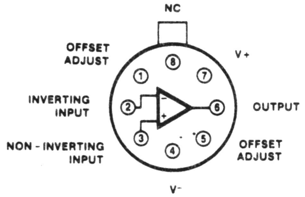
FE,N PACKAGE


OFFSET ADJUST 1
INVERTING INPUT 2
NON-INVERTING INPUT 3
V- 4
8 NC
7 V+
6 OUTPUT
5 OFFSET ADJUST
-
+

TOP VIEW

ORDER NUMBERS
NE530FE, NE530N
SE530FE, SE530N

H PACKAGE*


NC
OFFSET ADJUST
V+
INVERTING INPUT
OUTPUT
NON-INVERTING INPUT
OFFSET ADJUST
V-
1
2
3
4
5
6
7
8
-
+

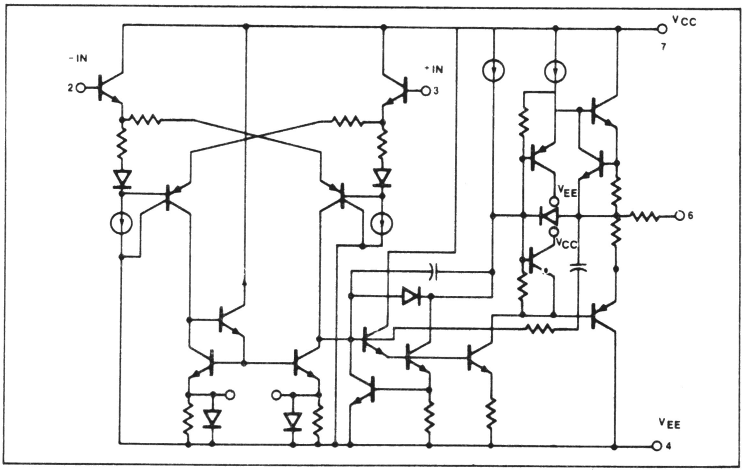
ORDER NUMBERS
NE530H SE530H

*Metal cans (H) not recommended for new designs.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
SE530	±22	V
NE530	±18	V
Internal power dissipation		
N Package	500	mW
H Package	800	mW
FE Package	1000	mW
Differential input voltage	±30	V
Input voltage	±15	V
Operating temperature range		
SE530	-55 to +125	°C
NE530	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature range (Solder, 60sec)	300	°C*
Output short circuit	Indefinite	

EQUIVALENT SCHEMATIC EACH AMPLIFIER


VCC
7
-IN
2
+IN
3
VEE
VCC
6
VEE
4

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = \pm 15V$ unless otherwise specified.[1]

PARAMETER		TEST CONDITIONS	SE530			NE530			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S \leq 10k\Omega$		0.7	4.0		2.0	6.0	mV
		Over temperature			5.0			7.0	mV
ΔV_{OS}	Temperature coefficient of input offset voltage	Over temperature		3	15		6		µV/°C
I_{OS}	Input offset current			5	20		15	40	nA
		Over temperature			40			80	nA
ΔI_{OS}	Input offset current	Over temperature		25			40		pA/°C
I_B	Input bias current			45	80		65	150	nA
		Over temperature			200			200	nA
ΔI_B	Input current	Over temperature		50			80		pA/°C
R_{IN}	Input resistance		3	10		1	6		MΩ
V_{CM}	input common mode voltage range		± 12	± 13		± 12	± 13		V
A_{VOL}	Large signal voltage gain	$R_L \geq 2k\Omega$, $V_O = \pm 10V$	50	200		50	200		V/mV
		Over temperature	25			25			V/mV
V_{OUT}	Output voltage swing	$R_L \geq 10k\Omega$	± 12	± 14		± 12	± 14		V
		$R_L \geq 2k\Omega$	± 10	± 13		± 10	± 13		V
I_{SC}	Output short circuit current		10	25	50	10	25	50	mA
R_{OUT}	Output resistance			100			100		Ω
I_{CC}	Supply current	Each amplifier		2.0	3.0		2.0	3.0	mA
		Over temperature		2.2	3.6		2.2		mA
CMRR	Common mode rejection ratio	$R_S \leq 10k\Omega$	70	90		70	90		dB
		Over temperature							
PSRR	Power supply rejection ratio	$R_S \leq 10k\Omega$		30	150		30	150	µV/V
		Over temperature							

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = \pm 15V$ unless otherwise specified.

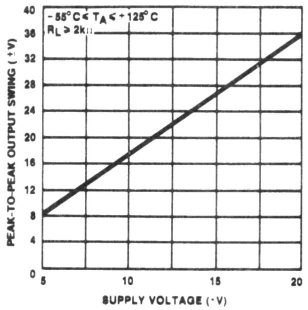
PARAMETER	TEST CONDITIONS	SE530/5530			NE530/5530			UNIT
		Min	Typ	Max	Min	Typ	Max	
Transient Response								
Small signal rise time			.06			.06		µs
Small signal overshoot			13			13		%
Settling time	TO 0.1% (10V step)		0.9			0.9		µs
Slew rate	±15V supply, $V_O = \pm 10V$, $R_L \geq 2k\Omega$							
Unity gain inverting		25	35		20	35		V/µs
Unity gain non-inverting		18	25		12	25		V/µs
Power bandwidth	5% THD, $V_O = \pm 10V$, $R_L \geq 2k\Omega$	360	500		280	500		kHz
Small signal bandwidth	Open loop		3			3		MHz
Input noise voltage	f = 1kHz		30			30		nV/√Hz

NOTE

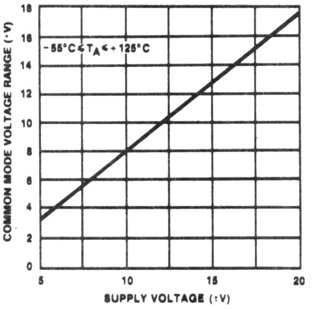
1. Operating temperature range for the SE530 is −55°C to +125°C
   Operating temperature range for the NE530 is 0°C to +70°C.

TYPICAL PERFORMANCE CHARACTERISTICS

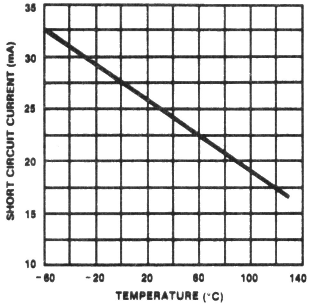
OUTPUT VOLTAGE SWING
AS A FUNCTION OF
SUPPLY VOLTAGE



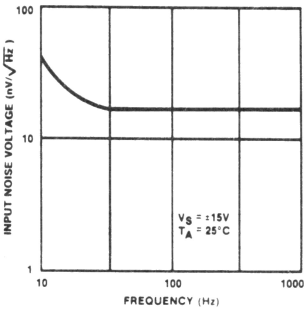
INPUT COMMON MODE
VOLTAGE RANGE AS A
FUNCTION OF SUPPLY VOLTAGE



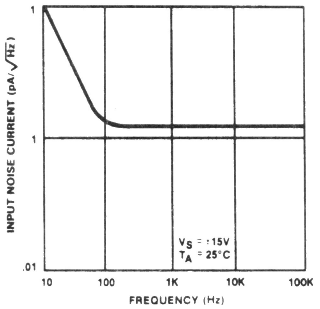
OUTPUT SHORT-CIRCUIT CURRENT
AS A FUNCTION OF
AMBIENT TEMPERATURE



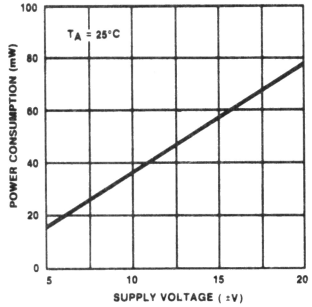
INPUT NOISE VOLTAGE
AS A FUNCTION OF
FREQUENCY



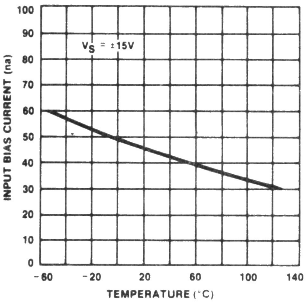
INPUT NOISE CURRENT
AS A FUNCTION OF
FREQUENCY



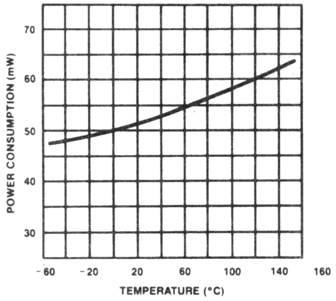
POWER CONSUMPTION
AS A FUNCTION OF
SUPPLY VOLTAGE
(EACH AMPLIFIER)



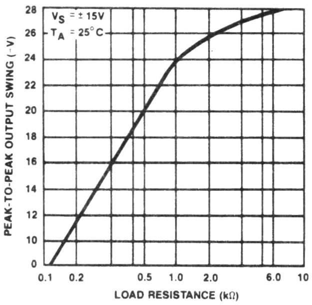
INPUT BIAS CURRENT
AS A FUNCTION OF
AMBIENT TEMPERATURE



POWER CONSUMPTION
AS A FUNCTION OF
AMBIENT TEMPERATURE
(EACH AMPLIFIER)



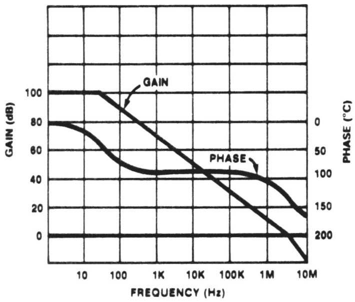
OUTPUT VOLTAGE SWING
AS A FUNCTION OF
LOAD RESISTANCE



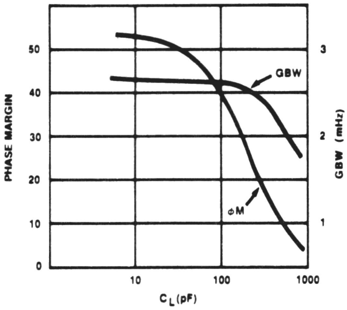
HIGH SLEW RATE OPERATIONAL AMPLIFIER SE/NE530

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

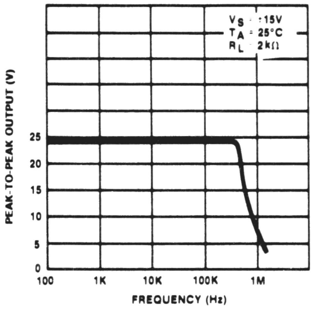
NE530 OPEN-LOOP GAIN AND PHASE vs FREQUENCY



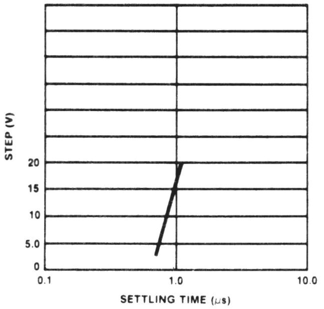
GAIN-BANDWIDTH PRODUCT AND PHASE MARGIN vs LOAD CAPACITANCE



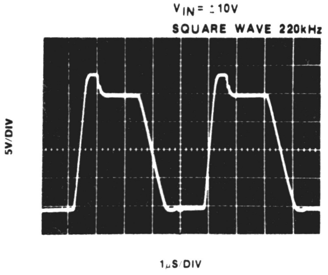
POWER BANDWIDTH



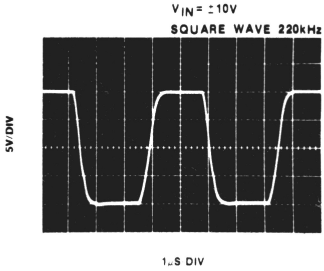
INPUT VOLTAGE STEP vs SETTLING TIME TO 10mV



SLEW RATE—VOLTAGE FOLLOWER

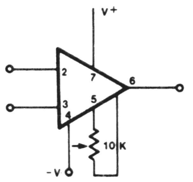


SLEW RATE (-1 AMPLIFIER)



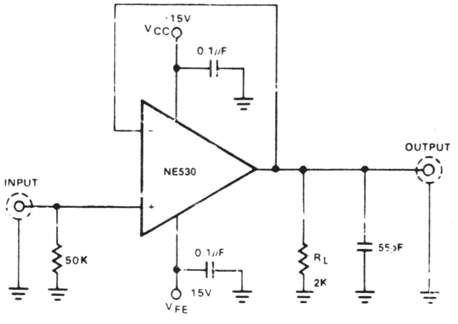
TYPICAL CIRCUIT CONNECTION

OFFSET ADJUST CIRCUIT



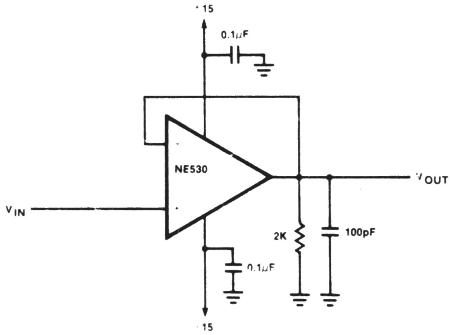
TEST LOAD CIRCUITS

SLEW RATE AND SETTLING TIME

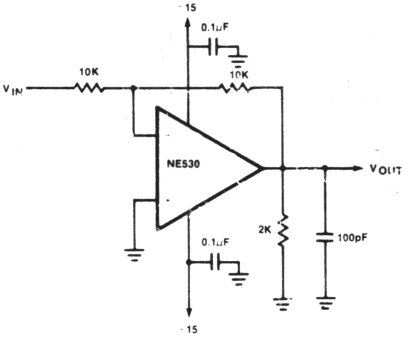

+15V
V_{CC}
0.1μF
NE530
INPUT
50K
0.1μF
−15V
V_{EE}
R_L
2K
55pF
OUTPUT

Pins not shown are not connected.
All resistor values are typical and in ohms.

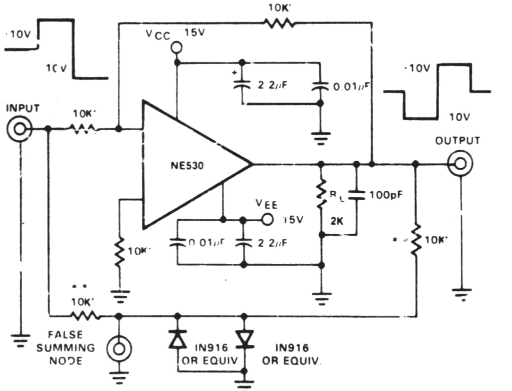
HIGH SLEW RATE—VOLTAGE FOLLOWER


+15
0.1μF
NE530
V_{IN}
V_{OUT}
2K
100pF
0.1μF
−15

HIGH SLEW RATE—INVERTING AMPLIFIER


+15
0.1μF
10K
10K
V_{IN}
NE530
V_{OUT}
2K
100pF
0.1μF
−15

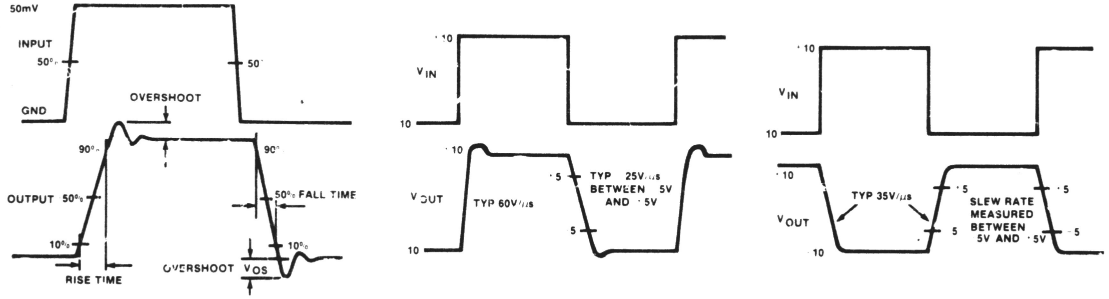
TESTING SLEW RATE AND SETTLING TIME


+10V
−10V
10K*
V_{CC} +15V
2.2μF
0.01μF
+10V
−10V
INPUT
10K*
NE530
OUTPUT
R_L
100pF
2K
V_{EE}
−15V
0.01μF
2.2μF
10K*
**
10K*
10K*
FALSE SUMMING NODE
IN916 OR EQUIV
IN916 OR EQUIV.

Pins not shown are not connected.
All resistor values are typical and in ohms.

*Match to within 0.01%.
**Open for slew rate.

VOLTAGE WAVEFORMS



SMALL SIGNAL TRANSIENT RESPONSE DEFINITIONS

SLEW RATE—VOLTAGE FOLLOWER

SLEW RATE—INVERTING AMPLIFIER

HIGH SLEW RATE OPERATIONAL AMPLIFIER SE/NE531

DESCRIPTION

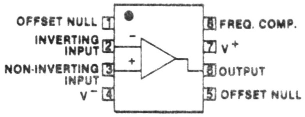
The 531 is a fast slewing high performance operational amplifier which retains dc performance equal to the best general purpose types while providing far superior large signal ac performance. A unique input stage design allows the amplifier to have a large signal response nearly identical to its small signal response. The amplifier is compensated for truly negligible overshoot with a single capacitor. In applications where fast settling and superior large signal bandwidths are required, the amplifier out performs conventional designs which have much better small signal response. Also, because the small signal response is not extended, no special precautions need be taken with circuit board layout to achieve stability. The high gain, simple compensation and excellent stability of this amplifier allow its use in a wide variety of instrumentation applications.

FEATURES

- **35V/μsec slew rate at unity gain**
- **Pin for pin replacement for μA709, μA748 or LM101**
- **Compensated with a single capacitor**
- **Same low drift offset null circuitry as μA741**
- **Small signal bandwidth 1MHz**
- **Large signal bandwidth 500KHz**
- **True op amp dc characteristics make the 531 the ideal answer to all slew rate limited operational amplifier applications.**

PIN CONFIGURATIONS

N,FE PACKAGE

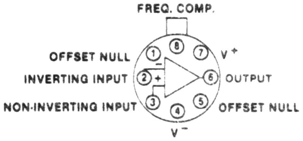

OFFSET NULL 1
INVERTING INPUT 2
NON-INVERTING INPUT 3
V⁻ 4
8 FREQ. COMP.
7 V⁺
6 OUTPUT
5 OFFSET NULL
−
+

TOP VIEW

ORDER NUMBERS

NE531N	SE531N
NE531FE	SE531FE

H PACKAGE*

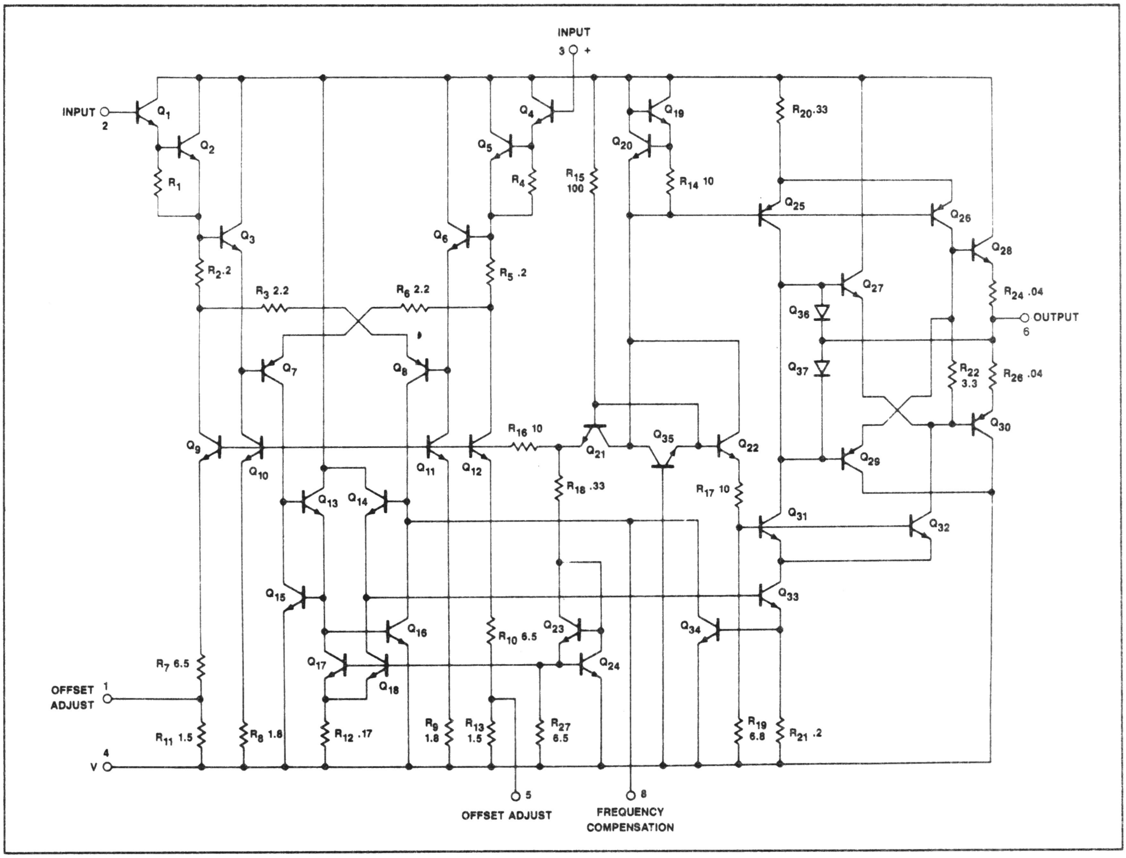

FREQ. COMP.
OFFSET NULL
INVERTING INPUT
NON-INVERTING INPUT
V⁺
OUTPUT
OFFSET NULL
V⁻
1
2
3
4
5
6
7
8
−
+

ORDER NUMBERS

NE531H/SE531H

*Metal cans (H) not recommended for new designs

EQUIVALENT SCHEMATIC


INPUT 3 +
INPUT 2
Q1
Q2
R1
Q3
R2 .2
R3 2.2
R6 2.2
Q4
Q5
R4
Q6
R5 .2
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
Q16
Q17
Q18
R15 100
R16 10
Q19
Q20
R14 10
Q21
R18 .33
Q35
Q22
R17 10
Q23
Q24
R10 6.5
R20 .33
Q25
Q26
Q27
Q28
Q36
Q37
R24 .04
OUTPUT 6
R22 3.3
R26 .04
Q29
Q30
Q31
Q32
Q33
Q34
R7 6.5
OFFSET ADJUST 1
R11 1.5
R8 1.8
R12 .17
R9 1.8
R13 1.5
R27 6.5
R19 6.8
R21 .2
V⁻ 4
5 OFFSET ADJUST
8 FREQUENCY COMPENSATION

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	±22	V
Internal power dissipation[1]	300	mW
Differential input voltage	±15	V
Common mode input voltage[2]	±15	V
Voltage between offset null and V-	±0.5	V
Operating temperature range		
NE531	0 to +70	°C
SE531	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60 sec)	300	°C
Output short circuit duration[3]	indefinite	

NOTES

1. Rating applies for case temperature to 125° C, derate linearly at 6.5mW/° C for ambient temperatures above +75° C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125° C case temperature or to +75° C ambient temperature.

DC ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$ unless otherwise specified.

	PARAMETER	TEST CONDITIONS	SE531[1]			NE531			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S \leq 10k\Omega$, $T_A = 25°C$		2.0	5.0		2.0	6.0	mV
		$R_S \leq 10k\Omega$, over temp			6.0			7.5	mV
ΔV_{OS}		Over temp		10			10		µV/°C
I_{OS}	Offset current	$T_A = 25°C$		30	200		50	200	nA
		T_A = HIGH			200			200	nA
		T_A = LOW			500			300	nA
ΔI_{OS}		Over temp		0.4			0.4		nA/°C
I_{BIAS}	Input current	$T_A = 25°C$		300	500		400	1500	nA
		T_A = HIGH			500			1500	nA
		T_A = LOW			1500			2000	nA
ΔI_B		Over temp		2			2		nA/°C
V_{CM}	Common mode voltage range	$T_A = 25°C$	± 10			± 10			V
CMRR	Common mode rejection ratio	$T_A = 25°C$, $R_S \leq 10k\Omega$				70	100		dB
		Over temp $R_S \leq 10k\Omega$	70	90					dB
R_{IN}	Input resistance	$T_A = 25°C$		20			20		MΩ
V_{OUT}	Output voltage swing	$R_L \geq 10k\Omega$, over temp	± 10	± 13		± 10	± 13		V
I_{CC}	Supply current	$T_A = 25°C$			7.0			10	mA
		T_{MAX}			7.0			10	mA
P_D	Power consumption	$T_A = 25°C$			210			300	mW
PSRR	Power supply rejection ratio	$R_S \leq 10k\Omega$, $T_A = 25°C$					10	150	µV/V
		$R_S \leq 10k\Omega$, over temp		10	150				µV/V
R_{OUT}	Output resistance	$T_A = 25°C$		75			75		Ω
A_{VOL}	Large signal voltage gain	$T_A = 25°C$, $R_L \geq 10k\Omega$, $V_{OUT} = \pm 10V$	50	100		20	60		V/mV
		$R_L \geq 10k\Omega$, $V_{OUT} = \pm 10V$, over temp	25			15			V/mV
V_{INN}	Input noise voltage	25°C, f = 1kHz		20			20		$nV/\sqrt{Hz}$
I_{SC}		25°C	5	15	45	5	15	45	mA

NOTE:

1. Temperature range:
   SE531 $-55°C \leq T_A \leq 125°C$
   NE531 $0°C \leq T_A \leq 70°C$

HIGH SLEW RATE OPERATIONAL AMPLIFIER

SE/NE531

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm15V$ unless otherwise specified.

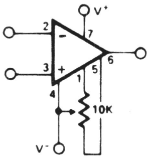
PARAMETER	TEST CONDITIONS	NE531			SE531			UNIT
		Min	Typ	Max	Min	Typ	Max	
Full power bandwidth			500			500		kHz
Settling time (1%) (.1%)	$A_V = +1$, $V_{IN} = \pm10V$		1.5 2.5			1.5 2.5		μs μs
Large signal overshoot	$A_V = +1$, $V_{IN} = \pm10V$		2			2		%
Small signal overshoot	$A_V = +1$, $V_{IN} = 400mV$		5			5		%
Small signal risetime	$A_V = +1$, $V_{IN} = 400mV$		300			300		ns
Slew rate	$A_V = 100$		35			35		V/μs
	$A_V = 10$		35			35		V/μs
	$A_V = 1$ (noninverting)		30		20	30		V/μs
	$A_V = 1$ (inverting)		35		25	35		V/μs

NOTE

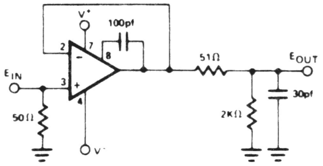
1. All AC testing is performed in the transient response test circuit.

TEST LOAD CIRCUITS

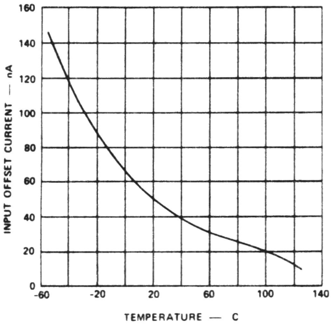
OFFSET NULL CIRCUIT

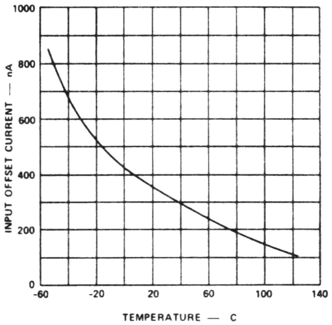


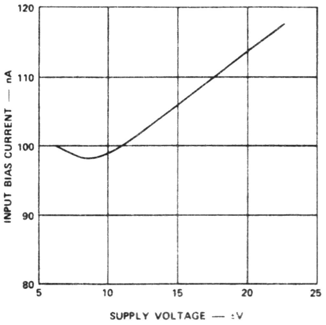
TRANSIENT RESPONSE CIRCUIT



TYPICAL PERFORMANCE CHARACTERISTICS ($V_S = \pm15V$, $T_A = +25°C$, unless otherwise specified.)


INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

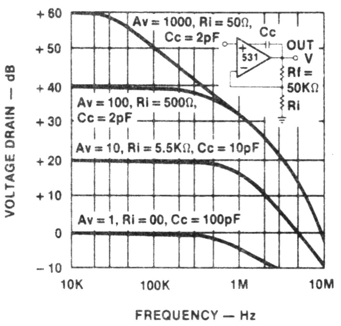

INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE


INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

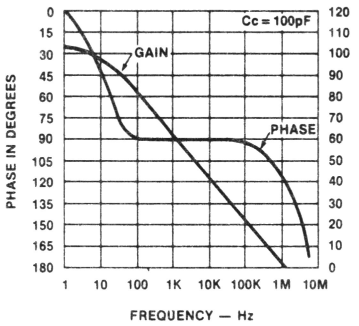
HIGH SLEW RATE OPERATIONAL AMPLIFIER SE/NE531

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

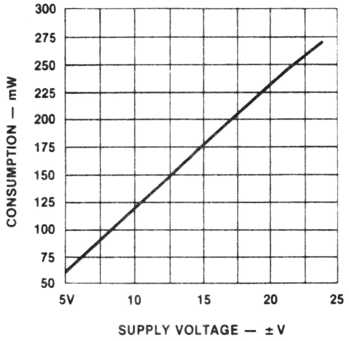
CLOSED LOOP NON-INVERTING VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



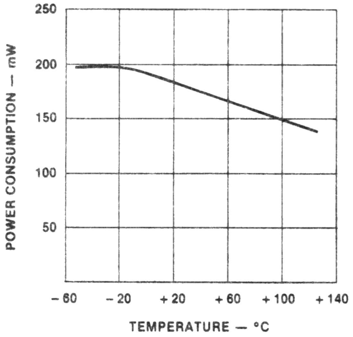
OPEN LOOP PHASE RESPONSE AND VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



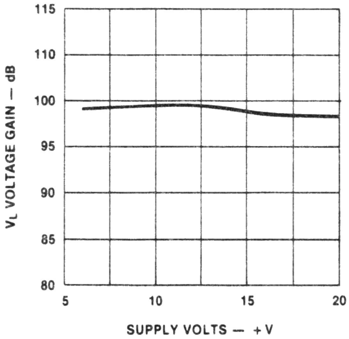
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



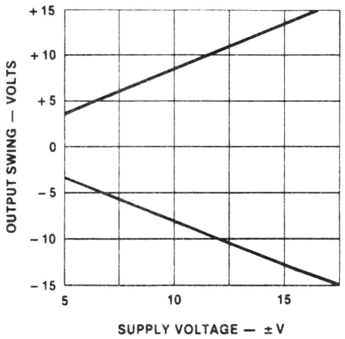
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



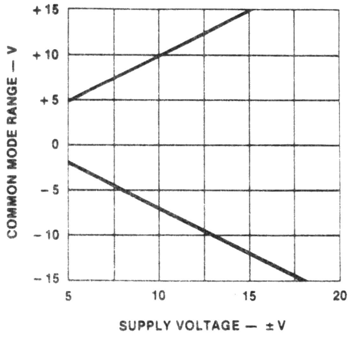
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



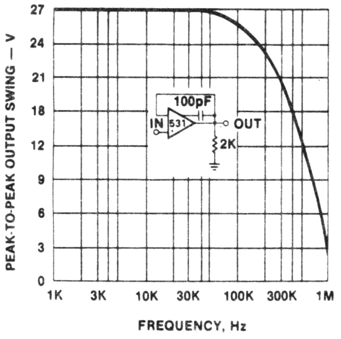
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



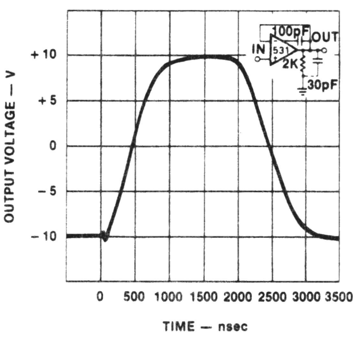
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

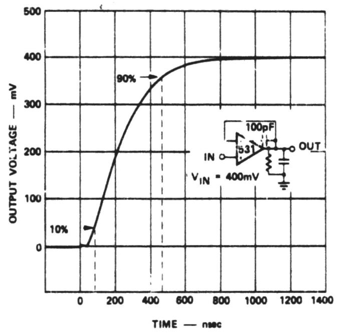


VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE

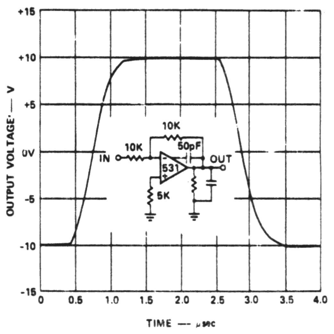


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

VOLTAGE FOLLOWER TRANSIENT RESPONSE

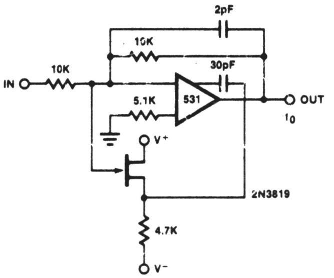


UNITY GAIN INVERTING AMPLIFIER LARGE SIGNAL RESPONSE

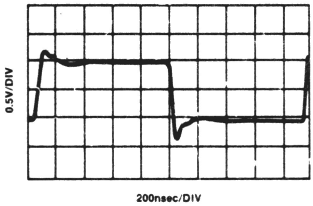


TYPICAL APPLICATIONS

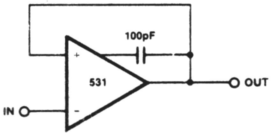
HIGH SPEED INVERTER (10MHz BANDWIDTH)


2pF
10K
10K
30pF
IN
5.1K
531
OUT
I_0
V+
2N3819
4.7K
V-

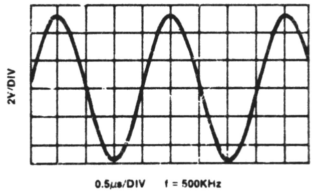
PULSE RESPONSE HIGH SPEED INVERTER



FAST SETTLING VOLTAGE FOLLOWER

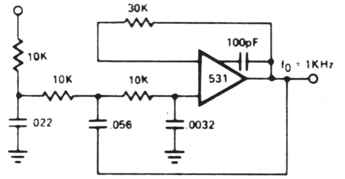

100pF
+
531
-
IN
OUT

LARGE SIGNAL RESPONSE VOLTAGE FOLLOWER

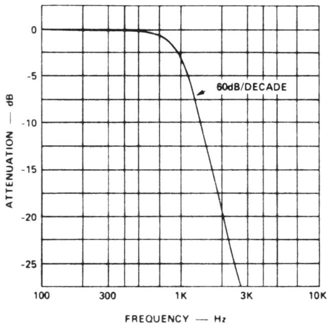


TYPICAL APPLICATIONS (Cont'd)

THREE POLE ACTIVE LOW PASS FILTER BUTTERWORTH MAXIMALLY FLAT RESPONSE*


30K
100pF
f0 = 1KHz
10K
10K
10K
531
.022
.056
.0032

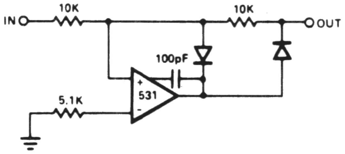
RESPONSE OF 3-POLE ACTIVE BUTTERWORTH MAXIMALLY FLAT FILTER



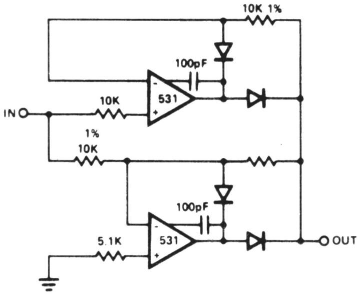
*Reference—EDN Dec. 15, 1970
Simplify 3-Pole Active Filter Design
A. Paul Brokow

PRECISION RECTIFIERS

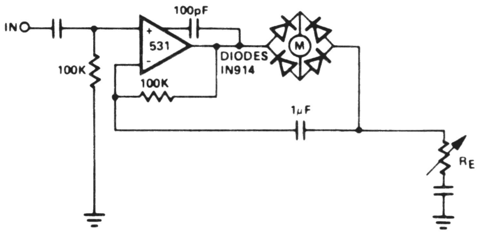
(a) HALF WAVE


IN
10K
10K
OUT
100pF
531
5.1K

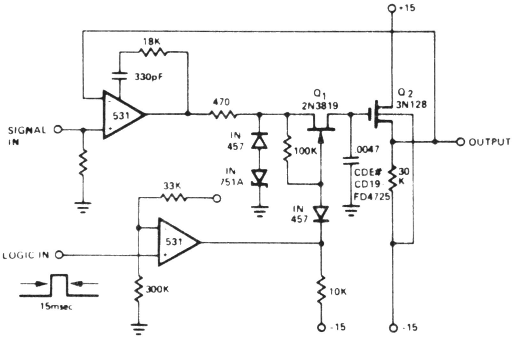
(b) FULL WAVE


10K 1%
100pF
10K
531
IN
1%
10K
100pF
5.1K
531
OUT

AC MILLIVOLTMETER


IN
100pF
531
100K
DIODES
IN914
M
100K
1μF
RE

SAMPLE AND HOLD


+15
18K
330pF
470
Q1
2N3819
Q2
3N128
SIGNAL IN
531
IN 457
IN 751A
100K
.0047
CDE#
CD19
FD4725
30 K
OUTPUT
33K
IN 457
531
LOGIC IN
15msec
300K
10K
-15
-15

HIGH SLEW RATE OPERATIONAL AMPLIFIER SE/NE531

CYCLIC A TO D CONVERTER

One interesting, but, much ignored A/D converter is the cyclic converter. This consists of a chain of identical stages, each of which senses the polarity of the input. The stage then subtracts V_{ref} from the input and doubles the remainder if the polarity was correct. In Figure 1 the signal is full wave rectified and the remainder of $V_{in} - V_{ref}$ is doubled. A chain of these stages gives the gray code equivalent of the input voltage in digitized form related to the magnitude of V_{ref}. Possessing high potential accuracy, the circuit using NE531 devices settles in 5μs.

TRIANGLE AND SQUARE WAVE GENERATOR

The circuit in Figure 2 will generate precision triangle and square waves. The output amplitude of the square wave is set by the output swing of the op amp A-1 and R1/R2 sets the triangle amplitude. The frequency of oscillation in either case is

$$f = \frac{1}{4RC} \bullet \frac{R2}{R1} \qquad (3\text{-}23)$$

The square wave will maintain 50% duty cycle even if the amplitude of the oscillation is not symmetrical.

The use of the NE531 in this circuit will allow good square waves to be generated to quite high frequencies. Since the amplifier A1 runs open loop, there is no need for compensation. The triangle-generating amplifier must be compensated. The NE5535 device can be used as well, except for the lower frequency response.

CYCLIC A TO D CONVERTER

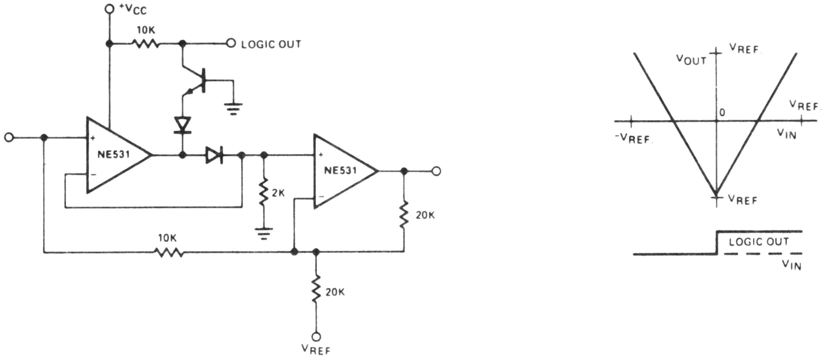


Figure 1a

Figure 1b

TRIANGLE AND SQUARE WAVE GENERATOR

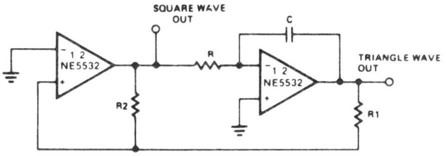


Figure 2

HIGH SLEW RATE OP AMP

SE/NE538

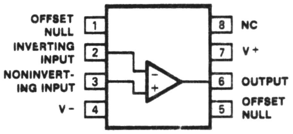
DESCRIPTION

The SE/NE538 is a new generation operational amplifier featuring high slew rates combined with improved input characteristics. Internally compensated for gains of 5 or larger, the SE538 offers guaranteed minimum slew rates of 40V/µs or larger. Featuring 2mV max input offset voltage, the 538 is a single amplifier. Industry standard pin out and internal compensation allow the user to upgrade system performance by directly replacing general purpose amplifiers, such as 748, 101A and 741.

FEATURES

- **2mV input offset voltage**
- **80nA max input offset current**
- **Short circuit protected**
- **Offset null capability**
- **Large common mode and differential voltage ranges**
- **60V/µs slew rate (gain of +5, −4 min)**
- **6MHz gain bandwidth product (gain +5, −4 minimum)**
- **Internal frequency compensation (gain of +5, −4 minimum)**
- **Pin out: 538 same as 741 (single)**

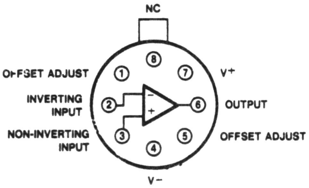
FE,N PACKAGE



TOP VIEW

ORDER NUMBERS
SE538N, FE NE538N, FE

H PACKAGE*



ORDER NUMBERS
SE538H NE538H

ABSOLUTE MAXIMUM RATINGS[1,2,3]

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		
	SE military grade	±22	V
	NE commercial grade	±18	V
P_D	Internal power dissipation FE package	1000	mW
P_D	Internal power dissipation[1] N package	500	mW
P_D	Internal power dissipation[1] H package	800	mW
	Differential input voltage	±30	V
	Input voltage[2]	±15	V
	Operating temperature range		
	SE military grade	-55 to +125	°C
	NE commercial grade	0 to 70	°C
	Output short circuit[3]	indefinite	
	Storage temperature range	-65 to +150	°C
	Lead temperature (solder, 60sec.)	300	°C

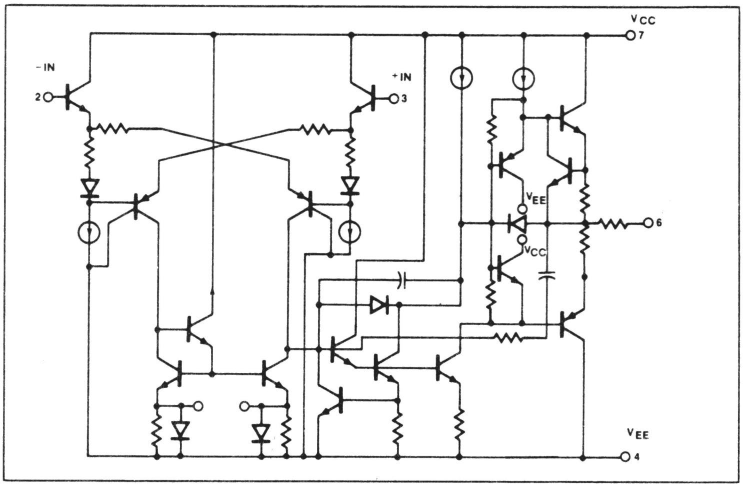
NOTES

1. Rating applies for thermal resistances of 240°C/W and 150°C/W junction to ambient for N and H packages. Maximum chip temperature is 150°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

HIGH SLEW RATE OP AMP

SE/NE538

EQUIVALENT SCHEMATIC (EACH AMPLIFIER)



DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SE538			NE538			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S \le 10k\Omega$		0.7	4.0		2.0	6.0	mV
		$R_S \le 10k\Omega$, over temp.			5.0			7.0	mV
ΔV_{OS}	Input offset voltage drift	$R_S = 0\Omega$, over temp.		4.0			6.0		μV/°C
I_{OS}	Input offset current			5	20		15	40	nA
		Over temp.			40			80	nA
ΔI_{OS}	Input offset current	Over temp		25			40		pA/°C
I_B	Input current			45	80		65	150	nA
		Over temp.			200			200	nA
ΔI_B	Input current	Over temp.		50			80		pA/°C
V_{CM}	Input common mode voltage range		± 12	± 13		± 12	± 13		V
CMRR	Common mode rejection ratio	$R_S \le 10k\Omega$, over temp.	70	90		70	90		dB
PSRR	Power supply rejection	$R_S \le 10k\Omega$, over temp.		30	150		30	150	μV/V
R_{IN}	Input resistance		3	10		1	6		MΩ
A_{VOL}	Large signal voltage gain	$R_L \ge 2k\Omega$, $V_{OUT} = \pm 10V$	50	200		50	200		V/mV
		Over temp., $R_L \ge 2k\Omega$, $V_{OUT} = \pm 10V$	25			25			V/mV
V_{OUT}	Output voltage	Over temp., $R_L \ge 2k\Omega$	± 10	± 13		± 10	± 13		V
		Over temp., $R_L \ge 10k\Omega$	± 12	± 14		± 12	± 14		V
I_{CC}	Supply current	Per amplifier		2	3		2	3	mA
		Over temp., per amplifier		2.2	3.6		2.2	3.6	mA
P_D	Power dissipation	Per amplifier		60	90		60	90	mW
		Over temp., per amplifier		66	108		66	108	mW
I_{SC}	Output short circuit current		10	25	50	10	25	50	mA
R_{OUT}	Output resistance			100			100		Ω

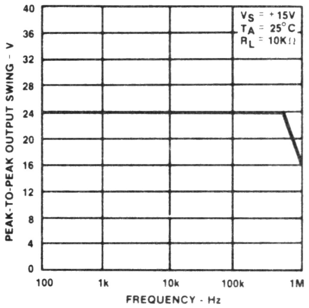
NOTE
Temperature Range
SE Types $-55°C \le T_A \le 125°C$
NE Types $0°C \le T_A \le 70°C$

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

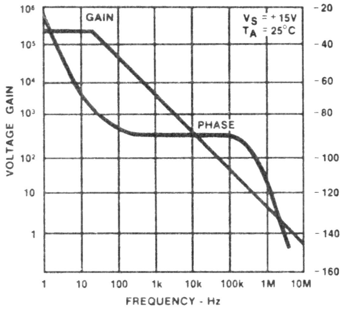
PARAMETER	TEST CONDITIONS	SE538/SE5538			SE538/NE5538			UNIT
		Min	Typ	Max	Min	Typ	Max	
Gain bandwidth product (Gain +5, -4 minimum)			6			6		MHz
Transient response Small signal rise time Small signal overshoot			 0.25 6			 0.25 6		 μs %
Settling time	To 0.1%		1.2			1.2		μs
Slew rate	Minimum gain = 5 Noninverting $R_L \geq 2k\Omega$	40	60			60		V/μs
Input noise voltage	$f = 1kHz$, $T_A = 25°C$		30			30		$nV/\sqrt{Hz}$

TYPICAL PERFORMANCE CHARACTERISTICS

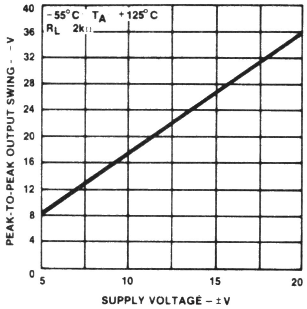
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



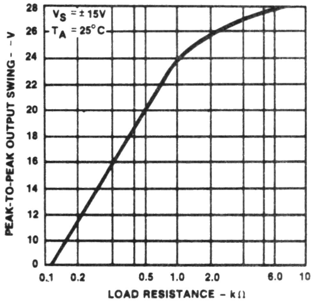
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



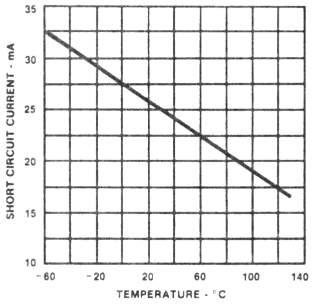
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



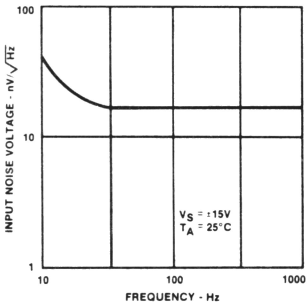
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

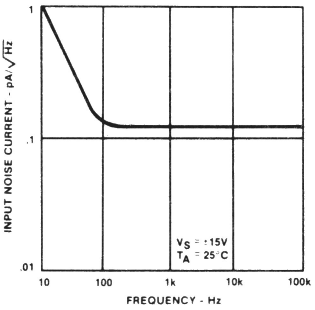


INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY

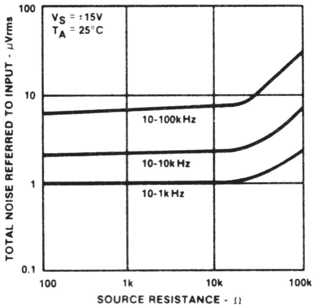


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

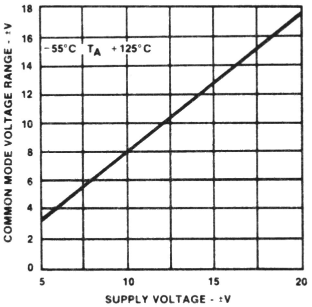
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



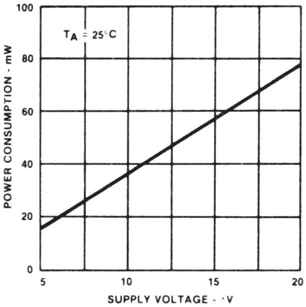
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



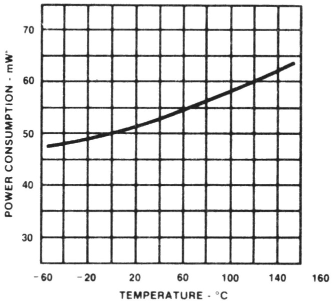
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



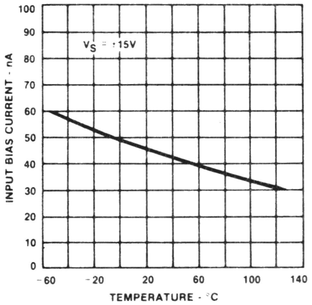
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



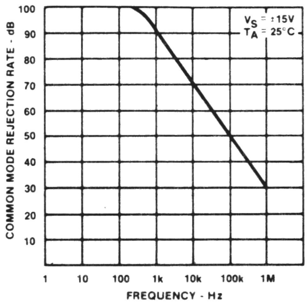
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



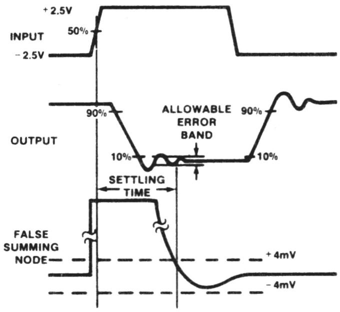
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



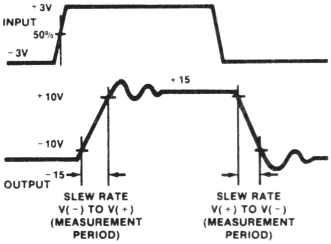
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



SETTLING TIME MEASUREMENT WAVEFORMS

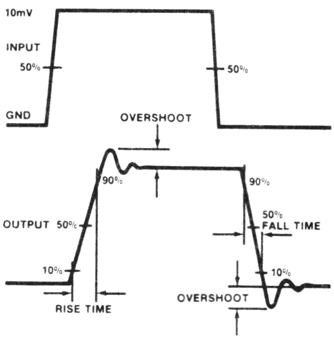

+2.5V
INPUT
50%
-2.5V
90%
ALLOWABLE ERROR BAND
90%
OUTPUT
10%
10%
SETTLING TIME
FALSE SUMMING NODE
+4mV
-4mV

SLEW RATE MEASUREMENT VCC = ±20V


+3V
INPUT
50%
-3V
+15
+10V
-10V
-15
OUTPUT
SLEW RATE V(-) TO V(+) (MEASUREMENT PERIOD)
SLEW RATE V(+) TO V(-) (MEASUREMENT PERIOD)

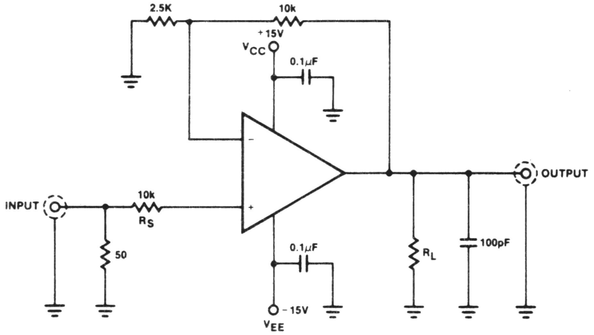
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

SMALL-SIGNAL TRANSIENT RESPONSE DEFINITIONS


10mV
INPUT
50%
50%
GND
OVERSHOOT
90%
90%
OUTPUT 50%
50%
FALL TIME
10%
10%
RISE TIME
OVERSHOOT

TEST LOAD CIRCUITS

SLEW RATE AND SMALL SIGNAL TRANSIENT RESPONSE TEST CIRCUIT


2.5K
10k
+15V
V_{CC}
0.1μF
INPUT
10k
R_S
50
0.1μF
-15V
V_{EE}
R_L
100pF
OUTPUT

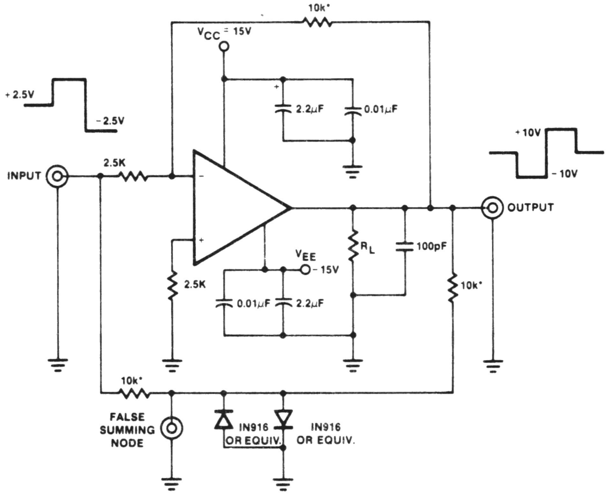
NOTE

Pins not shown are not connected.

All resistors values are typical and in ohms.

TEST LOAD CIRCUITS (Cont'd)

SETTLING TIME TEST CIRCUIT


10k*
V_{CC} = 15V
+2.5V
-2.5V
2.2μF
0.01μF
+10V
-10V
INPUT
2.5K
OUTPUT
V_{EE}
-15V
R_L
100pF
2.5K
0.01μF
2.2μF
10k*
10k*
FALSE SUMMING NODE
IN916 OR EQUIV.
IN916 OR EQUIV.

*Match to within 0.01%.

NOTE

Pins not shown are not connected.

All resistors values are typical and in ohms.

HIGH SLEW RATE OP AMP SE/NE538

INTRODUCTION

The Signetics NE538 is an undercompensated op amp. The NE538 has a typical slew rate of 50V/μs and a gain bandwidth product of 6MHz.

The internal frequency compensation is designed for a minimum inverting gain of 4 and a minimum non-inverting gain of 5. Below these gains the NE538 will be unstable and will need external compensation (see Figure 1 and 2).

The higher slew rate of the NE538 has made this device quite appealing for high speed designs and the fact that it has a standard pinout will allow it to be used to upgrade existing systems that now use the μA741 or μ748.

Equations:

$$f_{LAG} = \frac{1\ (6\text{MHz})}{10} = \frac{1}{2\pi R_L C_L}$$

$$f_{LEAD} = 6\text{MHz} = \frac{1}{2\pi R_F C_F}$$

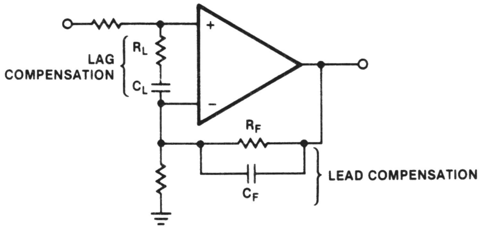

+
−
LAG
COMPENSATION
R_L
C_L
R_F
C_F
LEAD COMPENSATION

Figure 1. Non-Inverting Configuration

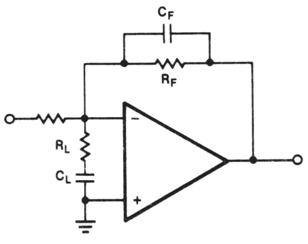


Figure 2. Inverting Configuration

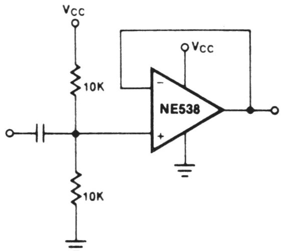

V_{CC}
10K
10K
V_{CC}
−
+
NE538

Figure 3. Voltage Follower with Single Power Source

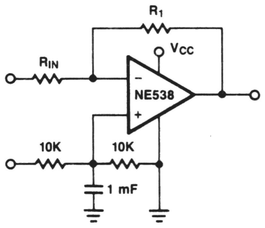

R_1
V_{CC}
R_{IN}
−
+
NE538
10K
10K
1 mF

Figure 4. Inverting Amp With Single Power Supply

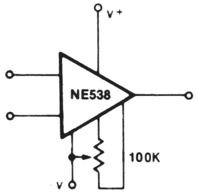
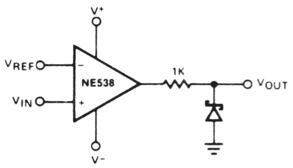

V+
NE538
100K
V

Figure 5. Offset Adjust Circuit


V+
V_{REF}
V_{IN}
−
+
NE538
1K
V_{OUT}
V−

All resistor values are in ohms.

Figure 6. Voltage Comparator

DUAL HIGH PERFORMANCE OPERATIONAL AMPLIFIER SE/NE5512

DESCRIPTION

The 5512 series of high performance operational amplifier provides very good input characteristics. These amplifiers feature low input bias and voltage characteristics such as a 108 op amp with improved CMRR and a high differential input voltage limit achieved through the use of a bias cancellation and PNP input circuits with collector to emitter clamping. The output characteristics are like those of a 741 op amp with improved slew rate and drive capability yet have low supply quiescent current.

APPLICATIONS

- AC amplifiers
- RC active filters
- Transducer amplifiers
- DC gain block
- Battery operation
- Instrumentation amplifiers

FEATURES

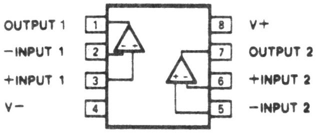
- Low input bias < ±20nA
- Low input offset current < ±20nA
- Low input offset voltage < 1mV
- Low V_{OS} temperature drift 5μV/°C
- Low input bias temperature drift 40pA/°C
- Low input voltage noise 30nV/√Hz
- Low supply current 1.5mA/amp
- High slew rate 1.0V/μs
- High CMRR 100dB
- High input impedance 100MΩ
- High PSRR 110dB
- High differential input voltage limit
- No cross-over distortion
- Indefinite output short circuit protection
- Internally compensated for unity gain
- 600Ω drive capability

ABSOLUTE MAXIMUM RATINGS

Parameter		Rating	Unit
V_{CC}	Supply Voltage	±16	V
V_D	Power dissipation	500	mW
T_A	Operating temperature range		
	NE5512	0 to 70	°C
	SE5512	−55 to +125	°C
T_{STG}	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead temperature soldering	300	°C

PIN CONFIGURATIONS

FE,N PACKAGE

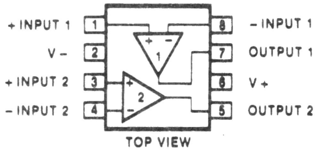


TOP VIEW

ORDER NUMBERS

SE/NE5512FE SE/NE5512N

D³ PACKAGE



TOP VIEW

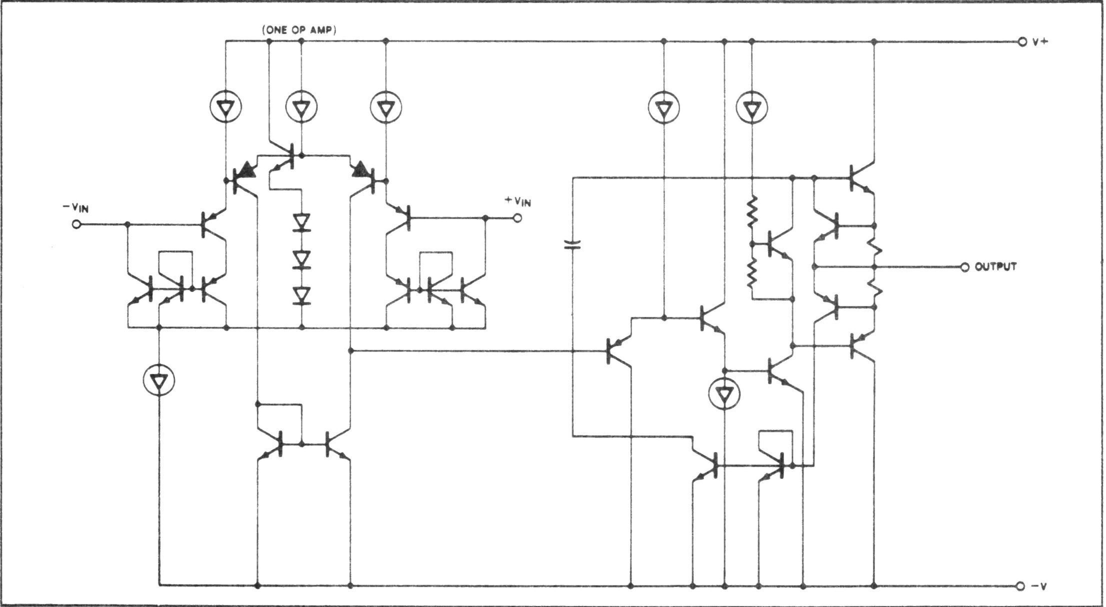
ORDER NUMBER

NE5512D

NOTES:

1. SOL - Released in large SO package only.
2. SOL and non-standard pinout.
3. SO and non-standard pinouts.

EQUIVALENT SCHEMATIC



DUAL HIGH PERFORMANCE OPERATIONAL AMPLIFIER SE/NE5512

ELECTRICAL PERFORMANCE CHARACTERISTICS V_{CC} = ± 15V, F.R. = − 55°C to + 125°C (SE), 0°C to + 70°C (NE)

	PARAMETER	TEST CONDITIONS	SE5512			NE5512			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	R_S = 100Ω							
		T_A = + 25°C		0.7	2		1	5	mV
		T_A = F.R.		1	3		1.5	6	
ΔV_{OS}		Over Temp.		4			5		µV/°C
I_{OS}	Input offset current	R_S = 100kΩ							
		T_A = + 25°C		3	10		6	20	nA
		T_A = F.R.		4	20		8	30	
ΔI_{OS}		Over Temp.		30			40		pA/°C
I_B	Input bias current	R_S = 100kΩ							
		T = + 25°C		3	10		6	20	nA
		T_A = F.R.		4	20		8	30	
ΔI_B		Over Temp.		30			40		pA/°C
R_{IN}	Input resistance differential	T_A = 25°C		100			100		MΩ
V_{CM}	Input common mode range	T_A = 25°C	± 13.5	± 13.7		± 13.5	± 13.7		V
		T_A = F.R.	± 13	± 13.2		± 13	± 13.2		
CMRR	Input common-mode rejection ratio	V_{CC} = ± 15V							
		V_{IN} = ± 13.5V (RM)							
		T_A = 25°C	70	100		70	100		dB
		V_{IN} = ± 13V (F.R.)							
		T_A = F.R.							
A_{VOL} GAIN	Large-signal voltage gain	R_L = 2kΩ T_A = 25°C	50	200		50	200		V/mV
		V_O = ± 10V T_A = F.R.	25			25			
S.R.	Slew rate	T_A = 25°C	0.6	1			1		V/µs
GBW	Small-signal unity gain bandwidth	T_A = 25°C		3			3		MHz
θ_M	Phase margin	T_A = 25°C		45			45		Degree
V_{OUT}	Output voltage swing	R_L = 2kΩ							
		T_A = 25°C	± 13	± 13.5		± 13	± 13.5		V
		T_A = F.R.	± 12.5	± 13		± 12.5	± 13		
V_{OUT}	Output voltage swing	R_L = 600Ω*							
		T_A = 25°C	± 10	± 11.5		± 10	± 11.5		V
		T_A = F.R.	± 7.5	± 9		± 8	± 9		
I_{CC}	Power supply current	R_L = Open							
		T_A = 25°C		3.4	5		3.4	5	mA
		T_A = F.R.		3.6	5.5		3.6	5.5	
P_{SRR}	Power supply rejection ratio	T_A = 25°C	80	110		80	110		dB
		T_A = F.R.	80	100		80	100		
AA	Amplifier to amplifier coupling	f = 1kHz to 20kHz							
		T_A = 25°C		− 120			− 120		dB
HD	Total harmonic distortion	f = 10kHz							
		T_A = 25°C		0.01			0.01		%
		V_O = 7V_{RMS}							
V_{IN_N}	Input noise voltage	f = 1kHz							
		T_A = 25°C		30			30		nV/ $\sqrt{Hz}$
I_{IN_N}	Input noise current	f = 1kHz							
		T_A = 25°C		.2			.2		pA/ $\sqrt{Hz}$
I_{SC}	Short circuit	± 15V T_A = 25°C		40			40		mA

NOTE

For operation at elevated temperature, N package must be derated based on a thermal resistance of 120°/W junction to ambient. Thermal resistance of the FE package is 125°/W.

***For additional information, consult the Applications Section.**

QUAD HIGH PERFORMANCE OP AMP SE/NE5514

DESCRIPTION

The SE/NE5514 family of Quad Operational Amplifiers sets new standards in Bipolar Quad Amplifier Performance. The amplifiers feature low input bias current and low offset voltages. Pin-out is identical to LM324/LM348 which facilitates direct product substitution for improved system performance. Output characteristics are similar to a μA741 with improved slew and drive capability.

FEATURES

- **Low input bias current: <±3nA**
- **Low input offset current: <±3nA**
- **Low input offset voltage: <1mV**
- **Low supply current: 1.5mA/Amp**
- **1 V/μsec slew rate**
- **High input impedance: 100MΩ**
- **High common mode impedance: 10GΩ**
- **Internal compensation for unity gain**
- **600Ω drive capability (7 Vrms)**

APPLICATIONS

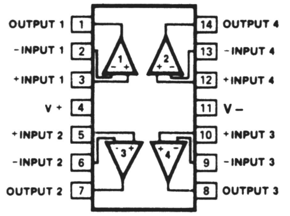
- **AC amplifiers**
- **RC active filters**
- **Transducer amplifiers**
- **DC gain block**
- **Instrumentation amplifier**

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	±16	V
V_{DIFF}	Differential input voltage	32	V
V_{IN}	Input voltage	0 to 32	V
	Output short to ground	Continuous	
TS	Storage temperature range	−65 to +150	°C
T_{SOLD}	Lead soldering temperature	300	°C
T_A	Operating temperature range		
	NE5514	0 to 70	°C
	SE5514	−55 to +125	°C

PIN CONFIGURATION

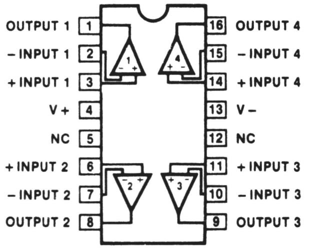
F,N PACKAGE


OUTPUT 1
1
−INPUT 1
2
+INPUT 1
3
V+
4
+INPUT 2
5
−INPUT 2
6
OUTPUT 2
7
14
OUTPUT 4
13
−INPUT 4
12
+INPUT 4
11
V−
10
+INPUT 3
9
−INPUT 3
8
OUTPUT 3
1
2
3
4

TOP VIEW

ORDER NUMBERS
NE5514F, N SE5514F, N

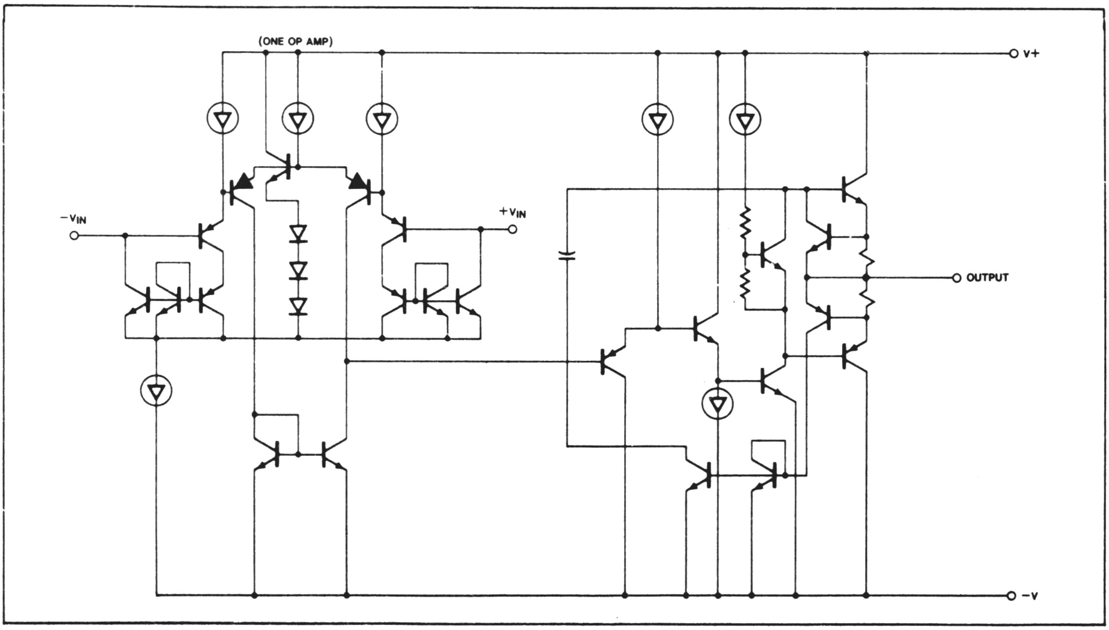
D² PACKAGE


OUTPUT 1
1
−INPUT 1
2
+INPUT 1
3
V+
4
NC
5
+INPUT 2
6
−INPUT 2
7
OUTPUT 2
8
16
OUTPUT 4
15
−INPUT 4
14
+INPUT 4
13
V−
12
NC
11
+INPUT 3
10
−INPUT 3
9
OUTPUT 3
1
2
3
4

TOP VIEW
ORDER NUMBER
NE5514D[1]

NOTES:
1. SOL - Released in large SO package only.
2. SOL and non-standard pinout.
3. SO and non-standard pinouts.

EQUIVALENT SCHEMATIC


(ONE OP AMP)
V+
−VIN
+VIN
OUTPUT
−V

QUAD HIGH PERFORMANCE OP AMP

SE/NE5514

ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 15V$, F.R. = −55°C to +125°C (SE); 0°C to 70°C (NE)

PARAMETER		TEST CONDITIONS	SE5514			NE5514			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S = 100\Omega$, $T_A = +25°C$,		0.7	2		1	5	mV
		T_A = F.R.		1	3		1.5	6	
ΔV_{OS}		Over temp.		4			5		µV/°C
I_{OS}	Input offset current	$R_S = 100k\Omega$, $T_A = +25°C$,		3	10		6	20	nA
		T_A = F.R.		4	20		8	30	
ΔI_{OS}		Over temp.		30			40		pA/°C
I_B	Input bias current	$R_S = 100k\Omega$, $T_A = +25°C$,		3	10		6	20	nA
		T_A = F.R.		4	20		8	30	
ΔI_B		Over temp.		30			40		pA/°C
R_{IN}	Input resistance differential	$T_A = 25°C$		100			100		MΩ
V_{CM}	Input common mode range	$T_A = 25°C$, T_A = F.R.	± 13.5 ± 13	± 13.7 ± 13.2		± 13.5 ± 13	± 13.7 ± 13.2		V
CMRR	Input common-mode rejection ratio	$V_{CC} = \pm 15V$, $V_{IN} = \pm 13.5V$ (RM), $T_A = 25°C$, $V_{IN} = \pm 13V$ (F.R.), T_A = F.R.	70	100		70	100		dB
AVOL GAIN	Large-signal voltage gain	$R_L = 2k\Omega$, $T_A = 25°C$ $V_C = \pm 10V$, T_A = F.R.	50 25	200		50 25			V/mV
S.R.	Slew rate	$T_A = 25°C$	0.6	1		0.6	1		V/µs
GBW	Small-signal unity gain bandwidth	$T_A = 25°C$		3			3		MHz
θ_M	Phase margin	$T_A = 25°C$		45			45		Degr
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$, $T_A = 25°C$, T_A = F.R.	± 13 ± 12.5	± 13.5 ± 13		± 13 ± 12.5	± 13.5 ± 13		V
V_{OUT}	Output voltage swing	$R_L = 600\Omega$*, $T_A = 25°C$, T_A = F.R.	± 10 ± 7.5	± 11.5 ± 9		± 10 ± 8	± 11.5 ± 9		V
I_{CC}	Power supply current	R_L = Open, $T_A = 25°C$, T_A = F.R.		6 7	10 12		6 7	10 12	mA
PSRR	Power supply rejection ratio	$T_A = 25°C$, T_A = F.R.	80 80	110 100		80 80	110 100		dB
AA	Amplifier to amplifier coupling	f = 1kHz to 20kHz, $T_A = 25°C$		− 120			− 120		dB
HD	Total harmonic distortion	f = 10kHz, $T_A = 25°C$, V_O = 7VRMS		0.01			0.01		%
V_{INN}	Input-noise voltage	f = 1kHz, $T_A = 25°C$		30			30		$nV/\sqrt{Hz}$
I_{SC}	Short Circuit	$T_A = 25°C$	10	40	60	10	40	60	mA

NOTE

*For operation at elevated temperature, N package must be derated based on a thermal resistance of 95°C/W junction to ambient.

***For additional information, consult the Applications Section.**

INTERNALLY COMPENSATED DUAL LOW NOISE OP AMP SE/NE5532/5532A

DESCRIPTION

The 5532 is a dual high-performance low noise operational amplifier. Compared to most of the standard operational amplifiers, such as the 1458, it shows better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

This makes the device especially suitable for application in high quality and professional audio equipment, instrumentation and control circuits, and telephone channel amplifiers. The op amp is internally compensated for gains equal to one. If very low noise is of prime importance, it is recommended that the 5532A version be used which has guaranteed noise voltage specifications.

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_S	Supply voltage	±22	V
V_{IN}	Input voltage	±V supply	V
V_{DIFF}	Differential input voltage[1]	±.5	V
T_A	Operating temperature range		
	NE5532/A	0 to 70	°C
	SE5532/A	−55 to +125	°C
T_{STG}	Storage temperature	−65 to +150	°C
T_J	Junction temperature	150	°C
P_D	Power dissipation		
	5532FE	1000	mW
	Lead temperature (soldering, 10 sec)	300	°C

NOTES:

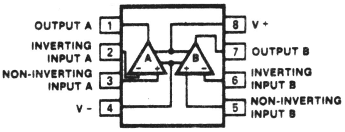
1. Diodes protect the inputs against over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ± 10mA.
2. Thermal resistance of the FE package is 125°C/W.

FEATURES

- Small-signal bandwidth: 10MHz
- Output drive capability: 600Ω, 10V (rms)
- Input noise voltage: $5nV/\sqrt{Hz}$ (typical)
- DC voltage gain: 50000
- AC voltage gain: 2200 at 10kHz
- Power bandwidth: 140kHz
- Slew-rate: 9V/μs
- Large supply voltage range: ±3 to ±20V
- Compensated for unity gain

PIN CONFIGURATION

FE,N PACKAGE



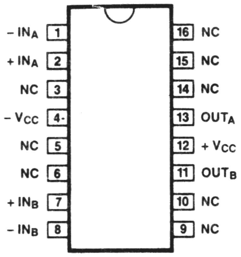
TOP VIEW

ORDER NUMBERS

NE5532FE, N SE5532FE

NE5532AFE, N SE5532AFE

D² PACKAGE

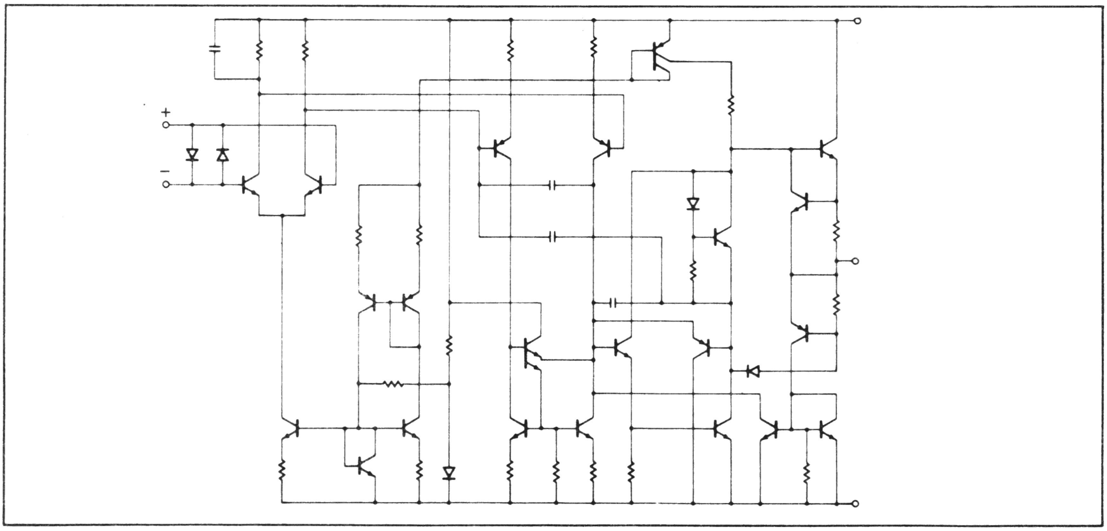


TOP VIEW

ORDER NUMBER

NG5532D

EQUIVALENT SCHEMATIC (EACH AMPLIFIER)



DC ELECTRICAL CHARACTERISTICS $T_A = 25°C, V_S = \pm 15V$ unless otherwise specified.[1,2]

PARAMETER		TEST CONDITIONS	SE5532/55232A			NE5532/5532A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage			0.5	2		0.5	4	mV
		Over temperature			3			5	mV
$\Delta V_{OS}/\Delta T$				5			5		µV/°C
I_{OS}	Offset current				100		10	150	nA
		Over temperature			200			200	nA
$\Delta I_{OS}/\Delta T$				200			200		pA/°C
I_B	Input current			200	400		200	800	nA
		Over temperature			700			1000	nA
$\Delta I_B/\Delta T$				5			5		mA/°C
I_{CC}	Supply current						8	16	mA
		Over temperature			13				mA
V_{CM}	Common mode input range		± 12	± 13		± 12	± 13		V
CMRR	Common mode rejection ratio		80	100		70	100		dB
PSRR	Power supply rejection ratio			10	50		10	100	µV/V
A_{VOL}	Large signal voltage gain	$R_L \geq 2k\Omega, V_0 = \pm 10V$	50			25	100		V/mV
		Over temperature	25			15			V/mV
		$R_L \geq 600\Omega, V_0 = \pm 10V$	40			15	50		V/mV
		Over temperature	20			10			V/mV
V_{OUT}	Output swing	$R_L \geq 600\Omega$				± 12	± 13		V
		Over temperature				± 10	± 12		V
		$R_L \geq 600\Omega, V_S = \pm 18V$	± 15	± 16					V
		Over temperature				± 12	± 14		V
		$R_L \geq 2k\Omega$ over temp.	± 12	± 13		± 10	± 13		V
R_{IN}	Input resistance		30	300		30	300		kΩ
I_{SC}	Output short circuit current		10	38	60	10	38	60	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C, V_S = \pm 15V$ unless otherwise specified.

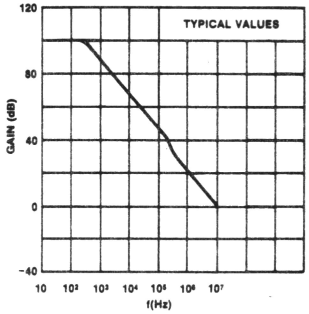
PARAMETER		TEST CONDITIONS	SE/NE5532/5532A			UNIT
			Min	Typ	Max	
R_{OUT}	Output resistance	$A_V = 30dB$ Closed loop $f = 10kHz, R_L = 600\Omega$		0.3		Ω
	Overshoot	Voltage follower $V_{IN} = 100mV$ p-p $C_L = 100pF \quad R_L = 600\Omega$		10		%
	Gain	$f = 10kHz$		2.2		V/mV
	Gain bandwidth product	$C_L = 100pF \quad R_L = 600\Omega$		10		MHz
	Slew rate			9		V/µs
	Power bandwidth	$V_{OUT} = \pm 10V$		140		kHz
		$V_{OUT} = \pm 14V, R_L = 600\Omega,$ $V_{CC} = \pm 18V$		100		kHz

ELECTRICAL CHARACTERISTICS $T_A = 25°C, V_S = \pm 15V$ unless otherwise specified.

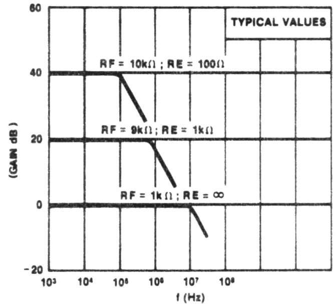
PARAMETER	TEST CONDITIONS	SE/NE5532			SE/NE5532A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input noise voltage	$f_o = 30Hz$		8			8	12	$nV/\sqrt{Hz}$
	$f_o = 1kHz$		5			5	6	$nV/\sqrt{Hz}$
Input noise current	$f_o = 30Hz$		2.7			2.7		$pA/\sqrt{Hz}$
	$f_o = 1kHz$		0.7			0.7		$pA/\sqrt{Hz}$
Channel separation	$f = 1kHz, RS = 5k\Omega$		110			110		dB

TYPICAL PERFORMANCE CHARACTERISTICS

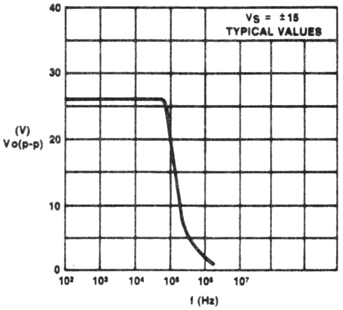
OPEN LOOP FREQUENCY RESPONSE



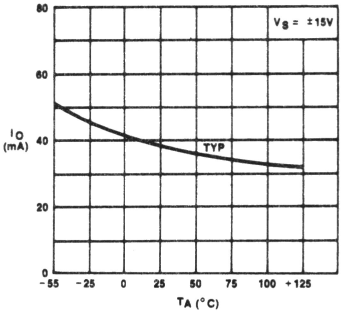
CLOSED LOOP FREQUENCY RESPONSE



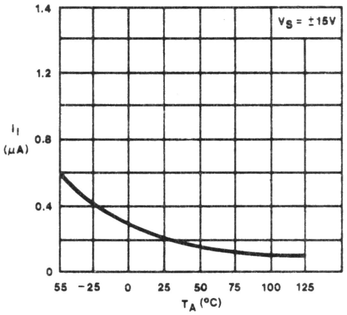
LARGE-SIGNAL FREQUENCY RESPONSE



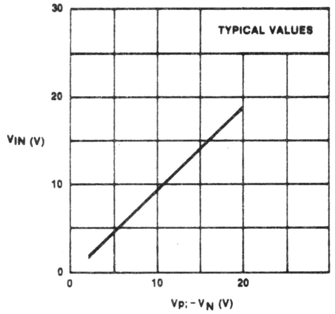
OUTPUT SHORT-CIRCUIT CURRENT



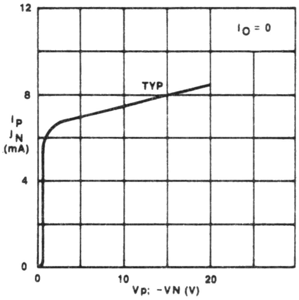
INPUT BIAS CURRENT



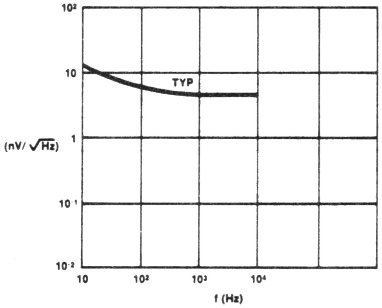
INPUT COMMON MODE VOLTAGE RANGE



SUPPLY CURRENT



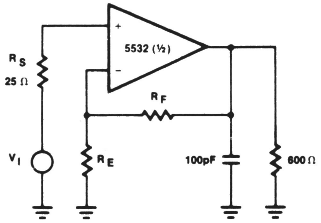
INPUT NOISE VOLTAGE DENSITY



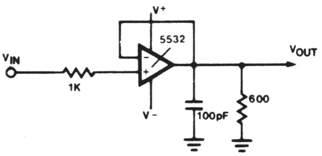
INTERNALLY COMPENSATED DUAL LOW NOISE OP AMP SE/NE5532/5532A

TEST CIRCUITS

CLOSED LOOP FREQUENCY RESPONSE



VOLTAGE FOLLOWER



AUDIO CIRCUITS USING THE NE5532/33/34

More detailed information is available in the communications section of this manual, regarding other audio circuits. The following will explain the Signetics line of low noise op amps and show their use in some audio applications.

DESCRIPTION

The 5532 is a dual high-performance low noise operational amplifier. Compared to most of the standard operational amplifiers, such as the 1458, it shows better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

This makes the device especially suitable for application in high quality and professional audio equipment, instrumentation and control circuits, and telephone channel amplifiers. The op amp is internally compensated for gains equal to one. If very low noise is of prime importance, it is recommended that the 5532A version be used which has guaranteed noise voltage specifications.

APPLICATIONS

The Signetics 5532 High Performance Op Amp is an ideal amplifier for use in high quality and professional audio equipment which requires low noise and low distortion.

The circuit included in this application note has been assembled on a P.C. board, and tested with actual audio input devices (Tuner and Turntable). It consists of an RIAA pre-amp, input buffer, 5-band equalizer, and mixer. Although the circuit design is not new, its performance using the 5532 has been improved.

The RIAA pre-amp section is a standard compensation configuration with low frequency boost provided by the Magnetic cartridge and the RC network in the op amp feedback loop. Cartridge loading is accomplished via R1. 47k was chosen as a typical value, and may differ from cartridge to cartridge.

The Equalizer section consists of an input buffer, 5 active variable band pass/notch (depending on R9's setting) filters, and an output summing amplifier. The input buffer is a standard unity gain design providing impedance matching between the pre amplifiers and the equalizer section. Because the 5532 is internally compensated, no external compensation is required. The 5-band active filter section is actually 5 individual active filters with the same feedback design for all 5. The main differance in all five stages is the values of C5 and C6 which are responsible for setting the center frequency of each stage. Linear pots are recommended for R9. To simplify use of this circuit, a component value table is provided, which lists center frequencies and their associated capacitor values. Notice that C5 equals (10) C6, and that the Value of R8 and R10 are related to R9 by a factor of 10 as well. The values listed in the table are common and easily found standard values.

RIAA EQUALIZATION AUDIO PREAMPLIFIER USING NE5532A

With the onset of new recording techniques along with sophisticated playback equipment, a new breed of low noise operational amplifiers was developed to complement the state-of-the-art in audio reproduction. The first ultra low noise op amp introduced by Signetics was called the NE5534A. This is a single operational amplifier with less than $4nV/\sqrt{Hz}$ input noise voltage. The NE5534A is internally compensated at a gain of three. This device has been used in many audio preamp and equalizer (active filter) applications since its introduction early last year.

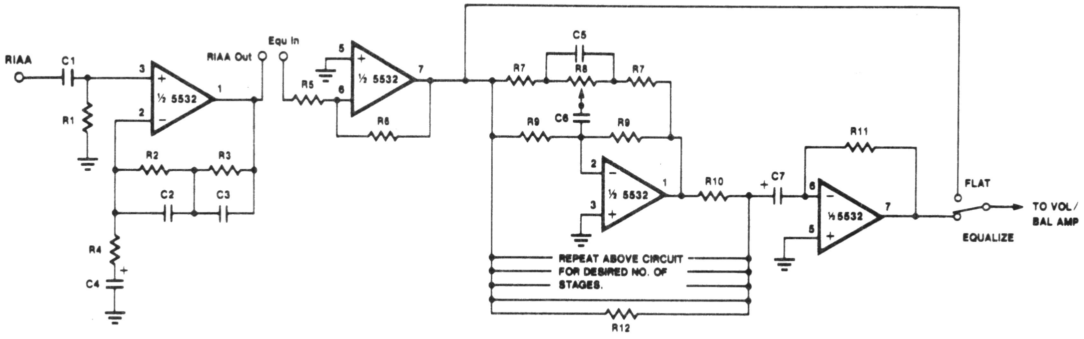
Many of the amplifiers that are being designed today are dc coupled. This means that very low frequencies (2-15Hz) are being amplified. These low frequencies are common to turntables because of rumble and tone arm resonancies. Since the amplifiers can reproduce these sub-audible tones, they become quite objectionable because the speakers try to reproduce these tones. This causes non-linearities when the actual recorded material is amplified and converted to sound waves.

The RIAA has proposed a change in its standard playback response curve in order to alleviate some of the problems that were previously discussed. The changes occur primarily at the low frequency range with a slight modification to the high frequency range. (See Figure 2). Note that the response peak for the bass section of the playback curve now occurs at 31.5Hz and begins to roll off below that frequency. The rolloff occurs by introducing a fourth R/C network occurs by introducing a fourth R/C network with a $7950\mu s$ time constant to the three existing networks that make up the equalization circuit. The high end of the equalization curve is extended to 20kHz, because recordings at these frequencies are achievable on many current discs.

NE5533/34 DESCRIPTION

The 5533/5534 are dual and single high-performance low noise operational amplifiers. Compared to other operational amplifiers

RIAA—EQUALIZER SCHEMATIC



COMPONENT VALUE TABLES

R8 = 25k R7 = 2.4k R9 = 240k			R8 = 50k R7 = 5.1k R9 = 510k			R8 = 100k R7 = 10k R9 = 1meg		
fo	C5	C6	fo	C5	C6	fo	C5	C6
23 Hz	1μF	.1μF	25 Hz	.47μF	.047μF	12 Hz	.47μF	.047μF
50 Hz	.47μF	.047μF	36 Hz	.33μF	.033μF	18 Hz	.33μF	.033μF
72 Hz	.33μF	.033μF	54 Hz	.22μF	.022μF	27 Hz	.22μF	.022μF
108 Hz	.22μF	.022μF	79 Hz	.15μF	.015μF	39 Hz	.15μF	.015μF
158 Hz	.15μF	.015μF	119 Hz	.1μF	.01μF	59 Hz	.1μF	.01μF
238 Hz	.1μF	.01μF	145 Hz	.082μF	.0082μF	72 Hz	.082μF	.0082μF
290 Hz	.082μF	.0082μF	175 Hz	.068μF	.0068μF	87 Hz	.068μF	.0068μF
350 Hz	.068μF	.0068μF	212 Hz	.056μF	.0056μF	106 Hz	.056μF	.0056μF
425 Hz	.056μF	.0056μF	253 Hz	.047μF	.0047μF	126 Hz	.047μF	.0047μF
506 Hz	.047μF	.0047μF	360 Hz	.033μF	.0033μF	180 Hz	.033μF	.0033μF
721 Hz	.033μF	.0033μF	541 Hz	.022μF	.0022μF	270 Hz	.022μF	.0022μF
1082 Hz	.022μF	.0022μF	794 Hz	.015μF	.0015μF	397 Hz	.015μF	.0015μF
1588 Hz	.015μF	.0015μF	1191 Hz	.01μF	.001μF	595 Hz	.01μF	.001μF
2382 Hz	.01μF	.001μF	1452 Hz	.0082μF	820pF	726 Hz	.0082μF	820pF
2904 Hz	.0082μF	820pF	1751 Hz	.0068μF	680pF	875 Hz	.0068μF	680pF
3502 Hz	.0068μF	680pF	2126 Hz	.0056μF	560pF	1063 Hz	.0056μF	560pF
4253 Hz	.0056μF	560pF	2534 Hz	.0047μF	470pF	1267 Hz	.0047μF	470pF
5068 Hz	.0047μF	470pF	3609 Hz	.0033μF	330pF	1804 Hz	.0033μF	330pF
7218 Hz	.0033μF	330pF	5413 Hz	.0022μF	220pF	2706 Hz	.0022μF	220pF
10827 Hz	.0022μF	220pF	7940 Hz	.0015μF	150pF	3970 Hz	.0015μF	150pF
15880 Hz	.0015μF	150pF	11910 Hz	.001μF	100pF	5955 Hz	.001μF	100pF
23820 Hz	.001μF	100pF	14524 Hz	820pF	82pF	7262 Hz	820pF	82pF
			17514 Hz	680pF	68pF	8757 Hz	680pF	68pF
			21267 Hz	560pF	56pF	10633 Hz	560pF	56pF
						12670 Hz	470pF	47pF
						18045 Hz	330pF	33pF

COMPONENT VALUES

R1	1meg	C1	.22μF
R2	100k	C2	750pF
R3	1meg	C3	.0033μF
R4	1.1k	C4	33μF
R5	100k	C5	SEE TABLE
R6	100k	C6	SEE TABLE
R7	SEE TABLE	C7	2.2μF
R8	(pot) SEE TABLE		
R9	SEE TABLE		
R10	100k		
R11	100k		
R12	20k (5 STAGES)		

Figure 1

such as TL083, they show better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

This makes the devices especially suitable for application in high quality and professional audio equipment, in instrumentation and control circuits and telephone channel amplifiers. The op amps are internally compensated for gain equal to, or higher than, three. The frequency response can be optimized with an external compensation capacitor for various applications (unity gain amplifier, capacitive load, slew-rate, low overshoot, etc.) If very low noise is of prime importance, it is recommended that the 5533A/5534A version be used which has guaranteed noise specifications.

APPLICATIONS

Diode Protection of Input

The input leads of the device are protected from differential transients above ±0.6V by internal back-to-back diodes. Their presence imposes certain limitations on the amplifier dynamic characteristics related to closed-loop gain and slew rate.

INTERNALLY COMPENSATED DUAL LOW NOISE OP AMP SE/NE5532/5532A

PROPOSED RIAA PLAYBACK EQUALIZATION

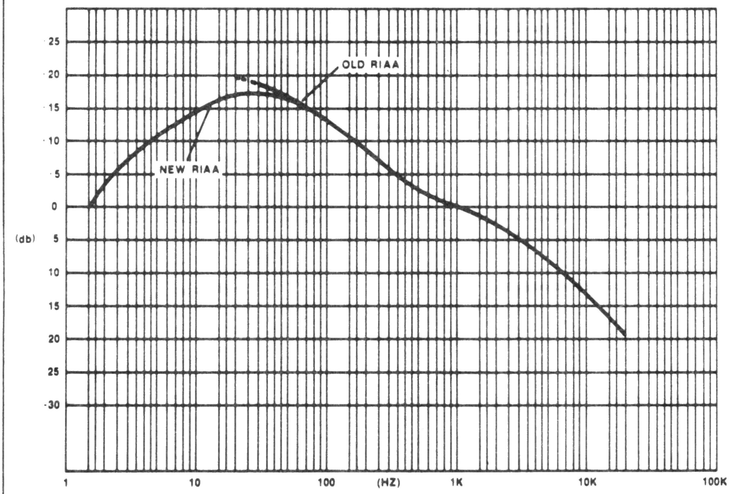
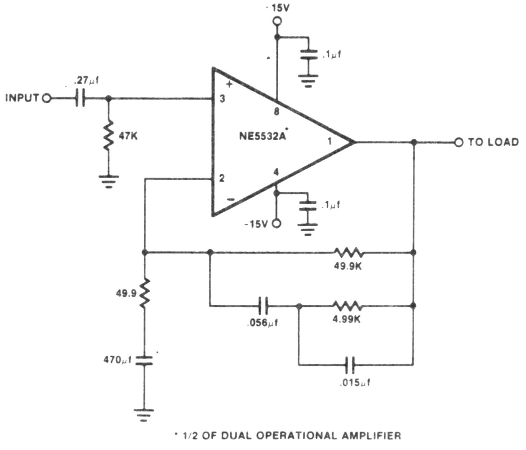


Figure 2

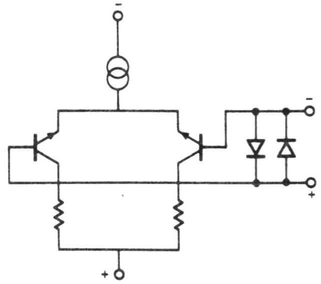
RIAA PHONOGRAPH PREAMPLIFIER USING THE NE5532A


+15V
.1µf
.27µf
INPUT
47K
+
3
8
NE5532A*
1
TO LOAD
2
4
−
.1µf
-15V
49.9K
49.9
.056µf
4.99K
470µf
.015µf

* 1/2 OF DUAL OPERATIONAL AMPLIFIER

NOTE
All resistors are 1% metal film and are valued in

Figure 3

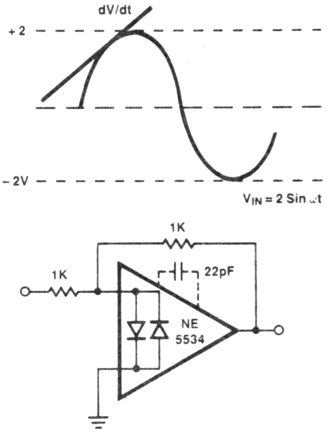


Consider the unity gain follower as an example:

Assume a signal input square wave with dV/dt of 250V per µs and 2V peak amplitude as shown. If a 22 pF compensation capacitor is inserted and the R_1 C_1 circuit deleted, the device slew rate falls to approximately 7V/µs. The input waveform will reach 2V/250V/µs or 8 ns, while the output will have changed (8×10^{-3}) (7) only 56 mV. The differential input signal is then $(V_{IN} - V_O)\ R_i/R_i + R_f$ or approximately 1V.

The diode limiter will definitely be active and output distortion will occur; therefore, $V_{in} < 1V$ as indicated.

Next, a sine wave input is used with a similar circuit.


dV/dt
+2
−2V
$V_{IN} = 2 \text{ Sin } \omega t$
1K
1K
22pF
NE
5534

The slew rate of the input waveform now depends on frequency and the exact expression is

$$\frac{dv}{dt} = 2\omega \cos \omega t$$

The upper limit before slew rate distortion occurs for *small signal* ($V_{IN} < 100$ mV) conditions is found by setting the slew rate to 7V/μs. That is:

$$7 \times 10^6 \text{ V}/\mu\text{s} = 2\omega \cos \omega t$$

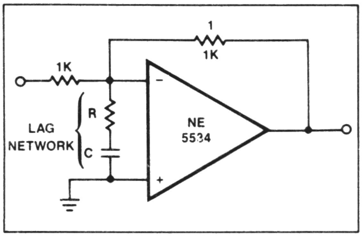
at $\omega t = 0$

$$\omega_{LIMIT} = \frac{7 \times 10^6}{2} = 3.5 \times 10^6 \text{ rad/s}$$

$$f_{LIMIT} \frac{3.5 \times 10^6}{2\pi} \cong 560 \text{ kHz}$$

External Compensation Network Improves Bandwidth

By using an external lead-lag network, the follower circuit slew rate and small signal bandwidth can be increased. This may be useful in situations where a closed-loop gain less than 3 to 5 is indicated. A number of examples are shown in subsequent figures. The principle benefit of using the network approach is that the full slew rate and bandwidth of the device is retained, while impulse-related parameters such as damping and phase margin are controlled by choosing the appropriate circuit constants. For example, consider the following configuration:



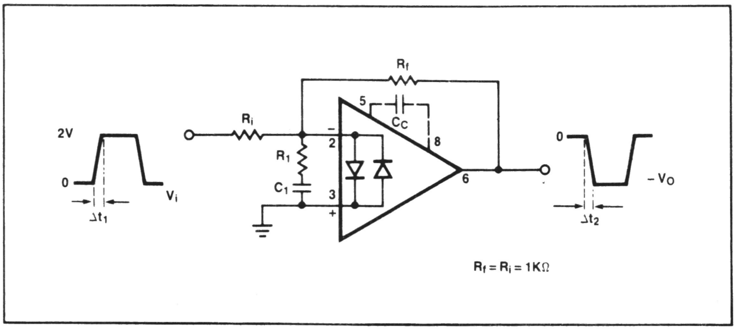
The major problem to be overcome is poor phase margin leading to instability.

By choosing the lag network break frequency one decade below the unity gain crossover frequency (30-50 MHz), the phase and gain margin are improved. An appropriate value for R is 270Ω. Setting the lag network break frequency at 5 MHz, C may be calculated

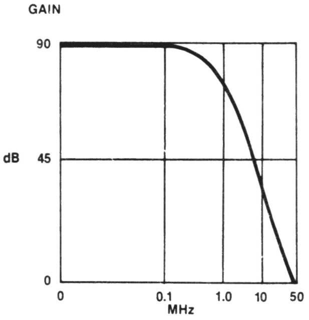
$$C = \frac{1}{2\pi \cdot 270 \cdot 5 \times 10^6}$$

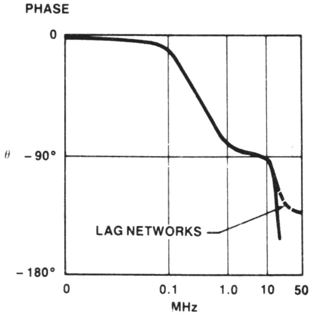
$$118 = \text{pF}$$

A single pole and zero inserted in the transfer function will give an added 45° of phase margin depending on the network values.



$R_f = R_i = 1K\Omega$

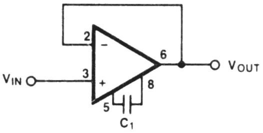




RULES AND EXAMPLES

Compensation Using Pins 5 and 8

(Limited Bandwidth and Slew Rate)

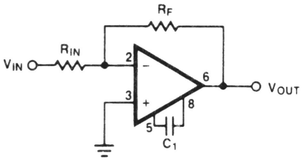


$C_1 = C_C$ (1)

$C_C = 22$pF for NE5533/34

∴ $C_1 = 22$pF [SEE GRAPH UNDER TYPICAL PERFORMANCE CHARACTERISTICS]

Figure 4. Unity Gain Non-Inverting Configuration



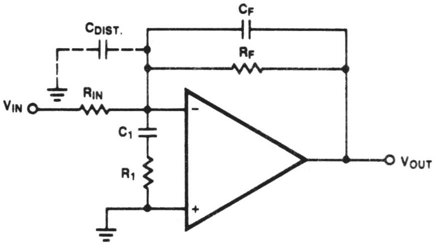
$R_F = R_{IN}$

$$C_1 = C_C\left[\frac{R_{IN}}{R_F + R_{IN}}\right] = \frac{C_C}{2}$$

∴ $C_1 = 11$pF

Figure 5. Unity Gain Inverting Configuration

External Compensation for Wideband Voltage Follower



NOTE: Input diodes limit differential to < 0.5V

Figure 6 . External Compensation for Wideband Voltage Follower

Calculating the Lead-Lag Network

$$C_1 = \frac{1}{2\pi F_1 R_1} \qquad \text{Let } R_1 = \frac{R_{IN}}{10}$$

where $F_1 = \frac{1}{10}(\text{UGBW})$

$\text{UGBW} = 30\text{ MHz}$

Shunt Capacitance Compensation

$$C_F = \frac{1}{2\pi F_F R_F},\ F_F \cong 30\text{ MHz}$$

or $C_F \cong \frac{C_{DIST}}{A_{CL}}$

C_{DIST} ≅ Distributed Capacitance ≅ 2-3pF

Many audio circuits involve carefully tailored frequency responses. Pre-emphasis is used in all recording mediums to reduce noise and produce flat frequency response. The most often used de-emphasis curves for broadcast and home entertainment systems are shown in Figure 7. Operational amplifiers are well suited to these applications because of their high gain and easily tailored frequency response.

RIAA EQUALIZATION

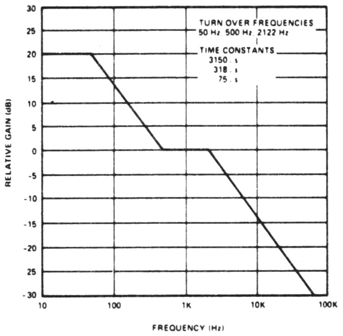


Figure 7a

NAB STANDARD PLAYBACK 7 1/2 IPS

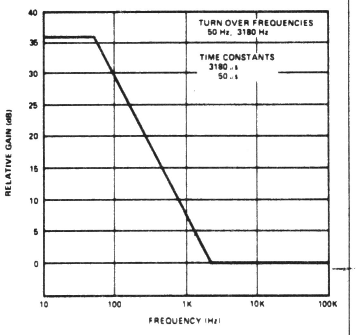


Figure 7b

3.75 IPS TAPE EQUALIZATION

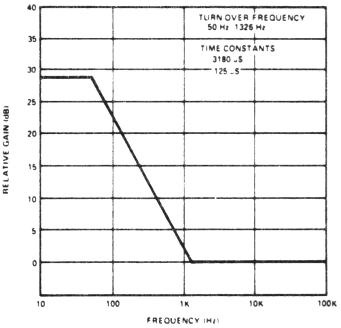


Figure 7c

BASE TREBLE CONTROL CURVE

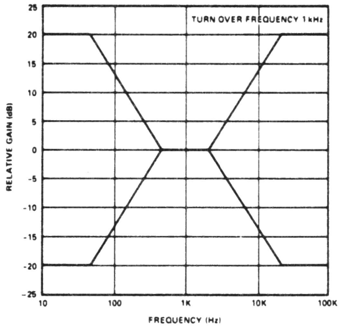


Figure 7d

STANDARD FM BROADCAST EQUALIZATION

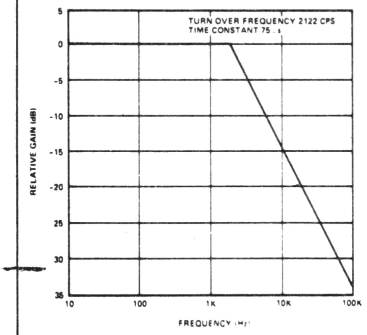


Figure 7e

RIAA PREAMP USING THE NE5534

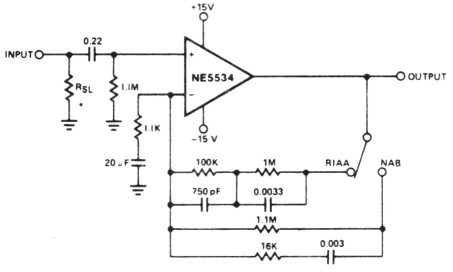
The preamplifier for phono equalization is shown in Figure 8 along with the theoretical and actual circuit response.

Low frequency boost is provided by the inductance of the magnetic cartridge with the RC network providing the necessary break points to approximate the theoretical RIAA curve.

RUMBLE FILTER

Following the amplifier stage, rumble and scratch filters are often used to improve overall quality. Such a filter designed with op amps uses the 2 pole Butterworth approach and features switchable break points. With the circuit of Figure 9 any degree of filtering from fairly sharp to none at all is switch selectable.

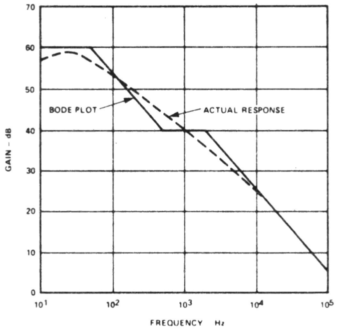
PREAMPLIFIER—RIAA/NAB COMPENSATION


+15V
INPUT
0.22
R_{SL}
*
1.1M
NE5534
OUTPUT
1.1K
−15 V
20 μF
100K
1M
RIAA
NAB
750 pF
0.0033
1.1M
16K
0.003

*Select to provide specified transducer loading.
Output Noise ~ 0.8mV rms (with input shorted)

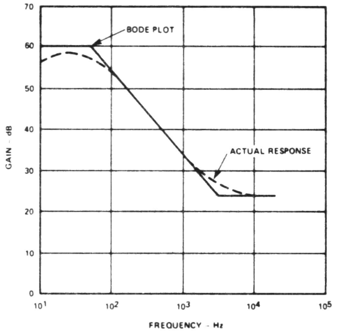
All resistor values are in ohms.

Figure 8a



Bode Plot of RIAA Equalization and the response realized in an actual circuit using the 531

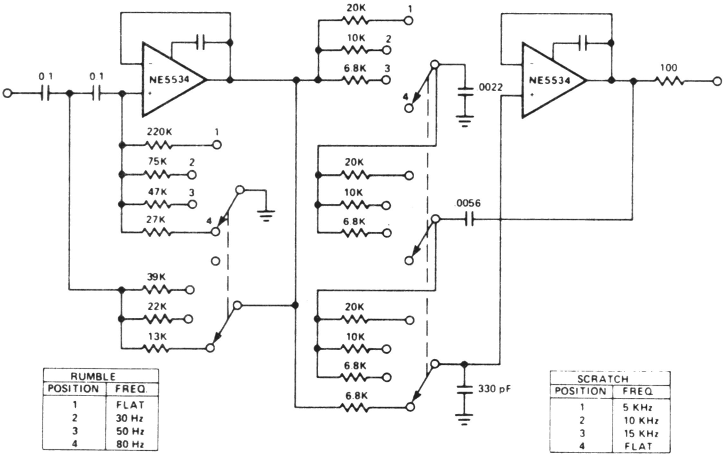
Figure 8b



Bode Plot of NAB Equalization and the response realized in the actual circuit using the 531

Figure 8c

RUMBLE/SCRATCH FILTER


0.1
0.1
NE5534
220K
1
75K
2
47K
3
27K
4
39K
22K
13K
20K
1
10K
2
6.8K
3
4
.0022
20K
10K
6.8K
.0056
20K
10K
6.8K
6.8K
330 pF
NE5534
100

RUMBLE	
POSITION	FREQ.
1	FLAT
2	30 Hz
3	50 Hz
4	80 Hz

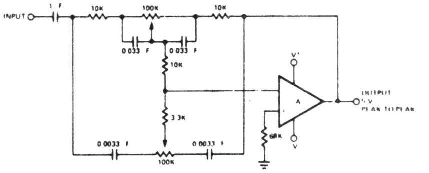
SCRATCH	
POSITION	FREQ.
1	5 KHz
2	10 KHz
3	15 KHz
4	FLAT

All resistor values are in ohms.

Figure 9

INTERNALLY COMPENSATED DUAL LOW NOISE OP AMP SE/NE5532/5532A

TONE CONTROL CIRCUIT FOR OPERATIONAL AMPLIFIERS


INPUT
1 F
10K
100K
10K
0 033 F
0 033 F
10K
V+
A
OUTPUT
5 V
PEAK TO PEAK
3 3K
68K
V-
0 0033 F
0 0033 F
100K

All resistor values are in ohms.

NOTES

1. Amplifier A may be a NE531 or 301. Frequency compensation, as for unity gain non-inverting amplifiers, must be used.
2. Turn-over frequency—1kHz.
3. Bass boost +20dB at 20Hz, bass cut -20dB at 20Hz, treble boost +19dB at 20kHz, treble cut -19dB at 20kHz.

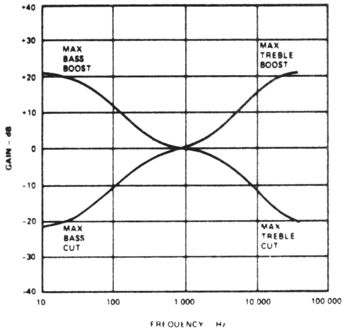


Figure 10

TONE CONTROL

Tone control of audio systems involves altering the flat response in order to attain more low frequencies or more high ones dependent upon listener preference. The circuit of Figure 10 provides 20dB of bass or treble boost or cut as set by the variable resistance. The actual response of the circuit is shown also.

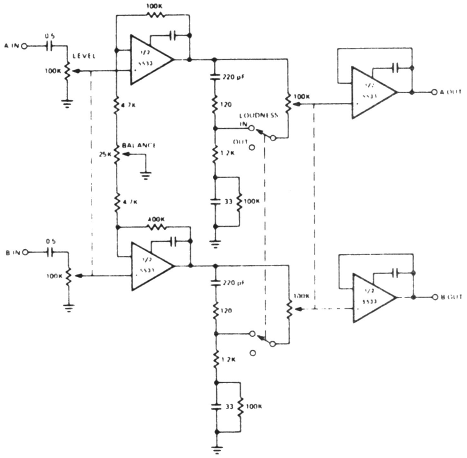
BALANCE AND LOUDNESS AMPLIFIER

Figure 11 shows a combination of balance and loudness controls. Due to the non-linearity of the human hearing system the low frequencies must be boosted at low listening levels. Balance, level, and loudness controls provide all the listening controls to produce the desired music response.

VOLTAGE AND CURRENT OFFSET ADJUSTMENTS

Many IC amplifiers include the necessary pin connections to provide external offset adjustments. Many times, however, it becomes necessary to select a device not possessing external adjustments. Figure 12, 13, and 14 suggest some possible arrangements for offset voltage adjust and bias current nulling circuitry. The circuitry of Figure 14 provides sufficient current into the input to cancel the bias current requirement. Although more simplified arrangements are possilb the addition of Q2 and Q3 provide a fixed current level to Q1, thus, bias cancellation can be provided without regard to input voltage level.

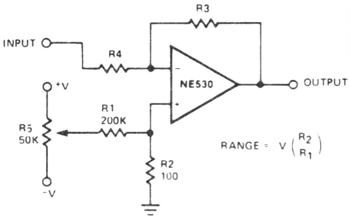
BALANCE AMPLIFIER WITH LOUDNESS CONTROL


100K
A IN
0 5
LEVEL
100K
1/2 5533
220 pF
4 7K
120
100K
LOUDNESS
IN
OUT
BALANCE
25K
1 2K
33
100K
4 7K
400K
A OUT
B IN
0 5
100K
1/2 5533
220 pF
120
100K
1 2K
33
100K
B OUT

All resistor values are in ohms.

Figure 11

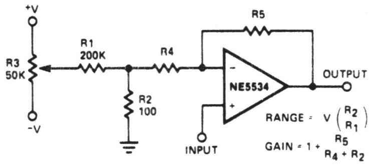
UNIVERSAL OFFSET NULL FOR INVERTING AMPLIFIERS


R3
INPUT
R4
+V
NE530
OUTPUT
R1
200K
R5
50K
RANGE = V (R2/R1)
R2
100
-V

All resistor values are in ohms.

Figure 12

UNIVERSAL OFFSET NULL FOR NONINVERTING AMPLIFIERS


+V
R3
50K
-V
R1
200K
R4
R5
R2
100
NE5534
OUTPUT
INPUT
RANGE = $V\left(\frac{R_2}{R_1}\right)$
GAIN = $1 + \frac{R_5}{R_4 + R_2}$

All resistor values are in ohms.

Figure 13

BIAS CURRENT COMPENSATION

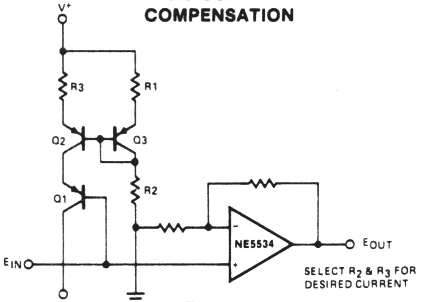

V+
R3
R1
Q2
Q3
R2
Q1
NE5534
E$_{IN}$
E$_{OUT}$
V-
SELECT R_2 & R_3 FOR DESIRED CURRENT

Figure 14

***For additional information, consult the Applications Section.**

SINGLE AND DUAL LOW NOISE OP AMP NE5533/5533A/SA/SE/NE5534/5534A

DESCRIPTION

The 5533/5534 are dual and single high-performance low noise operational amplifiers. Compared to other operational amplifiers, such as TL083, they show better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

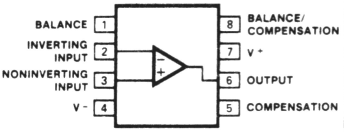
This makes the devices especially suitable for application in high quality and professional audio equipment, in instrumentation and control circuits and telephone channel amplifiers. The op amps are internally compensated for gain equal to, or higher than, three. The frequency response can be optimized with an external compensation capacitor for various applications (unity gain amplifier, capacitive load, slew-rate, low overshoot, etc.) If very low noise is of prime importance, it is recommended that the 5533A/5534A version be used which has guaranteed noise specifications.

FEATURES

- **Small-signal bandwidth: 10MHz**
- **Output drive capability: 600Ω, 10V (rms) at $V_S = \pm18V$**
- **Input noise voltage: 4nV/$\sqrt{Hz}$**
- **DC voltage gain: 100000**
- **AC voltage gain: 6000 at 10kHz**
- **Power bandwidth: 200kHz**
- **Slew-rate: 13V/μs**
- **Large supply voltage range: ±3 to ±20V**

PIN CONFIGURATIONS

D,FE,N PACKAGE

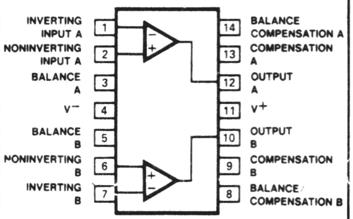

BALANCE
INVERTING INPUT
NONINVERTING INPUT
V -
1
2
3
4
8
7
6
5
BALANCE/ COMPENSATION
V +
OUTPUT
COMPENSATION
−
+

TOP VIEW

ORDER NUMBERS

SE/NE5534N,FE *NE5534AD SE/NE5534AN,FE
SA5534A NE5534D SA5534AN

N PACKAGE


INVERTING INPUT A
NONINVERTING INPUT A
BALANCE A
V−
BALANCE B
NONINVERTING B
INVERTING B
1
2
3
4
5
6
7
14
13
12
11
10
9
8
BALANCE COMPENSATION A
COMPENSATION A
OUTPUT A
V+
OUTPUT B
COMPENSATION B
BALANCE COMPENSATION B
−
+
+
−

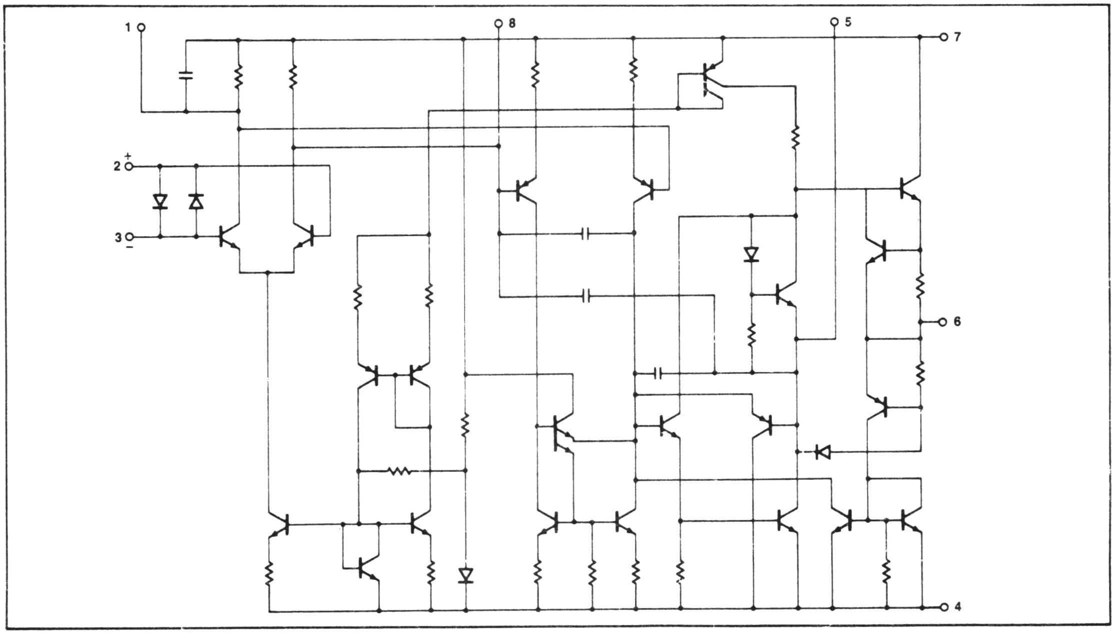
TOP VIEW

ORDER NUMBERS

NE5533N
NE5533AN

*NOTE:
This device may not be symbolled in standard format.

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_S	Supply voltage	± 22	V
V_{IN}	Input voltage	± V supply	V
V_{DIFF}	Differential input voltage[1]	± 0.5	V
T_A	Operating temperature range		
	SE5534/5534A	− 55 to + 125	°C
	NE5533/5533A/5534/5534A	0 to + 70	°C
T_{STG}	Storage temperature	− 65 to + 150	°C
T_J	Junction temperature	150	°C
P_D	Power dissipation at 25°C[2]		
	5533N, 5534N, 5534FE	800	mW
	Output short circuit duration[3]	Indefinite	
	Lead temperature (soldering, 10 sec)	300	°C

NOTES

1. Diodes protect the inputs against over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ±10mA.
2. For operation at elevated temperature, derate packages based on the following junction-to-ambient thermal resistances:
   8-pin ceramic (FE) 140°C/W
   14-pin ceramic (F) 110°C/W
   8-pin plastic (N) 162°C/W
   14-pin plastic (N) 150°C/W
3. Output may be shorted to ground at V_S = ±15V, T_A = 25°C. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.[1,2]

PARAMETER		TEST CONDITIONS	SE5534/5534A			NE5533/5533A 5534/5534A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage			0.5	2		0.5	4	mV
		Over temperature			3			5	mV
$\Delta V_{OS}/\Delta T$				5			5		μV/°C
I_{OS}	Offset current			10	200		20	300	nA
		Over temperature			500			400	nA
$\Delta I_{OS}/\Delta T$				200			200		pA/°C
I_B	Input current			400	800		500	1500	nA
		Over temperature			1500			2000	nA
$\Delta I_B/\Delta T$				5			5		nA/°C
I_{CC}	Supply current Per op amp			4	6.5		4	8	mA
		Over temperature			9			10	mA
V_{CM}	Common mode input range		± 12	± 13		± 12	± 13		V
CMRR	Common mode rejection ratio		80	100		70	100		dB
PSRR	Power supply rejection ratio			10	50		10	100	μV/V
A_{VOL}	Large signal voltage gain	$R_L \geq 600\Omega$, $V_O = \pm 10V$	50	100		25	100		V/mV
		Over temperature	25			15			V/mV
V_{OUT}	Output swing 5534 only	$R_L \geq 600\Omega$	± 12	± 13		± 12	± 13		V
		Over temperature	± 10	± 12		± 10	± 12		V
		$R_L \geq 600\Omega$, $V_S = \pm 18V$	± 15	± 16		± 15	± 16		V
		$R_L \geq 2k\Omega$	± 13	± 13.5		± 13	± 13.5		V
		Over Temperature	± 12	± 12.5		± 12	± 12.5		V
R_{IN}	Input resistance		50	100		30	100		kΩ
I_{SC}	Output short circuit current			38			38		mA

NOTES

1. For NE5533/5533A/5534/5534A, $T_{MIN} = 0°C$, $T_{MAX} = 70°C$
2. For SE5534/5534A, $T_{MIN} = -55°C$, $T_{MAX} = +125°C$

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_S = ±15V unless otherwise specified.

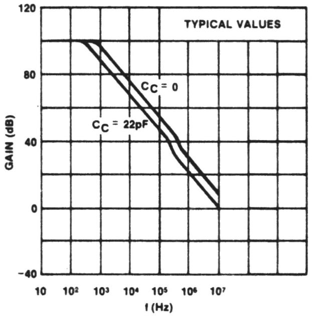
PARAMETER		TEST CONDITIONS	SE5534/5534A			NE5533/5533A 5534/5534A			UNIT
			Min	Typ	Max	Min	Typ	Max	
R_{OUT}	Output resistance	A_V = 30dB closed loop f = 10kHz, R_L = 600Ω, C_C = 22pF		0.3			0.3		Ω
Transient response		Voltage follower, V_{IN} = 50mV R_L = 600Ω, C_C = 22pF, C_L = 100pF							
T_R	Rise time			20			20		ns
	Overshoot			20			20		%
Transient response		V_{IN} = 50mv, R_L = 600Ω C_C = 47pF, C_L = 500pF							
T_R	Rise time			50			50		ns
	Overshoot			35			35		%
AC	Gain	f = 10kHz, C_C = 0		6			6		V/mV
		f = 10kHz, C_C = 22pF		2.2			2.2		V/mV
	Gain bandwidth product	C_C = 22pF, C_L = 100pF		10			10		mHz
	Slew rate	C_C = 0		13			13		V/μS
		C_C = 22pF		6			6		V/μS
	Power bandwidth	V_{OUT} = ±10V, C_C = 0		200			200		kHz
		V_{OUT} = ±10V, C_C = 22pF		95			95		kHz
		V_{OUT} = ±14V, R_L = 600Ω C_C = 22pF, V_{CC} = ±18V		70			70		kHz

ELECTRICAL CHARACTERISTICS T_A = 25°C, V_S = ±15V unless otherwise specified.

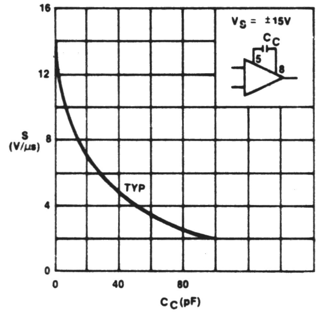
PARAMETER	TEST CONDITIONS	5533/5534			5533A/5534A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input noise voltage	f_O = 30Hz		7			5.5	7	nV/√Hz
	f_O = 1kHz		4			3.5	4.5	nV/√Hz
Input noise current	f_O = 30Hz		2.5			1.5		pA/√Hz
	f_O = 1kHz		0.6			0.4		pA/√Hz
Broadband noise figure	f = 10Hz – 20kHz, R_S = 5kΩ					0.9		dB
Channel separation	f = 1kHz, R_S = 5kΩ		110			110		dB

TYPICAL PERFORMANCE CHARACTERISTICS

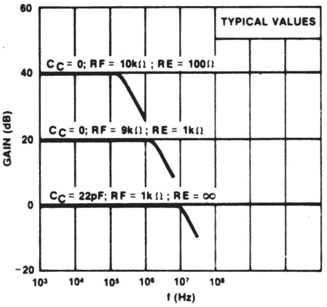
OPEN LOOP FREQUENCY RESPONSE



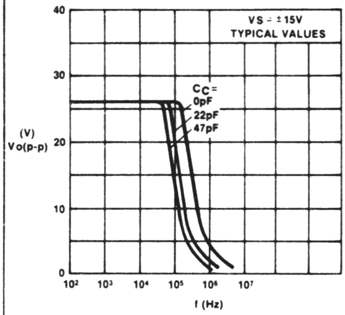
SLEW-RATE AS A FUNCTION OF COMPENSATION CAPACITANCE



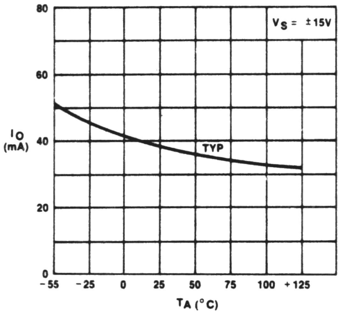
CLOSED LOOP FREQUENCY RESPONSE



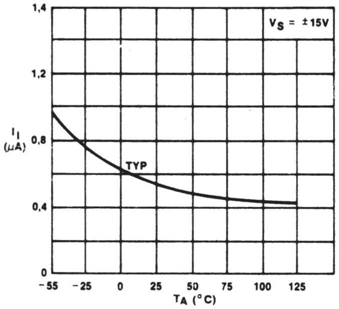
LARGE-SIGNAL FREQUENCY RESPONSE



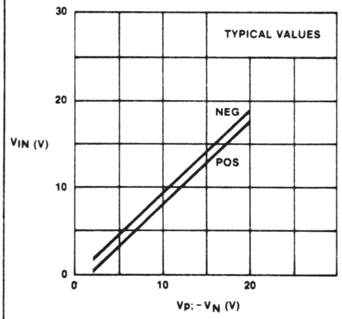
OUTPUT SHORT-CIRCUIT CURRENT



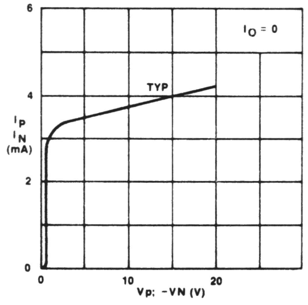
INPUT BIAS CURRENT



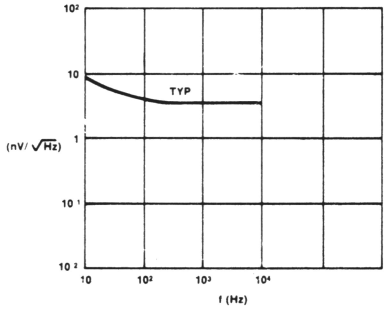
INPUT COMMON MODE VOLTAGE RANGE



SUPPLY CURRENT PER OP AMP

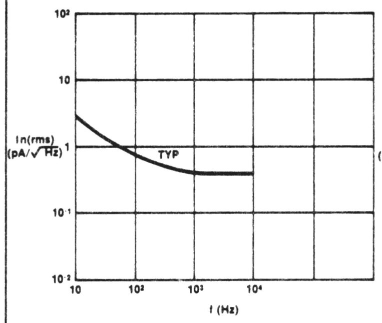


INPUT NOISE VOLTAGE DENSITY

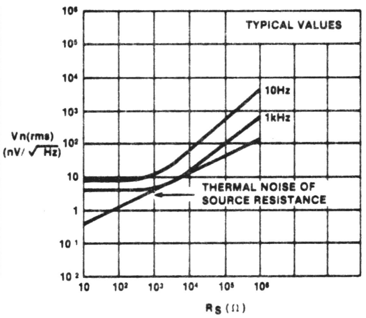


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

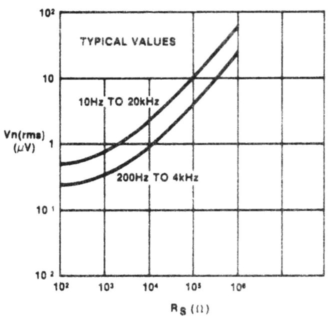
INPUT NOISE CURRENT DENSITY



TOTAL INPUT NOISE DENSITY

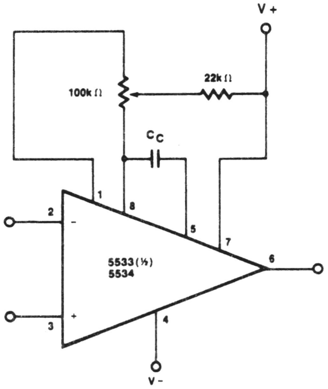


BROADBAND INPUT NOISE VOLTAGE

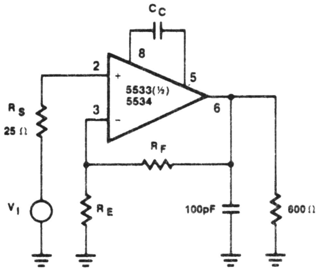


TEST LOAD CIRCUITS

FREQUENCY COMPENSATION AND OFFSET VOLTAGE ADJUSTMENT CIRCUIT

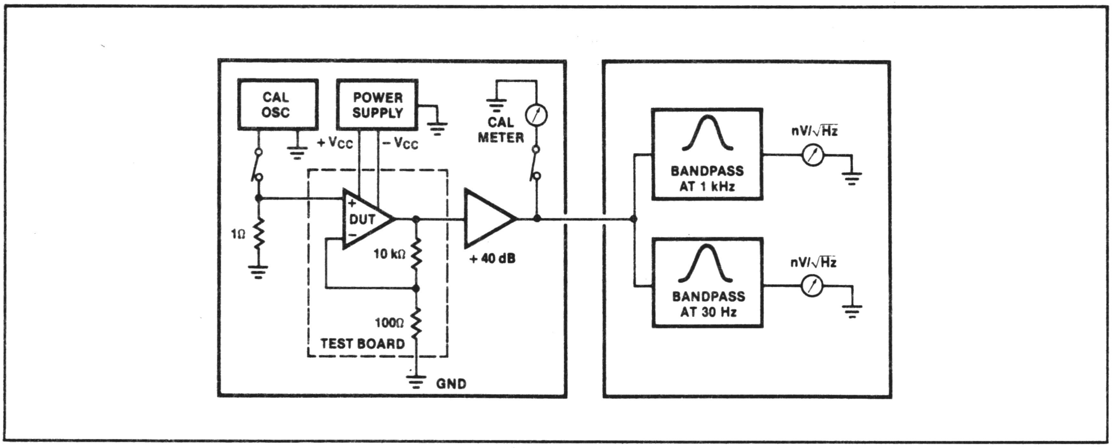

V +
100k Ω
22k Ω
C_C
1
8
5
7
6
2
3
4
−
+
5533(½)
5534
V −

CLOSED LOOP FREQUENCY RESPONSE


C_C
8
2
5
3
6
+
−
5533(½)
5534
R_S
25 Ω
R_F
V_I
R_E
100pF
600 Ω

SINGLE AND DUAL LOW NOISE OP AMP NE5533/5533A/SA/SE/NE5534/5534A

NOISE TEST BLOCK DIAGRAM


CAL OSC
POWER SUPPLY
+Vcc
−Vcc
CAL METER
1Ω
+
DUT
−
10 kΩ
100Ω
TEST BOARD
GND
+40 dB
BANDPASS AT 1 kHz
BANDPASS AT 30 Hz
nV/√Hz
nV/√Hz

*For additional information, consult the Applications Section.

DUAL HIGH SLEW RATE OP AMP

SE/NE5535

DESCRIPTION

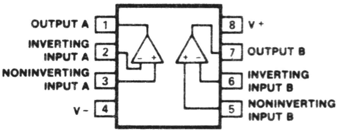
The 5535 is a new generation operational amplifier featuring high slew rates combined with improved input characteristics. The 5535 is a dual configuration. Internally compensated for unity gain, the SE5535 features a guaranteed unity gain slew rate of 10V/μs with 2mV maximum offset voltage. Industry standard pin out and internal compensation allow the user to upgrade system performance by directly replacing general purpose amplifiers, such as 747 and 1558.

FEATURES

- **15V/μs unity gain slew rate**
- **Internal frequency compensation**
- **Low input offset voltage—2mV**
- **Low input bias current 80nA max**
- **Short circuit protected**
- **Large common mode and differential voltage ranges**
- **Pin compatibility** **5535** / **747,1558**
- **Configuration** **Dual**
- **Low noise current 0.15 pA/$\sqrt{Hz}$ typ.**

PIN CONFIGURATIONS

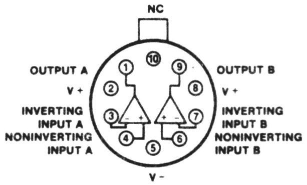
N PACKAGE


OUTPUT A
1
INVERTING INPUT A
2
NONINVERTING INPUT A
3
V-
4
8
V+
7
OUTPUT B
6
INVERTING INPUT B
5
NONINVERTING INPUT B

TOP VIEW

ORDER NUMBERS
SE5535N NE5535N

H PACKAGE*


NC
OUTPUT A
V+
INVERTING INPUT A
NONINVERTING INPUT A
1
2
3
4
5
6
7
8
9
10
OUTPUT B
V+
INVERTING INPUT B
NONINVERTING INPUT B
V-

ORDER NUMBERS
SE5535H NE5535H

*Metal cans (H) not recommended for new designs

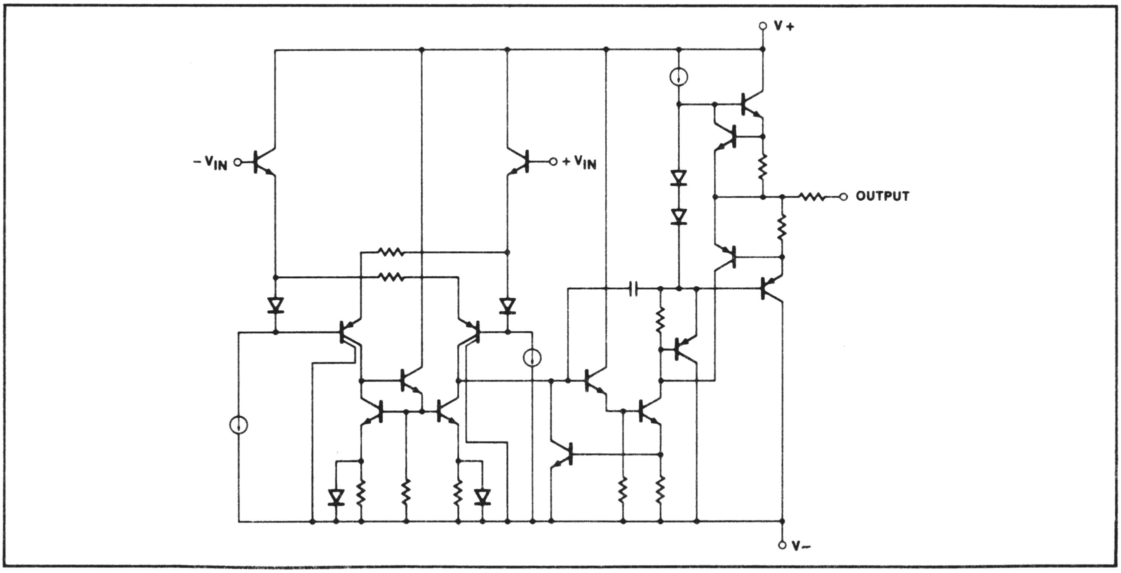
ABSOLUTE MAXIMUM RATINGS

PARAMETER	SE5535	NE5535	UNIT
Supply voltage	±22	±18	V
Internal power dissipation[1]			
N Package	500	500	mW
H Package	800	800	mW
F Package	1000	1000	mW
Differential input voltage	±30	±30	V
Input voltage[2]	±15	±15	V
Operating temperature range	-55 to +125	0 to +70	°C
Storage temperature range	-65 to +150	-65 to +150	°C
Lead temperature (solder, 60sec)	300	300	°C
Output short circuit[3]	Indefinite	Indefinite	

NOTES

1. Rating applies for thermal resistances junction to ambient of 240°C/W and 150°C/W for N and H packages, respectively. Maximum chip temperature is 150°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

EQUIVALENT SCHEMATIC (One Amplifier)


V+
$-V_{IN}$
$+V_{IN}$
OUTPUT
V–

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.*

PARAMETER		TEST CONDITIONS	SE5535			NE5535			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S \leq 10k\Omega$		0.7	4.0		2.0	6.0	mV
		$R_S \leq 10k\Omega$, over temp.			5.0			7.0	mV
ΔV_{OS}	Input offset voltage drift	$R_S = 0\Omega$, over temp.		4.0			6.0		μV/°C
I_{OS}	Input offset current			5	20		15	40	nA
		Over temp.			40			80	VnA
ΔI_{OS}	Input offset current	Over temp.		25			40		pA/°C
I_B	Input current			45	80		65	150	nA
		Over temp.			200			200	nA
ΔI_B	Input current	Over temp.		50			80		pA/°C
V_{CM}	Common mode voltage range		±12	±13		±12	±13		V
CMRR	Common mode rejection ratio	$R_S \leq 10k\Omega$, over temp.	70	90		70	90		dB
PSRR	Power supply rejection	$R_S \leq 10k\Omega$, over temp.		30	150		30	150	μV/V
R_{IN}	Input resistance		3	10		1	6		MΩ
A_{VOL}	Large signal voltage gain	$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	50	500		50	500		V/mV
		$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$, over temp.	25			25			V/mV
V_{OUT}	Output voltage	$R_L \geq 2k\Omega$, over temp.	±10	±13		±10	±13		V
		$R_L \geq 10k\Omega$, over temp.	±12	±14		±12	±14		V
I_{CC}	Supply current	Per amplifier		1.8	2.8		1.8	2.8	mA
		Per amplifier, over temp.		2	3.3		2		mA
P_D	Power dissipation	Per amplifier		54	84		54	84	mW
		Per amplifier, over temp.		60	99		60		mW
I_{SC}	Output short circuit current		10	25	50	10	25	50	mA
R_{OUT}	Output resistance			100			100		Ω

*NOTE

Temperature range

SE types $-55°C \leq T_A \leq 125°C$

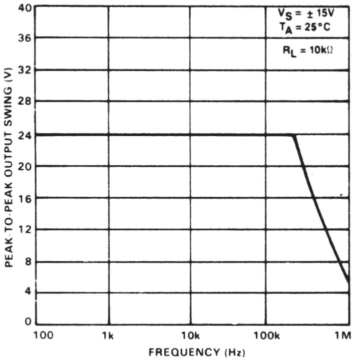
NE types $0°C \leq T_A \leq 70°C$

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.

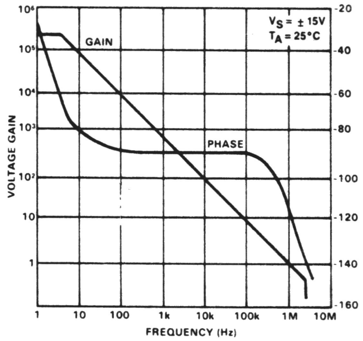
PARAMETER	TEST CONDITIONS	SE5535			NE5535			UNIT
		Min	Typ	Max	Min	Typ	Max	
Gain/bandwidth product			1			1		MHz
Transient response								
Small signal rise time			0.25			0.25		μs
Small signal overshoot			6			6		%
Settling time	To 0.1%		3			3		μs
Slew rate	$R_L \geq 10k\Omega$, unity gain, non-inverting	10	15		10	15		V/μs
Input noise voltage	f = 1kHz, $T_A = 25°C$		30			30		nV/$\sqrt{Hz}$

TYPICAL PERFORMANCE CHARACTERISTICS

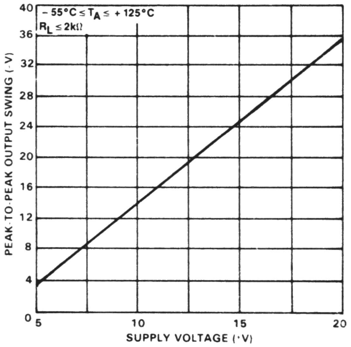
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



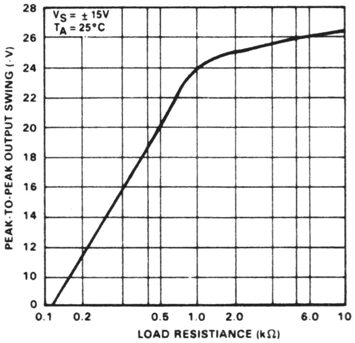
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



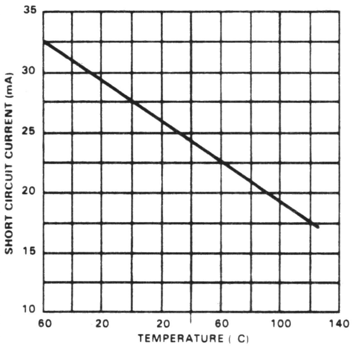
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

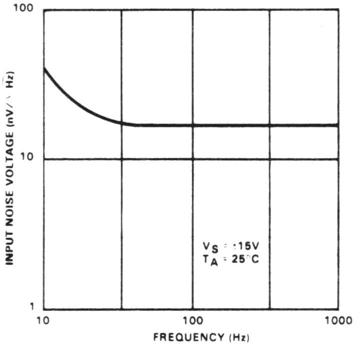


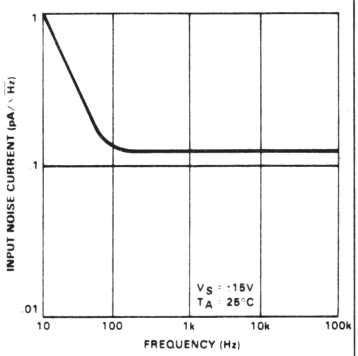
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

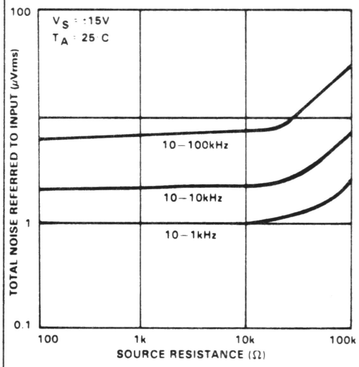


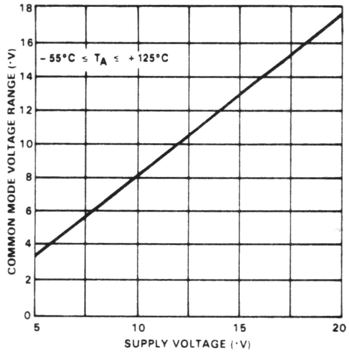
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

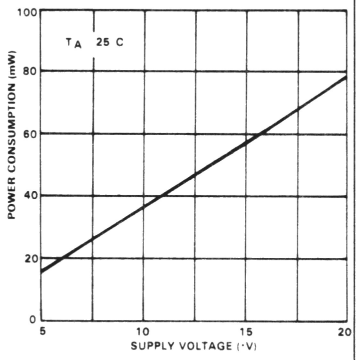

OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

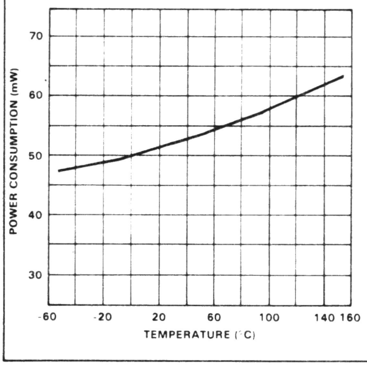

INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY

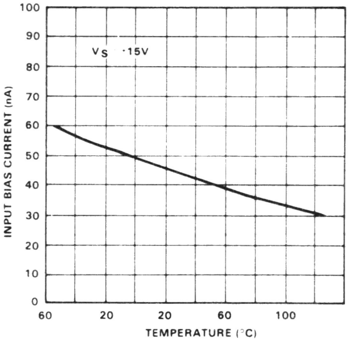

INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

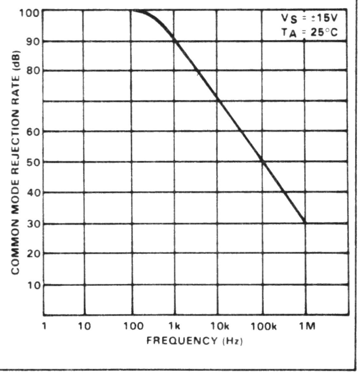

BROADBAND NOISE FOR VARIOUS BANDWIDTHS


INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE


POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE

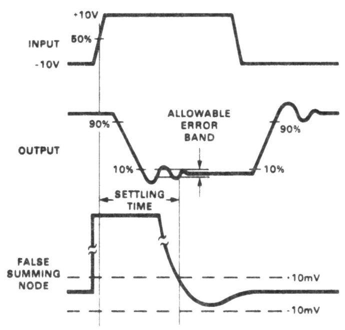

POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE


INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

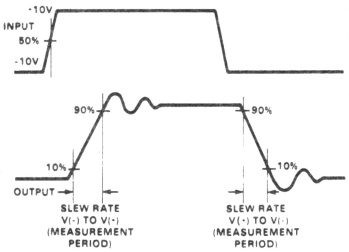

COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY

VOLTAGE WAVEFORMS

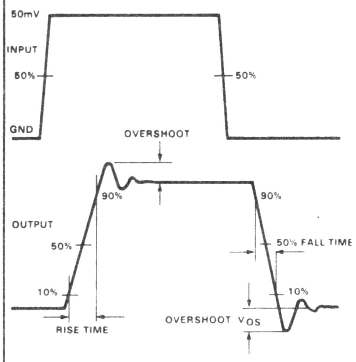
SETTLING TIME MEASUREMENT



SLEW RATE MEASUREMENT

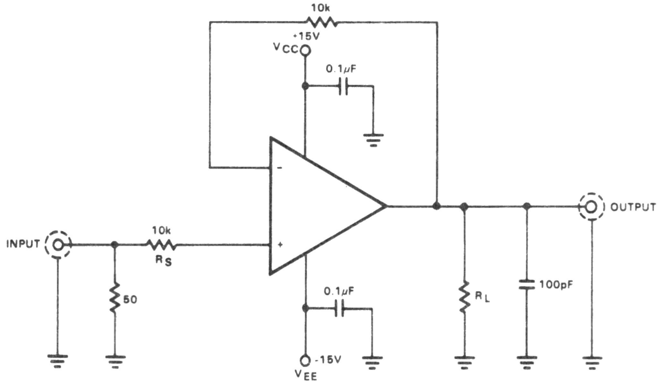


SMALL-SIGNAL TRANSIENT RESPONSE DEFINITIONS



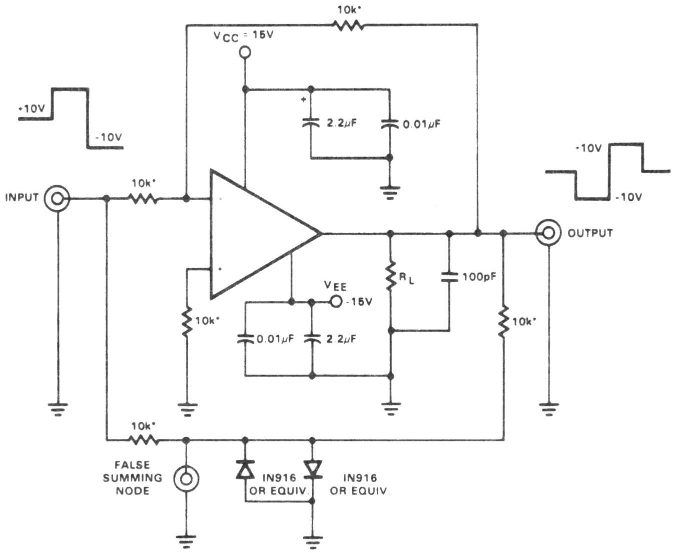
TEST CIRCUITS

SLEW RATE AND SMALL SIGNAL TRANSIENT RESPONSE


10k
+15V
VCC
0.1μF
INPUT
10k
RS
50
0.1μF
-15V
VEE
RL
100pF
OUTPUT

NOTE
Pins not shown are not connected.
All resistors values are typical and in ohms.

SETTLING TIME


10k*
VCC = 15V
+10V
-10V
2.2μF
0.01μF
+10V
-10V
INPUT
10k*
OUTPUT
VEE
-15V
RL
100pF
10k*
0.01μF
2.2μF
10k*
10k*
FALSE SUMMING NODE
IN916 OR EQUIV
IN916 OR EQUIV

*Match to within 0.01%.

NOTE

Pins not shown are not connected.
All resistors values are typical and in ohms.

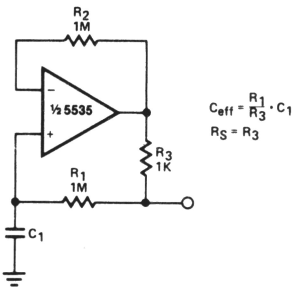
DUAL HIGH SLEW RATE OP AMP

SE/NE5535

APPLICATIONS

Introduction

The NE5535 is a new generation monolithic op amp which features improved input characterisics. The device is compensated to unity gain and has a minimum guaranteed unity gain slew rate of 10V/μs. This is achieved by employing a clamped super beta input stage which has lower input bias current.



All resistor values are in ohms.

Figure 1. Capacitance Multiplier

Applications

These improved parameters can be put to good use in applications such as sample and hold circuits which require low input current and in voltage follower circuits which require high slew rates. The circuit that follows will yield slew rates. The circuit that follows will yield maximum small signal transient response and slew rate for the NE5535 at unity gain.

It is always good practice in designing a system to use dual tracking regulators to power the dual supply op amps. This will guarantee the positive and negative supply voltage will be equal during power up. With the NE5535, it is possible to degrade the input circuit characteristics by not applying the power supplies simultaneously. The NE5535 is capable of directly replacing the μA741 with higher input resistance which will improve such designed as active filters, sample and hold, as well as voltage followers.

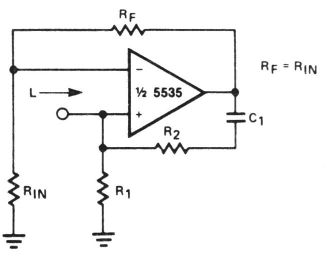


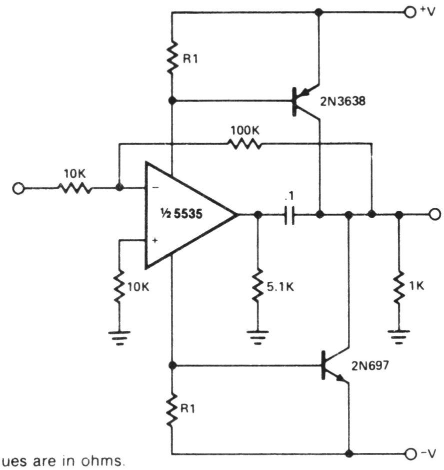
Figure 2. Virtual Inductor

The NE5535 can be used either with single or split power supplies.

APPLICATIONS

CAPACITANCE MULTIPLIER

The circuit in Figure 1 can be used to simulate large capacitances using small value components. With the values shown and C = 10μF, an effective capacitance of 10,000μF was obtained. The Q available is limited by the effective series resistance. So R1 should be as large as practical.



All resistor values are in ohms.

Figure 3. Power Booster

SIMULATED INDUCTOR

With a constant current excitation, the voltage dropped across an inductance increases with frequency. Thus, an active device whose output increases with frequency can be characterized as an inductance. The circuit of Figure 2 yields such a response with the effective inductance being equal to:

$$L = R1R2C$$

The Q of this inductance depends upon R1 being equal to R2. At the same time, however, the positive and negative feedback paths of the amplifier are equal leading to the distinct possibility of instability at high frequencies. R1 should therefore always be slightly smaller than R2 to assure stable operation.

POWER AMPLIFIER

For most applications, the available power from op amps is sufficient. There are times when more power handling capability is necessary. A simple power booster capable of driving moderate loads is offered in Figure 3.

The circuit as shown uses a NE5535 device. Other amplifiers may be substituted only if R1 values are changed because of the ICC current required by the amplifier. R1 should be calculated from the expression

$$R1 = \frac{600mV}{ICC}$$

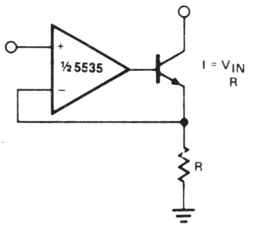
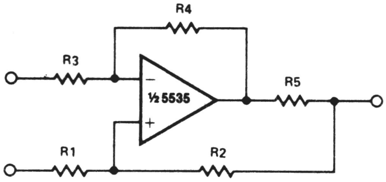


Figure 4. Voltage to Current Converters



$\frac{R2}{R1} = \frac{R4}{R3}$

$I_{OUT} = \frac{V_{IN} \cdot R2}{R5 \cdot R1}$

Figure 5. Voltage to Current Converter

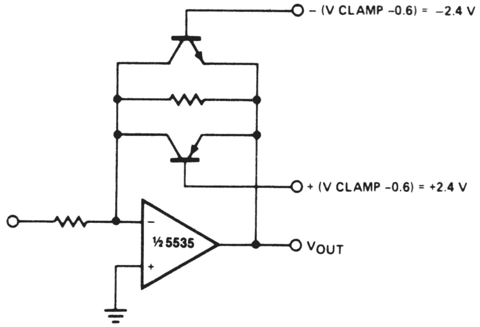
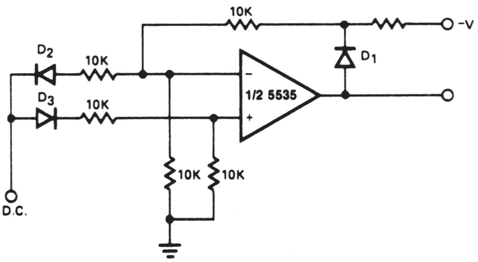


Figure 6. Active Clamp Limiting Amplifier



All resistor values are in ohms.

Figure 7. Absolute Value Amplifier

VOLTAGE-TO-CURRENT CONVERTERS

A simple voltage-to-current converter is shown in Figure 4. The current out is $I_{out} \cong V_{in}/R$. For negative currents, a pnp can be used and, for better accuracy, a Darlington pair can be substituted for the transistor. With careful design, this circuit can be used to control currents of many amps. Unity gain compensation is necessary.

The circuit in Figure 5 has a different input and will produce either polarity of output current. The main disadvantages are the error current flowing in R2 and the limited current available.

ACTIVE CLAMP LIMITING AMPLIFIER

The modified inverting amplifier in Figure 6 uses an active clamp to limit the output swing with precision. Allowance must be made for the Vbe of the transistors. The swing is limited by the base-emitter breakdown of the transistors. A simple circuit uses two back-to-back zener diodes across the feedback resistor, but tends to give less precise limiting and cannot be easily controlled.

ABSOLUTE VALUE AMPLIFIER

The circuit in Figure 7 generates a positive output voltage for either polarity of input. For positive signals, it acts as a non-inverting amplifier and for negative signals, as an inverting amplifier. The accuracy is poor for input voltages under 1V, but for less stringent applications, it can be effective.

HALF WAVE RECTIFIER

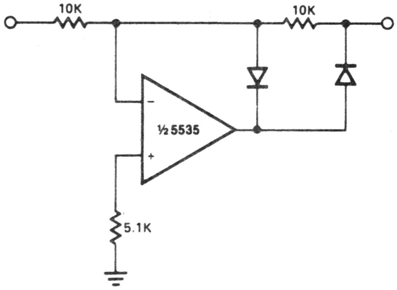
Figure 8 provides a circuit for accurate half wave rectification of the incoming signal. For positive signals, the gain is 0; for negative signals, the gain is −1. By reversing both diodes, the polarity can be inverted. This circuit provides an accurate output, but the output impedance differs for the two input polarities and buffering may be needed. The output must slew through two diode drops when the input polarity reverses. The NE5535 device will work up to 10kHz with less than 5% distortion.

PRECISION FULL WAVE RECTIFIER

The circuit in Figure 9 provides accurate full wave rectification. The output impedance is low for both input polarities, and the errors are small at all signal levels. Note that the output will not sink heavy currents, except a small amount through the 10kΩ resistors. Therefore, the load applied should be referenced to ground or a negative voltage. Reversal of all diode polarities will reverse the polarity of the output. Since the outputs of the amplifiers must slew through two diode drops when the input polarity changes, 741 type devices give 5% distortion at about 300Hz.

TWO-PHASE SINE WAVE OSCILLATOR

The circuit (referring to Figure 10, uses a 2-pole pass Butterworth, followed by a phase shifting single pole stage, fed back through a voltge limiter to achieve sine and cosine outputs. The values shown using 741 amplifiers give about 1.5% distortion at the sine output and about 3% distortion at the cosine output. By careful trimming of C_G and/or the limiting network, better distortion figures are possible. The component values shown give a frequency of oscillation of about 2kHz. The values can be readily selected for other frequencies. The NE5535 should be used at higher frequencies to reduce distortion due to slew limiting.


10K
10K
½5535
5.1K

All resistor values are in ohms.

Figure 8. Half Wave Rectifier

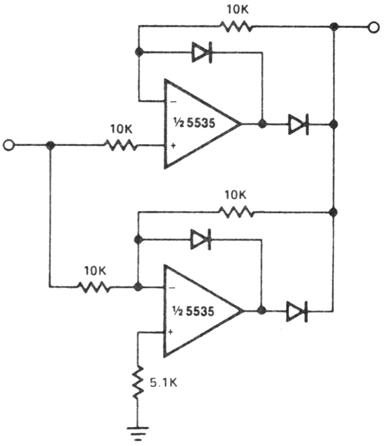
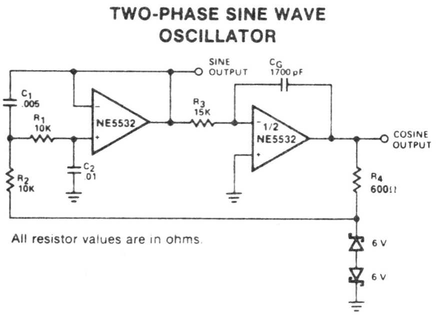

10K
½5535
10K
10K
10K
½5535
5.1K

Figure 9. Precision Full Wave Rectifier


TWO-PHASE SINE WAVE
OSCILLATOR
SINE OUTPUT
CG 1700 pF
C1 .005
R1 10K
NE5532
R3 15K
1/2 NE5532
COSINE OUTPUT
R2 10K
C2 .01
R4 600Ω
6 V
6 V

All resistor values are in ohms.

Figure 10. Two-Phase Sine Wave Oscillator

GENERAL PURPOSE OPERATIONAL AMPLIFIER μA741/μA741C/SA741C

DESCRIPTION

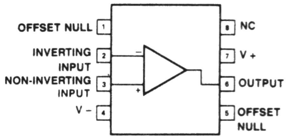
The μA741 is a high performance operational amplifier with high open loop gain, internal compensation, high common mode range and exceptional temperature stability. The μA741 is short-circuit protected and allows for nulling of offset voltage.

FEATURES

- **Internal frequency compensation**
- **Short circuit protection**
- **Excellent temperature stability**
- **High input voltage range**

PIN CONFIGURATION

D,FE,N PACKAGE


OFFSET NULL
1
INVERTING INPUT
2
NON-INVERTING INPUT
3
V −
4
8
NC
7
V +
6
OUTPUT
5
OFFSET NULL
−
+

TOP VIEW

ORDER NUMBERS

μA741N	μA741FE
μA741CN	μA741CFE
SA741CN	
μA741CD	

ABSOLUTE MAXIMUM RATINGS

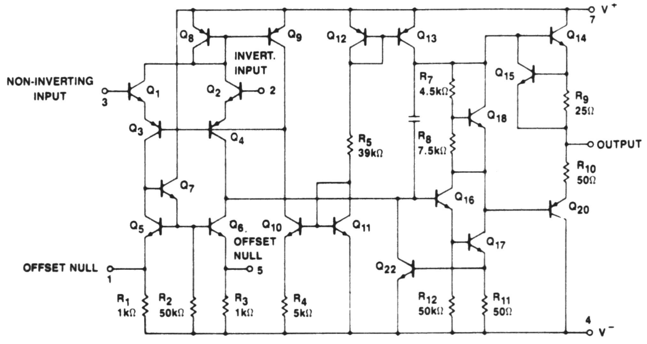
PARAMETER	RATING	UNIT
Supply voltage		
μA741C	±18	V
μA741	±22	V
Internal power dissipation		
N package	500	mW
FE package	1000	mW
Differential input voltage	±30	V
Input voltage[1]	±15	V
Output short-circuit duration	Continuous	
Operating temperature range		
μA741C	0 to +70	°C
SA741C	-40 to +85	°C
μA741	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 60sec)	300	°C

NOTE

1. For supply voltages less than ± 15V, the absolute maximum input voltage is equal to the supply voltage.

EQUIVALENT SCHEMATIC

μA741, μA741C, SA741C


V+
7
Q_8
Q_9
Q_{12}
Q_{13}
Q_{14}
INVERT. INPUT
2
NON-INVERTING INPUT
3
Q_1
Q_2
R_7 4.5kΩ
Q_{15}
R_9 25Ω
Q_3
Q_4
Q_{18}
R_5 39kΩ
R_8 7.5kΩ
OUTPUT
R_{10} 50Ω
Q_7
Q_{16}
Q_{20}
Q_5
Q_6
Q_{10}
Q_{11}
OFFSET NULL
5
Q_{17}
OFFSET NULL
1
Q_{22}
R_1 1kΩ
R_2 50kΩ
R_3 1kΩ
R_4 5kΩ
R_{12} 50kΩ
R_{11} 50Ω
4
V−

GENERAL PURPOSE OPERATIONAL AMPLIFIER µA741/µA741C/SA741C

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.

PARAMETER		TEST CONDITIONS	µA741			µA741C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S = 10k\Omega$		1.0	5.0		2.0	6.0	mV
		$R_S = 10k\Omega$, over temp.		1.0	6.0			7.5	mV
$\Delta V_{OS}/\Delta T$				10			10		µV/°C
I_{OS}	Offset current			20	200		20	200	nA
		Over temp.						300	nA
		$T_A = +125°C$		7.0	200				nA
		$T_A = -55°C$		20	500				nA
$\Delta I_{OS}/\Delta T$				200			200		pA/°C
I_{BIAS}	Input bias current			80	500		80	500	nA
		Over temp.						800	nA
		$T_A = +125°C$		30	500				nA
		$T_A = -55°C$		300	1500				nA
$\Delta I_B/\Delta T$				1			1		nA/°C
V_{OUT}	Output voltage swing	$R_L = 10k\Omega$	± 12	± 14		± 12	± 14		V
		$R_L = 2k\Omega$, over temp.	± 10	± 13		± 10	± 13		V
A_{VOL}	Large signal voltage gain	$R_L = 2k\Omega$, $V_O = \pm 10V$	50	200		20	200		V/mV
		$R_L = 2k\Omega$, $V_O = \pm 10V$, over temp.	25			15			V/mV
	Offset voltage adjustment range			± 30			± 30		mV
PSRR	Supply voltage rejection ratio	$R_S \leq 10k\Omega$					10	150	µV/V
		$R_S \leq 10k$, over temp.		10	150				µV/V
CMRR	Common mode rejection ratio								dB
		Over temp.	70	90					dB
I_{CC}	Supply current			1.4	2.8		1.4	2.8	mA
		$T_A = +125°C$		1.5	2.5				mA
		$T_A = -55°C$		2.0	3.3				mA
V_{IN}	Input voltage range	(µA741, over temp.)	± 12	± 13		± 12	± 13		V
R_{IN}	Input resistance		0.3	2.0		0.3	2.0		MΩ
P_d	Power consumption			50	85		50	85	mW
		$T_A = +125°C$		45	75				mW
		$T_A = -55°C$		45	100				mW
R_{OUT}	Output resistance			75			75		Ω
I_{SC}	Output short-circuit current		10	25	60	10	25	60	mA

PARAMETER		TEST CONDITIONS	SA741C			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage	$R_S = 10k\Omega$		2.0	6.0	mV
		$R_S = 10k\Omega$, over temp.			7.5	mV
$\Delta V_{OS}/\Delta T$				10		µV/°C
I_{OS}	Offset current			20	200	nA
		Over temp.			500	nA
$\Delta I_{OS}/\Delta T$				200		pA/°C
I_{BIAS}	Input bias current			80	500	nA
		Over temp.			1500	nA
$\Delta I_B/\Delta T$				1		nA/°C
V_{OUT}	Output voltage swing	$R_L = 10k\Omega$	± 12	± 14		V
		$R_L = 2k\Omega$, over temp.	± 10	± 13		V
A_{VOL}	Large signal voltage gain	$R_L = 2k\Omega$, $V_O = \pm 10V$	20	200		V/mV
		$R_L = 2k\Omega$, $V_O = \pm 10V$, over temp.	15			V/mV
	Offset voltage adjustment range			± 30		mV

DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25°C$, $V_S = \pm 15V$, unless otherwise specified.

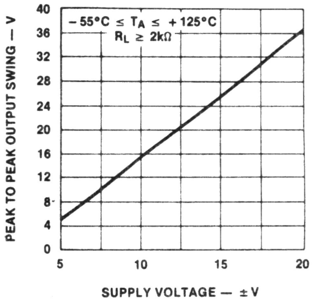
PARAMETER		TEST CONDITIONS	SA741C			UNIT
			Min	Typ	Max	
PSRR	Supply voltage rejection ratio	$R_S \leq 10k\Omega$		10	150	μV/V
CMRR	Common mode rejection ratio					dB
V_{IN}	Input voltage range	(μA741, over temp.)	± 12	± 13		V
	Input resistance		0.3	2.0		MΩ
P_d	Power consumption			50	85	mW
R_{OUT}	Output resistance			75		Ω
I_{SC}	Output short-circuit current			25		mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm15V$, unless otherwise specified.

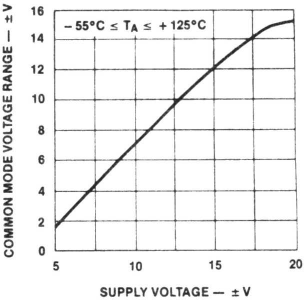
PARAMETER	TEST CONDITIONS	μA741, μA741C			UNIT
		Min	Typ	Max	
Parallel input resistance	Open loop, f = 20Hz				MΩ
Parallel input capacitance	Open loop, f = 20Hz		1.4		pF
Unity gain crossover frequency	Open loop		1.0		MHz
Transient response unity gain	$V_{IN} = 20mV$, $R_L = 2k\Omega$, $C_L \leq 100pf$				
Rise time			0.3		μs
Overshoot			5.0		%
Slew rate	$C \leq 100pf$, $R_L \geq 2k$, $V_{IN} = \pm10V$		0.5		V/μs

TYPICAL PERFORMANCE CHARACTERISTICS

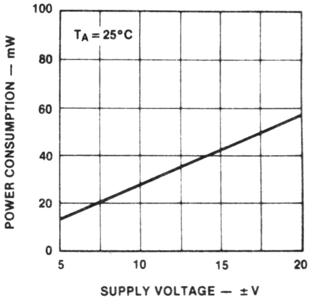
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

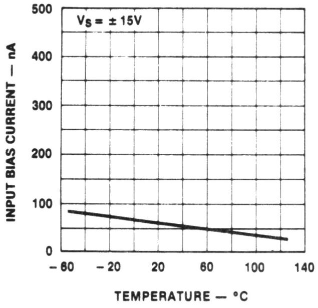


POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE

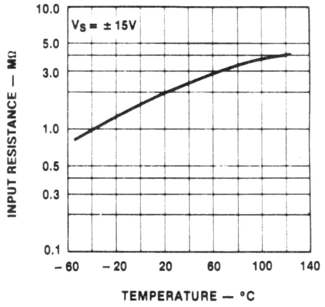


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

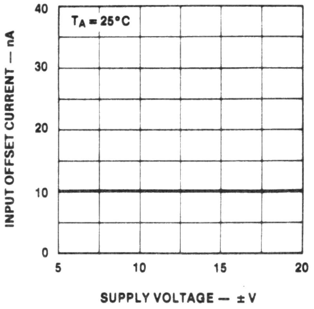
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



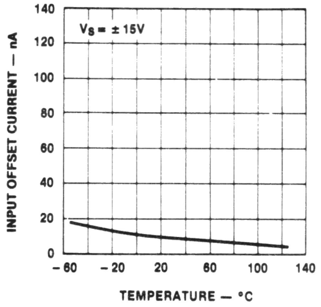
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



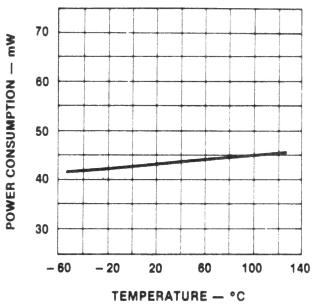
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



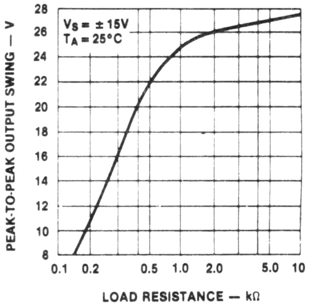
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



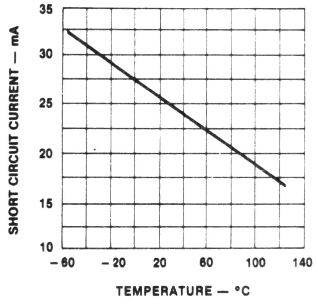
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



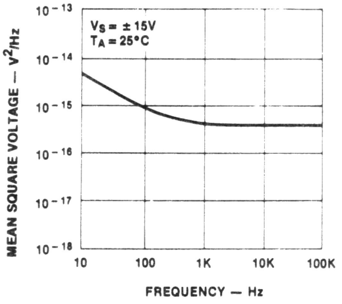
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



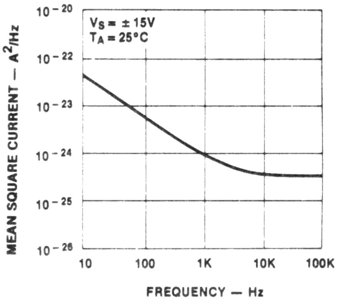
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



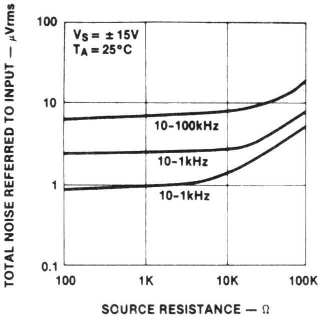
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY

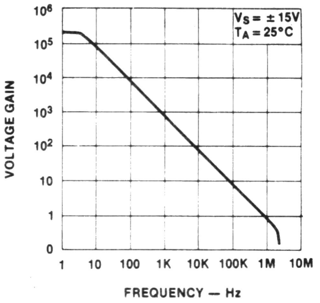


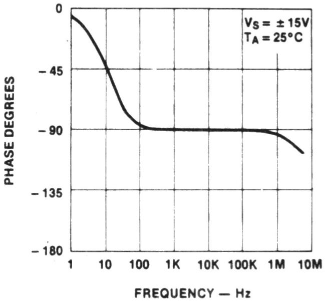
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

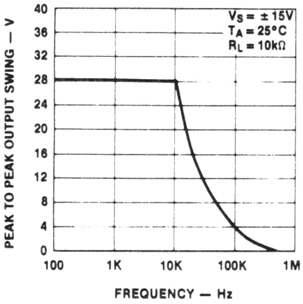


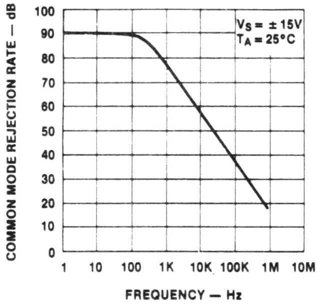
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

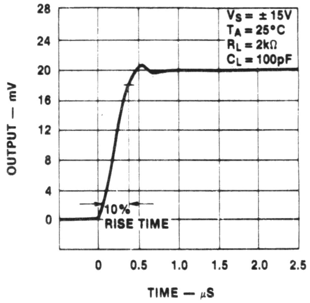

BROADBAND NOISE FOR VARIOUS BANDWIDTHS

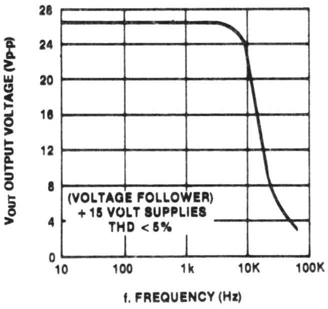

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

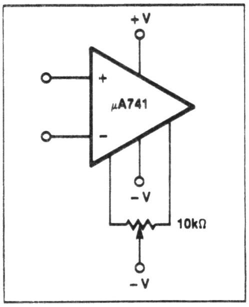

OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY


OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY


COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY


TRANSIENT RESPONSE


POWER BANDWIDTH
(Large Signal Swing vs Frequency)


VOLTAGE OFFSET NULL

DUAL OPERATIONAL AMPLIFIER μA747/747C/SA747C

DESCRIPTION

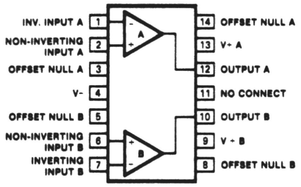
The 747 is a pair of high performance monolithic operational amplifiers constructed on a single silicon chip. High common mode voltage range and absence of "latch-up" make the 747 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications. The 747 is short-circuit protected and requires no external components for frequency compensation. The internal 6dB/octave roll-off insures stability in closed loop applications. For single amplifier performance, see μA741 data sheet.

FEATURES

- **No frequency compensation required**
- **Short-circuit protection**
- **Offset voltage null capability**
- **Large common-mode and differential voltage ranges**
- **Low power consumption**
- **No latch-up**

PIN CONFIGURATIONS

D,F,N PACKAGE


INV. INPUT A 1
NON-INVERTING INPUT A 2
OFFSET NULL A 3
V- 4
OFFSET NULL B 5
NON-INVERTING INPUT B 6
INVERTING INPUT B 7
14 OFFSET NULL A
13 V+ A
12 OUTPUT A
11 NO CONNECT
10 OUTPUT B
9 V+ B
8 OFFSET NULL B
A
B
-
+
+
-

TOP VIEW

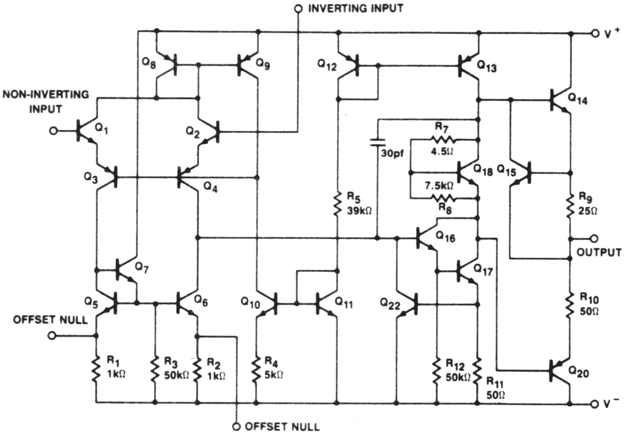
ORDER NUMBERS
μA747CN, μA747CF, μA747N,
μA747F, SA747CN, μA747C
μA747CD

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
μA747	±22	V
μA747C	±18	V
SA747C	±18	V
Internal power dissipation		
H Package	500	mW
N,F Packages	670	mW
Differential input voltage	±30	V
Input voltage	±15	V
Voltage between offset null and V-	±0.5	V
Storage temperature range	-65 to +155	°C
Operating temperature range		
μA747	-55 to +125	°C
μA747C	0 to +70	°C
SA747C	-40 to +85	°C
Lead temperature (soldering, 60 sec)	300	°C
Output short-circuit duration	indefinite	

EQUIVALENT SCHEMATIC

EQUIVALENT CIRCUIT (EACH SIDE)


INVERTING INPUT
V+
NON-INVERTING INPUT
Q8
Q9
Q12
Q13
Q14
Q1
Q2
R7
4.5Ω
30pf
Q18
Q15
Q3
Q4
7.5kΩ
R8
R5
39kΩ
R9
25Ω
Q16
OUTPUT
Q7
Q17
Q5
Q6
Q10
Q11
Q22
R10
50Ω
OFFSET NULL
R1
1kΩ
R3
50kΩ
R2
1kΩ
R4
5kΩ
R12
50kΩ
R11
50Ω
Q20
V-
OFFSET NULL

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SA747C			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage	$R_S = 10k\Omega$		2.0	6.0	mV
		$R_S \leq 10k\Omega$, over temperature		3.0	7.5	mV
$\Delta V_{OS}/\Delta T$				10		µV/°C
I_{OS}	Offset current			20	200	nA
		Over temperature			500	nA
$\Delta I_{OS}/\Delta T$				300		pA/°C
I_{BIAS}	Input bias current				500	nA
		Over temperature			1500	nA
$\Delta I_B/\Delta T$				1		nA/°C
V_{OUT}	Output voltage swing	$R_L \geq 2k\Omega$, over temperature	± 10	± 13		V
		$R_L \geq 10k\Omega$, over temperature	± 12	± 14		V
I_{CC}	Supply current			1.7	2.8	mA
		Over temperature		2.0	3.3	mA
	Power consumption			50	85	mW
		Over temperature		60	100	mW
	Input capacitance			1.4		pF
	Offset voltage adjustment range			± 15		V
	Output resistance			75		Ω
	Channel separation			120		dB
PSRR	Supply voltage rejection ratio	$R_S \leq 10k\Omega$, over temperature		30	150	µV/V
A_{VOL}	Large signal voltage gain (DC)	$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	25,000			V/V
CMRR		$R_S \leq 10k\Omega$, $V_{CM} = \pm 12V$				
		Over temperature	70			dB
I_{SC}			10	25	60	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	µA747/µA747C/SA747C			UNIT
		Min	Typ	Max	
Transient response	$V_{IN} = 20mV$, $R_1 = 2k\Omega$, $C_1 < 100pf$				
Risetime	Unity gain CL ≤ 100pf		0.3		µs
Overshoot	Unity gain CL ≤ 100pf		5.0		%
Slew rate	RL > 2kΩ		0.5		V/µs

DUAL OPERATIONAL AMPLIFIER

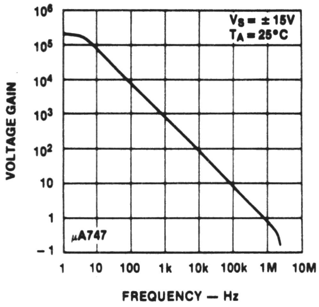
μA747/747C/SA747C

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = \pm 15V$ unless otherwise specified.[1]

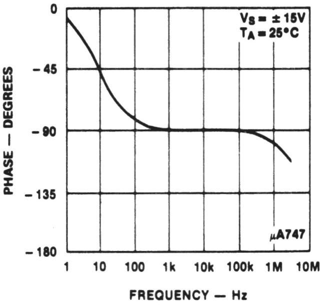
PARAMETER		TEST CONDITIONS	μA747			μA747C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage	$R_S \le 10k\Omega$		2.0	5.0		2.0	6.0	mV
		$R_S \le 10k\Omega$, over temp.		3.0	6.0		3.0	7.5	mV
$\Delta V_{OS}/\Delta T$				10			10		μV/°C
I_{OS}	Offset current			20	200		20	200	nA
		$T_A = +125°C$		7.0	200				nA
		$T_A = -55°C$		85	500				nA
		Over temperature					7.0	300	nA
$\Delta I_{OS}/\Delta T$				200			200		pA/°C
I_{BIAS}	Input current			80	500		80	500	nA
		$T_A = +125°C$		30	500				nA
		$T_A = -55°C$		300	1500				nA
		Over temperature					30	800	nA
$\Delta I_B/\Delta T$				1			1		nA/°C
V_{OUT}	Output voltage swing	$R_L \ge 2k\Omega$, over temp.	± 10	± 13		± 10	± 13		V
		$R_L \ge 10k\Omega$, over temp.	± 12	± 14		± 12	± 14		V
I_{CC}	Supply current each side			1.7	2.8		1.7	2.8	mA
		$T_A = +125°C$		1.5	2.5				mA
		$T_A = -55°C$		2.0	3.3				mA
		Over temperature					2.0	3.3	mA
	Power consumption			50	85		50	85	mW
		$T_A = +125°C$		45	75				mW
		$T_A = -55°C$		60	100				mW
		Over temperature					60	100	mW
	Input capacitance			1.4			1.4		pF
	Offset voltage adjustment range			± 15			± 15		V
	Output resistance			75			75		Ω
	Channel separation			120			120		dB
PSRR	Supply voltage rejection ratio	$R_S \le 10k\Omega$, over temp.		30	150		30	150	μV/V
A_{VOL}	Large signal voltage gain (DC)	$R_L \ge 2k\Omega$, $V_{OUT} = \pm 10V$	50,000			25,000			V/V
		Over temperature	25,000			15,000			V/V
CMRR		$R_S \le 10k\Omega$, $V_{CM} = \pm 12V$							
		Over temperature	70			70			dB

TYPICAL PERFORMANCE CHARACTERISTICS

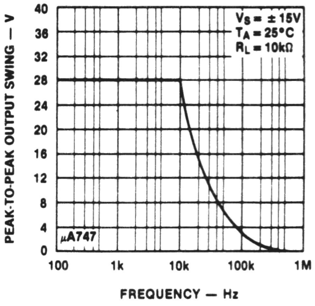
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



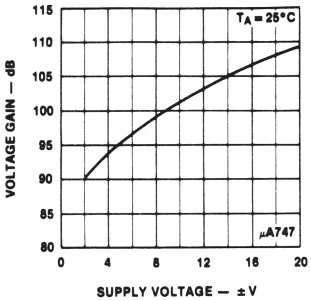
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



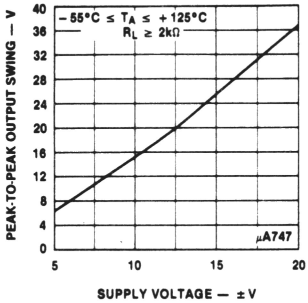
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



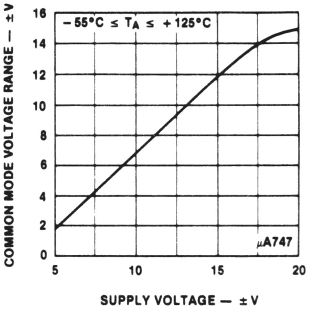
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



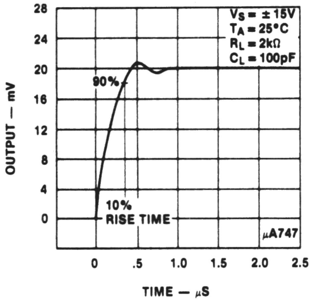
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



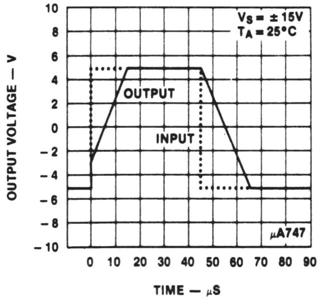
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



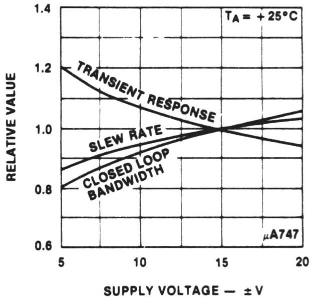
TRANSIENT RESPONSE



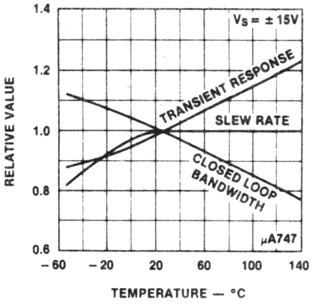
VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



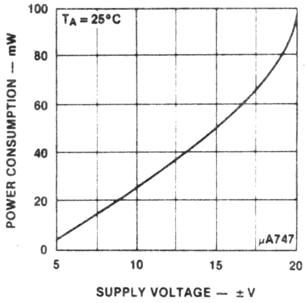
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



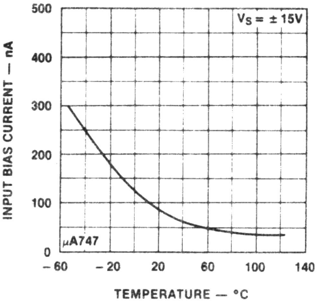
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)



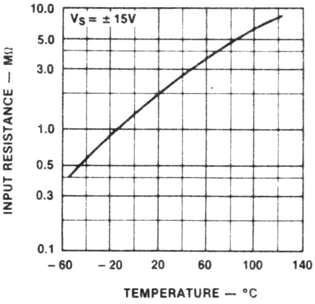
FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



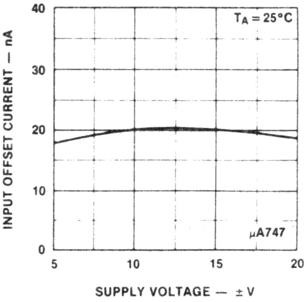
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



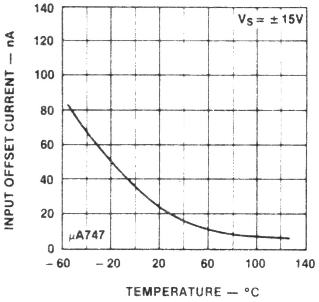
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



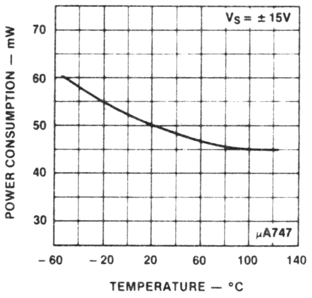
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



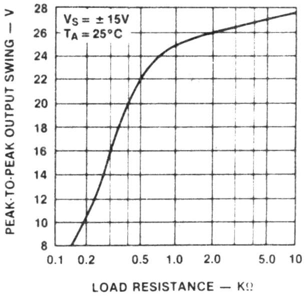
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



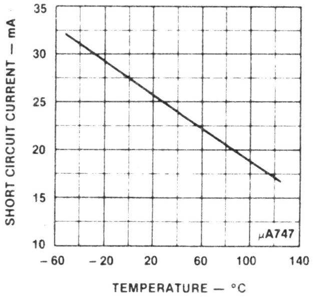
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



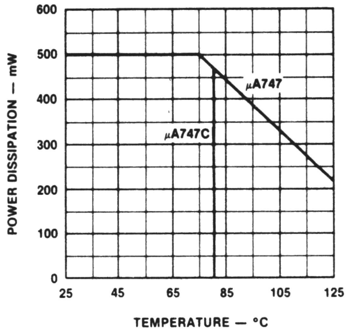
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



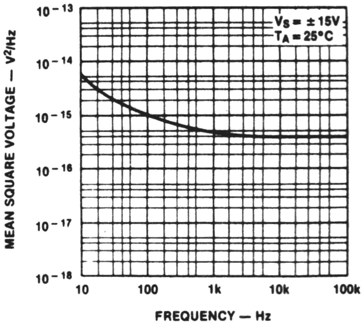
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

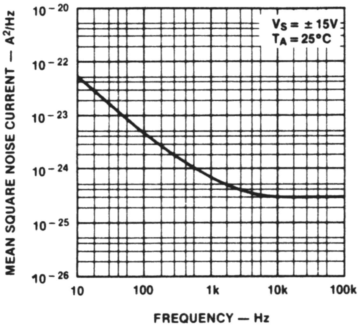
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



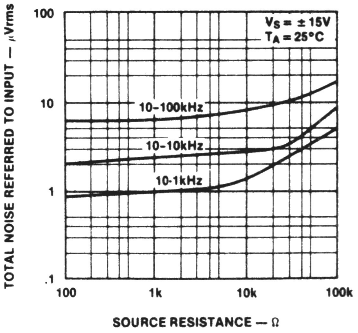
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

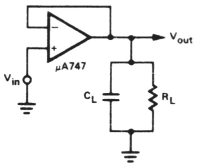


BROADBAND NOISE FOR VARIOUS BANDWIDTHS

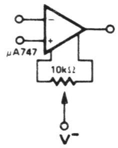


TEST CIRCUITS

TRANSIENT RESPONSE TEST CIRCUIT



VOLTAGE OFFSET NULL CIRCUIT



DUAL OPERATIONAL TRANSCONDUCTANCE AMPLIFIER NE5517/5517A

DESCRIPTION

The NE5517 contains two current controlled transconductance amplifiers, each with a differential input and push-pull output. The NE5517 offers significant design and performance advantages over similar devices for all types of programmable gain applications. Circuit performance is enhanced through the use of linearizing diodes at the inputs which enable a 10dB signal to noise improvement referenced to .5 percent THD. The NE5517 is suited for a wide variety of industrial and consumer applications and is recommended as the preferred circuit in the Dolby* HX (Headroom Extension) system.

Constant-Impedance-Buffers on the chip allow general use of the NE5517. These buffers are made of Darlington-Transistor and a biasing-network which changes bias current in dependence of I_{ABC}.

Therefore changes of output offset voltages are almost eliminated. This is an advantage of the NE5517 compared to LM13600. With the LM13600 a burst in the bias current I_{ABC} guides to an audible offset voltage change at the output. With the Constant-Impedance-Buffers of the NE5517 this effect can be avoided and makes this circuit preferable for high quality audio applications.

FEATURES

- **Constant impedance buffers**
- **ΔV_{BE} of buffer is constant with amplifier I_{BIAS} change**
- **Pin compatible with LM13600**
- **Excellent matching between amplifiers**
- **Linearizing diodes**
- **High output signal-to-noise ratio**

APPLICATIONS

- **Multiplexers**
- **Timers**
- **Electronic music synthesizers**
- **Dolby* HX Systems**
- **Current-controlled amplifiers, filters**
- **Current-controlled oscillators, impedances**

NOTE

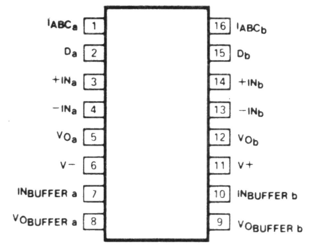
*Dolby is a registered trademark of Dolby Laboratories Inc., San Francisco, Calif.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply Voltage[1]		
NE5517	36 V_{DC} or ± 18	V
NE5517A	44 V_{DC} or ± 22	V
Power Dissipation[2] T_A = 25°C		
NE5517N, NE5517AN	570	mW
Differential Input Voltage	±5	V
Diode Bias Current (I_D)	2	mA
Amplifier Bias Current (I_{ABC})	2	mA
Output Short Circuit Duration	Indefinite	
Buffer Output Current[3]	20	mA
Operating Temperature Range		
NE5517N, NE5517AN	0°C to +70	°C
DC Input Voltage	$+V_S$ to $-V_S$	
Storage Temperature Range	−65°C to +150	°C
Lead Temperature (Soldering, 10 Seconds)	300	°C

PIN CONFIGURATION

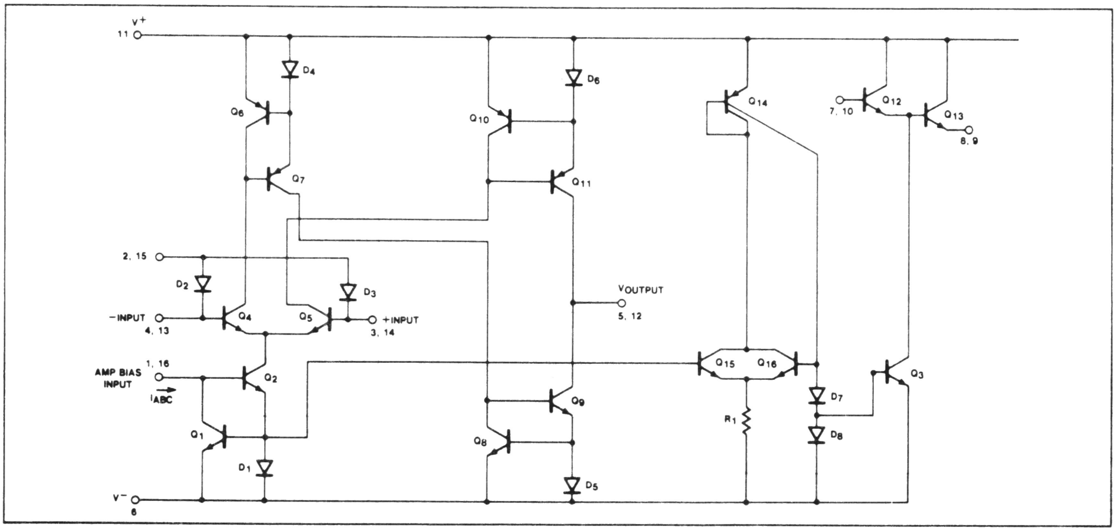
D,N PACKAGE



TOP VIEW

ORDER NUMBERS
NE5517N NE5517D NE5517AN

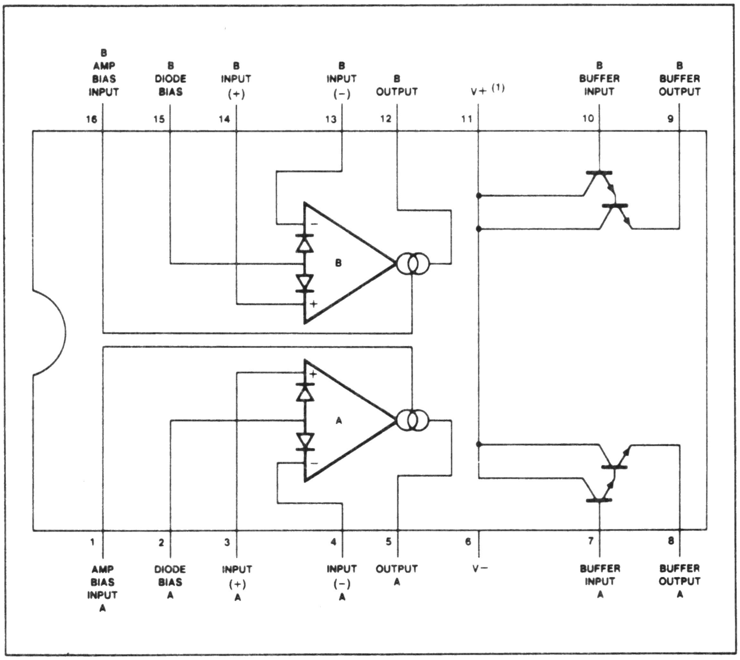
CIRCUIT SCHEMATIC



PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	I_{ABCa}	Amplifier bias input A
2	D_a	Diode bias A
3	$+IN_a$	Non-inverting input A
4	$-IN_a$	Inverting input A
5	V_{oa}	Output A
6	V−	negative supply
7	$IN_{Buffer\ (a)}$	Buffer input A
8	$Vo_{Buffer\ (a)}$	Buffer output A
9	$Vo_{Buffer\ (b)}$	Buffer output B
10	$IN_{Buffer\ (b)}$	Buffer input B
11	V+	Positive supply
12	V_{ob}	Output B
13	$-IN_b$	Inverting input B
14	$+IN_b$	Non-inverting input B
15	D_b	Diode bias B
16	I_{ABCb}	Amplifier bias input B

CONNECTION DIAGRAM


B AMP BIAS INPUT
B DIODE BIAS
B INPUT (+)
B INPUT (−)
B OUTPUT
V+ (1)
B BUFFER INPUT
B BUFFER OUTPUT
16
15
14
13
12
11
10
9
B
A
1
2
3
4
5
6
7
8
AMP BIAS INPUT A
DIODE BIAS A
INPUT (+) A
INPUT (−) A
OUTPUT A
V−
BUFFER INPUT A
BUFFER OUTPUT A

NOTE:

1. V+ of output buffers and amplifiers are internally connected.

DUAL OPERATIONAL TRANSCONDUCTANCE AMPLIFIER NE5517/5517A

ELECTRICAL CHARACTERISTICS[4]

PARAMETER	TEST CONDITIONS	NE5517			NE5517A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage (V_{OS})			0.4	5		0.4	2	mV
	Over temperature range						5	mV
	I_{ABC} 5μA		0.3	5		0.3	2	mV
$\Delta V_{OS}/\Delta T$	Avg. TC of input offset voltage		7			7		μV/°C
V_{OS} including diodes	Diode bias current (I_D) = 500μA		0.5	5		0.5	2	mV
Input offset change	$5\mu A \leq I_{ABC} \leq 500\mu A$		0.1			0.1	3	mV
Input offset current			0.1	0.6		0.1	0.6	μA
$\Delta I_{OS}/\Delta T$	Avg. TC of input offset current		0.001			0.001		μA/°C
Input bias current			0.4	5		0.4	5	μA
	Over temperature range		1	8		1	7	μA
$\Delta I_B/\Delta T$	Avg. TC of input current		0.01			0.01		μA/°C
Forward Transconductance (gm)		6700	9600	13000	7700	9600	12000	μmho
	Over temperature range	5400			4000			μmho
gm tracking			0.3			0.3		dB
Peak output current	RL = 0, I_{ABC} = 5μA		5		3	5	7	μA
	RL = 0, I_{ABC} = 500μA	350	500	650	350	500	650	μA
	RL = 0,	300			300			μA
Peak output voltage								
Positive	RL = ∞, $5\mu A \leq I_{ABC} \leq 500\mu A$	+12	+14.2		+12	+14.2		V
Negative	RL = ∞, $5\mu A \leq I_{ABC} \leq 500\mu A$	−12	−14.4		−12	−14.4		V
Supply current	I_{ABC} = 500μA, both channels		2.6	4		2.6	4	mA
V_{OS} sensitivity								
Positive	$\Delta V_{OS}/\Delta V+$		20	150		20	150	μV/V
Negative	$\Delta V_{OS}/\Delta V-$		20	150		20	150	μV/V
CMRR		80	110		80	110		dB
Common mode range		±12	±13.5		±12	±13.5		V
Crosstalk	Referred to input[5] $20Hz < f < 20kHz$		100			100		dB
Diff. input current	I_{ABC} = 0, input = ±4V		0.02	100		0.02	10	nA
Leakage current	I_{ABC} = 0 (Refer to test circuit)		0.2	100		0.2	5	nA
Input resistance		10	26		10	26		KΩ
Open loop bandwidth			2			2		MHz
Slew rate	Unity gain compensated		50			50		V/μSec
Buff. input current	5		0.4	5		0.4	5	μA
Peak buffer output voltage	5	10			10			V
ΔV_{BE} of buffer	6 Refer to Buffer V_{BE} test circuit		0.5	5		0.5	5	mV

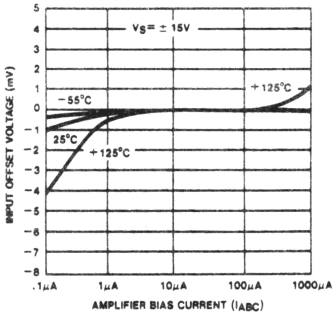
NOTES

1. For selections to a supply voltage above ±22V, contact factory.
2. For operating at high temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175° C/W which applies for the device soldered in a printed circuit board, operating in still air.
3. Buffer output current should be limited so as to not exceed package dissipation.
4. These specifications apply for $V_S = \pm 15V$, $T_A = 25°C$, amplifier bias current (I_{ABC}) = 500μA, pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.
5. These specifications apply for $V_S = \pm 15V$, $I_{ABC} = 500\mu A$, $R_{OUT} = 5k\Omega$ connected from the buffer output to $-V_S$ and the input of the buffer is connected to the transconductance amplifier output.
6. $V_S = \pm 15$, $R_{OUT} = 5K\Omega$ connected from Buffer output to $-V_S$ and $5\mu A \leq I_{ABC} \leq 500\mu A$.

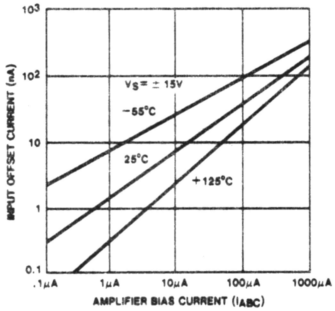
DUAL OPERATIONAL TRANSCONDUCTANCE AMPLIFIER NE5517/5517A

TYPICAL PERFORMANCE CHARACTERISTICS

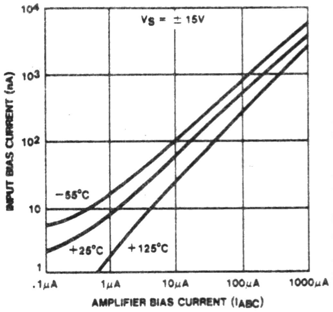
INPUT OFFSET VOLTAGE



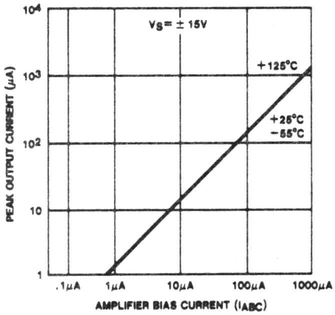
INPUT OFFSET CURRENT



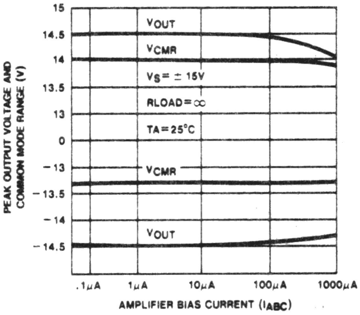
INPUT BIAS CURRENT



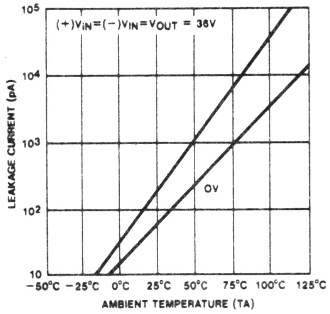
PEAK OUTPUT CURRENT



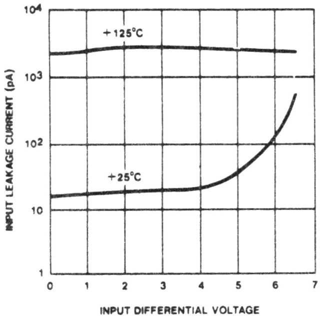
PEAK OUTPUT VOLTAGE AND COMMON MODE RANGE



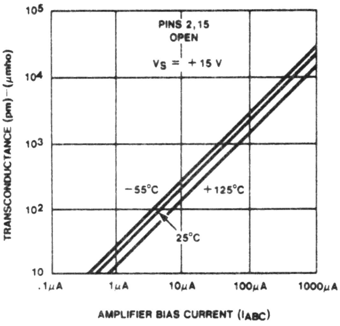
LEAKAGE CURRENT



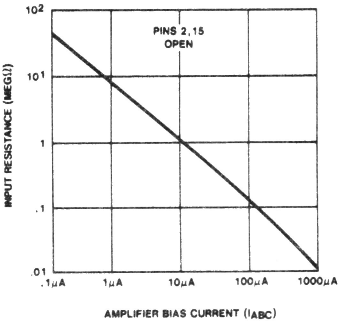
INPUT LEAKAGE



TRANSCONDUCTANCE



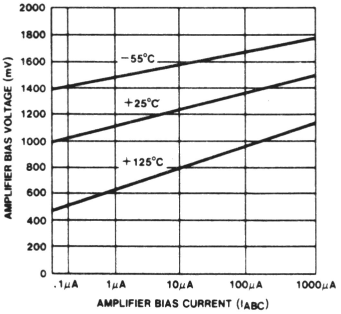
INPUT RESISTANCE



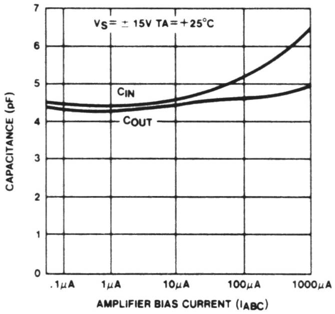
DUAL OPERATIONAL TRANSCONDUCTANCE AMPLIFIER NE5517/5517A

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

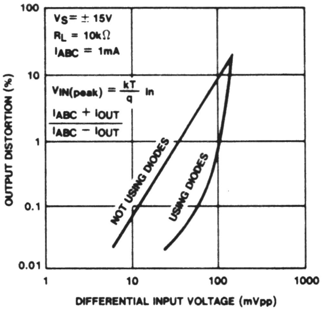
AMPLIFIER BIAS VOLTAGE vs AMPLIFIER BIAS CURRENT



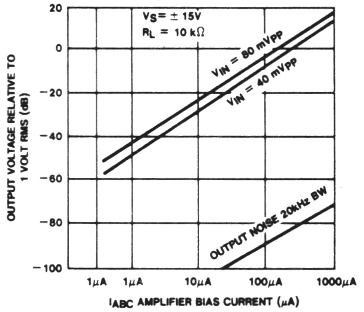
INPUT AND OUTPUT CAPACITANCE



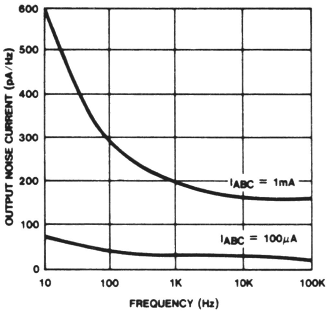
DISTORTION vs DIFFERENTIAL INPUT VOLTAGE



VOLTAGE vs AMPLIFIER BIAS CURRENT

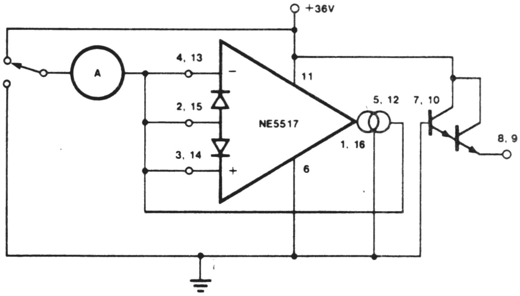


OUTPUT NOISE vs FREQUENCY

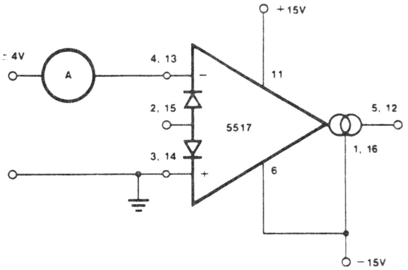


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

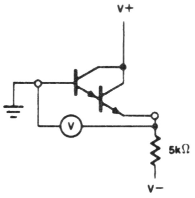
LEAKAGE CURRENT TEST CIRCUIT


+36V
A
4, 13
11
2, 15
NE5517
5, 12
7, 10
1, 16
8, 9
3, 14
6

DIFFERENTIAL INPUT CURRENT TEST CIRCUIT

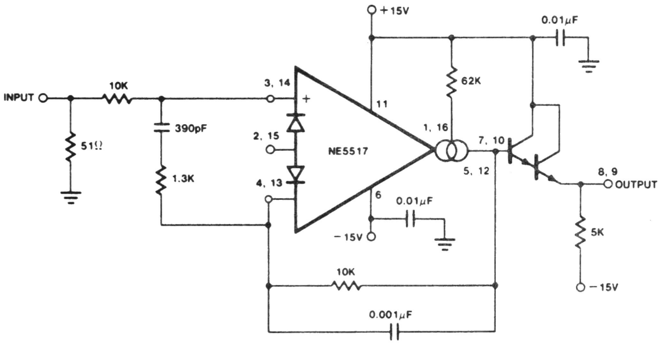

+15V
±4V
A
4, 13
11
2, 15
5517
5, 12
1, 16
3, 14
6
−15V

BUFFER V_{BE} TEST CIRCUIT



APPLICATIONS

UNITY GAIN FOLLOWER


+15V
0.01μF
INPUT
10K
3, 14
62K
11
51Ω
390pF
2, 15
NE5517
1, 16
7, 10
5, 12
1.3K
4, 13
8, 9
OUTPUT
6
0.01μF
−15V
5K
10K
−15V
0.001μF

CIRCUIT DESCRIPTION

The circuit schematic diagram of one half of the NE5517, a dual operational transconductance amplifier with linearizing diodes and impedance buffers, is shown in Figure 1.

1. Transconductance Amplifier

The transistor pair Q_4 and Q_5 form a transconductance stage. The ratio of their collector currents (I_4 and I_5 respectively) is defined by the differential input voltage, V_{IN}, which is shown in equation 1.

$$V_{IN} = \frac{KT}{q} \ln \frac{I_5}{I_4} \tag{1}$$

Where V_{IN} is the difference of the two input voltages

KT ≅ 26mV at room temperature (300°K)

Transistors Q_1, Q_2 and diode D_1 form a current mirror which focuses the sum of current I_4 and I_5 to be equal to amplifier bias current I_B:

$$I_4 + I_5 = I_B \tag{2}$$

If V_{IN} is small the ratio of I_5 and I_4 will approach to unity and the Taylor series of ln function can be approximated as:

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{I_4} \tag{3}$$

and $I_4 \approx I_5 \approx {}^1\!/\!_2 I_B$

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{{}^1\!/\!_2 I_B} = \frac{2KT}{q} \frac{I_5 - I_4}{I_B} = V_{IN}$$

$$I_5 - I_4 = V_{IN} \frac{(I_B{}^q)}{2KT} \tag{4}$$

The remaining transistors (Q_6 to Q_{11}) and diodes (D_4 to D_6) form three current mirrors that produce an output current equal to I_5 minus I_4. Thus:

$$V_{IN} \left\{ I_B \frac{q}{2KT} \right\} = I_0 \tag{5}$$

The term $\frac{(I_B{}^q)}{2KT}$ is then the transconductance of the amplifier and is proportional to I_B.

2. Linearizing Diodes

For V_{IN} greater than a few millivolts, equation 3 becomes invalid and the transconductance increases nonlinearly. Figure 2 shows how the internal diodes can linearize the transfer function of the operational amplifier. Assume D_2 and D_3 are biased with current sources and the input signal current is I_S. Since

$I_4 + I_5 = I_B$ and $I_5 - I_4 = I_0$, that is:

$I_4 = {}^1\!/\!_2(I_B - I_0)$, $I_5 = {}^1\!/\!_2(I_B + I_0)$

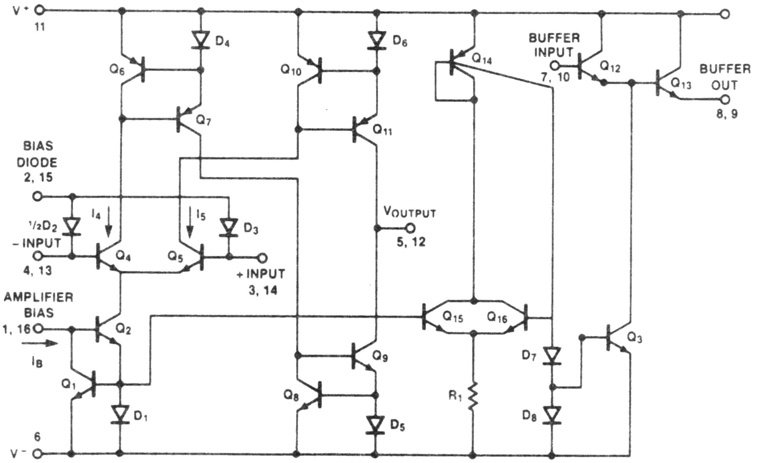


Figure 1. Circuit Diagram of NE5517

DUAL OPERATIONAL TRANSCONDUCTANCE AMPLIFIER NE5517/5517A

For the diodes and the input transistors that have identical geometries and are subject to similar voltages and temperatures, the following equations is true:

$$\frac{KT}{q} \ln \frac{\frac{I_D}{2} + I_S}{\frac{I_D}{2} - I_S} = \frac{KT}{q} \ln \frac{1/2(I_B + I_0)}{1/2(I_B - I_0)}$$

$$I_0 = I_S \frac{(2^I B)}{I_D} \text{ for } |I_S| < \frac{I_D}{2} \qquad (6)$$

The only limitation is that the signal current should not exceed 1/2 I_D.

3. Impedance Buffer

The upper limit of transconductance is defined by the maximum value of I_B (2mA). The lowest value of I_B for which the amplifier will function therefore determines the overall dynamic range. At low values of I_B, a buffer with very low input bias current is desired. A Darlington amplifier with constant current source (Q_{14}, Q_{15}, Q_{16}, D_7, D_8, and R_1) suits the need.

APPLICATIONS

Voltage Controlled Amplifier

The voltage-divider R_2, R_3 divides the input-voltage into small values (mV-range) so the amplifier operates in a linear manner.

It is:

$$I_{OUT} = -V_{IN} \times \frac{R_3}{R_2 + R_3} \times gm;$$

$$V_{OUT} = I_{OUT} \times R_L;$$

$$A = \frac{V_{OUT}}{V_{IN}} = \frac{R_3}{R_2 + R_3} gm R_L;$$

$$\boxed{A = \frac{R_3}{R_2 + R_3} \times gm \times R_L} \quad (3) \; gm = 19.2 \, I_{ABC}$$

(gm in mS for I_{ABC} in mA)

Since gm is directly proportional to I_{ABC}, the amplification is controlled by the voltage V_C in a simple way.

When V_C is taken relative to $-V_{CC}$ the following formula is valid:

$$I_{ABC} = \frac{(V_C - 1.2V)}{R_1};$$

The 1.2V is the voltage across two base-emitter paths in the current mirrors. This circuit is the base for many applications of the NE5517.

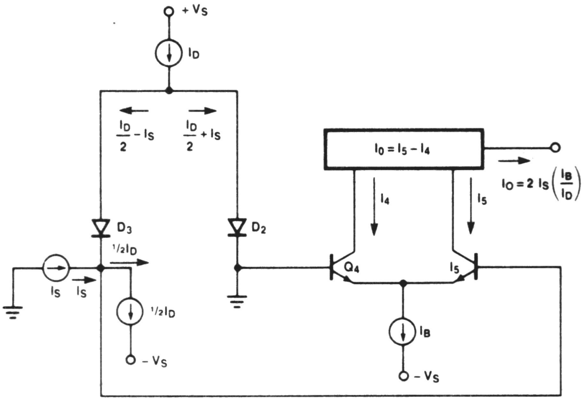
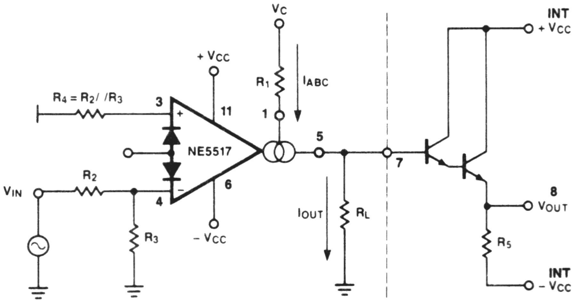

+Vs
I_D
$\frac{I_D}{2} - I_S$
$\frac{I_D}{2} + I_S$
$I_0 = I_5 - I_4$
$I_0 = 2 I_S \left(\frac{I_B}{I_D}\right)$
I_4
I_5
D_3
D_2
$1/2 I_D$
Q_4
I_5
I_S
I_S
$1/2 I_D$
−Vs
I_B
−Vs

Figure 2. Linearizing Diode


V_C
R_1
I_{ABC}
+Vcc
$R_4 = R_2 / / R_3$
3
11
1
NE5517
5
R_2
V_{IN}
4
6
I_{OUT}
R_L
R_3
−Vcc
7
INT
+Vcc
8
V_{OUT}
R_5
INT
−Vcc

TYPICAL VALUES: $R_1 = 47K$
$R_2 = 10K$
$R_3 = 200\Omega$
$R_4 = 200\Omega$
$R_1 = 100K$
$R_5 = 47K$

Figure 3.

Stereo Amplifier With Gain Control

Figure 4 shows a stereo amplifier with variable gain via a control input. Excellent tracking of typical 0.3dB is easy to achieve. With the potentiometer R_P, the offset can be adjusted. For AC-coupled amplifiers you can replace the potentiometer with two 510Ω resistors.

Modulators

Because the transconductance of an OTA is directly proportional to I_{ABC}, the amplification of a signal can be controlled easily. The output current is the product from transconductance × input voltage. The circuit works up to approximately 200KHz. Modulation of 99 percent is easy to achieve.

Voltage Controlled Resistors (VCR)

The principle is based on the capability of an OTA to vary a current proportional to a controlled voltage which is according to a resistor. The circuit takes advantage of the possibility to control a resistor via gm.

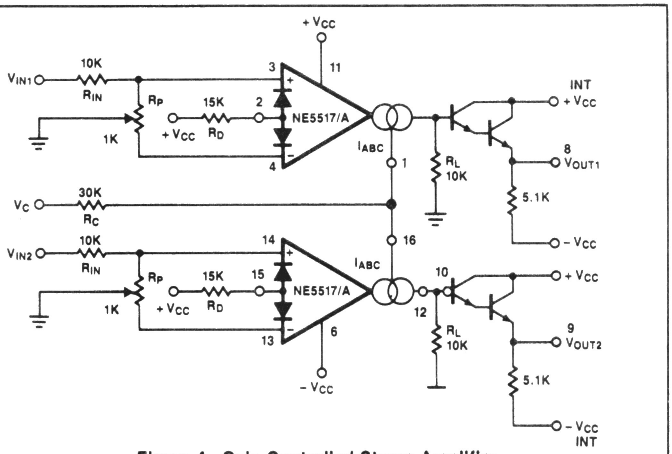

+Vcc
11
10K
VIN1
RIN
3
RP
15K
2
NE5517/A
1K
+Vcc
RD
4
IABC
1
RL
10K
INT
+Vcc
8
VOUT1
5.1K
-Vcc
Vc
30K
Rc
16
10K
VIN2
RIN
14
RP
15K
15
NE5517/A
1K
+Vcc
RD
13
6
-Vcc
IABC
10
12
RL
10K
+Vcc
9
VOUT2
5.1K
-Vcc
INT

Figure 4. Gain Controlled Stereo Amplifier

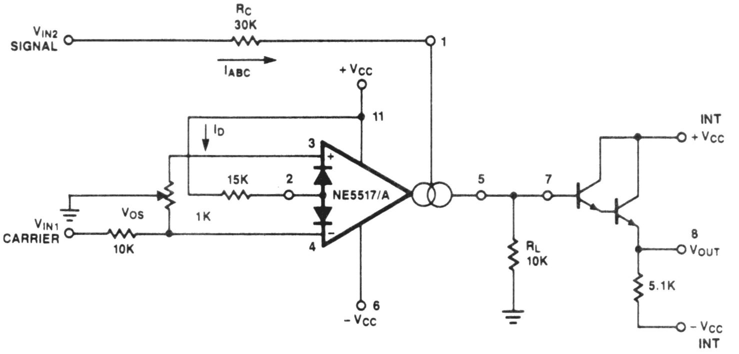

VIN2
SIGNAL
Rc
30K
IABC
1
+Vcc
11
ID
3
15K
2
NE5517/A
VOS
1K
VIN1
CARRIER
10K
4
6
-Vcc
5
7
RL
10K
INT
+Vcc
8
VOUT
5.1K
-Vcc
INT

Figure 5. Amplitude modulator

Voltage Controlled Filters

Voltage controlled filters can be realized extremely easily with the help of an OTA.

Figure 8 shows the circuit for a low-pass filter. Below the corner frequency the circuit has an amplification of 0dB. Above the corner frequency the attentuation drops by 6dB/octave.

The high-pass filter is built in a similar manner, except the input is coupled via capacitor.

Voltage Controlled Oscillators

Figure 12 shows a voltage controlled triangle-square-wave-generator. With the indicated values a range from 2Hz to 200kHz is possible by varying I_{ABC} from 1mA to 10μA.

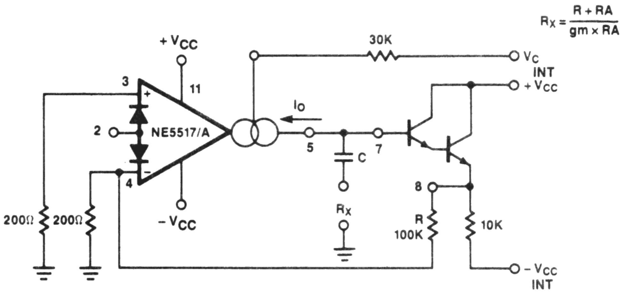

Rx = (R + RA)/(gm × RA)
+Vcc
30K
Vc
INT
+Vcc
3
11
IO
2
NE5517/A
5
C
7
4
8
200Ω
200Ω
-Vcc
RX
R
100K
10K
-Vcc
INT

Figure 6. VCR

DUAL OPERATIONAL TRANSCONDUCTANCE AMPLIFIER NE5517/5517A

The output amplitude is determined by $I_{OUT} \times R_{OUT}$.

Please notice the differential-input-voltage is not allowed to be above 5V.

With a slight modification of this circuit you can get the sawtooth-pulse-generator as shown in Figure 13.

Programmable Amplifier
The intention of the following application is to show how the NE5517 works in connection with a DAC. Almost all applications described above can be made digitally programmable (μP-compatible) in this way.

In the application Figure 14 the NE5118 is used, an eight-bit DAC with current output (see Section), its input-register makes this device fully μP-compatible.

The circuitry of Figure 14 consists of three functional blocks: the NE5118, which generates a control current equivalent to the applied data byte, a current mirror, and the NE5517.

The amplification is given by the following equation:

$$A = \frac{DW\,(10)}{256} \times \frac{I_{DAC}\ max}{2 \times V_T} \times R_L$$

DW (10) = Data word decimal
I_{DAC} max = Maximum DAC output current (here − 1mA)
R_L = Load resistance

The equation is only valid for the amplification of the signal directly applied to the OTA. To get the gain overall A must be multiplied with the input-attenuation factor.

APPLICATION HINTS:

To hold the transconductance gm within the linear range, I_{ABC} should be chosen not greater than 1mA. The current mirror ratio should be as accurate as possible over the entire current range. A current mirror with only two transistors is not recommended. A suitable current mirror can be built with a pnp-transistor array which causes excellent matching and thermal coupling among the transistors. The output current range of the DAC normally reaches from 0 . . . −2mA. In this application, however, the current range is set through R_{REF} (10KΩ) to 0 . . . −1mA.

$$I_{DAC}\ max = 2 \times \frac{V_{REF}}{R_{REF}} = 2 \times \frac{5V}{10K} = 1mA$$

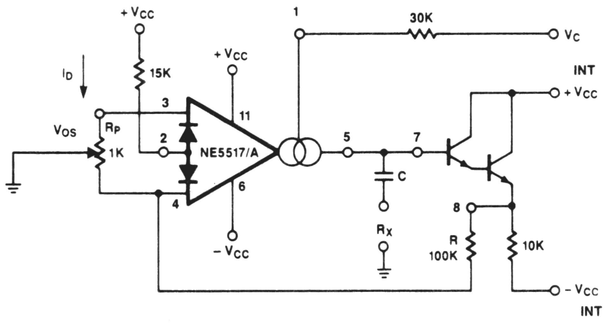
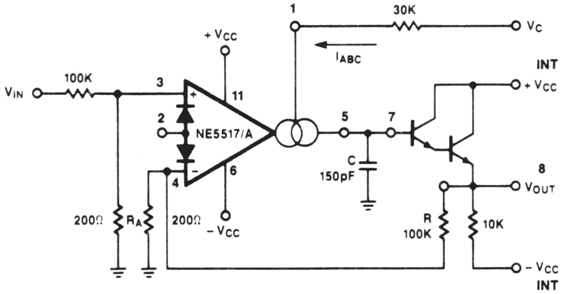

+Vcc
1
30K
Vc
+Vcc
ID
15K
INT
+Vcc
3
11
VOS
RP
1K
2
NE5517/A
5
7
C
6
4
8
RX
R
100K
10K
−Vcc
−Vcc
INT

Figure 7. VCR with Linearizing Diodes


1
30K
Vc
+Vcc
IABC
INT
+Vcc
100K
3
VIN
11
2
NE5517/A
5
7
C
150pF
8
VOUT
4
6
200Ω
RA
200Ω
−Vcc
R
100K
10K
−Vcc
INT

$$f_o = \frac{R_A \times gm}{(R + RA) \times 2\pi C}$$

Figure 8. Voltage Controlled Low Pass Filter

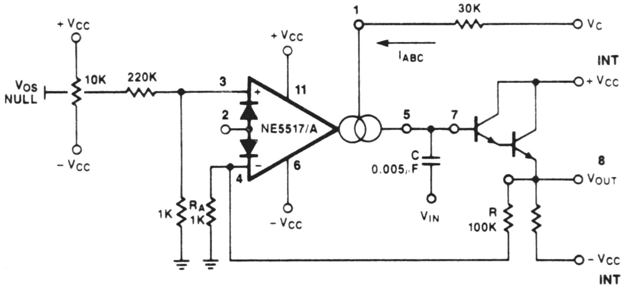

1
30K
Vc
+Vcc
+Vcc
IABC
INT
+Vcc
VOS
NULL
10K
220K
3
11
2
NE5517/A
5
7
−Vcc
C
0.005μF
8
VOUT
4
6
1K
RA
1K
VIN
R
100K
−Vcc
−Vcc
INT

Figure 9. Voltage Controlled High Pass Filter

DUAL OPERATIONAL TRANSCONDUCTANCE AMPLIFIER NE5517/5517A

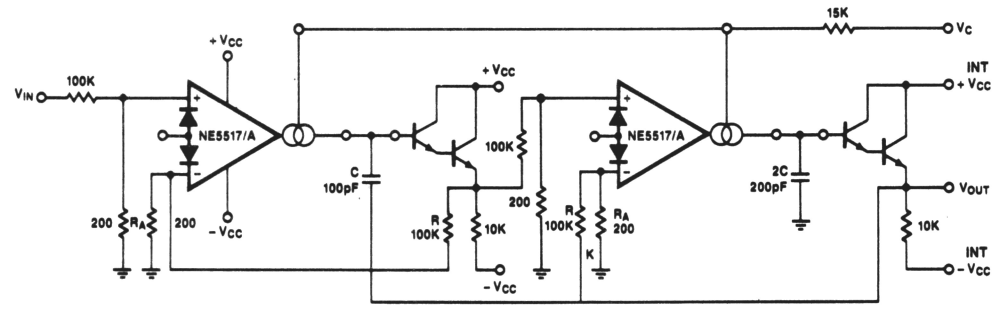

15K
VC
+VCC
VIN
100K
NE5517/A
+VCC
C
100pF
100K
R
100K
10K
-VCC
200
RA
200
-VCC
200
R
100K
K
RA
200
NE5517/A
2C
200pF
INT
+VCC
VOUT
10K
INT
-VCC

Figure 10. Butterworth Filter — 2nd Order

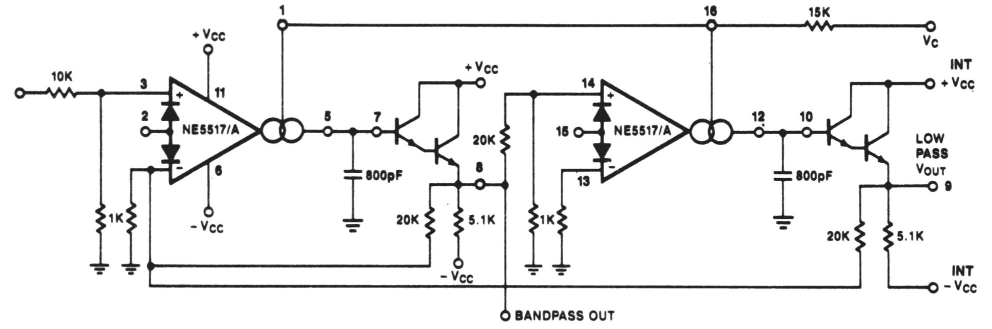

1
16
15K
VC
+VCC
10K
3
2
11
NE5517/A
6
-VCC
1K
5
7
800pF
+VCC
20K
8
20K
5.1K
-VCC
14
15
NE5517/A
13
1K
12
10
800pF
INT
+VCC
LOW
PASS
VOUT
9
20K
5.1K
INT
-VCC
BANDPASS OUT

Figure 11. State Variable Filter

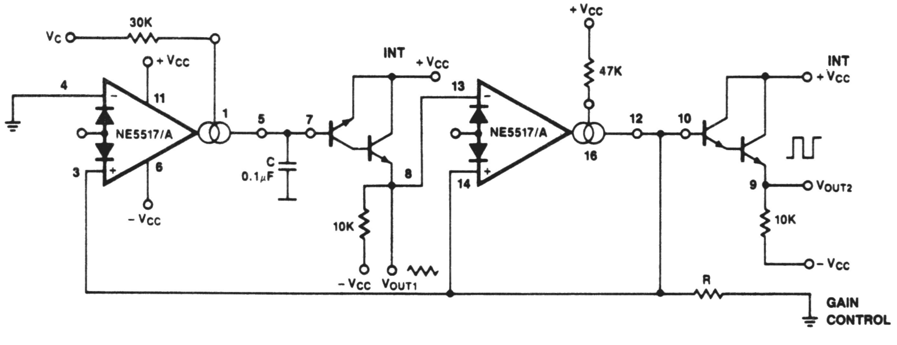
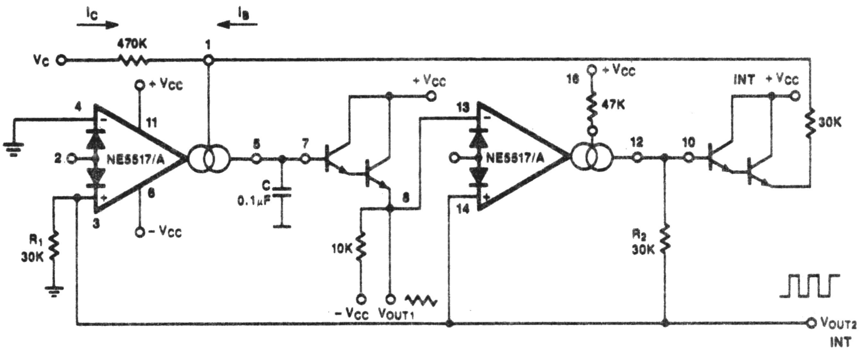

VC
30K
+VCC
4
11
NE5517/A
3
6
-VCC
1
5
7
C
0.1μF
INT
+VCC
8
10K
-VCC
VOUT1
+VCC
47K
13
NE5517/A
14
16
12
10
INT
+VCC
9
VOUT2
10K
-VCC
R
GAIN
CONTROL

Figure 12. Triangle-Squarewave-Generator (VCO)


I_C
I_B
470K
1
V_C
+ V_{CC}
4
11
2
NE5517/A
5
7
C
0.1μF
8
6
3
- V_{CC}
R_1
30K
+ V_{CC}
13
NE5517/A
14
16
+ V_{CC}
47K
12
10
INT + V_{CC}
30K
10K
R_2
30K
- V_{CC}
V_{OUT1}
V_{OUT2}
INT

$$V_{PK} = \frac{(V_S - 0.8)\ R_1}{R_1 + R_2}\ T_H = \frac{2V_{PK} \times C}{I_B}\ T_L = \frac{2V_{PK} \times C}{I_C}\ f_{osc}\ \frac{I_C}{2V_{PK} \times C}\quad I_C << I_B$$

Figure 13. Sawtooth-Pulse-VCO

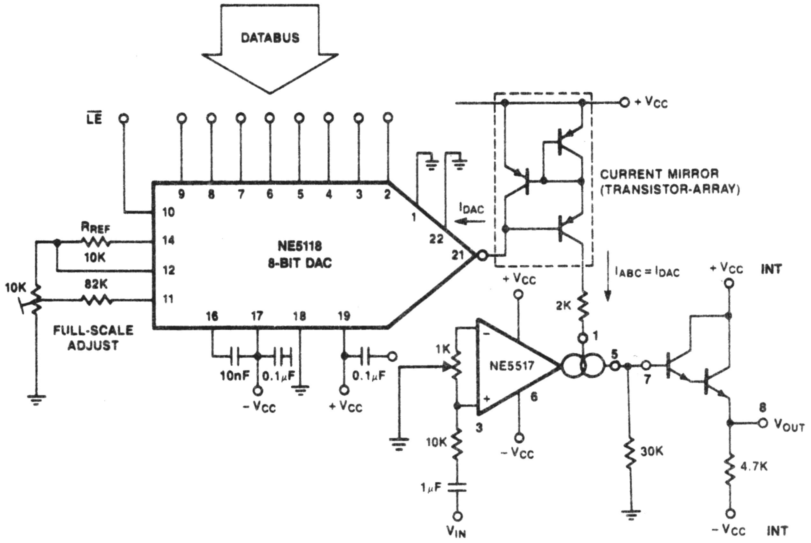

DATABUS
$\overline{LE}$
9
8
7
6
5
4
3
2
1
22
21
10
14
12
11
R_{REF}
10K
82K
10K
FULL-SCALE ADJUST
NE5118
8-BIT DAC
16
17
18
19
10nF
0.1μF
0.1μF
- V_{CC}
+ V_{CC}
I_{DAC}
+ V_{CC}
CURRENT MIRROR
(TRANSISTOR-ARRAY)
$I_{ABC} = I_{DAC}$
+ V_{CC}
2K
1
+ V_{CC} INT
1K
NE5517
5
7
6
3
8
V_{OUT}
10K
1μF
V_{IN}
- V_{CC}
30K
4.7K
- V_{CC} INT

Figure 14. Digital Programmable Amplifier

*For additional information, consult the Applications Section.

ULTRA HIGH FREQUENCY OPERATIONAL AMPLIFIER

SE/NE5539

DESCRIPTION

The Signetics SE/NE5539 is a very wide bandwidth, high slew rate, monolithic operational amplifier for use in video amplifiers, RF amplifiers, and extremely high slew rate amplifiers.

Emitter follower inputs provide a true differential high input impedance device. Proper external compensation will allow design operation over a wide range of closed loop gains, both inverting and non-inverting, to meet specific design requirements.

FEATURES

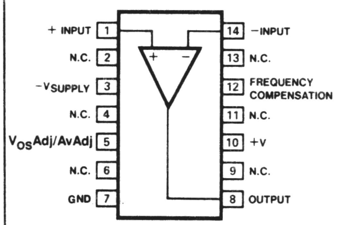
- **Gain bandwidth product: 1.2GHz at 17dB**
- **Slew rate: 600/Vμsec**
- **Full power response: 48MHz**
- **A_{VOL}: 52dB typical**
- **350MHz unity gain**

APPLICATIONS

- **Fast pulse amplifiers**
- **RF oscillators**
- **Fast sample and hold**
- **High gain video amplifiers (BW > 20MHz)**

PIN CONFIGURATION

D,F,N PACKAGE



+ INPUT 1
N.C. 2
$-V_{SUPPLY}$ 3
N.C. 4
V_{OS}Adj/AvAdj 5
N.C. 6
GND 7
14 −INPUT
13 N.C.
12 FREQUENCY COMPENSATION
11 N.C.
10 +V
9 N.C.
8 OUTPUT
+
−

TOP VIEW

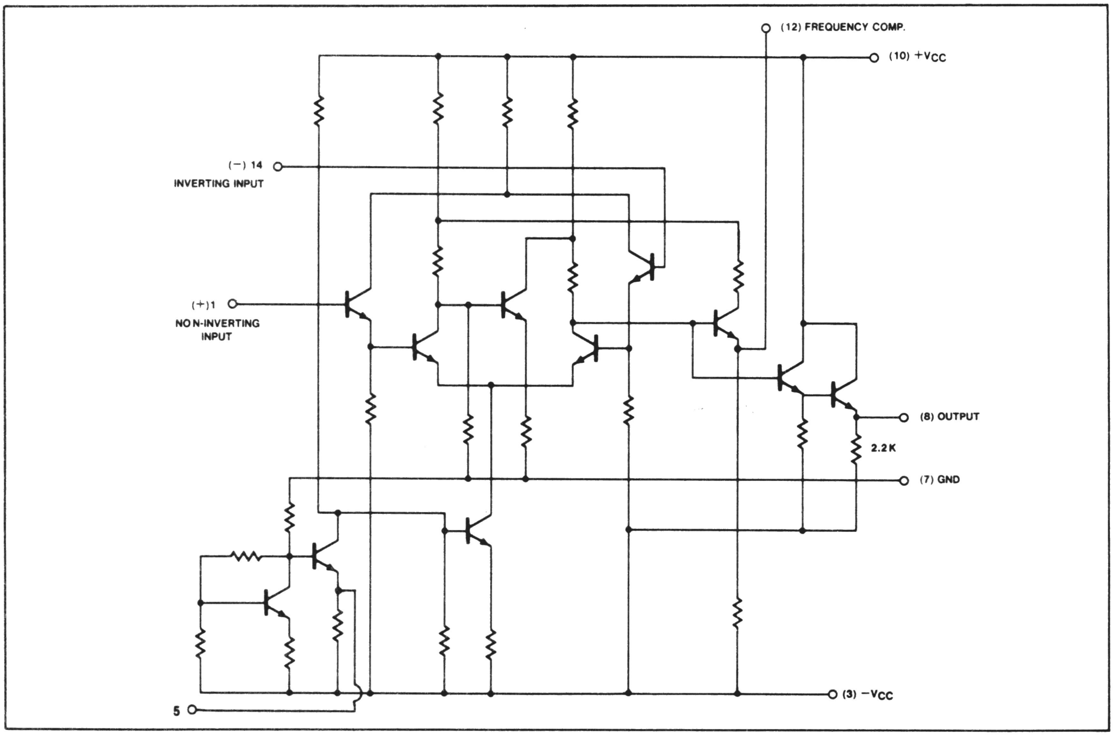
ORDER NUMBERS

SE/NE5539F SE/NE5539N
NE5539D

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	± 12	V
P_D	Internal power dissipation	550	mW
T_{STG}	Storage temperature range	−65 to +150	°C
T_J	Max junction temperature	150	°C
T_A	Operating temperature range		
	NE	0 to 70	°C
	SE	−55 to +125	°C
	Lead temperature	300	°C

EQUIVALENT CIRCUIT



(12) FREQUENCY COMP.
(10) $+V_{CC}$
(−) 14
INVERTING INPUT
(+)1
NON-INVERTING INPUT
(8) OUTPUT
2.2 K
(7) GND
(3) $-V_{CC}$
5

ULTRA HIGH FREQUENCY OPERATIONAL AMPLIFIER SE/NE5539

DC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $T_A = 25°C$ unless otherwise specified

PARAMETER		TEST CONDITIONS		SE5539			NE5539			UNIT
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$V_O = 0V$, $R_S = 100\Omega$	Over temp		2	5				mV
			$T_A = 25°C$		2	3		2.5	5	
$\Delta V_{OS}/\Delta T$					5			5		µV/°C
I_{OS}	Input offset current		Over temp		.1	3				µA
			$T_A = 25°C$		.1	1			2	
$\Delta I_{OS}/\Delta T$					.5			.5		nA/°C
I_B	Input bias current		Over temp		6	25				µA
			$T_A = 25°C$		5	13		5	20	
$\Delta I_B/\Delta T$					10			10		nA/°C
CMRR	Common mode rejection ratio	$F = 1kHz$, $R_S = 100\Omega$, V_{CM} ± 1.7V		70	80		70	80		dB
			Over temp	70	80					dB
R_{IN}	Input impedance				100			100		kΩ
R_{OUT}	Output impedance				10			10		Ω
V_{OUT}	Output voltage swing	$R_L = 150\Omega$ to GND and 470Ω to $-V_{CC}$	+Swing				+2.3	+2.7		V
			−Swing				−1.7	−2.2		
V_{OUT}	Output voltage swing	$R_L = 2k\Omega$ to GND, Over temp	+Swing	+2.3	+3.0					V
			−Swing	−1.5	−2.1					
		$T_A = 25°C$	+Swing	+2.5	+3.1					V
			−Swing	−2.0	−2.7					
$I_{CC}+$	Positive supply current	$V_O = 0$, $R_1 = \infty$	Over temp		14	18				mA
			$T_A = 25°C$		14	17		14	18	
$I_{CC}-$	Negative supply current	$V_O = 0$, $R_1 = \infty$	Over temp		11	15				mA
			$T_A = 25°C$		11	14		11	15	
PSRR	Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$	Over temp		300	1000				µV/V
			$T_A = 25°C$					200	1000	
A_{VOL}	Large signal voltage gain	$V_O = +2.3V, -1.7V$ $R_L = 150\Omega$ to GND, 470Ω to $-V_{CC}$					47	52	57	dB
A_{VOL}	Large signal voltage gain	$V_O = +2.3V, -1.7V$ $R_L = 2K$ to GND								dB
			$T_A = 25°C$				47	52	57	
A_{VOL}	Large signal voltage gain	$V_O = +2.5V, -2.0V$ $R_L = 2k\Omega$ to GND	Over temp	46		60				dB
			$T_A = 25°C$	48	53	58				

NOTE

1. Differential input voltage should not exceed 0.25 volts to prevent excessive input bias current and common mode voltage 2.5 volts. These voltage limits may be exceeded if current limit is 10mA.

ULTRA HIGH FREQUENCY OPERATIONAL AMPLIFIER SE/NE5539

AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $R_L = 150\Omega$ to GND & 470Ω to $-V_{CC}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE5539			NE5539			UNIT
		Min	Typ	Max	Min	Typ	Max	
Gain bandwidth product	$A_{CL} = 7$ $V_O = 0.1$ Vp-p		1200			1200		MHz
Small signal bandwidth	$A_{CL} = 2$ $R_L = 150\Omega^1$		110			110		MHz
Settling time	$A_{CL} = 2$ $R_L = 150\Omega^1$		15			15		nSec
Slew rate	$A_{CL} = 2$ $R_L = 150\Omega^1$		600			600		V/μSec
Propagation delay	$A_{CL} = 2$ $R_L = 150\Omega^1$		7			7		nSec
Full power response	$A_{CL} = 2$ $R_L = 150\Omega^1$		48			48		MHz
Full power response	$A_V = 7$, $R_L = 150\Omega$		20			20		MHz
Input noise voltage	$R_S = 50\Omega$		4			4		nV/$\sqrt{Hz}$

NOTE 1: External compensation.

DC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 6V$, $T_A = 25°C$ unless otherwise specified

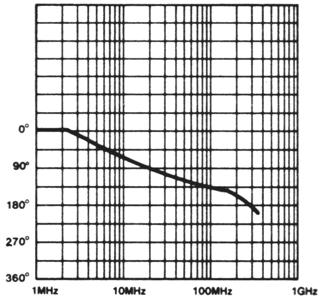
PARAMETERS		TEST CONDITIONS			SE5539			UNIT
					Min	Typ	Max	
V_{OS}	Input offset voltage			Over temp		2	5	mV
				$T_A = 25°C$		2	3	
I_{OS}	Input offset current			Over temp		.1	3	μA
				$T_A = 25°C$		.1	1	
I_B	Input bias current			Over temp		5	20	μA
				$T_A = 25°C$		4	10	
CMRR	Common mode rejection ratio	$V_{CM} = \pm 1.3V$, $R_S = 100\Omega$			70	85		dB
$I_{CC}+$	Positive supply current			Over temp		11	14	mA
				$T_A = 25°C$		11	13	
$I_{CC}-$	Negative supply current			Over temp		8	11	mA
				$T_A = 25°C$		8	10	
PSRR	Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$		Over temp		300	1000	μV/V
				$T_A = 25°C$				
V_{OUT}	Output voltage swing	$R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$	Over temp	+ Swing	+ 1.4	+ 2.0		V
				− Swing	− 1.1	− 1.7		
			$T_A = 25°C$	+ Swing	+ 1.5	+ 2.0		
				− Swing	− 1.4	− 1.8		

AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 6V$, $R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$ unless otherwise specified

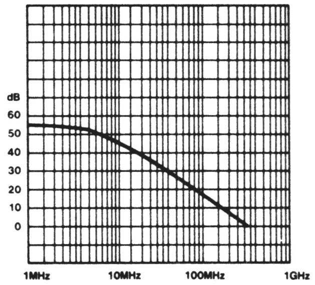
PARAMETER	TEST CONDITIONS	SE5539			UNIT
		Min	Typ	Max	
Gain bandwidth product	$A_{CL} = 7$		700		MHz
Small signal bandwidth	$A_{CL} = 2^1$		120		MHz
Settling time	$A_{CL} = 2^1$		23		ns
Slew rate	$A_{CL} = 2^1$		330		V/μs
Propagation delay	$A_{CL} = 2^1$		4.5		ns
Full power response	$A_{CL} = 2^1$		20		MHz

NOTE 1: External compensation.

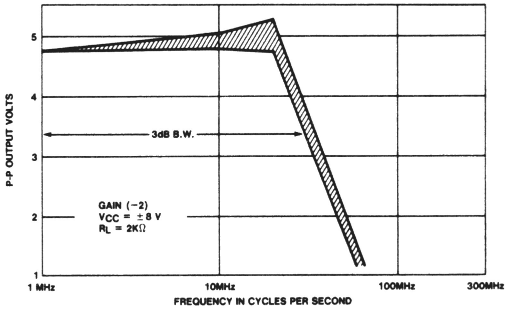
NE5539 OPEN LOOP PHASE



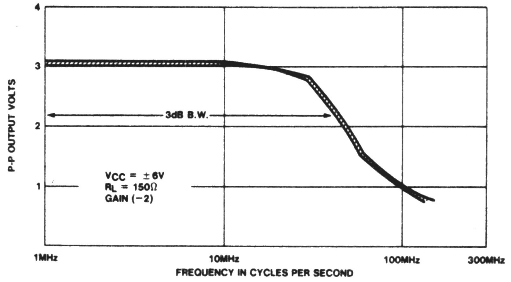
NE5539 OPEN LOOP GAIN



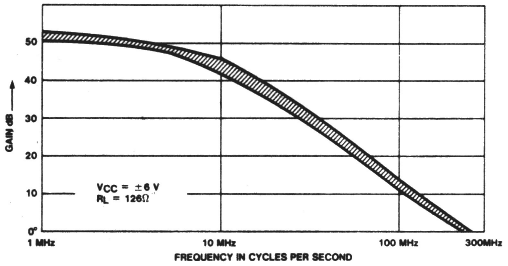
POWER BANDWIDTH (SE)



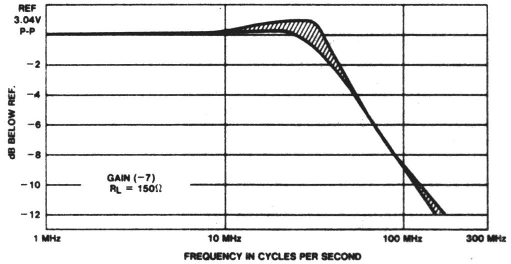
POWER BANDWIDTH (NE)



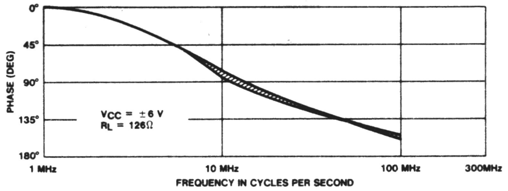
SE5539 OPEN LOOP GAIN vs FREQUENCY



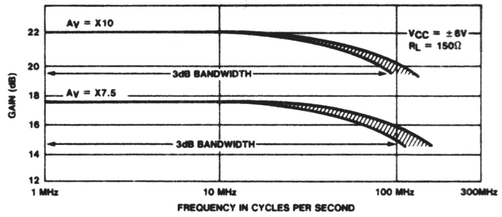
POWER BANDWIDTH



SE5539 OPEN LOOP PHASE vs FREQUENCY



GAIN BANDWIDTH PRODUCT vs FREQUENCY



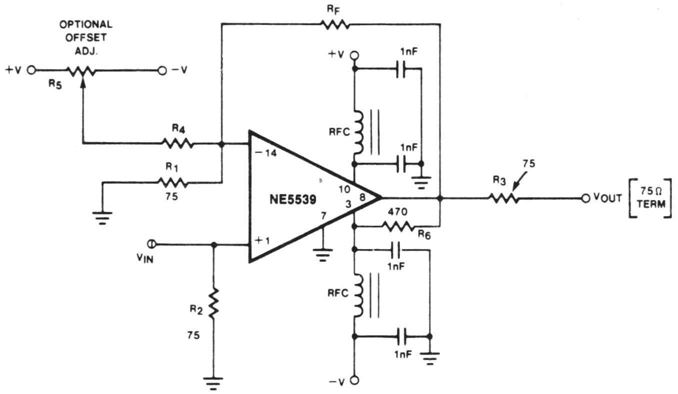
NOTE

▨ Indicates typical distribution −55°C ≤ T_A ≤ 125°C

6

CIRCUIT LAYOUT CONSIDERATIONS

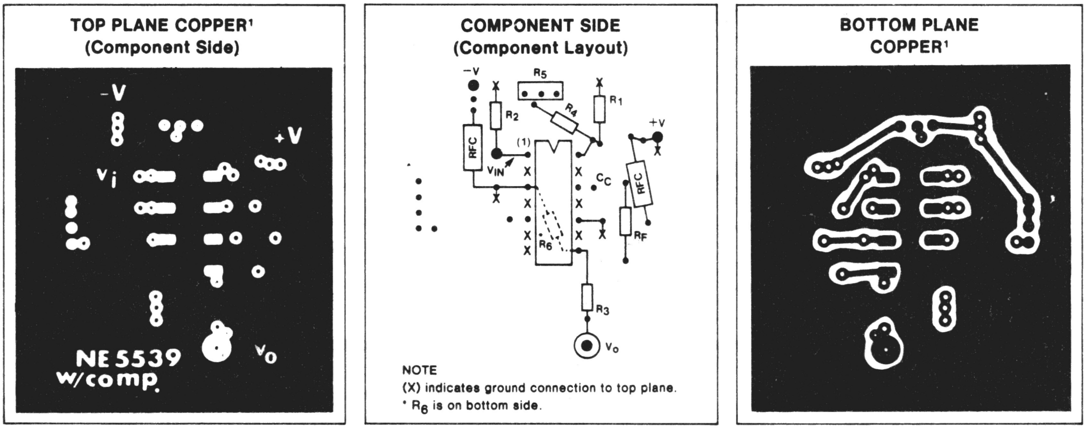
As may be expected for an ultra-high frequency, wide gain bandwidth amplifier, the physical circuit layout is extremely critical. Breadboarding is not recommended. A double-sided copper clad printed circuit board will result in more favorable system operation. An example utilizing a 28dB non-inverting amp is shown in Figure 1.


OPTIONAL OFFSET ADJ.
+V
R5
−V
RF
+V
1nF
RFC
1nF
R4
R1
75
−14
NE5539
10
3
8
7
+1
VIN
470
R6
1nF
RFC
R2
75
1nF
−V
75
R3
VOUT
75Ω TERM

R1 = 75Ω 5% CARBON
R2 = 75Ω 5% CARBON
R3 = 75Ω 5% CARBON
R4 = 36K 5% CARBON

R5 = 20K TRIMPOT (CERMET)
RF = 1.5K (28dB GAIN)
R6 = 470Ω 5% CARBON

RFC 3T # 26 BUSSWIRE ON
FERROXCUBE VK 200 09/3B CORE
BYPASS CAPACITORS
1nF CERAMIC
(MEPCO OR EQUIV.)


−V
+V
Vi
NE5539
w/comp.
Vo
−V
R5
R1
R2
R4
+V
RFC
(1)
VIN
X
CC
RFC
RF
R6
R3
Vo

TOP PLANE COPPER¹ (Component Side)

COMPONENT SIDE (Component Layout)

NOTE
(X) indicates ground connection to top plane.
* R6 is on bottom side.

BOTTOM PLANE COPPER¹

NOTE 1: Bond edges of top and bottom ground plane copper.

Figure 1. 28dB Non-Inverting Amp Sample P.C. Layout

ULTRA HIGH FREQUENCY OPERATIONAL AMPLIFIER SE/NE5539

NE5539 COLOR VIDEO AMPLIFIER

The NE5539 wideband operational **amplifier** is easily adapted for use as a color **video** amplifier. A typical circuit is shown in **Figure** 2 along with vector-scope[1] photographs showing the amplifier differential gain and phase response to a standard five step modulated staircase linearity signal (Figures 3, 4 and 5). As can be seen in Figure 4, the gain varies less than 0.5% from the bottom to the top of the staircase. The maximum differential phase shown in Figure 5 is approximately +0.1°.

The amplifier circuit was optimized for a 75Ω input and output termination impedance with a gain of approximately 10 (20dB).

NOTE
The input signal was 200mV and the output 2V. V_{CC} was ±8V.

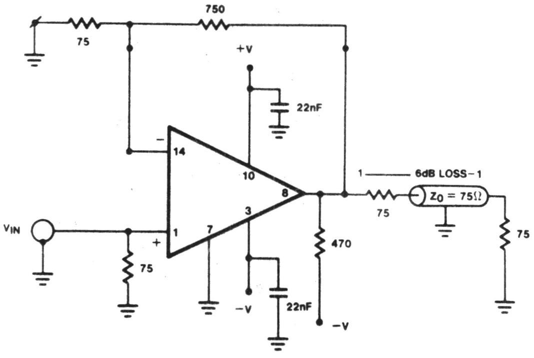


Figure 2. NE5539 Video Amplifier

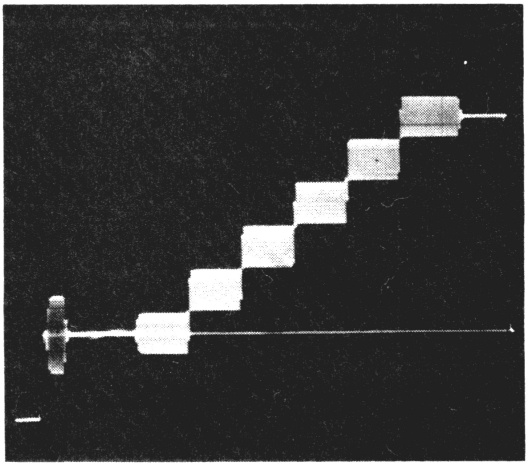


Figure 3. Input Signal

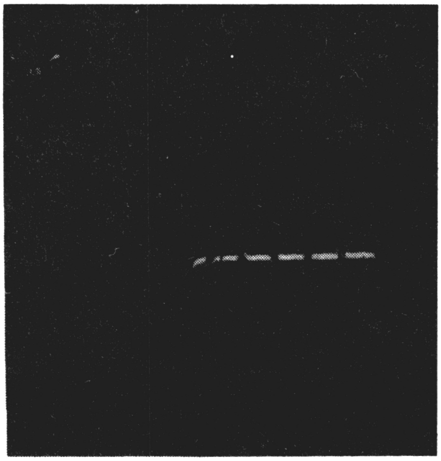


Figure 4. Differential Gain <0.5%

NOTE:
1. Instruments used for these measurements were Tektronix, 146 NTSC test signal generator, 520A NTSC vectorscope, and 1480 waveform monitor.

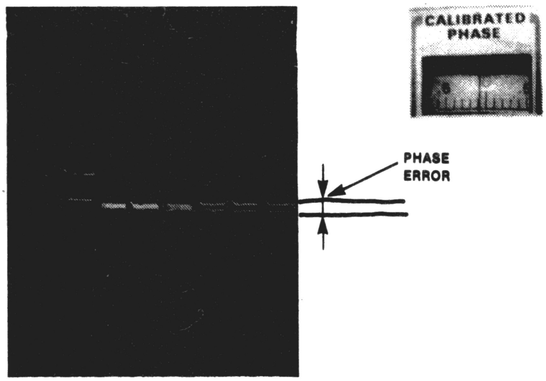
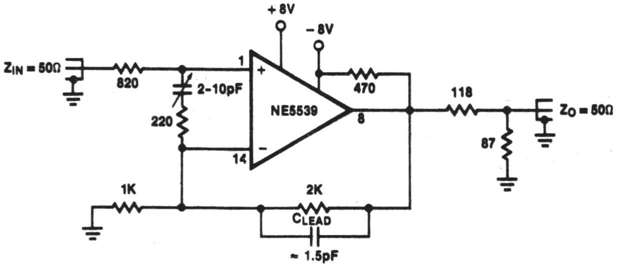

CALIBRATED PHASE
PHASE ERROR

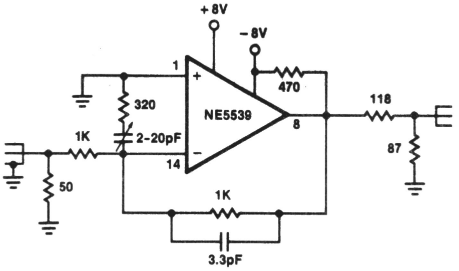
Figure 5. Differential Phase + 0.1°

APPLICATIONS


+8V
−8V
$Z_{IN} = 50\Omega$
820
2-10pF
220
1
14
NE5539
8
470
118
87
$Z_O = 50\Omega$
1K
2K
C_{LEAD}
≈ 1.5pF

[NON-INVERTING FOLLOWER]

Figure 6


+8V
−8V
1
320
2-20pF
1K
14
50
NE5539
8
470
118
87
1K
3.3pF

[INVERTING FOLLOWER]

Figure 7

*For additional information, consult the Applications Section.

VIDEO AMPLIFIER

NE5592

DESCRIPTION

The NE5592 is a dual monolithic, two stage, differential output, wideband video amplifier. It offers fixed gain of 400 without external components or adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers.

FEATURES

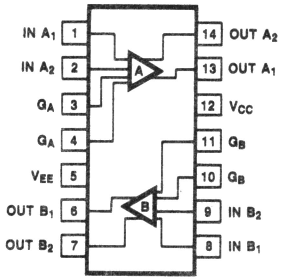
- **120MHz bandwidth**
- **Adjustable gains from 0 to 400**
- **Adjustable pass band**
- **No frequency compensation required**
- **Wave shaping with minimal external components**

APPLICATIONS

- **Floppy disk head amplifier**
- **Video amplifier**
- **Pulse amplifier in communications**
- **Magnetic memory**
- **Video recorder systems**

PIN CONFIGURATION

D,N PACKAGE


IN A_1 1
IN A_2 2
G_A 3
G_A 4
V_{EE} 5
OUT B_1 6
OUT B_2 7
IN B_1 8
IN B_2 9
G_B 10
G_B 11
V_{CC} 12
OUT A_1 13
OUT A_2 14
A
B

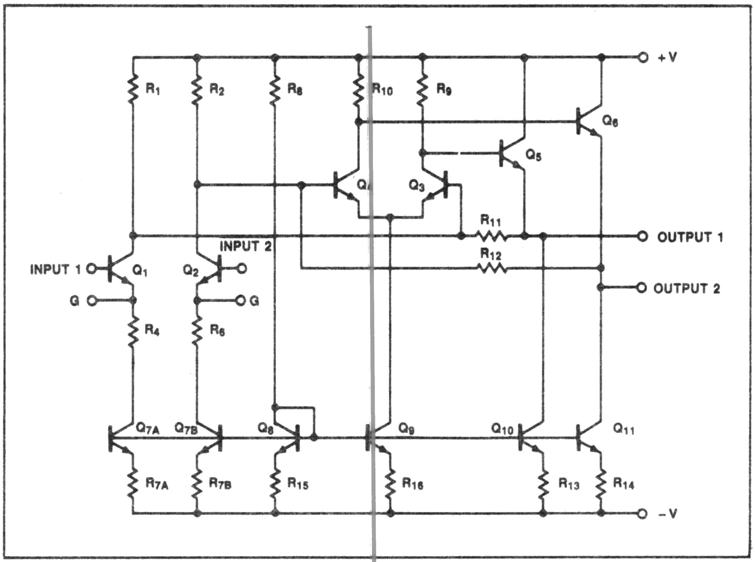
TOP VIEW

ORDER NUMBER
NE5592D, NE5592N

ABSOLUTE MAXIMUM RATINGS $T_A = 25°C$ unless otherwise specified.

SYMBOL AND PARAMETER	RATING	UNIT
Supply voltage	±8	V
Differential input voltage	±5	V
Common mode input voltage	±6	V
Output current	10	mA
Operating temperature range NE5592	0 to +70	°C
Storage temperature range	−65 to +150	°C
Power dissipation	500	mW

EQUIVALENT CIRCUIT


+V
R_1
R_2
R_8
R_{10}
R_9
Q_6
Q_5
Q_4
Q_3
R_{11}
R_{12}
OUTPUT 1
OUTPUT 2
INPUT 2
INPUT 1
Q_1
Q_2
G
G
R_4
R_6
Q_{7A}
Q_{7B}
Q_8
Q_9
Q_{10}
Q_{11}
R_{7A}
R_{7B}
R_{15}
R_{16}
R_{13}
R_{14}
−V

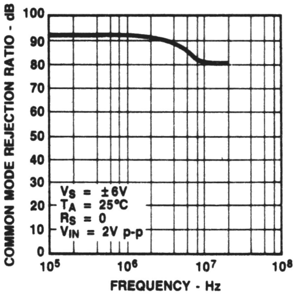
DC ELECTRICAL CHARACTERISTICS

$T_A = +25°C, V_{SS} = \pm 6V, V_{CM} = 0$ unless otherwise specified. Recommended operating supply voltage $V_S = \pm 6.0V$. Gain select pins connected together.

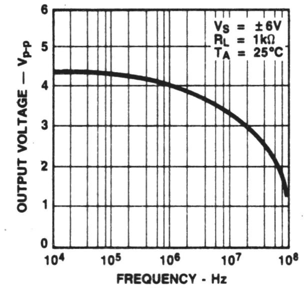
PARAMETER	TEST CONDITIONS	NE5592			UNITS
		Min	Typ	Max	
Differential voltage gain	$R_L = 2k\Omega$, $V_{OUT} = 3V$ p-p	400	480	600	V/V
Bandwidth	$V_{OUT} = 1V$ p-p		25		MHz
Rise time			15	20	ns
Propagation delay	$V_{OUT} = 1V$ p-p		7.5	12	ns
Input resistance		3	14		kΩ
Input capacitance			2.5		pF
Input offset current			0.3	3	μA
Input bias current			5	20	μA
Input noise voltage	BW 1kHz to 10MHz		4		nV/√Hz
Input voltage range				±1.0	V
Common mode rejection ratio	$V_{CM} \pm 1V$, $f < 100kHz$	60	93		dB
	$V_{CM} \pm 1V$, $f = 5MHz$		87		dB
Supply voltage rejection ratio	$\Delta V_S = \pm 0.5V$	50	85		dB
Channel separation	$V_{OUT} = 1V$ p-p; $f = 100kHz$ (output referenced) $R_L = 1k\Omega$	65	75		dB
Output offset voltage	$R_L = \infty$		0.5	1.5	V
Gain select pins open	$R_L = \infty$		0.25	0.75	V
Output common mode voltage	$R_L = \infty$	2.4	3.1	3.4	V
Output differential voltage swing	$R_L = 2k\Omega$	3.0	4.0		V
Output resistance			20		Ω
Power supply current (Total for both sides)	$R_L = \infty$		35	44	mA
THE FOLLOWING SPECS APPLY OVER TEMPERATURE		**$0°C \le T_A \le 70°C$**			
Differential voltage gain	$R_L = 2k\Omega$, $V_{OUT} = 3V$ p-p	350	430	600	V/V
Input resistance		1	11		kΩ
Input offset current				5	μA
Input bias current				30	μA
Input voltage range				±1.0	V
Common mode rejection ratio	$V_{CM} \pm 1V$, $f < 100kHz$	55			dB
	$R_S = \phi$				
Supply voltage rejection ratio	$\Delta V_S = \pm 0.5V$	50			dB
Channel separation	$V_{OUT} = 1V$ p-p; $f = 100kHz$ (output referenced) $R_L = 1k\Omega$		75		dB
Output offset voltage					
Gain select pins connected together	$R_L = \infty$			1.5	V
Gain select pins open	$R_L = \infty$			1.0	V
Output differential voltage swing	$R_L = 2k\Omega$	2.8			V
Power supply current (Total for both sides)	$R_L = \infty$			47	mA

TYPICAL PERFORMANCE CHARACTERISTICS

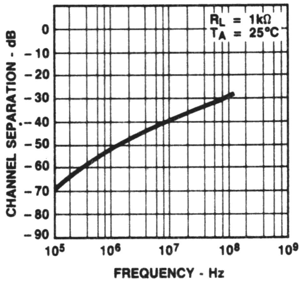
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



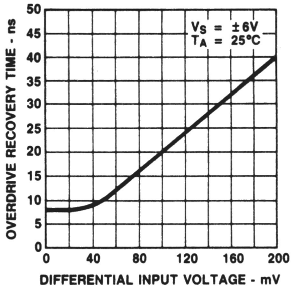
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



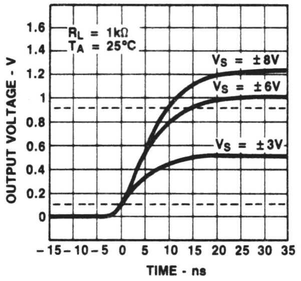
CHANNEL SEPARATION AS A FUNCTION OF FREQUENCY



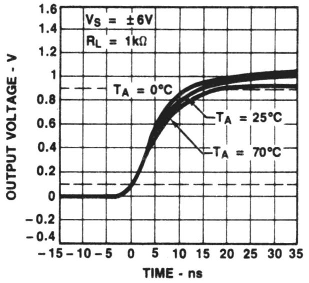
DIFFERENTIAL OVERDRIVE RECOVERY TIME



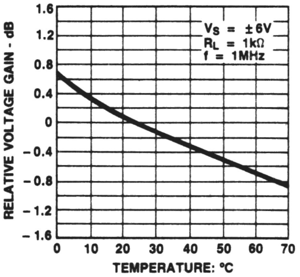
PULSE RESPONSE AS A FUNCTION OF SUPPLY VOLTAGE



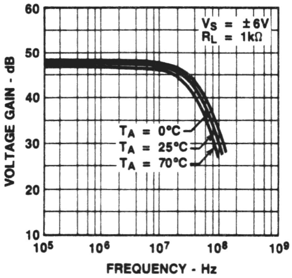
PULSE RESPONSE AS A FUNCTION OF TEMPERATURE



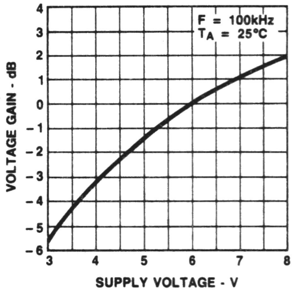
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



GAIN vs FREQUENCY AS A FUNCTION OF TEMPERATURE

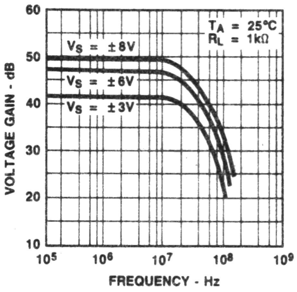


VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

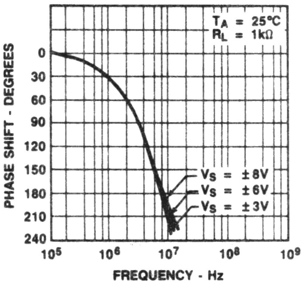


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

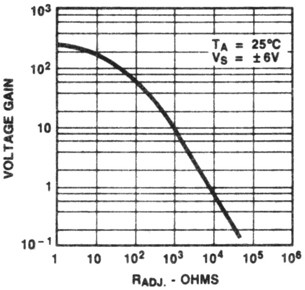
GAIN vs FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



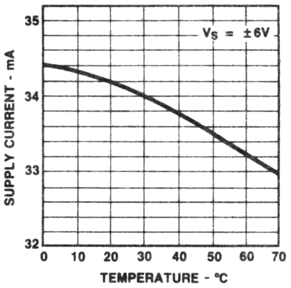
PHASE vs FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



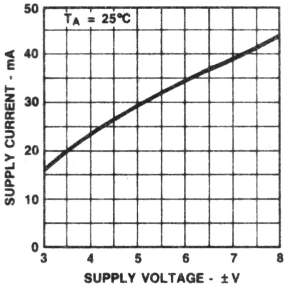
VOLTAGE GAIN AS A FUNCTION OF $R_{ADJ.}$



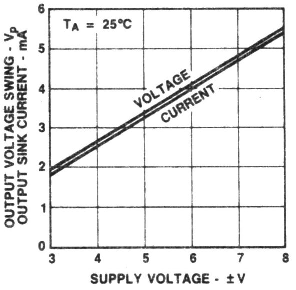
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



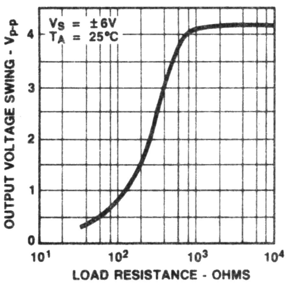
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



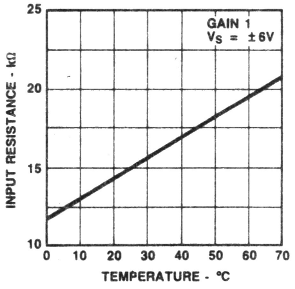
OUTPUT VOLTAGE SWING AND SINK CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



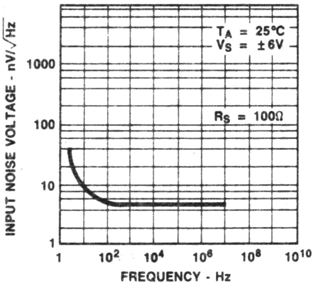
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



INPUT RESISTANCE AS A FUNCTION OF TEMPERATURE

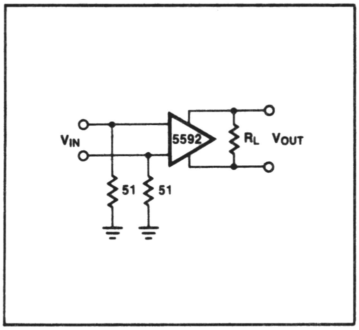


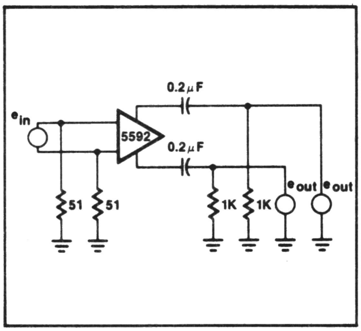
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY

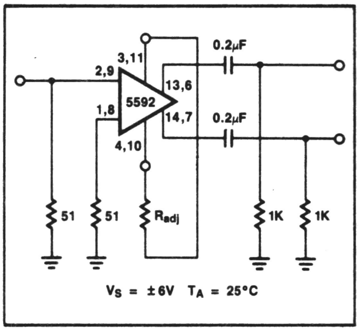


TEST CIRCUITS

T_A = 25°C unless otherwise specified


V_IN
5592
R_L
V_OUT
51
51


e_in
5592
0.2μF
0.2μF
51
51
1K
1K
e_out
e_out


3,11
2,9
1,8
5592
13,6
14,7
4,10
0.2μF
0.2μF
51
51
R_adj
1K
1K
V_S = ±6V T_A = 25°C

VIDEO AMPLIFIER

SE/NE592

DESCRIPTION

The SE/NE592 is a monolithic, two stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disk head amplifiers. Now available in an 8-pin version with fixed gain of 400 without external components and adjustable gain from 400 to 0 with one external resistor.

FEATURES

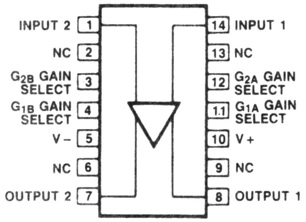
- **120MHz bandwidth**
- **Adjustable gains from 0 to 400**
- **Adjustable pass band**
- **No frequency compensation required**
- **Wave shaping with minimal external components**

APPLICATIONS

- **Floppy disk head amplifier**
- **Video amplifier**
- **Pulse amplifier in communications**
- **Magnetic memory**
- **Video recorder systems**

PIN CONFIGURATION

D14, F14, N14 PACKAGE

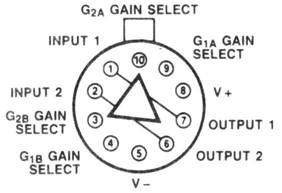

INPUT 2 1
NC 2
G_{2B} GAIN SELECT 3
G_{1B} GAIN SELECT 4
V− 5
NC 6
OUTPUT 2 7
14 INPUT 1
13 NC
12 G_{2A} GAIN SELECT
11 G_{1A} GAIN SELECT
10 V+
9 NC
8 OUTPUT 1

TOP VIEW

ORDER NUMBERS

NE592D14 NE592N14
NE592F14 SE592F14

H PACKAGE*


G_{2A} GAIN SELECT
INPUT 1
G_{1A} GAIN SELECT
INPUT 2
V+
G_{2B} GAIN SELECT
OUTPUT 1
G_{1B} GAIN SELECT
OUTPUT 2
V−
1
2
3
4
5
6
7
8
9
10

NOTE
Pin 5 connected to case

ORDER NUMBERS

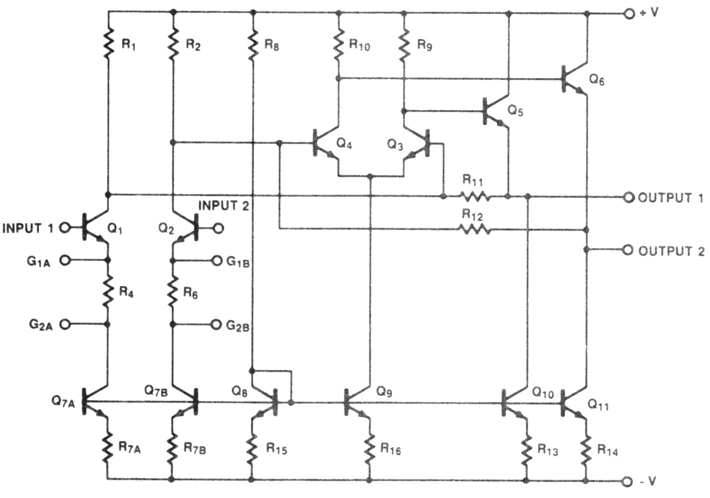
NE592H SE592H

*Metal cans (H) not recommended for new designs.

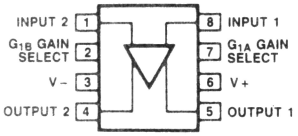
ABSOLUTE MAXIMUM RATINGS $T_A = +25°C$ unless otherwise specified.

SYMBOL AND PARAMETER	RATING	UNIT
Supply voltage	±8	V
Differential input voltage	±5	V
Common mode		
Input voltage	±6	V
Output current	10	mA
Operating temperature range		
SE592	−55 to +125	°C
NE592	0 to +70	°C
Storage temperature range	−65 to +150	°C
Power dissipation	500	mW

EQUIVALENT CIRCUIT


+V
R_1
R_2
R_8
R_{10}
R_9
Q_6
Q_5
Q_4
Q_3
R_{11}
OUTPUT 1
R_{12}
OUTPUT 2
INPUT 2
INPUT 1
Q_1
Q_2
G_{1A}
G_{1B}
R_4
R_6
G_{2A}
G_{2B}
Q_{7A}
Q_{7B}
Q_8
Q_9
Q_{10}
Q_{11}
R_{7A}
R_{7B}
R_{15}
R_{16}
R_{13}
R_{14}
−V

D8, F8, N8 PACKAGE


INPUT 2 1
G_{1B} GAIN SELECT 2
V− 3
OUTPUT 2 4
8 INPUT 1
7 G_{1A} GAIN SELECT
6 V+
5 OUTPUT 1

TOP VIEW

ORDER NUMBERS

NE592D8 NE592N8
NE592F8 SE592F8

Also N8, N14, D8 and D14 package parts available in "High" gain version by adding "H" before package designation, as: NE592HD8.

VIDEO AMPLIFIER

SE/NE592

DC ELECTRICAL CHARACTERISTICS: $T_A = +25°C$, $V_{SS} = \pm 6V$, $V_{CM} = 0$ unless otherwise specified. Recommended operating supply voltages $V_S = \pm 6.0V$. All specifications apply to both standard and high gain parts unless noted differently.

PARAMETER	TEST CONDITIONS	NE592 Min	NE592 Typ	NE592 Max	SE592 Min	SE592 Typ	SE592 Max	UNIT
Differential voltage gain, standard part								
Gain 1[1]	$R_L = 2k\Omega$, $V_{OUT} = 3V$ p-p	250	400	600	300	400	500	V/V
Gain 2[2,4]		80	100	120	90	100	110	V/V
High gain part		400	500	600				V/V
Bandwidth								
Gain 1[1]			40			40		MHz
Gain 2[2,4]			90			90		MHz
Rise time								
Gain 1[1]	$V_{OUT} = 1V$ p-p		10.5			10.5		ns
Gain 2[2,4]			4.5	12		4.5	10	ns
Propagation delay								
Gain 1[1]	$V_{OUT} = 1V$ p-p		7.5			7.5		ns
Gain 2[2,4]			6.0	10		6.0	10	ns
Input resistance								
Gain 1[1]			4.0			4.0		kΩ
Gain 2[2,4]		10	30		20	30		kΩ
Input capacitance[2]	Gain 2[4]		2.0			2.0		pF
Input offset current			0.4	5.0		0.4	3.0	μA
Input bias current			9.0	30		9.0	20	μA
Input noise voltage	BW 1kHz to 10MHz		12			12		μVrms
Input voltage range				±1.0			±1.0	V
Common mode rejection ratio								
Gain 2[4]	$V_{CM} \pm 1V$, f<100kHz	60	86		60	86		dB
Gain 2[4]	$V_{CM} \pm 1V$, f = 5MHz		60			60		dB
Supply voltage rejection ratio								
Gain 2[4]	$\Delta V_S = \pm 0.5V$	50	70		50	70		dB
Output offset voltage								
Gain 1	$R_L = \infty$			1.5			1.5	V
Gain 2[4]	$R_L = \infty$			1.5			1.0	V
Gain 3[3]	$R_L = \infty$		0.35	0.75		0.35	0.75	V
Output common mode voltage	$R_L = \infty$	2.4	2.9	3.4	2.4	2.9	3.4	V
Output voltage swing differential	$R_L = 2k\Omega$	3.0	4.0		3.0	4.0		V
Output resistance			20			20		Ω
Power supply current	$R_L = \infty$		18	24		18	24	mA
THE FOLLOWING SPECS APPLY OVER TEMPERATURE		**$0°C \leq T_A \leq 70°C$**			**$-55°C \leq T_A \leq 125°C$**			
Differential voltage gain, standard part								
Gain 1[1]	$R_L = 2k\Omega$, $V_{OUT} = 3V$ p-p	250		600	200		600	V/V
Gain 2[2,4]		80		120	80		120	V/V
High gain part		400	500	600				V/V
Input resistance								
Gain 2[2,4]		8.0			8.0			kΩ
Input offset current				6.0			5.0	μA
Input bias current				40			40	μA
Input voltage range		±1.0			±1.0			V

NOTES:

1. Gain select pins G_{1A} and G_{1B} connected together.
2. Gain select pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 14-pin version only.

DC ELECTRICAL CHARACTERISTICS: (cont.) T_A = +25°C, V_{SS} = ±6V, V_{CM} = 0 unless otherwise specified. Recommended operating supply voltages V_S = ±6.0V. All specifications apply to both standard and high gain parts unless noted differently.

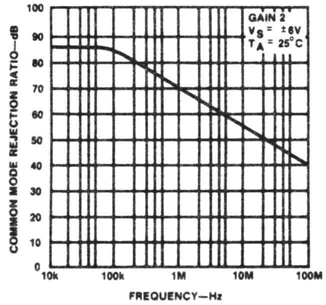
PARAMETER	TEST CONDITIONS	NE592			SE592			UNITS
		Min	Typ	Max	Min	Typ	Max	
THE FOLLOWING SPECS APPLY OVER TEMPERATURE		**0°C ≤ T_A ≤ 70°C**			**−55°C ≤ T_A ≤ 125°C**			
Common mode rejection ratio								
Gain 2[4]	V_{CM} ± 1V, f <100kHz	50			50			dB
Supply voltage rejection ratio								
Gain 2[4]	ΔV_S = ±0.5V	50			50			dB
Output offset voltage								
Gain 1	R_L = ∞			1.5			1.5	V
Gain 2[4]	R_L = ∞			1.5			1.2	V
Gain 3[3]	R_L = ∞			1.0			1.0	V
Output voltage swing differential	R_L = 2kΩ	2.8			2.5			V
Power supply current	R_L = ∞			27			27	mA

NOTES:

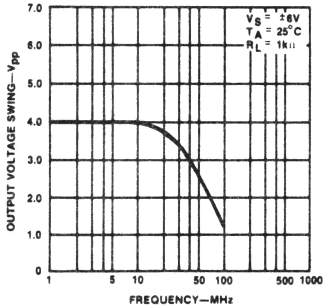
1. Gain select pins G_{1A} and G_{1B} connected together.
2. Gain select pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.
4. Applies to 14-pin version only.

TYPICAL PERFORMANCE CHARACTERISTICS

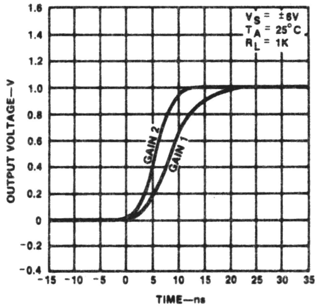
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



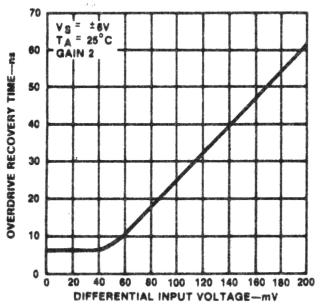
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



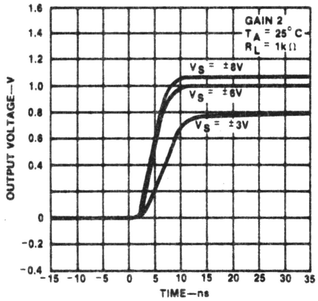
PULSE RESPONSE



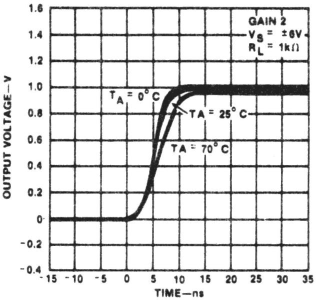
DIFFERENTIAL OVERDRIVE RECOVERY TIME



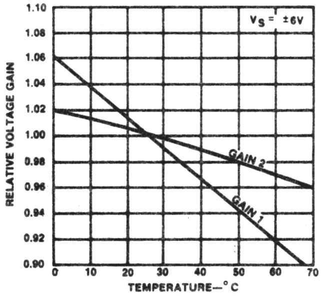
PULSE RESPONSE AS A FUNCTION OF SUPPLY VOLTAGE



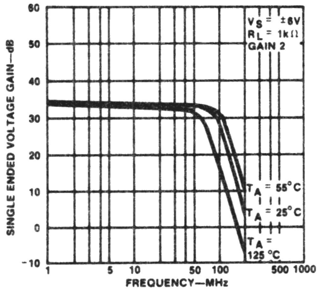
PULSE RESPONSE AS A FUNCTION OF TEMPERATURE



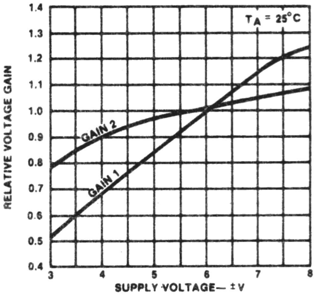
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



GAIN vs FREQUENCY AS A FUNCTION OF TEMPERATURE

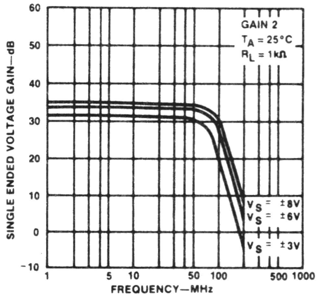


VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

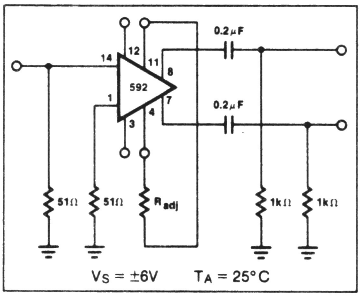


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

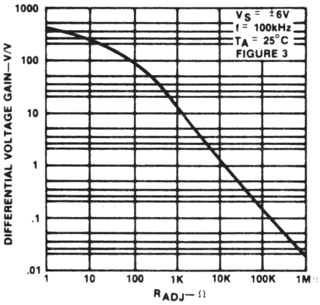
GAIN vs FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



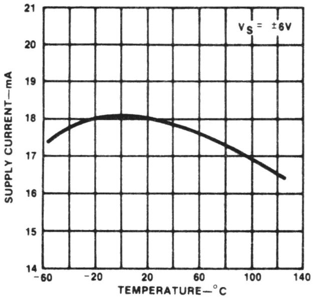
VOLTAGE GAIN ADJUST CIRCUIT



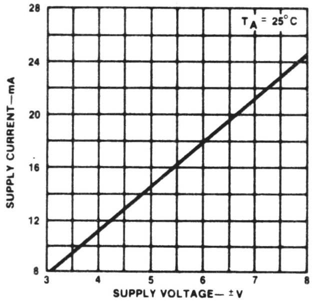
VOLTAGE GAIN AS A FUNCTION OF RADJ (FIGURE 3)



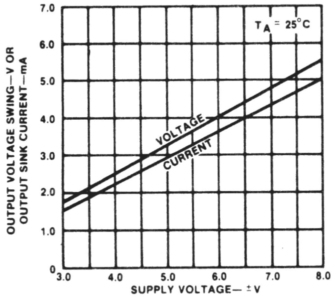
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



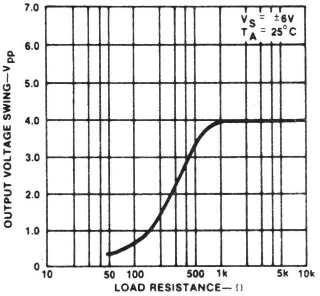
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



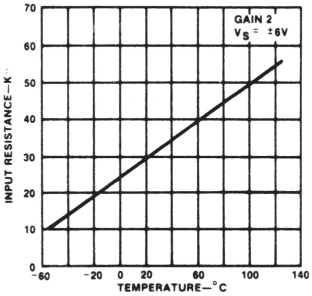
OUTPUT VOLTAGE AND CURRENT SWING AS A FUNCTION OF SUPPLY VOLTAGE



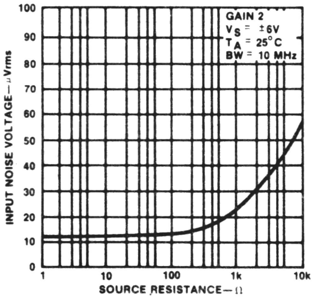
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



INPUT RESISTANCE AS A FUNCTION OF TEMPERATURE

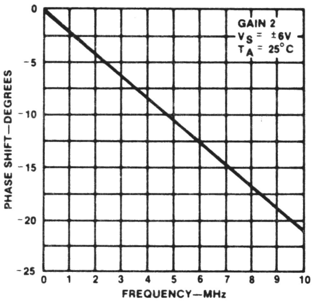


INPUT NOISE VOLTAGE AS A FUNCTION OF SOURCE RESISTANCE

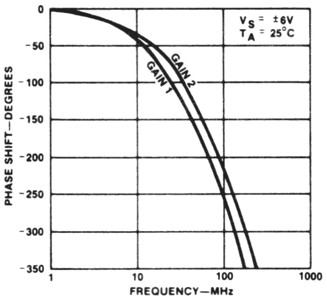


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

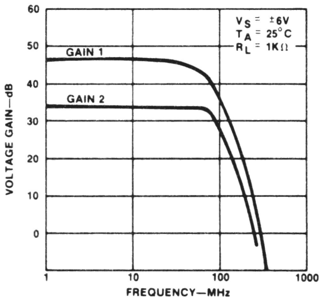
PHASE SHIFT AS A FUNCTION OF FREQUENCY



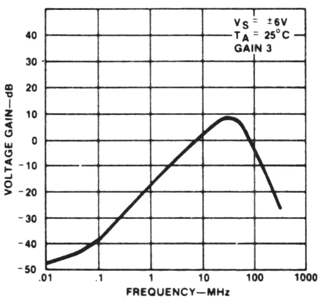
PHASE SHIFT AS A FUNCTION OF FREQUENCY



VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

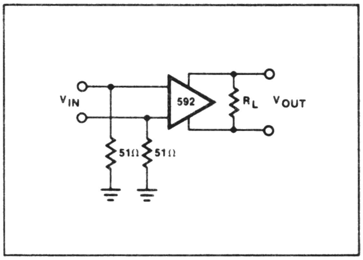


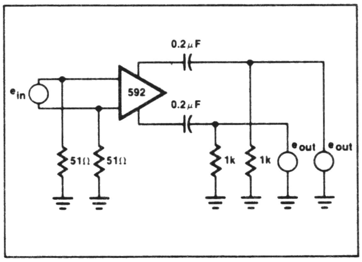
VOLTAGE GAIN AS A FUNCTION OF FREQUENCY (ALL GAIN SELECT PINS OPEN)



TEST CIRCUITS

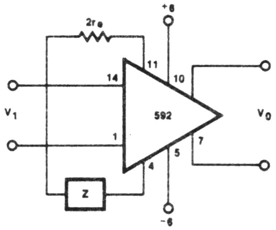
T_A = 25°C unless otherwise specified


V_{IN}
592
R_L
V_{OUT}
51Ω
51Ω


0.2μF
0.2μF
e_{in}
592
51Ω
51Ω
1k
1k
e_{out}
e_{out}

TYPICAL APPLICATIONS

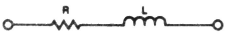
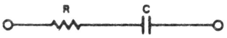
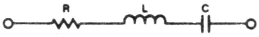
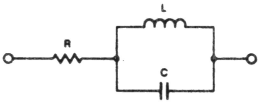
FILTER NETWORKS


2re
+6
11
14
10
V1
592
Vo
1
7
5
4
Z
-6

$$\frac{V_0\,(s)}{V_1\,(s)} \cong \frac{1.4 \times 10^4}{Z(s) + 2r_e}$$

$$\cong \frac{1.4 \times 10^4}{Z(s) + 32}$$

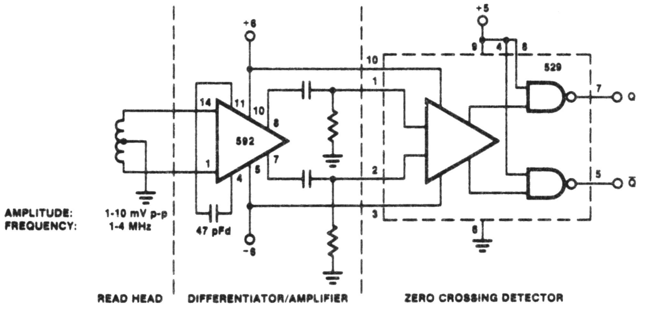
BASIC CONFIGURATION

Z NETWORK	FILTER TYPE	$\frac{V_0\,(s)}{V_1\,(s)}$ TRANSFER FUNCTION
	LOW PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
	HIGH PASS	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
	BAND PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/L\,s + 1/LC}\right]$
	BAND REJECT	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

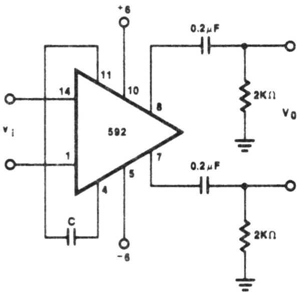
NOTE

In the networks above, the R value used is assumed to include $2r_e$, or approximately 32Ω.

DISC/TAPE PHASE MODULATED READBACK SYSTEMS


+6
14
11
10
8
592
1
7
5
4
47 pFd
-6
+5
9
4
8
10
529
1
7
Q
2
5
Q̄
3
6
AMPLITUDE:
FREQUENCY:
1-10 mV p-p
1-4 MHz
READ HEAD
DIFFERENTIATOR/AMPLIFIER
ZERO CROSSING DETECTOR

DIFFERENTIATION WITH HIGH COMMON MODE NOISE REJECTION


+6
0.2μF
11
10
14
8
2KΩ
Vo
Vi
592
1
7
0.2μF
5
4
C
2KΩ
-6

FOR FREQUENCY $F_1 << 1/2\,\pi\,(32)\,C$

$V_0 \cong 1.4 \times 10^4 C \frac{dVi}{dT}$

DIFFERENTIAL VIDEO AMPLIFIER µA733/733C

DESCRIPTION

The 733 is a monolithic differential input, differential output, wideband video amplifier. It offers fixed gains of 10,100 or 400 without external components, and adjustable gains from 10 to 400 by the use of an external resistor. No external frequency compensation components are required for any gain option. Gain stability, wide bandwidth and low phase distortion are obtained through use of the classic series-shunt feedback from the emitter follower outputs to the inputs of the second stage. The emitter follower outputs provide low output impedance, and enable the device to drive capacitive loads. The 733 is intended for use as a high performance video and pulse amplifier in communications, magnetic memories, display and video recorder systems.

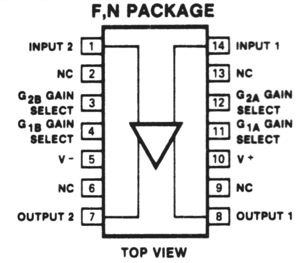
FEATURES

- **120MHz bandwidth**
- **250kΩ input resistance**
- **Selectable gains of 10,100 and 400**
- **No frequency compensation required**
- **Mil std 883A,B,C available**

APPLICATIONS

- **Video amplifier**
- **Pulse amplifier in communications**
- **Magnetic memories**
- **Video recorder systems**

PIN CONFIGURATION


F,N PACKAGE
INPUT 2 1
NC 2
G2B GAIN SELECT 3
G1B GAIN SELECT 4
V- 5
NC 6
OUTPUT 2 7
14 INPUT 1
13 NC
12 G2A GAIN SELECT
11 G1A GAIN SELECT
10 V+
9 NC
8 OUTPUT 1
TOP VIEW

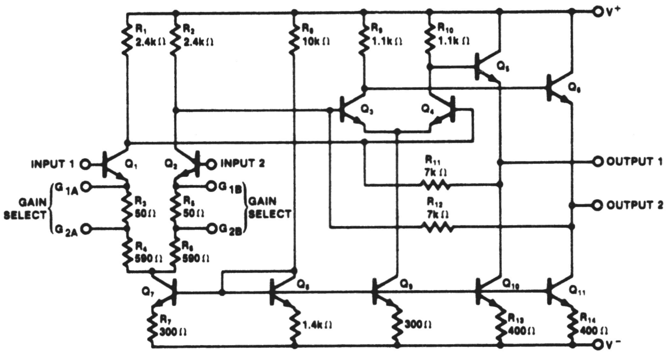
ORDER NUMBERS

µA733F µA733CN
µA733N µA733CF

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Differential input Voltage	±5	V
Common mode input Voltage	±6	V
Vcc	±8	V
Ouput current	10	mA
Junction temperature	+150	°C
Storage temperature range	-65 to +150	°C
Operation temperature range		
µA733C	0 to +75	°C
µA733	-55 to +125	°C
P_D Power dissipation		
K package	500	mW
N, F package	670	mW

CIRCUIT SCHEMATIC


V+
R1 2.4kΩ
R2 2.4kΩ
R8 10kΩ
R9 1.1kΩ
R10 1.1kΩ
Q5
Q6
Q3
Q4
INPUT 1
Q1
Q2
INPUT 2
G1A
G1B
GAIN SELECT
GAIN SELECT
G2A
G2B
R3 50Ω
R5 50Ω
R4 590Ω
R6 590Ω
R11 7kΩ
R12 7kΩ
OUTPUT 1
OUTPUT 2
Q7
Q8
Q9
Q10
Q11
R7 300Ω
1.4kΩ
300Ω
R13 400Ω
R14 400Ω
V-

DC ELECTRICAL CHARACTERISTICS

$T_A = +25°C$, $V_S = \pm 6V$, VCM = 0 unless otherwise specified.
Recommended operating supply voltages $V_S = \pm 6.0V$

PARAMETER	TEST CONDITIONS	μA733C			μA733			UNITS
		Min	Typ	Max	Min	Typ	Max	
Differential voltage gain								
Gain 1[2]		250	400	600	300	400	500	V/V
Gain 2[2]	$R_I = 2k\Omega$, $V_{OUT} = 3V_{p\text{-}p}$	80	100	120	90	100	110	V/V
Gain 3[3]		8	10	12	9	10	11	V/V
Bandwidth								
Gain 1[1]			40			40		MHz
Gain 2[2]			90			90		MHz
Gain 3[3]			120			120		MHz
Rise time								
Gain 1[1]			10.5			10.5		ns
Gain 2[2]	$V_{OUT} = 1V_{p\text{-}p}$		4.5	12		4.5	10	ns
Gain 3[3]			2.5			2.5		ns
Propagation delay								
Gain 1[1]			7.5			7.5		ns
Gain 2[2]	$V_{OUT} = 1V_{p\text{-}p}$		6.0	10		6.0	10	ns
Gain 3[3]			3.6			3.6		ns
Input resistance								
Gain 1[2]			4.0			4.0		kΩ
Gain 2[2]		10	30		20	30		kΩ
Gain 3[3]			250			250		kΩ
Input capacitance[2]	Gain 2		2.0			2.0		pF
Input offset current			0.4	5.0		0.4	3.0	μA
Input bias current			9.0	30		9.0	20	μA
Input noise voltage	BW = 1kHz to 10MHz		12			12		μVrms
Input voltage range		± 1.0			± 1.0			V
Common mode								
Rejection ratio								
Gain 2	VCM = ± 1V, f ≤ 100kHz	60	86		60	86		dB
Gain 2	VCM = ± 1V, F = 5MHz		60			60		dB
Supply voltage								
Rejection ratio								
Gain 2	$\Delta V_S = \pm 0.5V$	50	70		50	70		dB
Output offset voltage								
Gain 1[1]	$R_L = \infty$		0.6	1.5		0.6	1.5	V
Gain 2 and 3[2,3]			0.35	1.5		0.35	1.0	V
Output common mode voltage	$R_L = \infty$	2.4	2.9	3.4	2.4	2.9	3.4	V
Output voltage swing, differential	$R_L = 2k$	3.0	4.0		3.0	4.0		V_pK-$_pK$
Output sink current		2.5	3.6		2.5	3.6		mA
Output resistance			20			20		Ω
Power supply current	$R_L \pm \infty$		18	24		18	24	mA
THE FOLLOWING SPECS APPLY OVER TEMPERATURE		**0°C ≤ T_A ≤ 70°C**			**−55°C ≤ T_A ≤ 125°C**			
Differential voltage gain								
Gain 1[1]		250		600	200		600	V/V
Gain 2[2]	$R_I = 2k\Omega$, $V_{OUT} = 3Vp\text{-}p$	80		120	80		120	V/V
Gain[3]		8		12	8		12	V/V

DC ELECTRICAL CHARACTERISTICS (Continued)

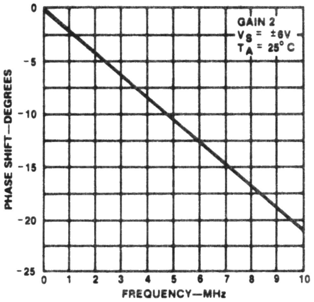
PARAMETER	TEST CONDITIONS	μA733C			μA733			UNITS
		Min	Typ	Max	Min	Typ	Max	
Input resistance								
Gain 2[2]		8			8			kΩ
Input offset current				6			5	μA
Input bias current				40			40	μA
Input voltage range		± 1.0			± 1.0			V
Common mode Rejection ratio								
Gain 2	VCM = ± V, F ≤ 100kHz	50			50			dB
Supply voltage Rejection ratio								
Gain 2	ΔV_S = ± 0.5V	50			50			dB
Output offset voltage								
Gain 1[1]	$R_L = \infty$			1.5			1.5	V
Gain 2 and 3[2, 3]				1.5			1.2	V
Output voltage swing, differential	R_L = 2k	2.8			2.5			Vpk-pk
Output sink current		2.5			2.2			mA
Power supply current	$R_L \pm \infty$			27			27	mA

NOTES

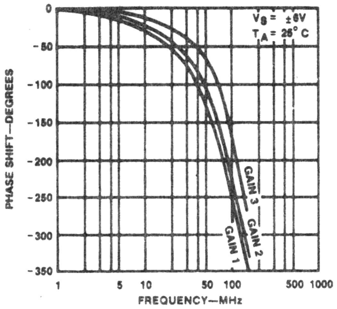
1. Gain select pins G_{1A} and G_{1B} connected together
2. Gain select pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.

TYPICAL PERFORMANCE CHARACTERISTICS

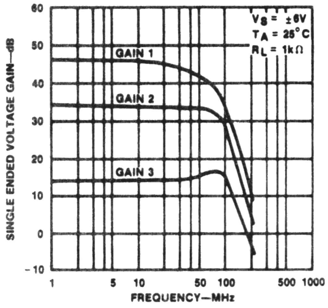
PHASE SHIFT AS A FUNCTION OF FREQUENCY



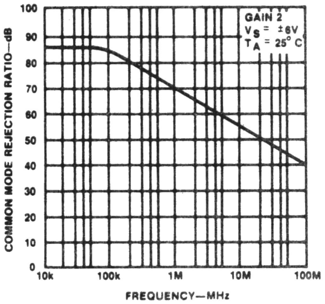
PHASE SHIFT AS A FUNCTION OF FREQUENCY



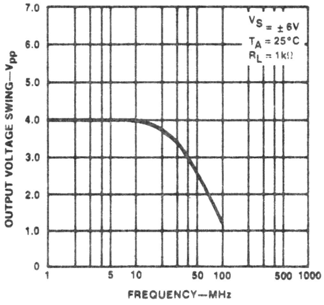
VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



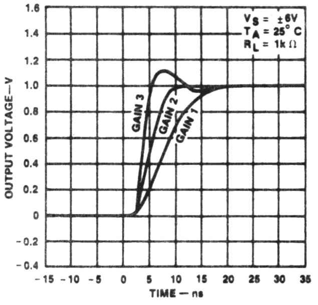
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

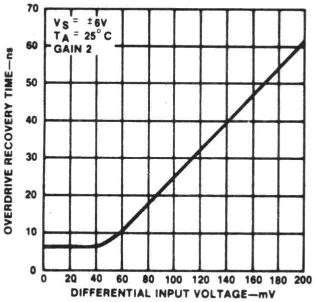


PULSE RESPONSE

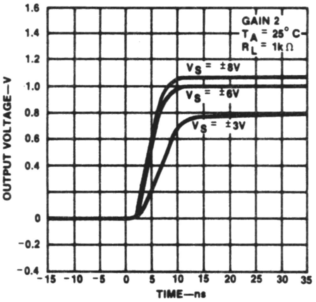


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

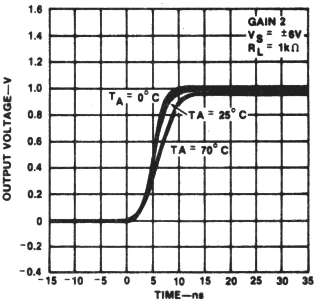
DIFFERENTIAL OVERDRIVE RECOVERY TIME



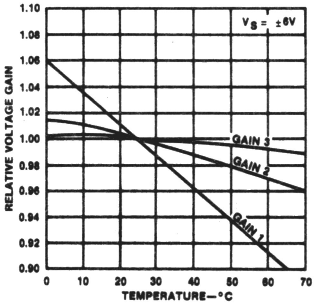
PULSE RESPONSE AS A FUNCTION OF SUPPLY VOLTAGE



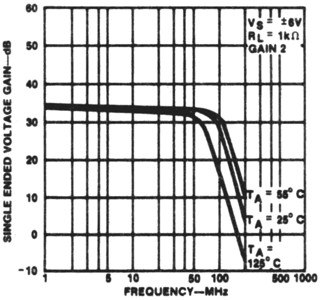
PULSE RESPONSE AS A FUNCTION OF TEMPERATURE



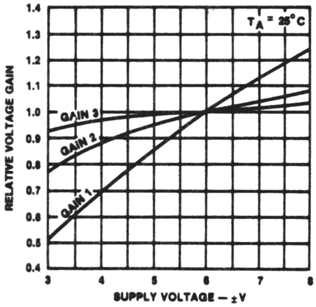
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



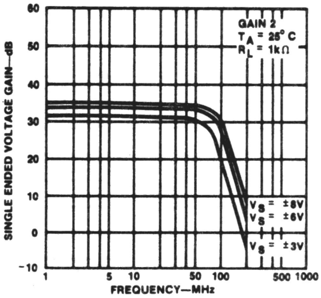
GAIN vs FREQUENCY AS A FUNCTION OF TEMPERATURE



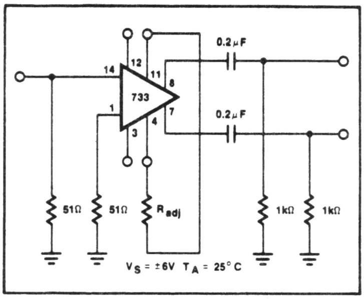
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



GAIN vs FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE

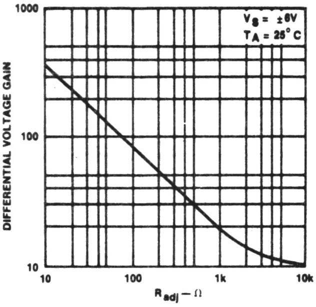


VOLTAGE GAIN ADJUST CIRCUIT



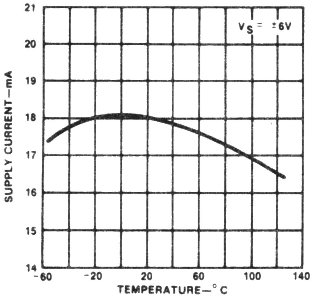
(Pin numbers apply to K Package)

VOLTAGE GAIN AS A FUNCTION OF RADJ (FIGURE 3)

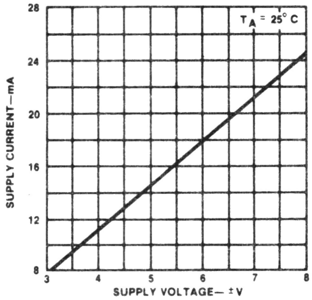


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

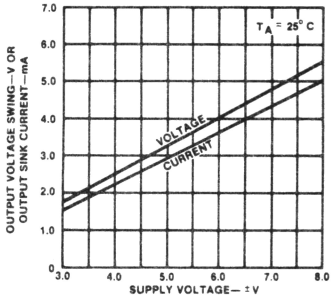
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



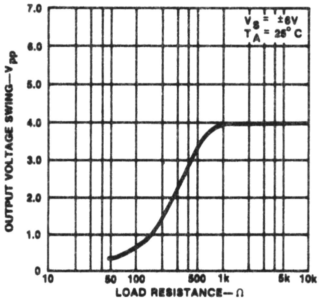
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



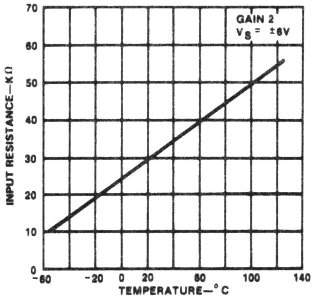
OUTPUT VOLTAGE AND CURRENT SWING AS A FUNCTION OF SUPPLY VOLTAGE



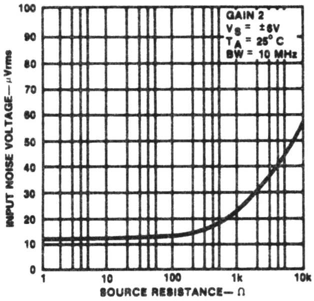
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



INPUT RESISTANCE AS A FUNCTION OF TEMPERATURE

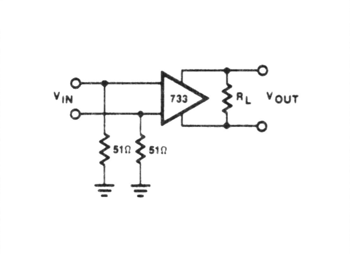


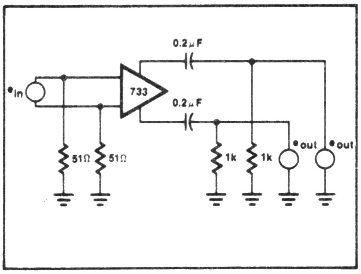
INPUT NOISE VOLTAGE AS A FUNCTION OF SOURCE RESISTANCE



TEST CIRCUITS

T_A = 25°C unless otherwise specified.


V_{IN}
733
R_L
V_{OUT}
51Ω
51Ω


e_{in}
733
0.2μF
0.2μF
51Ω
51Ω
1k
1k
e_{out}
e_{out}

Section 7
Power Conversion and Control

INDEX

SECTION 7 — POWER CONVERSION AND CONTROL

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PROGRAMMABLE SEVEN CHANNEL RC ENCODER

NE5044

DESCRIPTION

The NE5044 is a programmable parallel input, serial output pulsewidth encoder. A multiplexed dual linear ramp technique is used to allow up to 7 inputs to be converted to a serial pulsewidth modulated signal with excellent linearity and minimal crosstalk. Fixed or variable frame rates can be used, externally controlled, for ease of demodulation. An onboard 5V regulator eliminates power supply sensitivities and provides up to 20mA current capability for driving external loads.

FEATURES

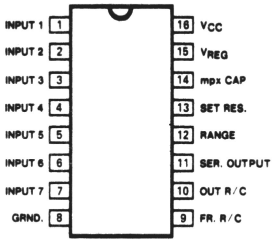
- **3 to 7 channels, externally selectable**
- **Constant current dual linear ramp for linearity better than .3%**
- **Internal voltage regulator for low drift**
- **Wide supply range 4.5 - 16V**
- **Fixed or variable frame rate set by external R-C**
- **External control for channel gain or range**
- **Versatile applications; exponential rates, mixing, dual rate, reversing etc.**
- **Compatible with all transmission mediums**

APPLICATIONS

- **Radio controlled aircraft, cars, boats, trains**
- **Industrial controllers**
- **Remote controlled entertainment systems**
- **Security systems**
- **Instrumentation recorders/controls**
- **Remote Analog/digital data transmission**
- **Automotive sensor systems**
- **Robotics**
- **Telemetry**

PIN CONFIGURATION

D,N PACKAGE


INPUT 1 1
INPUT 2 2
INPUT 3 3
INPUT 4 4
INPUT 5 5
INPUT 6 6
INPUT 7 7
GRND. 8
16 VCC
15 VREG
14 mpx CAP
13 SET RES.
12 RANGE
11 SER. OUTPUT
10 OUT R/C
9 FR. R/C

TOP VIEW

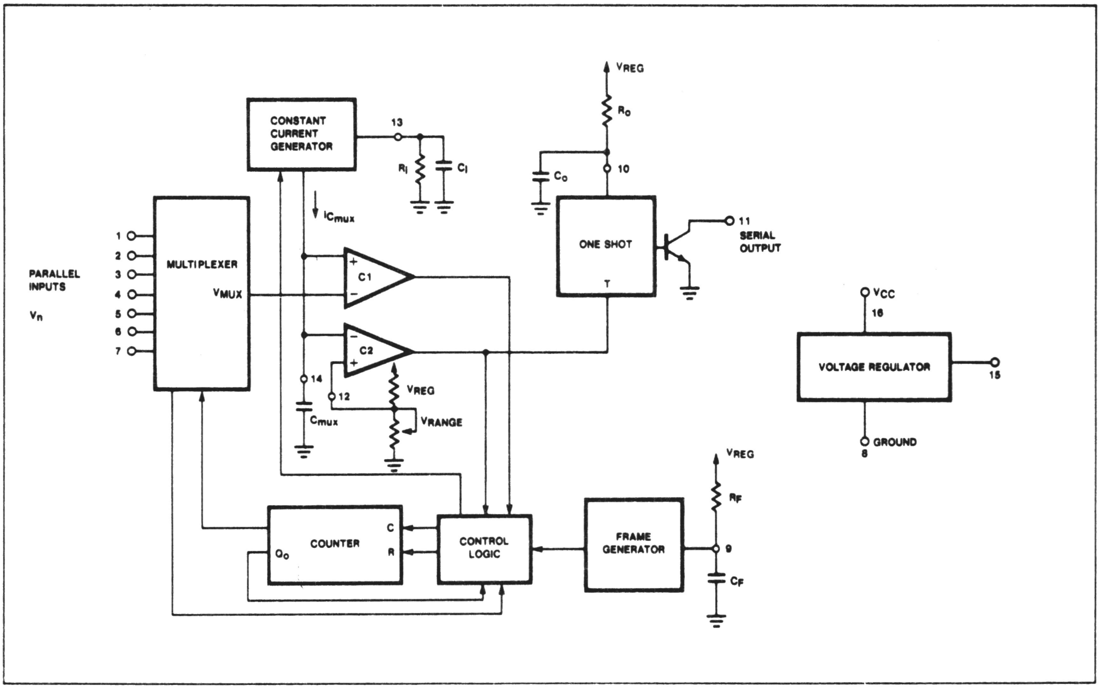
ORDER NUMBERS
NE5044D NE5044N

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
V_{CC}, Supply voltage	17	V
Regulator ouput current	−25	mA
Serial output peak current	30	mA
Constant current generator	−1	mA
Parallel inputs, range input	0-V_{REG}	V
One shot input, frame generator input	0-V_{REG}	V
Operating temperature	−20 to +75	°C
Storage temperature	−65 to +150	°C

NOTE
1. T_A = 25° unless otherwise stated.

BLOCK DIAGRAM


VREG
Ro
CONSTANT CURRENT GENERATOR
13
Ri
Ci
Co
10
ICmux
ONE SHOT
11 SERIAL OUTPUT
T
PARALLEL INPUTS
Vn
1
2
3
4
5
6
7
MULTIPLEXER
VMUX
C1
C2
14
12
Cmux
VREG
VRANGE
VCC
16
VOLTAGE REGULATOR
15
GROUND
8
VREG
RF
COUNTER
Qo
C
R
CONTROL LOGIC
FRAME GENERATOR
9
CF

DC ELECTRICAL CHARACTERISTICS

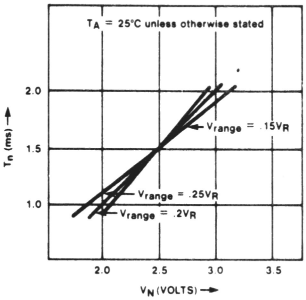
Test conditions $T_A = 25°C$, $V_{CC} = 10V$ using Test Circuit A unless otherwise stated.

PARAMETER	TEST CONDITIONS	NE 5044			UNIT
		Min	Typ	Max	
POWER SUPPLY REQUIREMENTS (Note 1)					
Power supply voltage range		4.5		16	V
Power supply current	Excluding control pots and serial output currents		11	15	mA
VOLTAGE REGULATOR					
V_{REG} Output voltage		4.5	5.0	5.5	V
Output current	$V_R \geq 4.5V$			−20	mA
Line regulation	$7 \leq V_{CC} \leq 16$		.005	0.2	V/V
MULTIPLEXER					
Input current	$V_n = 2.5v$		±30	±200	nA
Input voltage range	$V_n - V_{Range} \geq .75V$	1.5		5	V
Crosstalk			±1	±5	µs
OUTPUT PULSE					
T_n Position	$R_I \bullet C_{mux} = 1.25ms$ $V_n = .5V_{REG}$; $V_{RANGE} = .2V_{REG}$	1350	1500	1650	µs
Position linearity error			5		µs
Position tempco	$0°C \leq T_A \leq 70°C$.		.15		µs/°C
Position PSR	$6V \leq V_{CC} \leq 16V$		.5	1	µs/V
T_O Width	$R_OC_O = 300µs$	240	285	330	µs
Saturation voltage	$I_O = 25mA$		.6	1	V
I_{11} Leakage current			.05	50	µA
Range input voltage	$R_I = 50kΩ$	.75			V
	$R_I = 25kΩ$	1.00			V
Frame time (Fixed)	$R_FC_F = 30ms$	17	20	23	ms
Inhibit threshold				.4	V

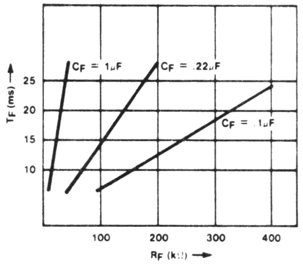
NOTE

1. At supply voltages exceeding 12V, a current limiting resistor of 20 to 50Ω in series with V_{CC} is recommended.

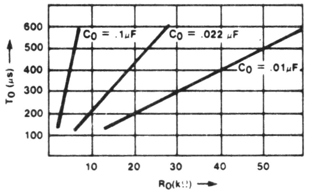
OUTPUT PULSE WIDTH (T_n) vs INPUT VOLTAGE (V_n)



FRAME TIME (T_F) vs R_F



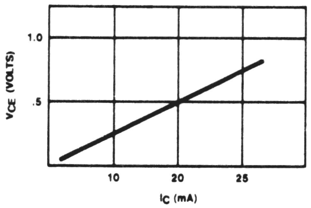
OUTPUT ONESHOT TIME (T_O) vs R_O



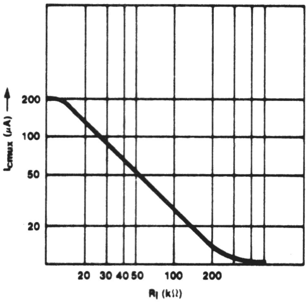
PROGRAMMABLE SEVEN CHANNEL RC ENCODER

NE5044

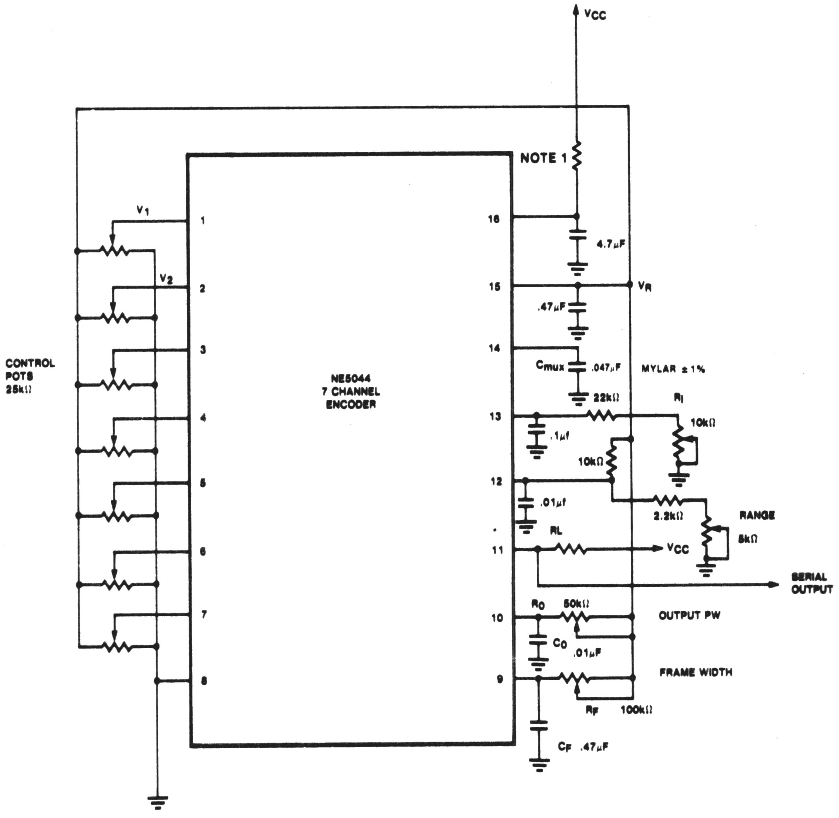
OUTPUT SATURATION VOLTAGE vs OUTPUT CURRENT



CONSTANT CURRENT vs R_I



TEST CIRCUIT


VCC
NOTE 1
V1
V2
CONTROL POTS 25kΩ
NE5044 7 CHANNEL ENCODER
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
4.7µF
VR
.47µF
Cmux
.047µF
MYLAR ± 1%
22kΩ
RI
10kΩ
.1µf
10kΩ
.01µf
2.2kΩ
RANGE
5kΩ
RL
VCC
SERIAL OUTPUT
RO
50kΩ
OUTPUT PW
CO
.01µF
FRAME WIDTH
RF
100kΩ
CF
.47µF

NOTE

1. At supply voltages exceeding 12V, a current limiting resistor of 20 to 50Ω in series with V_{CC} is recommended

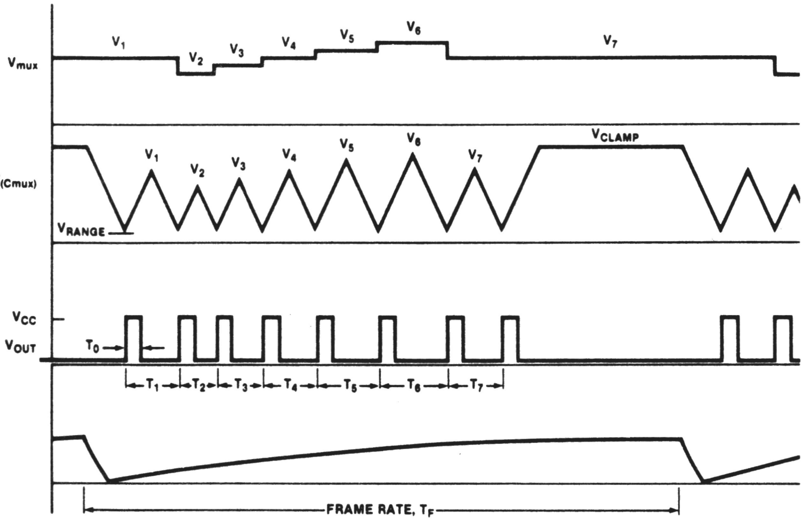

V_{mux}
V_1
V_2
V_3
V_4
V_5
V_6
V_7
$V_{(Cmux)}$
V_{CLAMP}
V_{RANGE}
V_{CC}
V_{OUT}
T_0
T_1
T_2
T_3
T_4
T_5
T_6
T_7
FRAME RATE, T_F

Figure 1. Encoder Timing Diagram — Fixed Frame

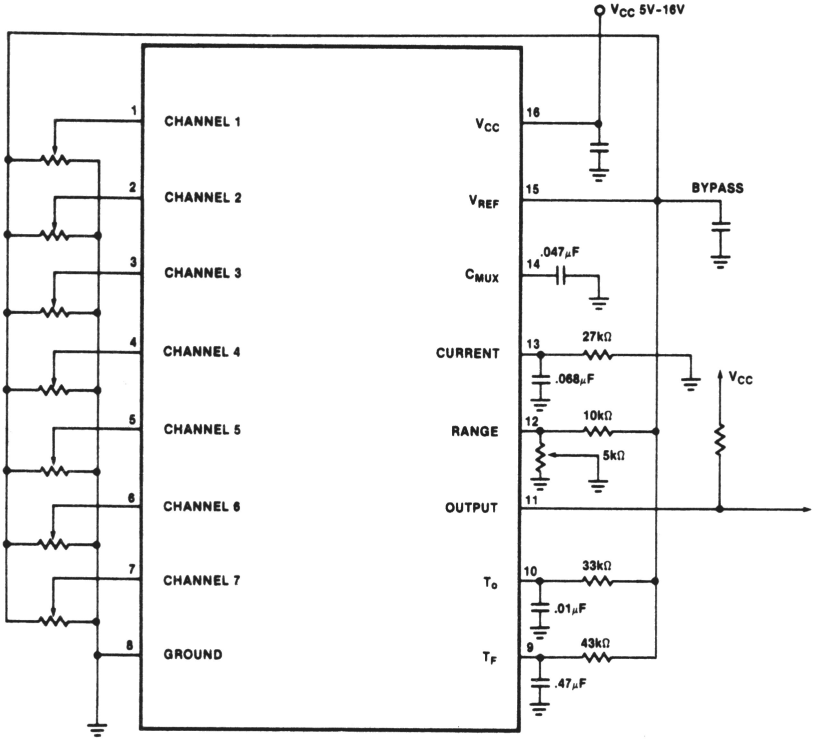

V_{CC} 5V-16V
1 CHANNEL 1
2 CHANNEL 2
3 CHANNEL 3
4 CHANNEL 4
5 CHANNEL 5
6 CHANNEL 6
7 CHANNEL 7
8 GROUND
16 V_{CC}
15 V_{REF}
BYPASS
14 C_{MUX}
.047µF
13 CURRENT
27kΩ
.068µF
V_{CC}
12 RANGE
10kΩ
5kΩ
11 OUTPUT
10 T_o
33kΩ
.01µF
9 T_F
43kΩ
.47µF

Figure 2

A. CIRCUIT OPERATION

The NE5044 is a programmable parallel input, serial output encoder containing all the active circuitry necessary to generate a precise pulsewidth modulated signal with 3 to 7 channels. The number of channels is externally programmable by grounding unused control inputs. A multiplexed dual linear ramp technique is used to provide excellent linearity, minimal crosstalk and low temperature drift. An onboard 5-volt regulator eliminates power supply sensitivities and has up to 20mA current capability for driving external loads. The encoder can be used in the fixed frame mode or, with the addition of one external NPN transistor, as a variable frame encoder.

The multiplexer functions as a strobed voltage follower so that each input, when active, appears as a high impedance input (>1MΩ) and transfers the input *voltage* to the output. Only one of the seven inputs is active at any time and when a given input is inactive, it appears as an open circuit. The high impedance multiplexer inputs eliminate loading on control inputs and simplify mixing circuits where several controls may be mixed onto one input.

Channel 4, 5, 6 and 7 inputs may also be used to select the desired number of output pulses by grounding one or more of these pins. That is, by grounding pin 4 (channel 4 input) only the first three inputs of the encoder will be used and a 3-channel encoder results. Grounding pin 5 results in a 4-channel encoder and so on. Thus, any number of channels between 3 and 7 may be selected. Internal voltage clamping prevents encoder malfunction if any input is shorted to supply, ground or open circuited. The remaining channels will continue to be encoded except as noted above. This feature eliminates catastrophic failures due to control pot opens or shorts.

The constant current generator is a bidirectional current source whose current is set by an external resistor R_I, where:

$$I_c = \pm \frac{V_R}{2R_I}$$

The current generator alternately charges and discharges the capacitor C_{mux}. An internal feedback loop maintains a constant current and very high output impedance. This yields a typical linearity error of voltage input to pulsewidth output for the encoder of less than 0.1%. An external capacitor, C_I, is required to insure stability of the feedback loop.

Two high gain comparators, C1 and C2, compare the voltage across C_{mux} with the multiplexer output voltage and the range input voltage. The input bias currents and offset voltages of these comparators are sufficiently low so as to not influence the overall accuracy of the encoder. The comparators feed the counter control logic which in turn controls the counter and current generator. The operation of this loop is as follows: When I_c is positive (sourced from the current generator into C_{mux}) the capacitor linearily charges up until it reaches a voltage equal to the multiplexer output voltage, assume this to be the voltage at pin 1, V1. At this time the output of C1 goes high which reverses the direction of I_c (sinking into current generator from C_{mux}). C_{mux} now linearly discharges until it reaches the voltage set on pin 12, V_{range}. At this time the output of C2 goes high which again reverses the polarity of I_c, clocks the counter and triggers the output one shot. C_{mux} again charges up but now C1 goes high when C_{mux} reaches V2, the voltage on pin 2. The resulting voltage waveform on C_{mux} is a triangle wave whose positive peaks correspond to the voltages on pins 1 through 7 for the first through seventh peak and whose negative peaks are constant and equal to V_{range}. This waveform is shown in the first portion of Figure 1.

Independent control of I_c and V_{range} allows the encoder to be tailored to virtually any combination of input voltage changes and output pulsewidth changes. The functional relationships between these variables will be defined in the next section.

The frame generator controls the encoder frame time. It can operate as an astable or monostable multivibrator whose period is .66X R_FC_F. The encoder will generate a synchronizing pulse at the end of each frame. When C_{mux} reaches the seventh positive peak it reverses and discharges to V_{range}. The counter is clocked to the state where Q_0 is high when $VC_{mux} = V_{range}$. C_{mux} again charges up but now the output of C1 is ignored, due to Q_0 being high, and charges up to V_{clamp} and remains there. The encoder will remain in this state until a pulse from the frame generator is received. If R_F and C_F are connected as shown in the Block Diagram, then the frame generator operates in the astable mode producing a narrow pulse output. This pulse allows C_{mux} to start discharging again. When C_{mux} reaches V_{range}, the counter is clocked to the state where Q_1 is high (channel 1) and the entire process starts over. The frame period in this mode is .66 × R_FC_F and is referred to as the fixed frame mode. The variable frame mode will be discussed in the application section.

The output one-shot generates a positive pulse whose width is equal to R_oC_o. The output is an open collector, NPN transistor capable of sinking 25mA. This configuration allows the encoder to drive a wide variety of RF stages as well as providing current pulses in 2 wire communications applications.

B. ENCODER DESIGN EQUATIONS

The triangular waveform on C_{mux} has a fixed slope (constant current) and variable positive peak voltages. The time between the negative peaks of C_{mux}, which is equal to the output period for that channel, is given by:

$$T_n = \frac{2\,(V_n - V_{range})\,C_{mux}}{I_c}$$

I_c is given by:

$$I_c = \frac{V_R}{2R_I}$$

where V_R = Reference Voltage.

Additionally, V_n, the voltage on pin n, which is the control voltage for channel n, is typically the wiper voltage on a pot connected between V_R and ground. Thus $V_n = X_nV_R$.

V_{range} is also derived from V_R so that $V_{range} = Y\ V_R$. The resulting channel time period is:

$$T_n = \frac{2\,(X_n - Y)\,V_R \bullet C_{mux}}{(V_R/2R_I)}$$

$$\boxed{T_n = 4R_I\,C_{mux}(X_n - Y)}$$

Thus, each channel pulse width, T_n, is independent of supply voltage and depends only on external passive components.

The conversion rate, CR, for each channel is the change in output period, ΔT_n, divided by the change in input voltage for that channel, ΔV_n.

$$CR = \frac{\Delta T_n}{\Delta V_n} = \frac{\Delta T_n}{\Delta x_n} = 4\ R_I\ C_{mux}$$

In most applications, the input variable X_n will have some neutral or center value about which it will vary, thus

$$X_n = X_o + x_n$$

and

$$\boxed{CR = \frac{\Delta T_n}{\Delta x_n} = 4R_I C_{mux}}$$

where X_o is the neutral value for X and is assumed to be the same for all n. Now

$$T_n = 4R_I C_{mux}\,(X_o - Y + x_n)$$

If we let $T_{Neutral} = 4R_I C_{mux}(X_o - Y)$ be the neutral value for T_n, then

$$\boxed{T_n = T_{neutral} + 4R_I C_{mux}(x_n)}$$

Consider the following example to see how these design equations are used.

Assume:

$T_{neutral} = 1.5ms$

$X_o = 0.5$ — Control pot in center at $T_n = T_{neutral}$

$\Delta x_n = \pm 0.1$ — Control pot resistance varies ± 10% (of total resistance) around neutral. This should include mechanical trim if used.

$\Delta T_n = \pm 0.5ms$

For this example, the conversion rate is

$$CR = \frac{\Delta T_n}{\Delta x_n} = \frac{.5ms}{.1} = 5ms$$

so

$$4R_I C_{mux} = 5ms.$$

If we let $C_{mux} = .047\mu F$

$$R_I = \frac{5ms}{4X.047\mu F} = 26.5k\Omega = 27k\Omega$$

and

$$T_{neutral} = 1.5ms = 4R_I C_{mux}\,(X_o - Y)$$

$$Y = 0.5 - \frac{1.5ms}{5ms} = 0.2$$

The output pulse width is given by

$$T_o = R_o C_o$$

so if $T_o = 330\mu s$ and $C_o = .01\mu F$

$$R_o = \frac{330\mu s}{.01\mu F} = 33k\Omega.$$

The frame time constant, T_F, is given by

$$T_F = .66\ R_F C_F$$

If $T_F = 20ms$ and $C_F = .47\mu F$

$$R_F = \frac{20ms}{.66 \times .47\mu F} = 62k$$

Figure 2 shows the external connections for this example.

It should be noted that the temperature stability of all the encoded times depend on the temperature coefficients of the respective external R_C time constants. No internal temperature compensation is used on the chip. The typical temperature sensitivity of T_n using wirewound resistors and polycarbonate capacitors is less than 100ppm/°C in the −20°C to +70°C temperature range. For the above example, this corresponds to a change in T_n of ±7.5μs for a change in temperature of ±50°C.*

***For additional information, consult the Applications Section.**

SEVEN CHANNEL RC DECODER

NE5045

DESCRIPTION

The NE5045 is a serial input, parallel output, decoder intended for applications in pulse width or pulse position modulation systems. The serial input pulse, either positive or negative, is shaped and amplified before being fed to the counter/decoder. An integrating type sync. separator detects pulses greater than $T_W = R_S C_S$. The amplified input pulse triggers an internal one-shot (minimum pulse) which in turn clocks the counter-decoder, thereby enhancing system noise rejection. A missing pulse detector resets the decoder during the sync. pause. An internal voltage regulator supplies power for the radio receiver providing excellent isolation from the power supply as well as the decoder logic.

FEATURES

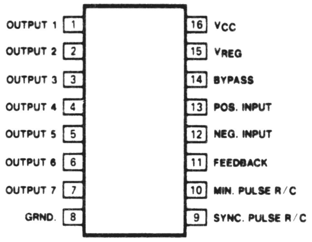
- **Decodes up to 7 channels**
- **High gain input amplifier**
- **Externally set sync. pause and minimum pulse**
- **Wide supply voltage range, 3.6V–8V.**
- **Positive or negative pulse inputs**
- **Noise and flutter rejection**
- **Outputs reset to zero without inputs**
- **Compatible with all transmission mediums**

APPLICATIONS

- **Radio controlled aircraft, cars, boats, trains**
- **Industrial controllers**
- **Remote controlled entertainment systems**
- **Security systems**
- **Instrumentation recorders/controls**
- **Remote Analog/digital data transmission**
- **Automotive sensor systems**
- **Robotics**
- **Telemetry**

PIN CONFIGURATION

D,N PACKAGE


OUTPUT 1 1
OUTPUT 2 2
OUTPUT 3 3
OUTPUT 4 4
OUTPUT 5 5
OUTPUT 6 6
OUTPUT 7 7
GRND. 8
16 VCC
15 VREG
14 BYPASS
13 POS. INPUT
12 NEG. INPUT
11 FEEDBACK
10 MIN. PULSE R/C
9 SYNC. PULSE R/C

TOP VIEW

ORDER NUMBERS

NE5045N NE5045D

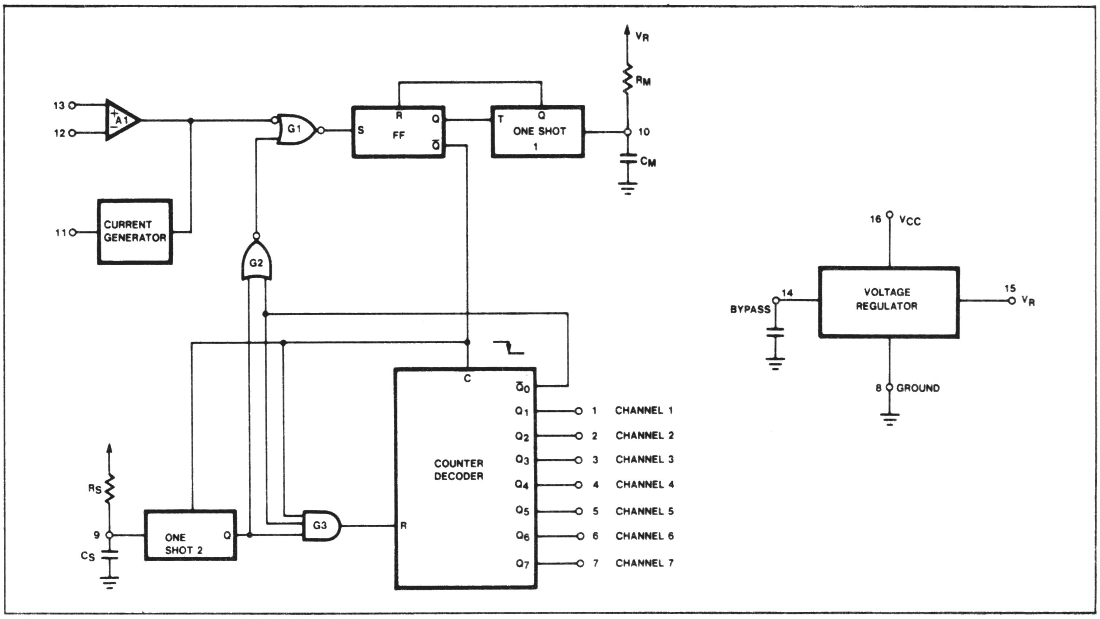
ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
V_{CC}, Supply voltage	10	V
Regulator output current	−25	mA
Decoded output current	±5	mA
Pause input voltage	0 to V_R	V
Input amplifier voltage	0 to V_R	V
Operating temperature	−20 to +75	°C
Storage temperature	−65 to +150	°C

NOTE

1. T_A = 25°C unless otherwise stated

BLOCK DIAGRAM

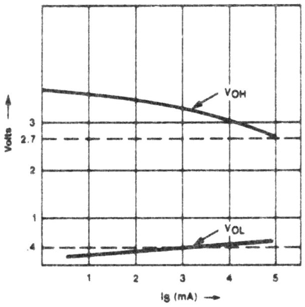

13
12
A1
G1
S
R
FF
Q
Q̄
T
Q
ONE SHOT 1
VR
RM
10
CM
11
CURRENT GENERATOR
G2
C
COUNTER DECODER
Q̄0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
1 CHANNEL 1
2 CHANNEL 2
3 CHANNEL 3
4 CHANNEL 4
5 CHANNEL 5
6 CHANNEL 6
7 CHANNEL 7
R
G3
RS
9
CS
ONE SHOT 2
Q
16 VCC
BYPASS
14
VOLTAGE REGULATOR
15 VR
8 GROUND

SEVEN CHANNEL RC DECODER NE5045

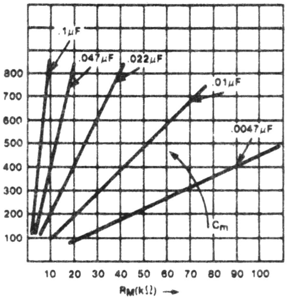
DC ELECTRICAL CHARACTERISTICS Standard conditions: (T_A = 25°C, V_{CC} = 5.0V unless otherwise stated), using Test Circuit #1

PARAMETER	TEST CONDITIONS	NE5045			UNIT
		Min	Typ	Max	
POWER SUPPLY REQUIREMENTS					
Power supply voltage range	Test circuit #1	3.6		8.0	V
Power supply current	Excluding input bias current		9.0	14.0	mA
VOLTAGE REGULATOR					
Output voltage		3.7	4.1	4.5	V
V_R Output current	$V_R \geq 3.7V$			−15	mA
Line regulation	V_{CC} = 6V to 8V		.01	.05	V/V
Voltage drop	V_{CC} = 4V, I_R = −10mA			1.3	V
INPUT AMPLIFIER					
Input bias current			10	100	nA
Input voltage range		2.0		4.0	V
Open loop gain			60		dB
Feedback current		100	200	400	µA
Detection threshold	Test circuit #1, ΔV12 & 13		8	20	mV
T_S Sync. pause time	$R_s C_s$ = 6.0ms	5.1	6.0	6.9	ms
T_M Minimum pulse time	$R_m C_m$ = 500µs	405	475	545	µs
OUTPUTS-ALL CHANNELS					
V_{OL}	I_{SINK} = 1mA		.25	.5	V
V_{OH}	I_{SOURCE} = 2mA	2.7			V

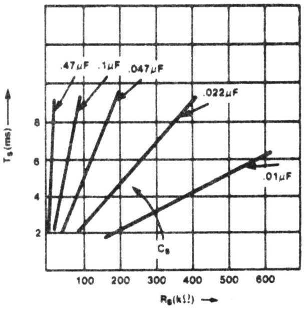
V_{OL} vs SINK CURRENT AND V_{OH} vs SOURCE CURRENT



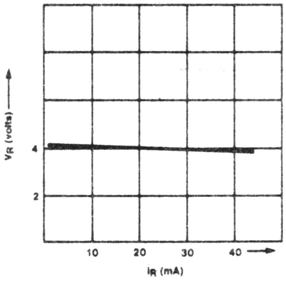
MINIMUM PULSE TIME, T_M vs R_M, C_M



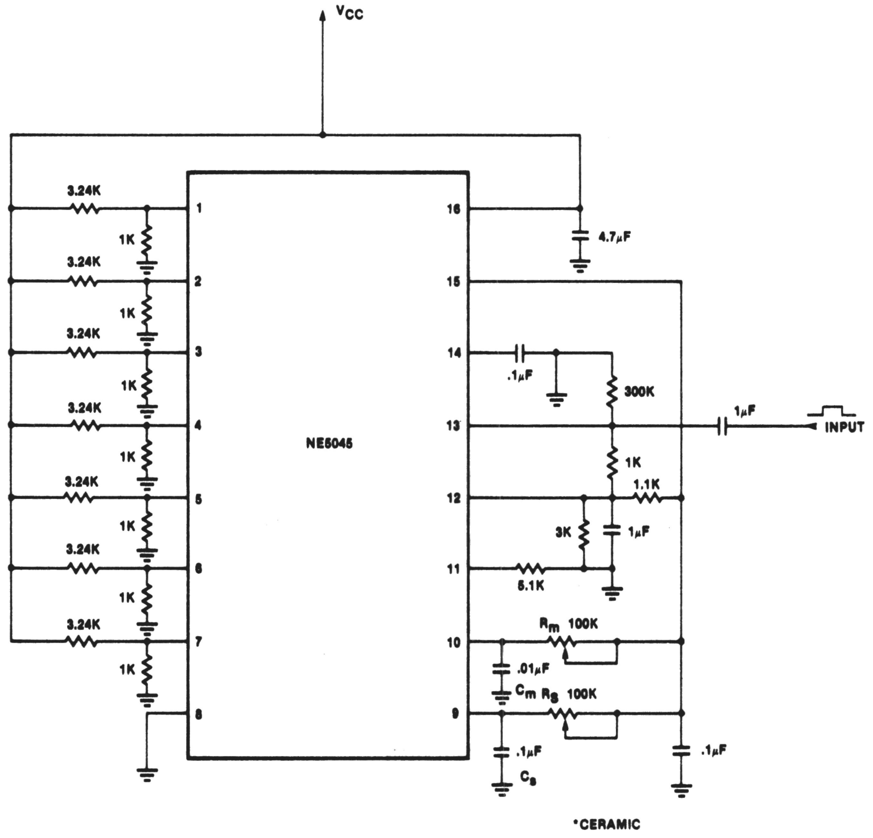
SYNC. PAUSETIME, T_s vs R_sC_s



REGULATOR VOLTAGE vs LOAD CURRENT



TEST CIRCUIT


VCC
3.24K
1K
1
2
3
4
5
6
7
8
NE5045
16
15
14
13
12
11
10
9
4.7µF
.1µF
300K
1µF
INPUT
1K
1.1K
3K
1µF
5.1K
Rm 100K
.01µF
Cm
Rs 100K
.1µF
Cs
.1µF
*CERAMIC

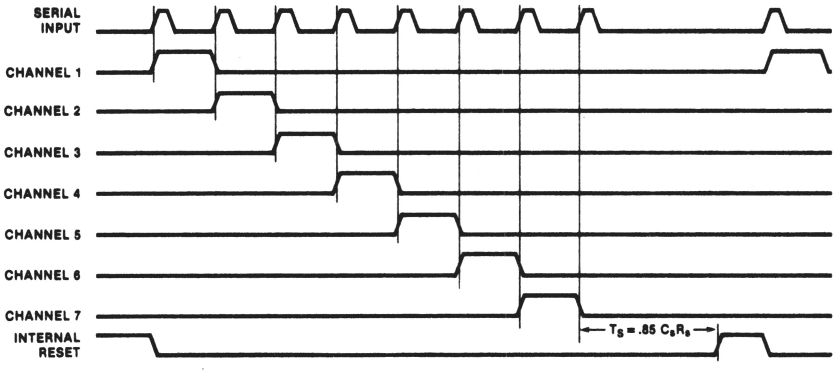

SERIAL INPUT
CHANNEL 1
CHANNEL 2
CHANNEL 3
CHANNEL 4
CHANNEL 5
CHANNEL 6
CHANNEL 7
INTERNAL RESET
TS = .85 CsRs

Figure 1. NE5045 Decoder Timing Diagram

A. CIRCUIT OPERATION

The NE5045 is a serial input, parallel output decoder containing all the active circuitry necessary to separate up to 7 channels of information in a pulsewidth modulated system. An internal voltage regulator provides excellent power supply rejection for the decoder as well as a regulated output for a radio receiver if used.

The high gain input amplifier, A1 ($A_v >$ 60dB), allows either positive or negative pulses to be used and has input bias currents less than 10nA. Signals as low as 10mV p-p can easily be demodulated. The feedback current generator can be used to provide positive feedback thereby creating hysteresis in the input switching levels. Hysteresis prevents false triggering due to noise or IF amplifier distortion. If positive input pulses are used, the signal would be connected to the noninverting input, pin 13. In this case, the input threshold would be set by the voltage difference between pin 12 and pin 13, established externally with a resistive divider network. Design of the divider will be covered in section B and C. Negative input signals would be coupled to pin 12, the inverting input.

The amplified signal from A1 is gated by G1 and in turn sets the FF. Assume, for the time, that G2 is low. The combination of the FF and One Shot 1 produces a minimum pulse to clock the counter-decoder for each positive *edge* at pin 13 which exceeds the voltage on pin 12. The width of this pulse is: $T_m = R_mC_m$. With this arrangement, the system will not respond to any pulse after the first edge and before the end of T_m. In effect the input is turned off for a period equal to T_m following the leading edge of each input pulse. The noise immunity of the decoder is thus enhanced by the ratio of T_m to the period between input pulses. Obviously T_m must be less than the shortest period between input pulses.

The counter is clocked and One Shot 2 is reset (capacitor C_s is discharged) each time the FF is set. When the FF is reset, C_s begins to charge up through R_s. The time constant $T_s = .85\ R_sC_s$ is normally much larger than the time between input pulses so that the output of One Shot 2 remains low until the last pulse of a given frame is received. Figure 1 shows the timing diagram for the decoder. After the last pulse in a frame (system synchronized) $\overline{Q}_o$ will go low and G2 will go high. The input is now disabled by G1 until One Shot 2 times out at which time G2 will go low. This connection serves two purposes:

(1) establishes synchronization in no more than one frame and

(2) prevents the counter-decoder from overflowing due to extra noise pulses in a given frame. Thus any noise pulses in a frame will only affect those channels after that pulse and only in that frame.

If fewer than 7 channels of input are used then $\overline{Q}_o$ is high after the last pulse and the counter-decoder is reset when One Shot 2 goes high.

Each channel has a totem pole output stage capable of sourcing 2mA and sinking 1mA.

The voltage regulator operates in two modes depending on the power supply voltage. If V_{CC} is greater than 5V, the voltage regulator acts as a series pass regulator with a nominal output voltage of 4.1V. When V_{CC} is less than 5V, the regulator acts as a dynamic decoupler where the bypass capacitor on pin 14 filters out line transients. The internal pass transistor acts like an emitter follower whose base is decoupled by the bypass capacitor. The value of capacitance will depend upon the degree of smoothing required and the amplitude of the line transients. If the regulator provides power for the radio receiver, this capacitor may have to be as large as 33μF. However if this is not done, 1μF should be sufficient.

B. DECODER DESIGN EQUATIONS

The design of the decoder's external circuitry is quite simple. The minimum pulse One Shot (#1) and the synchronization One Shot (#2) each have time periods given by:

$$\boxed{T_m = R_mC_m}$$

$$\boxed{T_s = .85\ R_sC_s}$$

respectively. The constraints on these time periods are: $T_m <$ the minimum input pulse width or time between leading edges of the input and $T_s >$ maximum input pulse width but $T_s <$ the sync pause (time between last pulse in frame and first pulse of the following frame).

The design of the input amplifier biasing network depends upon a number of factors, including:

1. Pulse Polarity
2. Pulse Amplitude
3. Variations in Amplitude and Noise
4. Detection Threshold and Hysteresis Levels

For a very simple case, assume the input is a positive pulse train and the threshold of detection is desired to be 400mV without hysteresis. Figure 2 shows the input amplifier along with the associated biasing circuits. The resistors R_1 and R_2 set the voltage on pin 12, which should be between 2V to 5V.

$$\boxed{V_{12} = V_R\ \frac{1}{1 + R_1/R_2}}$$

The threshold is set by the voltage drop across R_3, that is, the decoder will not be triggered until the voltage on pin 13 exceeds the voltage on pin 12.

$$V_{threshold} = V_{12} - V_{13}$$

$$V_{threshold} = V_{12}\left(\frac{1}{1 + R_4/R_3}\right)$$

If we assume $V_R = 4.1V$ and let $V_{12} = 3V$ then

$R_1 = 1.1k$

$R_2 = 3.0k$

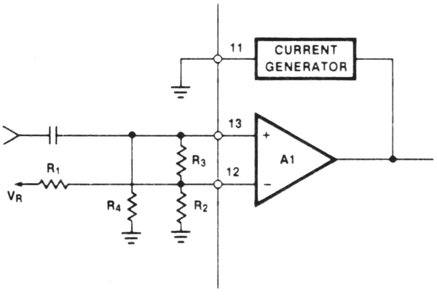


Figure 2. Input Amplifier Biasing NE5045

The threshold is then set to 400mV by setting

$R_4/R_3 = 6.5$

R_4 should be sufficiently large so as to not load the input signal. If we let $R_3 = 51k$ then $R_4 = 330k$. Figure 3 shows the external connections for a complete decoder. Note that this circuit does not have provisions for noise filtering or rejection of amplitude variations.

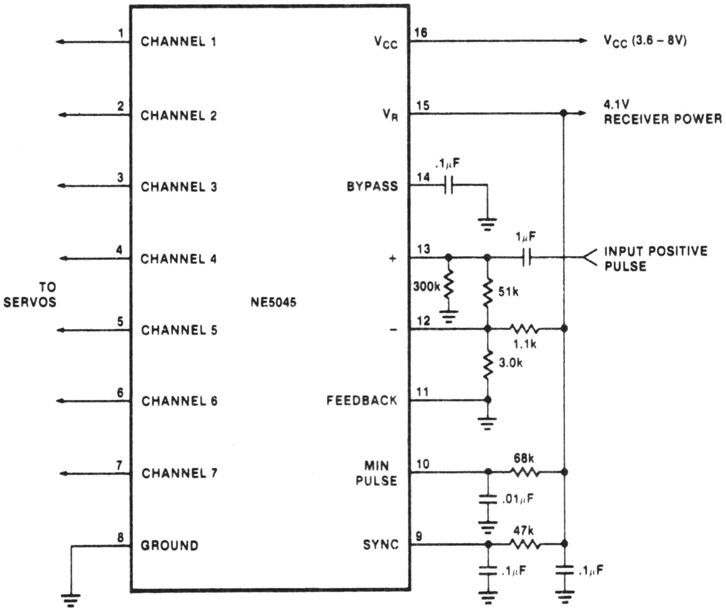

1
CHANNEL 1
2
CHANNEL 2
3
CHANNEL 3
4
CHANNEL 4
TO SERVOS
NE5045
5
CHANNEL 5
6
CHANNEL 6
7
CHANNEL 7
8
GROUND
VCC
16
VCC (3.6 – 8V)
VR
15
4.1V RECEIVER POWER
BYPASS
14
.1μF
+
13
1μF
INPUT POSITIVE PULSE
300k
51k
–
12
1.1k
3.0k
FEEDBACK
11
MIN PULSE
10
68k
.01μF
SYNC
9
47k
.1μF
.1μF

Figure 3. NE5045 Decoder External Connections
$T_m = .68ms$; $T_s = 4ms$, $V_{threshold} = 400mV$

***For additional information, consult the Applications Section.**

SERVO AMPLIFIER NE544

DESCRIPTION

The NE544 is a servo amplifier and pulse-width demodulator with internal motor drive transistors. It is designed for remote control applications in digital proportional systems but can be used in many other closed loop position control applications. It incorporates a linear one shot for improved positional accuracy and outputs for external pnp motor drive transistors.

FEATURES

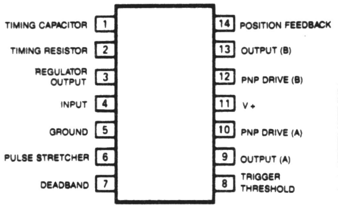
- **500mA load current capability**
- **Bidirectional bridge output with single power supply**
- **Low standby power drain**
- **Adjustable deadband and trigger thresholds**
- **High linearity, 0.5% maximum error**
- **Output drive for external PNP transistors (optional)**
- **Wide supply voltage range**

APPLICATIONS

- **Miniature position Servo**
- **Robotics**
- **Control devices**
- **Remote positioning**

PIN CONFIGURATIONS

N PACKAGE


TIMING CAPACITOR 1
TIMING RESISTOR 2
REGULATOR OUTPUT 3
INPUT 4
GROUND 5
PULSE STRETCHER 6
DEADBAND 7
14 POSITION FEEDBACK
13 OUTPUT (B)
12 PNP DRIVE (B)
11 V+
10 PNP DRIVE (A)
9 OUTPUT (A)
8 TRIGGER THRESHOLD

TOP VIEW

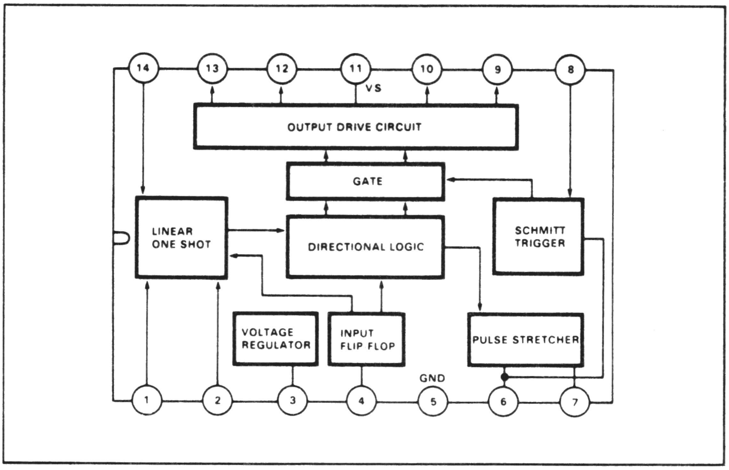
ORDER NUMBER
NE544N

ABSOLUTE MAXIMUM RATINGS

$T_A = 25°C$ unless otherwise specified.

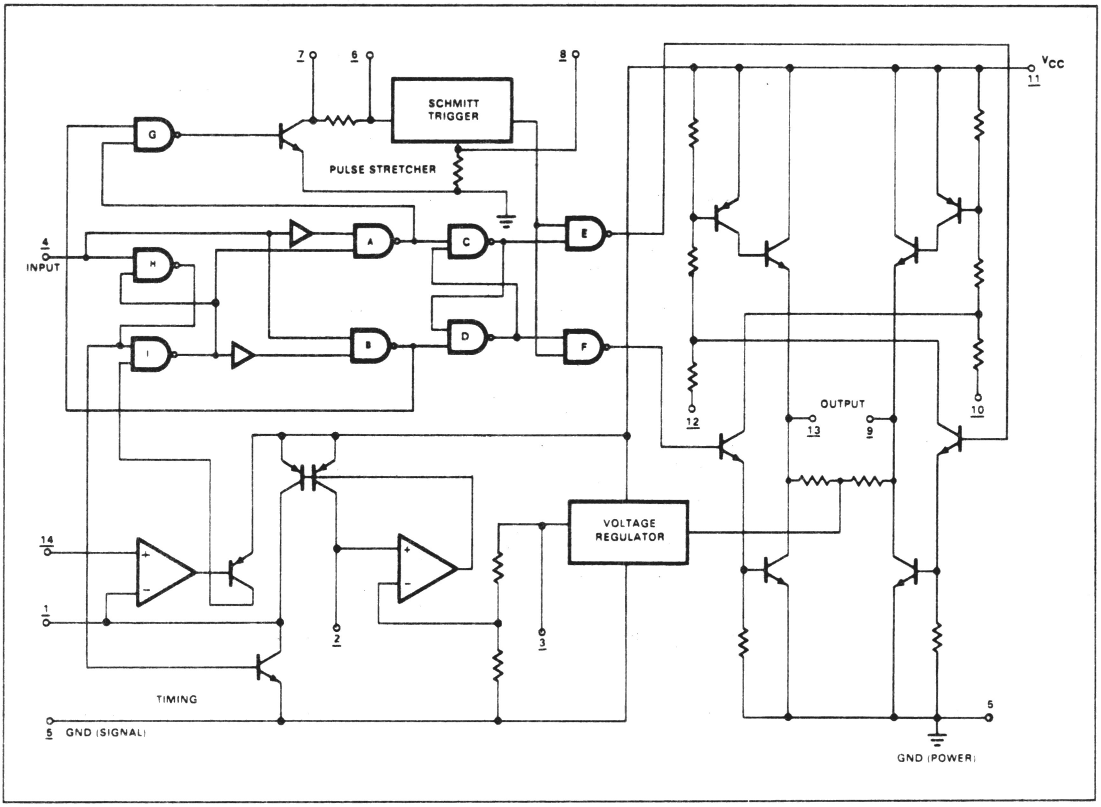
PARAMETER		RATING	UNIT
V+	Supply voltage	6.0	V
I_O	Output current	500	mA
T_A	Operating temperature	-20 to +75	°C
T_{stg}	Storage temperature	-65 to +150	°C

BLOCK DIAGRAM


14
13
12
11
VS
10
9
8
OUTPUT DRIVE CIRCUIT
GATE
LINEAR ONE SHOT
DIRECTIONAL LOGIC
SCHMITT TRIGGER
VOLTAGE REGULATOR
INPUT FLIP FLOP
PULSE STRETCHER
GND
1
2
3
4
5
6
7

SERVO AMPLIFIER NE544

EQUIVALENT CIRCUIT SCHEMATIC

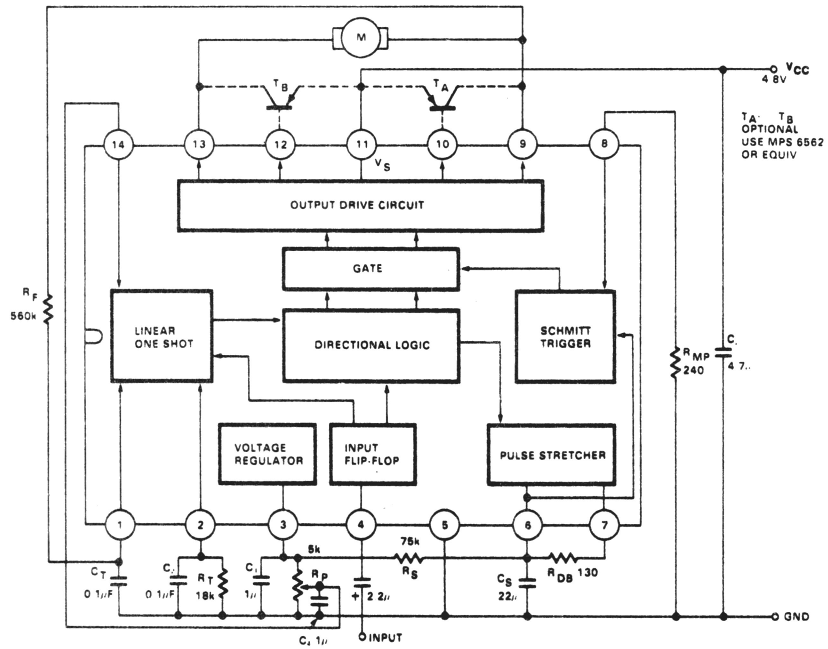

7
6
8
VCC
11
SCHMITT TRIGGER
G
PULSE STRETCHER
4
INPUT
H
A
C
E
I
B
D
F
12
10
OUTPUT
13
9
14
1
2
3
VOLTAGE REGULATOR
TIMING
5 GND (SIGNAL)
5
GND (POWER)

DC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_S = 4.8V unless otherwise specified.

PARAMETER			TEST CONDITIONS	LIMITS			UNIT
				Min	Typ	Max	
V_{CC}	Supply voltage			3.2	4.8	6	V
I_{CC}	Supply current	Pin 11	Quiescent	4.2	5.5	10	mA
V_{TH}	Input threshold	Pin 4					V
	On				1.5		
	Off				1.4		
Z_{IN}	Input resistance	Pin 4			18		kΩ
	Output voltage						V
V_{OL}	Low		Pin 9 or 13, I_L = 400mA		0.3		
V_{OH}	High				3.9		
V_{REG}	Regulated voltage	Pin 3		2.1	2.5	2.9	V
ΔV_{REG}	Regulation	Pin 3	3.9V ≤ V_{CC} ≤ 6V		10		mV/V
	Minimum dead band	Pin 7	R_{DB} = 0		1		μs
	One shot temperature coefficient				.01		%/°C
	Standby output voltage		Pin 9 and 13		2.5		V
	PNP drive current		Pin 10 and 12		20		mA

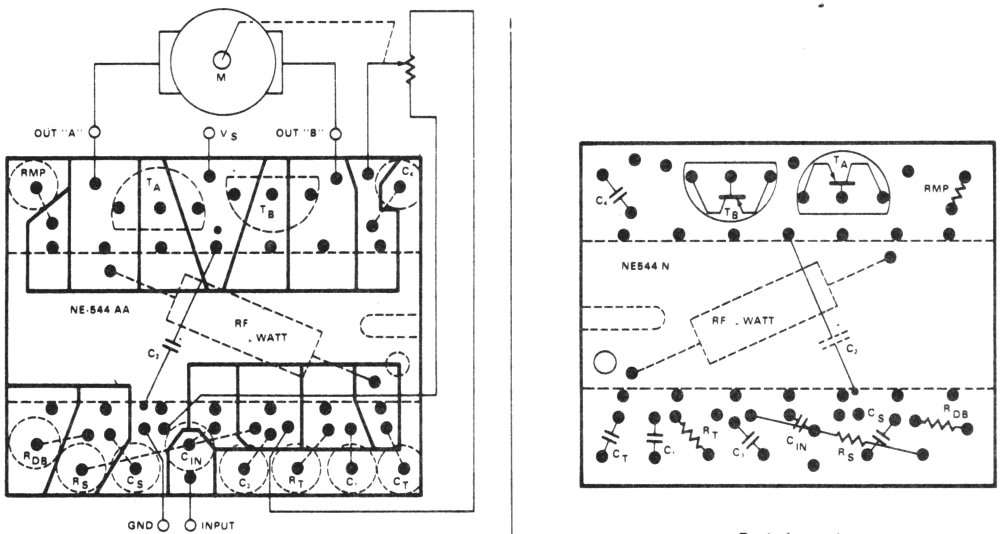
SERVO AMPLIFIER NE544

TYPICAL CONNECTION OF NE544N FOR LINEAR ONE SHOT TIMING


M
TB
TA
VCC
4 8V
TA· TB
OPTIONAL
USE MPS 6562
OR EQUIV
14
13
12
11
10
9
8
VS
OUTPUT DRIVE CIRCUIT
GATE
RF
560k
LINEAR
ONE SHOT
DIRECTIONAL LOGIC
SCHMITT
TRIGGER
RMP
240
C.
4 7..
VOLTAGE
REGULATOR
INPUT
FLIP-FLOP
PULSE STRETCHER
1
2
3
4
5
6
7
5k
75k
RS
CT
0 1μF
C.
0 1μF
RT
18k
C1
1μ
RP
+ 2 2μ
CS
22μ
RDB 130
GND
C2 1μ
INPUT

SERVO AMPLIFIER NE544

PC BOARD—N PACKAGE

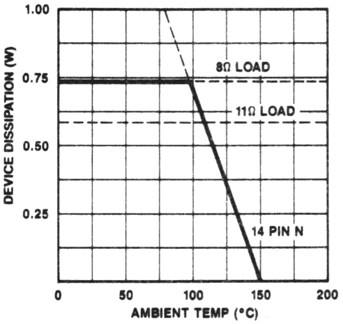

M
OUT "A"
V S
OUT "B"
RMP
T A
T B
C4
NE-544 AA
RF
WATT
C2
R DB
R S
C S
C IN
C3
R T
C1
C T
GND
INPUT
C4
T B
T A
RMP
NE544 N
RF
WATT
C2
C T
C1
R T
C1
C IN
C S
R S
R DB

Typical PC Board Layout Bottom View

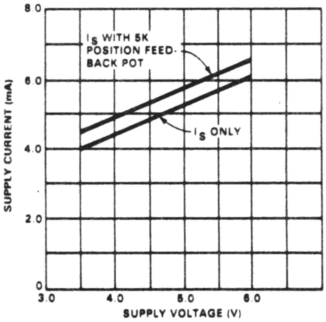
Parts Layout Top View

TYPICAL PERFORMANCE CHARACTERISTICS

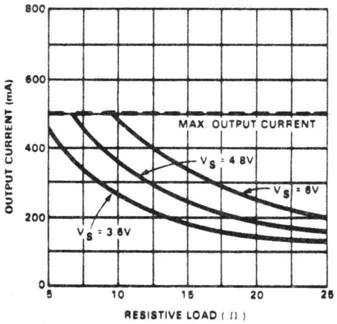
MAXIMUM DISSIPATION vs AMBIENT TEMPERATURE



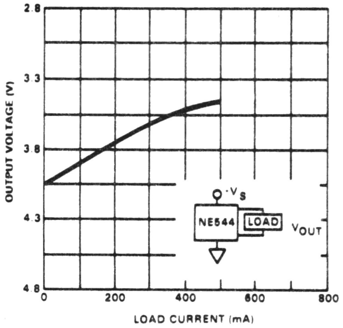
SUPPLY CURRENT vs SUPPLY VOLTAGE



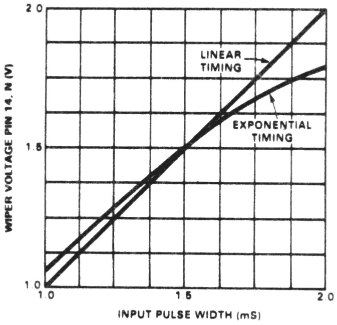
OUTPUT CURRENT vs LOAD RESISTANCE



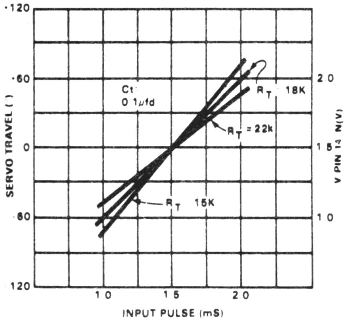
OUTPUT VOLTAGE vs LOAD CURRENT



INPUT PULSE WIDTH vs FEEDBACK POT OUTPUT



INPUT PULSE vs SERVO TRAVEL



*For additional information, consult the Applications Section.

VOLTAGE REGULATOR—SYMBOLS AND DEFINITIONS

Absolute Maximum Rating

Operating safe zones exceeding these limits could cause permanent damage to the device and are not meant to imply that devices can operate at these limits.

Current Limiting

The ability of the amplified segment to limit the output current of the device when safe operating limits are exceeded. Measured in amperes (pre-determined).

Efficiency

Regarding a regulator, the ratio of the total power input to the usable power output. Expressed as a percentage. (For example, if a regulator has a 50 watt input and a 40 watt output, its efficiency is 80 percent).

EMI/RFI

("Electromagnetic Interference/Radio Frequency Interference") regarding regulators, magnetic field disturbance and radio frequency interference signals generated especially by SMPS devices. Measurement is generally unspecified.

Line Regulation

Sometimes referred to as "static regulation". This term refers to the changes in the output as the input is varied slowly from its rated minimum value to its rated maximum value (from 105 VAC_{RMS} to 125 VAC_{RMS}). Measured in mv/V.

Load Regulation

Sometimes referred to as "dynamic regulation". This term refers to the changes in the output when load conditions are suddenly changed (from no load to full load). Measured in mv/V.

Package Type Designation

See full package designations in Appendix.

Power Dissipation

The power that the device can safely handle at 25°C. The dissipation must be derated as indicated for the individual package type.

Power Dissipation

The ability of the regulator to tolerate excessively high levels of input power while maintaining its operation within the safe operating area of its active devices. Measured in watts.

Safe Operating Area Restriction (SOAR)

Limits the output current of the amplifier to maintain safe (no thermal runaway) operating conditions. (Accomplished through internal sensor amplifiers.)

T_A

Ambient temperature range. Range of the surrounding environment of the operating device.

T_J

Junction Temperature. The maximum temperature of the device. 150°C is standard for silicon devices.

T_{SOLD}

Soldering Temperature. The temperature which can be applied to the lead frame of the device for short periods of time (normally specified for a duration of 10 sec).

T_{STG}

Storage temperature range. Temperature range that the device can be stored in a non-operating condition.

Thermal Regulation

Referred to as changes due to ambient variations of thermal drift. Also referred to as temperature coefficient, measured in ppm/°C or mv/°C.

Thermal Shutdown

The ability of the regulator to shut itself down when the maximum die temperature is exceeded. Measured in degrees Celsius (C).

Transient Response

The ability of a regulator to respond to rapid changes in line variations, load variations, or intermittent transient input conditions. (Transient Response is often referred to as "recovery time"). Measured in milliseconds (ms).

Truth Tables

0 is logic level low
1 is logic level high
X — don-t care condition — has no effect under circuit conditions listed.

V_{CC} ($-V_{CC}$)

Supply Voltage. The range of power supply voltage over which the device will operate safely.

Voltage Limiting

The ability of the regulator to "shut down" in the event that the internal reference sources fail to function properly. Measured in Volts.

SWITCHED-MODE POWER SUPPLY CONTROL CIRCUIT SE/NE5560

DESCRIPTION

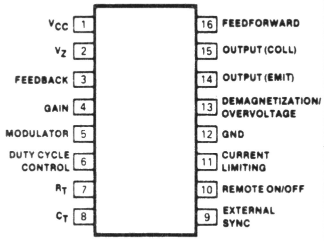
The SE/NE5560 is a control circuit for use in switched mode power supplies. This single monolithic chip incorporates all the control and housekeeping (protection) functions required in switched mode power supplies, including an internal temperature compensated reference source, internal Zener references, sawtooth generator, pulse width modulator, output stage and various protection circuits.

FEATURES

- **Stabilized power supply**
- **Temperature compensated reference source**
- **Sawtooth generator**
- **Pulse width modulator**
- **Remote on/off switching**
- **Current limiting**
- **Low supply voltage protection**
- **Loop fault protection**
- **Demagnetization/overvoltage protection**
- **Maximum duty cycle clamp**
- **Feed forward control**
- **External synchronization**

PIN CONFIGURATION

D,F,N PACKAGE


VCC 1
VZ 2
FEEDBACK 3
GAIN 4
MODULATOR 5
DUTY CYCLE CONTROL 6
RT 7
CT 8
16 FEEDFORWARD
15 OUTPUT (COLL)
14 OUTPUT (EMIT)
13 DEMAGNETIZATION/ OVERVOLTAGE
12 GND
11 CURRENT LIMITING
10 REMOTE ON/OFF
9 EXTERNAL SYNC

TOP VIEW

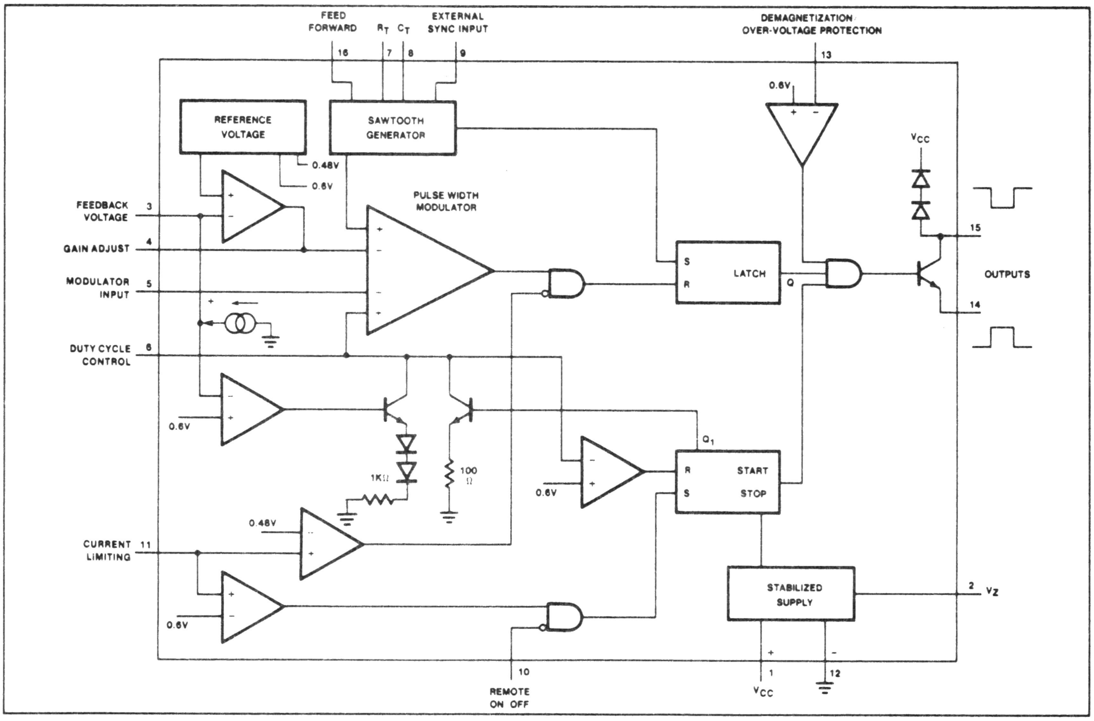
ORDER NUMBERS

NE5560N SE5560F
NE5560D SE5560N
NE5560F

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply[1]		
Voltage forced mode	+18	V
Current fed mode	30	mA
Output transistor (at 20-30V max)		
Output current	40	mA
Collector voltage (Pin 15)	V_{CC} + 1.4V	V
Max. emitter voltage (Pin 14)	+5	V
Operating temperature (ambient)		
SE5560	−55 to +125	°C
NE5560	0 to 70	°C
Storage temperature range	−65 to +150	°C

BLOCK DIAGRAM


FEED FORWARD
RT
CT
EXTERNAL SYNC INPUT
16
7
8
9
DEMAGNETIZATION OVER-VOLTAGE PROTECTION
13
0.6V
REFERENCE VOLTAGE
SAWTOOTH GENERATOR
0.48V
0.6V
PULSE WIDTH MODULATOR
VCC
FEEDBACK VOLTAGE 3
GAIN ADJUST 4
MODULATOR INPUT 5
DUTY CYCLE CONTROL 6
S
R
LATCH
Q
15
OUTPUTS
14
0.6V
Q1
1KΩ
100 Ω
0.6V
R
S
START
STOP
0.48V
CURRENT LIMITING 11
0.6V
STABILIZED SUPPLY
2 VZ
10
REMOTE ON OFF
+
−
1
VCC
12

Note:

1. See Voltage/Current fed supply characteristic curve.

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 12V unless otherwise specified)

PARAMETER	TEST CONDITIONS	SE5560			NE5560			UNIT
		Min	Typ	Max	Min	Typ	Max	
Reference Sections								
Internal reference voltage (V_{ref})	25°C	3.69	3.72	3.81	3.57	3.72	3.95	V
	Over temperature	3.65		3.85	3.53		4.00	V
Temperature coefficient of V_{ref}			-100			-100		ppm/°C
Internal Zener reference (V_Z)	I_L = -7 mA	7.8	8.4	8.8	7.8	8.4	8.8	V
Temperature coefficient of V_Z			200			200		ppm/°C
Oscillator Section								
Frequency range	Over temperature	50		100k	50		100k	Hz
Initial accuracy oscillator	R = 5 kΩ		5			5		%
Duty cycle range	f_o = 20 kHz	0		98	0		98	%
Modulator								
Modulation input current	Voltage at Pin 5 = 2V Over temperature		0.2	20		0.2	20	µA
Housekeeping Function								
Pin 6, input current	at 2V Over temperature		0.2	20		0.2	20	µA
Pin 6, duty cycle limit control	(for 50% maximum duty cycle) 15 kHz to 50 kHz/ 41% of V_Z	40	50	60	40	50	60	% of duty cycle
Pin 1, low supply voltage protection thresholds		8	9.0	10.5	8	9.0	10.5	V
Pin 3, feedback loop protection trip threshold		400	600	720	400	600	720	mV
Pin 3, pull up current	at 2V Over temperature	-7	-15	-35	-7	-15	-35	µA
Pin 13, demagnetization/over voltage protection trip on threshold		470	600	720	470	600	720	mV
Pin 13, input current	at 0.25V 25°C		-0.6	-10		-0.6	-10	µA
	Over temperature			-20			-20	
Pin 16, feed forward duty cycle control	Voltage at Pin 16 = 2V_Z	30	40	50	30	40	50	% original duty cycle
*Pin 16, feed forward input current	at 16V, V_{CC} = 18V 25°C		0.2	5		0.2	5	µA
	Over temperature			10			10	µA
External Synchronization								
Pin 9 off		0		0.8	0		0.8	V
on		2		V_Z	2		V_Z	V
sink current	Voltage at Pin 9 = 0V, 25°C		-65	-100		-65	-125	µA
	Over temperature			-125			-125	µA
Remote								
Pin 10 off		0		0.8	0		0.8	V
on		2		V_Z	2		V_Z	V
sink current	at 0V 25°C		-85	-100		-85	-125	µA
	Over temperature			-125			-125	µA
Current Limiting								
Pin 11, I_{IN}	Voltage at Pin 11 = 250 mV, 25°C		-2	-20		-2	-20	µA
	Over temperature			-40			-40	µA
Single pulse inhibit delay	Inhibit delay time for 20% overdrive at 40 mA I_{OUT}		0.7	0.8		0.7	0.8	µs
Trip Levels: Shut down, slow start		0.560	0.600	0.700	0.560	0.600	0.700	V
Current limit		0.400	0.480	0.500	0.400	0.480	0.500	V
Error Amplifier								
Output voltage swing (V_{OH})		6.2		9.5	6.2		9.5	V
Output voltage swing (V_{OL})				0.7			0.7	V
Open loop gain		54	60		54	60		dB
Feedback resistor		10k			10k			Ω
Small signal bandwidth			3			3		MHz

DC ELECTRICAL CHARACTERISTICS (Continued)

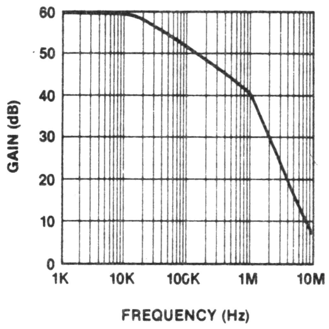
PARAMETER	TEST CONDITIONS	SE5560			NE5560			UNIT
		Min	Typ	Max	Min	Typ	Max	
Output Stage								
V_{CE}(SAT) $I_C = 40mA$				0.5			0.5	V
Output current (pin 15)		40			40			mA
Max emitter voltage (pin 14)		5	6		5	6		V
Supply Voltage/Current								
I_{CC}	$I_Z = 0$, voltage forced,							
	$V_{CC} = 12V$, 25°C			10			10	mA
	Over temp.			15			15	mA
V_{CC}	$I_{CC} = 10mA$ current fed	20		23	19		24	V
V_{CC}	$I_{CC} = 30mA$ current fed	20		30	20		30	V

Note:
Does not include current for timing resistors or capacitors. (See p. - "total standby current")

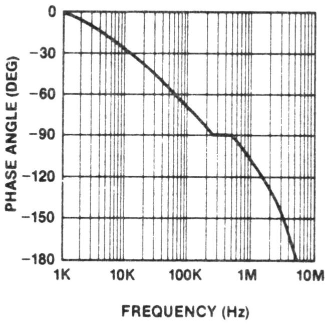
TYPICAL PERFORMANCE CHARACTERISTICS

ERROR AMPLIFIER

OPEN LOOP GAIN



OPEN LOOP PHASE



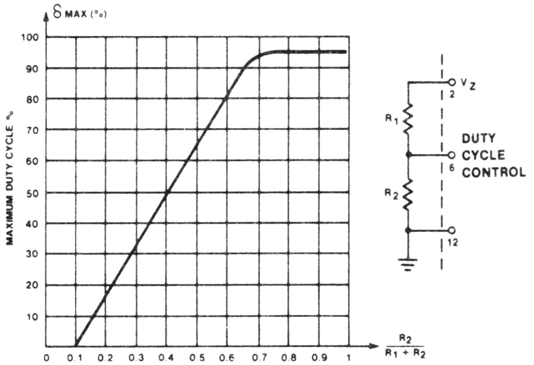
MAXIMUM PIN VOLTAGES

NE5560	
FUNCTION	MAXIMUM VOLTAGE
1. V_{CC}	See Note 1
2. V_Z	Do not force (8.4V)
3. Feedback	V_Z
4. Gain	
5. Modulator	V_Z
6. Duty Cycle Control	V_Z
7. R_T	Current force mode
8. C_T	
9. External Sync	V_Z
10. Remote On/Off	V_Z
11. Current Limiting	V_{CC}
12. GND	GND
13. Demagnetization/Overvoltage	V_{CC}
14. Output (Emit)	V_Z
15. Output (Collector)	V_{CC} + 2Vbe
16. Feed forward	V_{CC}

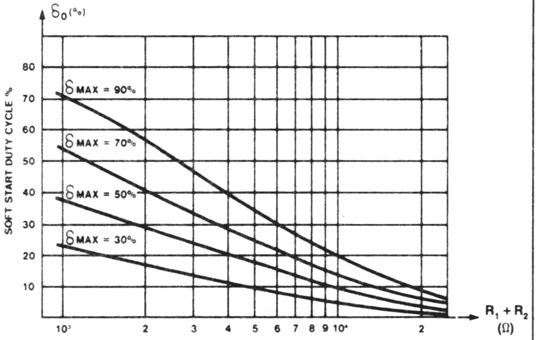
Note:
1. When voltage forced, maximum is 18V; when current fed, maximum is 30mA. See voltage/current fed supply characteristic curve.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

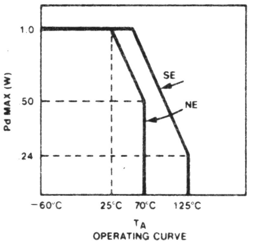
GRAPH FOR DETERMINING δ MAX



SOFT-START MIN DUTY CYCLE vs $R_1 + R_2$

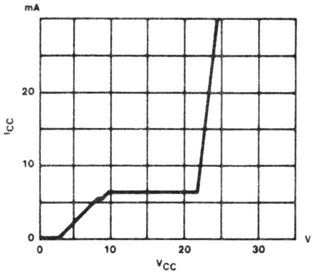


POWER DERATING CURVE

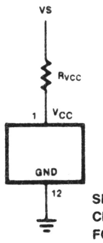


$P_d = V_{CC} I_{CC} + (V_{CC} - V_Z) I_Z$
$+ [(V_{15} - V_{14}) I_{15} \times \text{DUTY CYCLE}]$

NE5560 VOLTAGE/CURRENT FED SUPPLY CHARACTERISTICS



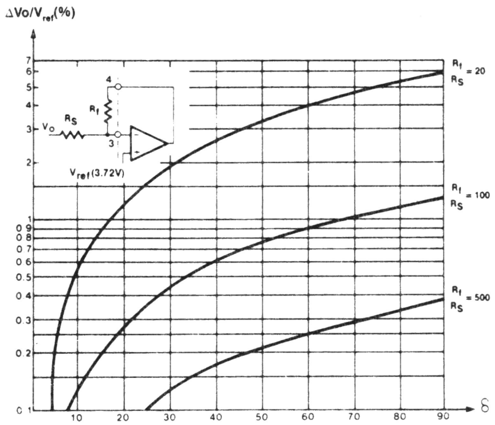
CURRENT FED DROPPING RESISTOR



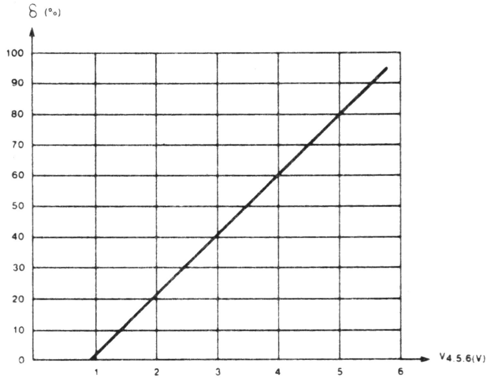
$R_{VCC} = \frac{V_S - V_{CC}}{(10 \text{ to } 20 \text{ mA})}$

SEE DC ELECTRICAL CHARACTERISTICS FOR CURRENT FED V_{CC} RANGE.

REGULATION vs ERROR AMP CLOSED LOOP GAIN

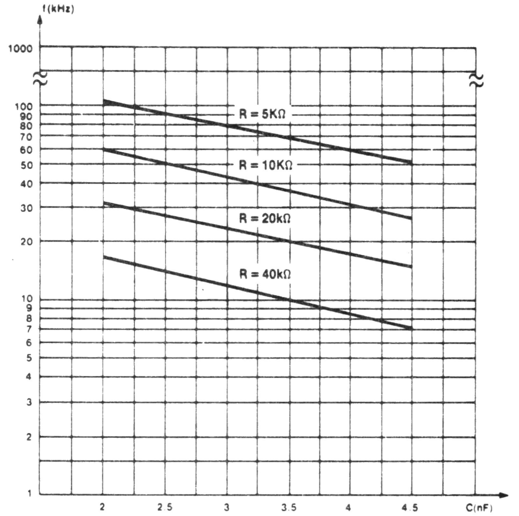


TRANSFER CURVE OF PULSE WIDTH MODULATOR DUTY CYCLE vs INPUT VOLTAGE

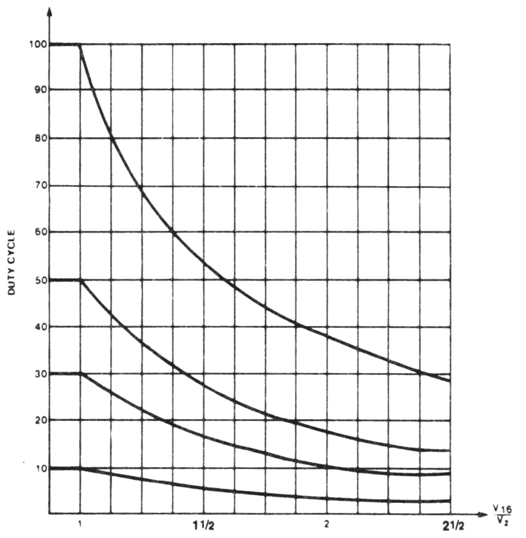


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

TYPICAL FREQUENCY PLOT vs R_T AND C_T



DUTY CYCLE SENSITIVITY TO FEED FORWARD VOLTAGE (PIN 16)



THEORY OF OPERATION

The following functions are incorporated:

- A temperature compensated reference source.
- An error amplifier with pin 3 as input. The output is connected to pin 4 so that the gain is adjustable with external resistors.
- A sawtooth generator with a TTL-compatible synchronization input (pins 7,8,9).
- A pulse-width modulator with a duty-cycle range from 0 to 95%.

(The PWM has two additional inputs:

Pin 6 can be used for a precise setting of δ max.

Pin 5 gives a direct access to the modulator, allowing for real constant current operation:)

- A gate at the output of the PWM provides a simple dynamic current limit.
- A latch that is set by the flyback of the sawtooth and reset by the output pulse of the above-mentioned gate prohibits double pulsing.
- Another latch functions as a start-stop circuit; it provides a fast switch-off and a slow start.
- A current protection circuit that operates via the start-stop circuit. This is a combined function with the current limit circuit, therefore pin 11 has two trip-on levels; the lower one for cycle-by-cycle current limiting, the upper one for current protection by means of switch-off and slow-start.
- A TTL-compatible remote on/off input at pin 10, also operating via the start-stop circuit.
- An inhibit input at pin 13. The output pulse can be inhibited immediately.
- An output gate that is commanded by the latches and the inhibit circuit.
- An output transistor of which both the collector (pin 15) and the emitter (pin 14) are externally available. This allows for normal or inverse output pulses.
- A power supply that can be either voltage or current driven (pins 1 and 12). The internally generated stabilized output voltage V_Z is connected to pin 2.
- A special function is the so-called feed-forward at pin 16. The amplitude of the sawtooth generator is modulated in such a way that the duty cycle becomes inversely proportional to the voltage on this pin: $\delta \sim 1/V16$
- Loop fault protection circuits assure that the duty-cycle is reduced to zero or a low value for open or short-circuited feedback loops.

Stabilized Power Supply (Pins 1, 2, 12)

The power supply of the NE5560 is of the well known series regulation type and provides a stablized output voltage of typically 8.5 volts.

This voltage V_Z is also present at pin 2 and can be used for precise setting of δ max. and to supply external circuitry. Its maximum current capability is 5mA.

The circuit can be fed directly from a DC voltage source between 10.5V and 18V or can be current driven via a limiting resistor. In the latter case, internal pinch-off resistors will limit the maximum supply voltage; typical 23V for 10mA and maximum 30V for 30mA.

The low supply voltage protection is active when V(1-12) is below 10.5V and inhibits the output pulse (no hysteresis).

When the supply voltage surpasses the 10.5V level, the IC starts delivering output pulses via the slow-start function.

The current consumption at 12V is less than 10mA, provided that no current is drawn from V_Z and $R(7-12) \geq 20k\Omega$.

The Sawtooth Generator

Figure 2 shows the principal circuitry of the oscillator. A resistor between pin 7 and pin 12 (ground) determines the constant current that charges the timing capacitor C(8–12).

This causes a linear increasing voltage on pin 8 until the upper level of 5.6V is reached. Comparator H sets the RS flip flop and Q1 discharges C(8–12) down to 1.1V, where comparator L resets the flip-flop. During this flyback time, Q2 inhibits the output.

Synchronization at a frequency lower than the free-running frequency is accomplished via the TTL gate on pin 9. By activating this gate ($V^9 < 2V$), the setting of the sawtoothis prevented. This is indicated in Figure 3.

Figure 4 shows a typical plot of the oscillator frequency against the timing capacitor. The frequency range of the NE5560 goes from <50Hz up to >100kHz.

Reference Voltage Source

The internal reference voltage source is based on the bandgap voltage of silicon. Good design practice assures a temperature dependency typically ± 100ppm/°C. The reference voltage is connected to the positive input of the error amplifier and has a typical value of 3.72V.

Error Amp Compensation

For closed loop gains less than 40 dB, it is necessary to add a simple compensation capacitor as shown in Figures 4, 5.

SAWTOOTH GENERATOR

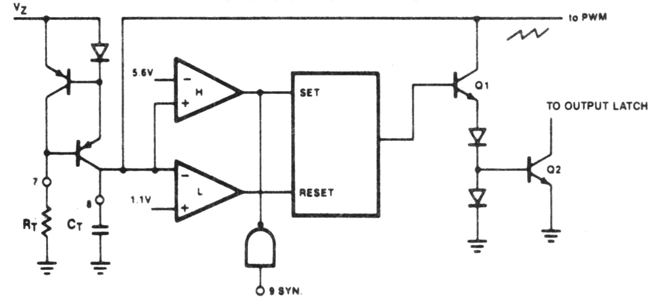


Figure 2

SAWTOOTH OSCILLATOR SYNCHRONIZATION

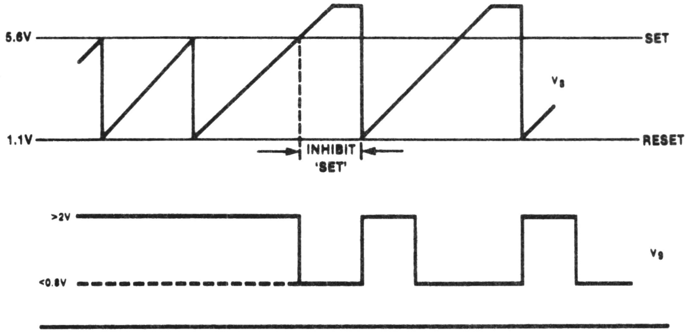


Figure 3

ERROR AMPLIFIER COMPENSATION

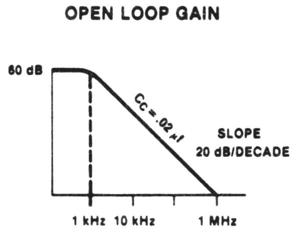


Figure 4

ERROR AMPLIFIER

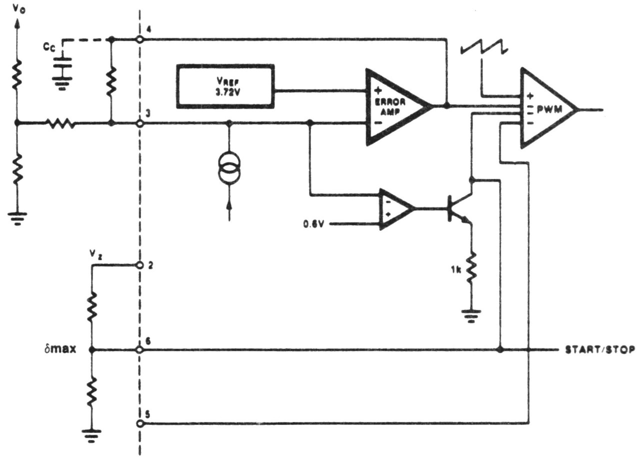


Figure 5

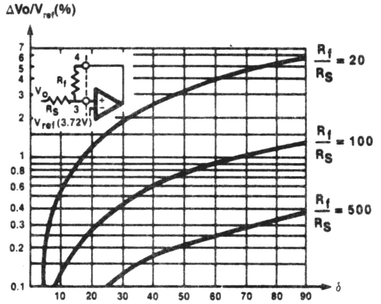
Error Amplifier with Loop-Fault Protection Circuits

This operational amplifier is of a generally used concept and has an open loop gain of typically 60dB. As can be seen in Figure 5, the inverting input is connected to pin 3 for a feedback information proportional to V_O.

The output goes to the PWM circuit, but is also connected to pin 4, so that the required gain can be set with R_S and R(3-4). This is indicated in Figure 5, showing the relative change of the feedback voltage as a function of the duty cycle. Additionally, pin 4 can be used for phase shift networks that improve the loop stability.

When the SMPS feedback loop is interrupted, the error amplifier would settle in the middle of its active region because of the feedback via R(3-4). This would result in a large duty cycle. A current source on pin 3 prevents this by pushing the input voltage high via the voltage drop over R(3-4). As a result, the duty cycle will become zero, provided that R(3-4)>100k. When the feedback loop is shortcircuited, the duty cycle would jump to the adjusted maximum duty cycle. Therefore, an additional comparator is active for feedback voltages at pin 3 below 0.6V. Now an internal resistor of typically 1k is shunted to the impedance on the δ_{max} setting pin 6. Depending on this impedance, δ will be reduced to a value δo. This will be discussed further.

DUTY CYCLE —δ— % REGULATION



PULSE WIDTH MODULATION

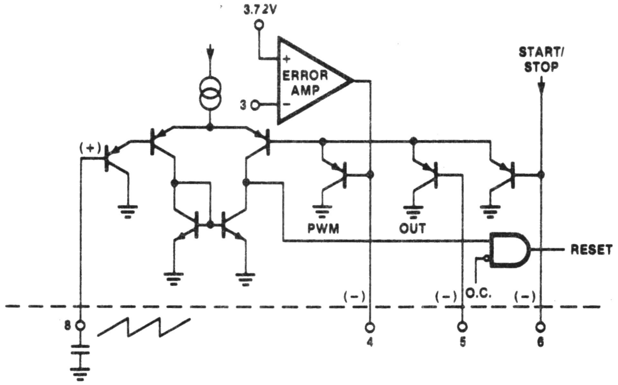


Figure 6

TRANSFER CURVE OF PULSE WIDTH MODULATOR DUTY CYCLE vs INPUT VOLTAGE

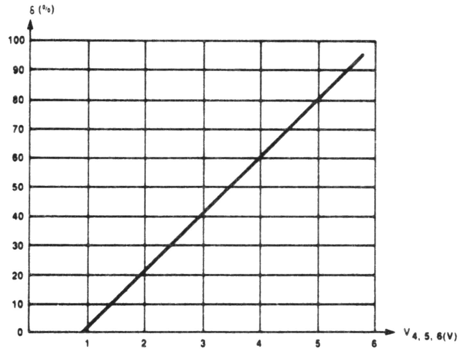


Figure 7

GRAPH FOR DETERMINING δ MAX

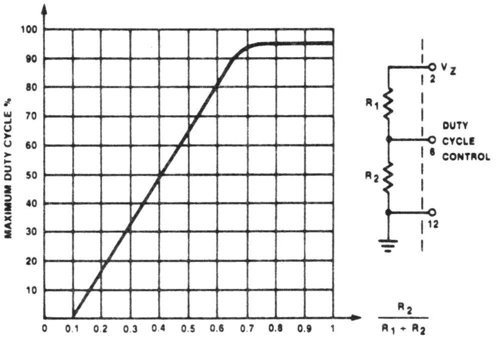


Figure 8

SOFT-START MIN DUTY CYCLE vs $R_1 + R_2$

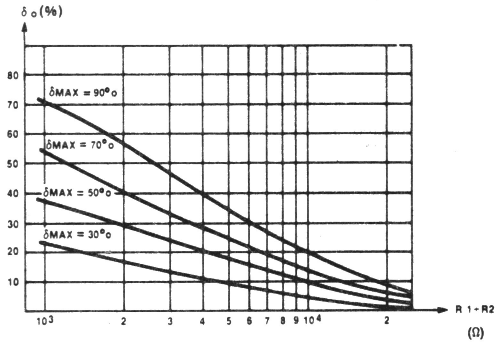


Figure 9

CURRENT PROTECTION INPUT

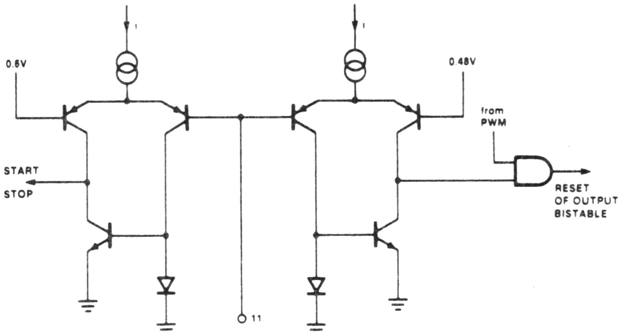


Figure 10

The Pulse-Width Modulator

The function of the PWM circuit is to translate a feedback voltage into a periodical pulse of which the duty cycle depends on that feedback voltage. As can be seen in Figure 6, the PWM circuit in the NE5560 is a long-tailed pair in which the sawtooth on pin 8 is compared with the LOWEST voltage on either pin 4 (error amplifier), pin 5, or pin 6 δ_{max} and slow-start). The transfer graph is given in Figure 7. The output of the PWM causes the resetting of the output bistable.

Limitation of the Maximum Duty Cycle

With pins 5 and 6 not connected and with a rather low feedback voltage on pin 3, the NE5560 will deliver output pulses with a duty cycle of ≈95%. In many SMPS applications, however, this high δ will cause problems. Especially in forward converters, where the transformer will saturate when δ exceeds 50%, a limitation of the maximum duty-cycle is a must.

A DC voltage applied to pin 6 (PWM input) will set δ_{max} at a value in accordance with Figure 7. For low tolerances of δ_{max}, this voltage on pin 6 should be set with a resistor divider from V_Z (pin 2). The upper and lower sawtooth levels are also set by means of an internal resistor divider from V_Z, so forming a bridge configuration with the δ_{max} setting is low because tolerances in V_Z are compensated and the sawtooth levels are determined by internal resistor matching rather than by absolute resistor tolerance. Figure 8 can be used for determining the tap on the bleeder for a certain δ_{max} setting.

As already mentioned, Figure 9 gives a graphical representation of this. The value δo is limited to the lower and the higher side;

- It must be large enough to ensure that at maximum load and minimum input voltage the resulting feedback voltage on pin 3 exceeds 0.6V.
- It must be small enough to limit the amount of energy in the SMPS when a loop-fault occurs. In practice a value of 10-15% will be a good compromise.

Extra PWM Input (Pin 5)

The PWM has an additional inverting input: pin 5. It allows for attacking the duty cycle via the PWM circuit, independently from the feedback and the δ_{max} information. This is necessary when the SMPS must have a real constant current behavior, possibly with a fold-back characteristic. However, the realization of this feature must be done with additional external components. When not used, pin 5 should be tied to pin 6.

Dynamic Current Limit and Current Protection (Pin 11)

In many applications, it is not necessary to have a real constant current output of the SMPS.

Protection of the power transistor will be the prime goal. This can be realized with the NE5560 in an economical way. A resistor (or a current transformer) in the emitter of the power transistor gives a replica of the collector current. This signal must be connected to pin 11. As can be seen in Figure 10, this input has two comparators with different reference levels. The output of the comparator with the lower 0.48V reference is connected to the same gate as the output of the PWM.

OUTPUT CHARACTERISTIC

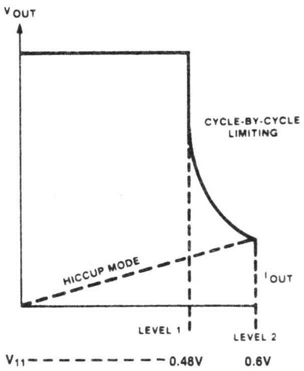


Figure 11

When activated, it will immediately reset the output flip flop, so reducing the duty cycle. The effectiveness of this cycle-by-cycle current limit diminishes at low duty cycle values. When δ becomes very small, the storage time of the power transistor becomes dominant. The current will now increase again, until it surpasses the reference of the second comparator. The output of this comparator activates the start/stop circuit and causes an immediate inhibit of the output pulses. After a certain dead-time, the circuit starts again with very narrow output pulses. The effect of this two-level current protection circuit is visualized in Figure 11.

The Start/Stop Circuit

The function of this protection circuit is to stop the output pulses as soon as a fault occurs and to keep the output stopped for several periods. After this dead time, the output starts with a very small, gradually increasing duty cycle. When the fault is persistent, this will cause a cyclic switch-off/switch-on condition. This "hiccup" mode limits effectively the energy during fault conditions. The realization and the working of the circuit is indicated in the Figures 12 and 13. The dead-time and the soft-start are determined by an external capacitor that is connected to pin 6 (δ_{max} setting).

A RS flip flop can be set by three different functions:

1. Remote on/off on pin 10.
2. Overcurrent protection on pin 11.
3. Low supply voltage protection (internal).

As soon as one of these functions cause a setting of the flip flop, the output pulses are blocked via the output gate. In the same time transistor Q1 is forward-biased, resulting in a discharge of the capacitor on pin 6.

The discharging current is limited by an internal 150Ω resistor in the emitter of Q1. The voltage at pin 6 decreases to below the lower level of the sawtooth. When V6 has dropped to 0.6V, this will activate a comparator and the flip flop is reset. The output stage is no longer blocked and Q1 is cut-off. Now V_Z will charge the capacitor via R1 to the normal δ_{max} voltage. The output starts delivering very narrow pulses as soon as V6 exceeds the lower sawtooth level. The duty-cycle of the output pulse now gradually increases to a value determined by the feedback on pin 3, or by the static δ_{max} setting on pin 6.

START/STOP CIRCUIT

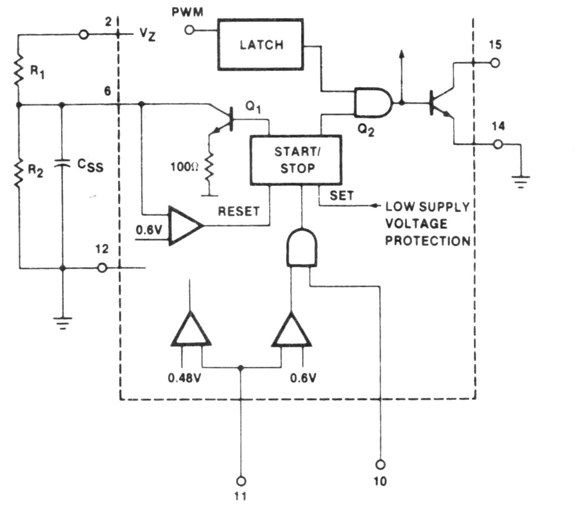


Figure 12

START/STOP CIRCUIT

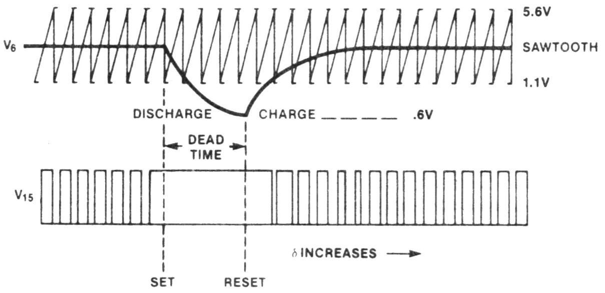


Figure 13

Remote On/Off Circuit (Pin 10)

In systems where two or more power supplies are used, it is often necessary to switch these supplies on and off in a sequential way. Furthermore, there are many applications in which a supply must be switched by a logical signal. This can be done via the TTL-compatible remote on/off input on pin 10. The output pulse is inhibited for levels below 0.8V. The output of the IC is no longer blocked when the remote on/off input is left floating or when a voltage >2V is applied. Start up occurs via the slow-start circuit.

The Output Stage

The output stage of the NE5560 contains a flip flop, a push-pull driven output transistor, and a gate, as indicated in Figure 14. The flip flop is set by the flyback of the sawtooth. Resetting occurs by a signal either from the PWM or the current limit circuit. With this configuration, it is assured that the output is switched only once per period, thus prohibiting double pulsing. The collector and emitter of the output transistor are connected to respectively pin 15 and pin 14, allowing for normal or inverted output pulses. An internally grounded emitter would cause untolerable voltage spikes over the bonding wire, especially at high output currents.

This current capability of the output transistor is 40mA peak for $V_{CE} = 0.4V$. An internal clamping diode to the supply voltage protects the collector against overvoltages. The maximum voltage at the emitter (pin 14) must not exceed +5V. A gate, activated by one of the set or reset pulses, or by a command from the start-stop circuit will immediately switch-off the output transistor by short-circuiting its base. The external inhibitor (pin 13) operates also via this base.

Demagnetization Sense

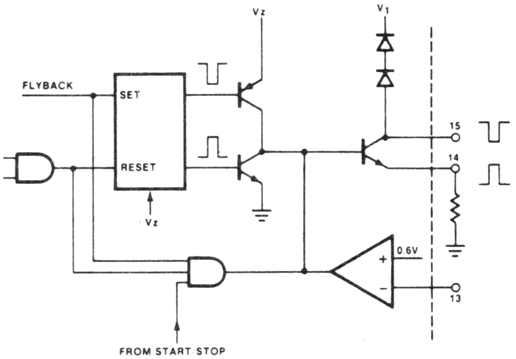
As indicated in Figure 14, the output of this NPN comparator will block the output pulse, when a voltage above 0.6V is applied to pin 13. A specific application for this function is to prevent saturation of forward converter transformers. This is indicated in Figure 15.

Feed-Forward (Pin 16)

The basic formula for a forward converter is

$$V_{OUT} = \frac{\delta V_{in}}{n} \text{ (n = transformer ratio)}$$

OUTPUT STAGE



NOTE:
The signal V_{13} can be derived from the demagnetizing winding in a forward converter as shown below.

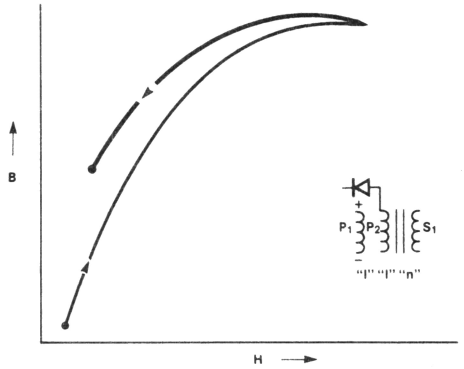


Figure 14

OUTPUT STAGE INHIBIT

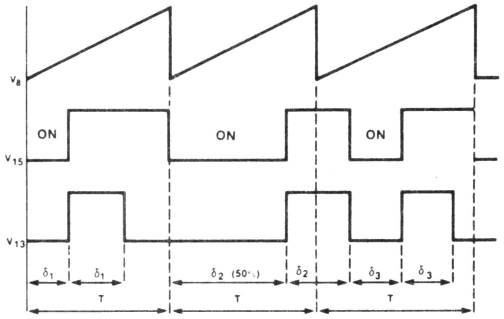


Figure 15

This means that in order to keep V_{OUT} at a constant value, the duty cycle δ must be made inversely proportional to the input voltage. A preregulation (feed-forward) with the function $\delta \sim 1/V_{in}$ can ease the feedback-loop design.

This loop now only has to regulate for load variations, which require only a low feedback gain in the normal operation area. The transformer of a forward converter must be designed in such a way that it does not saturate, even under transient conditions, where the maximum inductance is determined by $\delta_{max} \times V_{IN}$ max. A regulation of $\delta_{max} \sim 1/V_{IN}$ will allow for a considerable reduction or simplification of the transformer. The function of $\delta \sim 1/V_{IN}$ can be realized by using pin 16 of the NE5560.

Figure 16 shows the electrical realization. When the voltage at pin 16 exceeds the stabilized voltage V_Z (pin 2), it will increase the charging current for the timing capacitor on pin 8.

The operating frequency is not affected, because the upper trip level for sawtooth increases also. Note that the δ_{max} voltage on pin 6 remains constant because it is set via V_Z. Figure 17 visualizes the effect on δ_{max} and the normal operating duty cycle δ. For $V_{16} = 2 \times V_Z$ these duty cycles have halved. The graph for $\delta = f(V_{16})$ is given in Figure 18. (Note: V_{16} must be less than Pin 1 voltage.)

APPLICATIONS

NE/SE5560 Push-Pull Regulator

This application describes the use of the Signetics NE/SE5560 adapted to function as a push-pull switched mode regulator, as shown in Figures 19 and 20.

Input voltage range is +12 to +18V for a nominal output of +30 and −30V at a maximum load current of 1A with an average efficiency of 81%.

Features include feed forward input compensation, cycle-to-cycle drive current protection and other voltage sensing, line (to positive output) regulation <1% for an input range of +13 to +18V and load regulation to positive output of <3% for $\Delta I_L(+)$ of 0.1 to 1 Amp.

The main pulse width modulator operates to 48 kHz with power switching at 24 kHz.

EXTERNAL δ MAXIMUM CONTROL

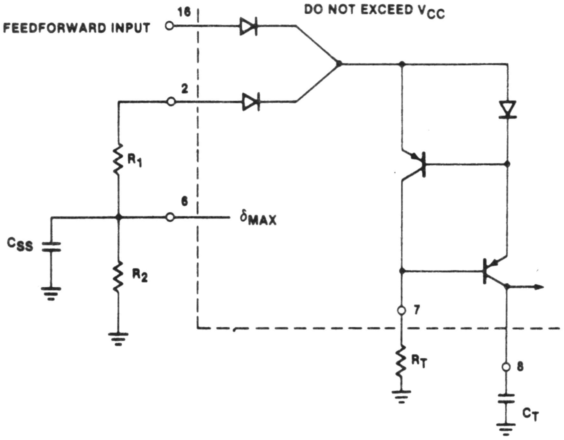


Figure 16

FEED FORWARD CIRCUITRY

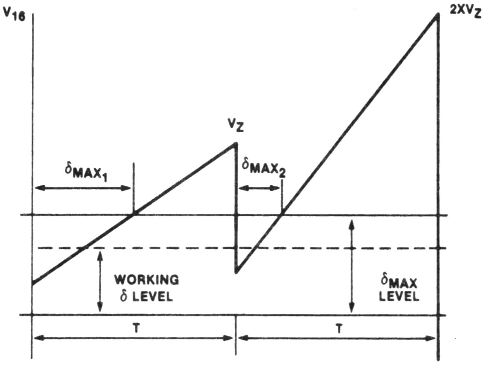


Figure 17

FEED-FORWARD REGULATION

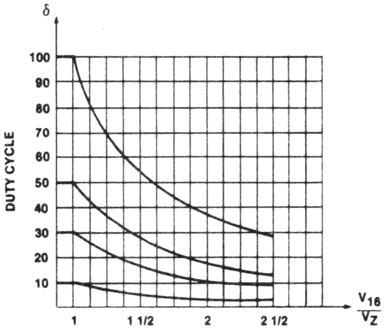
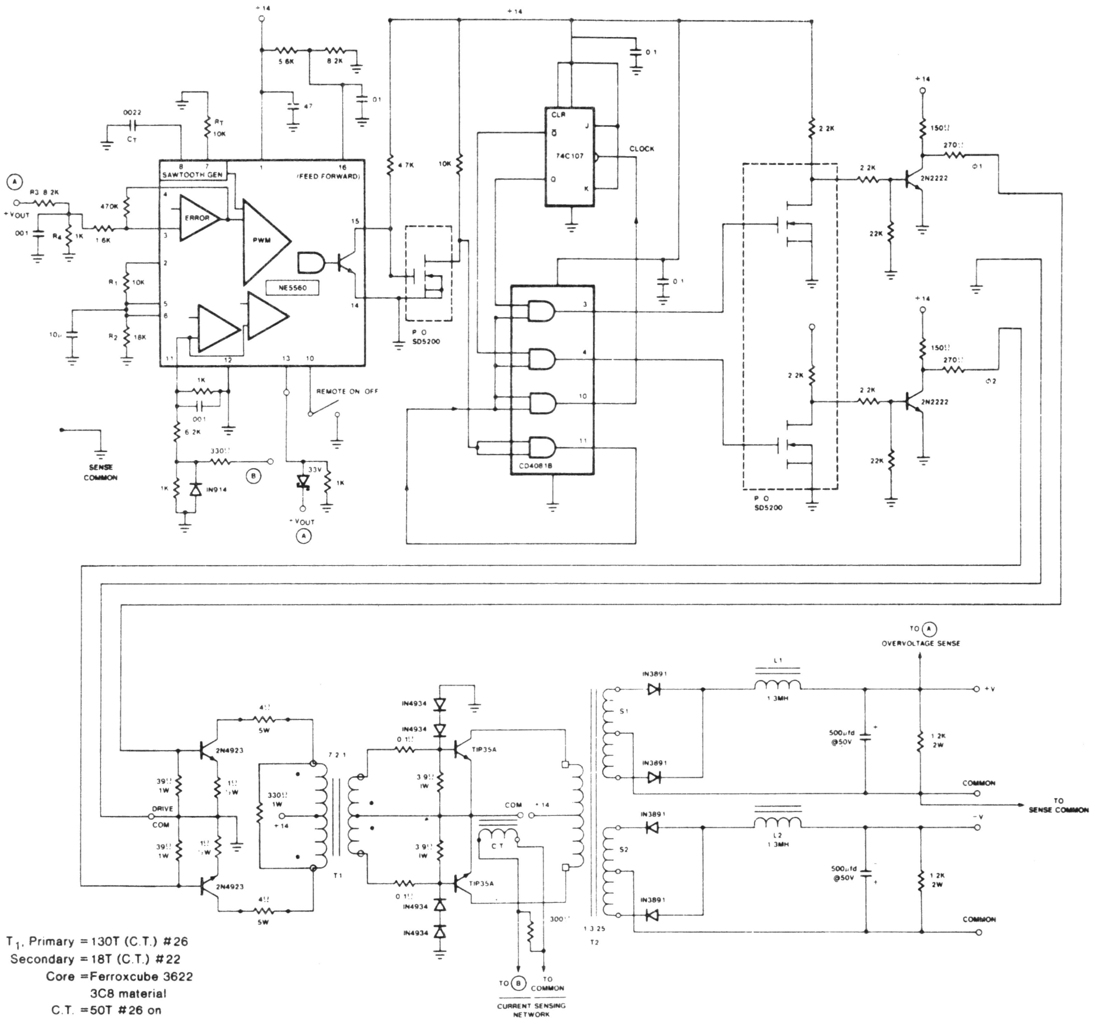


Figure 18

SWITCHED-MODE POWER SUPPLY CONTROL CIRCUIT SE/NE5560

NE/SE5560 PUSH-PULL SWITCH MODE REGULATED SUPPLY WITH CMOS DRIVE CONVERSION LOGIC


+14
5.6K
8.2K
.47
.01
.0022
CT
RT
10K
SAWTOOTH GEN
(FEED FORWARD)
8
7
1
16
4
3
2
5
6
11
12
13
10
15
14
A
R3 8.2K
+VOUT
.001
R4
1K
470K
1.6K
ERROR
PWM
NE5560
R1
10K
R2
18K
10µ
1K
.001
6.2K
330Ω
IN914
B
SENSE COMMON
REMOTE ON OFF
33V
+VOUT
4.7K
10K
P.O.
SD5200
CLR
J
Q̄
74C107
CLOCK
Q
K
.01
CD4081B
2.2K
22K
150Ω
270Ω
2N2222
Φ1
Φ2
TO A
OVERVOLTAGE SENSE
L1
1.3MH
IN3891
+V
500µfd
@50V
1.2K
2W
S1
S2
COMMON
TO SENSE COMMON
-V
L2
1.3MH
2N4923
4Ω
5W
39Ω
1W
1Ω
½W
DRIVE
COM
330Ω
1W
+14
T1
7.2:1
IN4934
0.1Ω
TIP35A
3.9Ω
1W
COM
C.T.
300Ω
1:3.25
T2
TO B
TO COMMON
CURRENT SENSING NETWORK

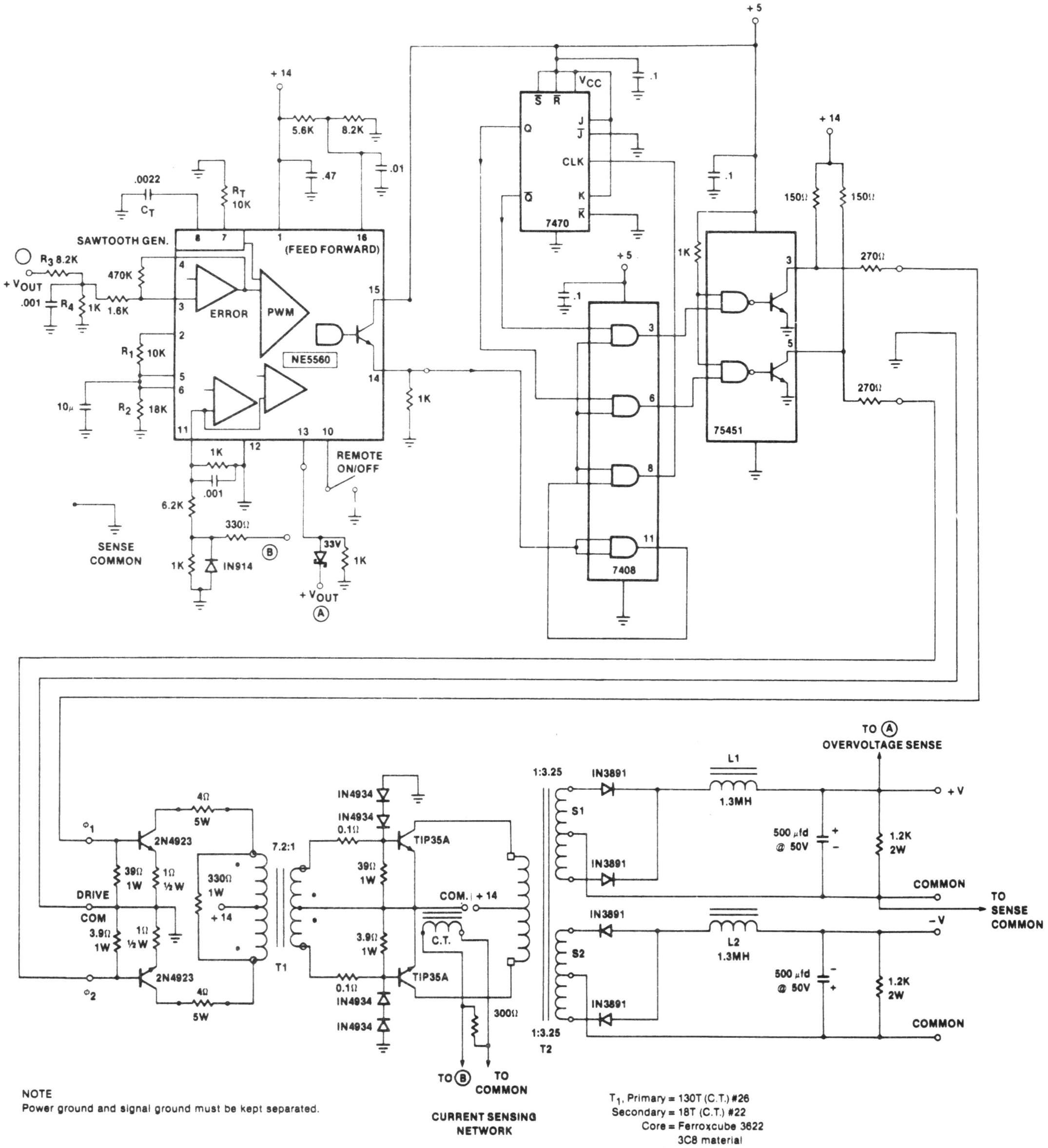
T_1, Primary = 130T (C.T.) #26
Secondary = 18T (C.T.) #22
Core = Ferroxcube 3622
3C8 material
C.T. = 50T #26 on
Ferroxcube 2616 core (3C8)
F2D bobbin
T_2, Primary = 16T (C.T.) # 18 Secondaries (each) 52T (C.T.) #22,
Core = Ferroxcube 4229 3C8 material
L_1, L_2 120T #20 on single gapped EC35 Ferroxcube core. 3C8 material

NOTE
Power ground and signal ground must be kept separated.

Figure 19

SWITCHED-MODE POWER SUPPLY CONTROL CIRCUIT SE/NE5560

NE/SE5560 PUSH-PULL SWITCH MODE REGULATED SUPPLY
WITH TTL DRIVE CONVERSION LOGIC


+5
+14
5.6K
8.2K
.47
.01
.0022
C_T
R_T 10K
SAWTOOTH GEN.
8
7
1
16
(FEED FORWARD)
R_3 8.2K
+V_{OUT}
470K
.001
R_4
1K
1.6K
4
3
2
5
6
11
12
13
10
14
15
ERROR
PWM
NE5560
R_1 10K
10μ
R_2 18K
1K
.001
6.2K
330Ω
Ⓑ
1K
IN914
REMOTE ON/OFF
33V
1K
+V_{OUT}
Ⓐ
SENSE COMMON
S̄
R̄
V_{CC}
.1
Q
J
J̄
CLK
Q̄
K
K̄
7470
.1
7408
3
6
8
11
1K
75451
150Ω
150Ω
270Ω
270Ω
TO Ⓐ
OVERVOLTAGE SENSE
L1
1.3MH
1:3.25
IN3891
S1
S2
+V
500 μfd @ 50V
1.2K 2W
COMMON
TO SENSE COMMON
−V
L2
1.3MH
T2
ϕ_1
ϕ_2
2N4923
4Ω 5W
39Ω 1W
1Ω ½W
330Ω 1W
+14
DRIVE COM
3.9Ω 1W
7.2:1
T1
IN4934
0.1Ω
TIP35A
39Ω 1W
3.9Ω 1W
COM. +14
C.T.
300Ω
TO Ⓑ
TO COMMON
CURRENT SENSING NETWORK

NOTE
Power ground and signal ground must be kept separated.

T_1, Primary = 130T (C.T.) #26
Secondary = 18T (C.T.) #22
Core = Ferroxcube 3622
3C8 material
C.T. = 50T #26 on
Ferroxcube 2616 core (3C8)
F2D bobbin
T_2, Primary = 16T (CT.) #18 Secondaries (each) 52T (C.T.) #22,
Core = Ferroxcube 4229 3C8 material
L_1, L_2 = 120T #20 on single gapped EC35 Ferroxcube core. 3C8 material.

Figure 20

SWITCHED-MODE POWER SUPPLY CONTROL CIRCUIT SE/NE5561

DESCRIPTION

The NE5561/SE5561 is a control circuit for use in switched mode power supplies. It contains an internal temperature compensated supply, PWM, sawtooth oscillator, over-current sense latch, and output stage. The device is intended for low cost SMPS applications where extensive housekeeping functions are not required.

FEATURES

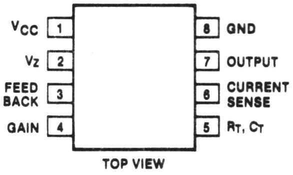
- **Micro-miniature (D) package**
- **Pulse-width modulator**
- **Current limiting (cycle by cycle)**
- **Sawtooth generator**
- **Stabilized power supply**
- **Double pulse protection**
- **Internal temperature compensated reference**

APPLICATIONS

- **Switched mode power supplies**
- **D/C motor controller inverter**
- **DC/DC converter**

PIN CONFIGURATION

D, FE, N PACKAGES


VCC 1
VZ 2
FEED BACK 3
GAIN 4
8 GND
7 OUTPUT
6 CURRENT SENSE
5 RT, CT
TOP VIEW

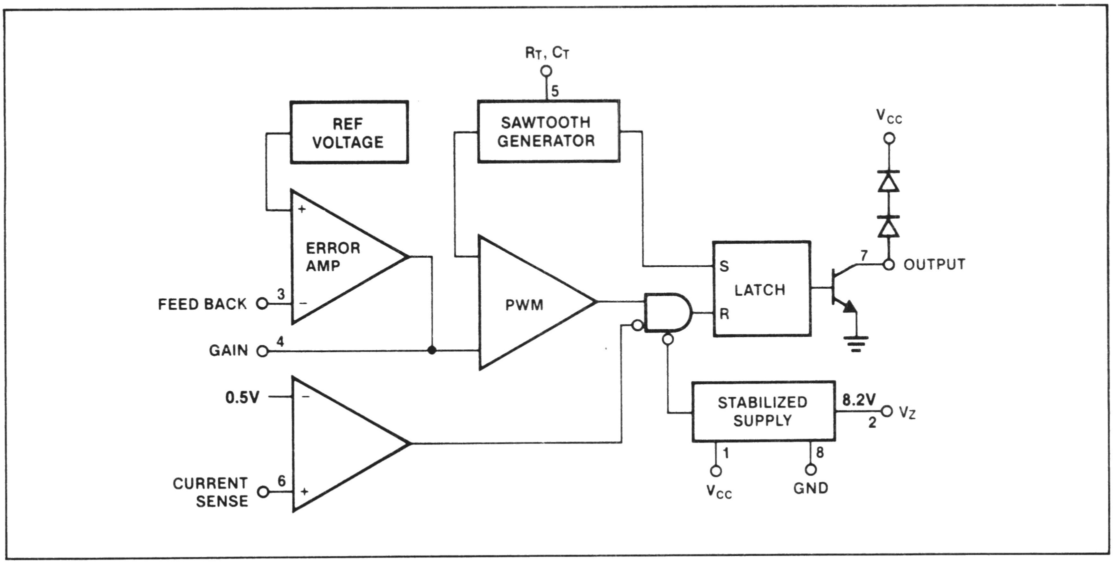
ORDER NUMBERS
NE5561D, NE5561FE, NE5561N,
SE5561FE, SE5561N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply[1]		
Voltage forced mode	+18	V
Current fed mode	30	mA
Output transistor (at 20-30V max)		
Output current	40	mA
Output voltage	V_{CC} + 1.4V	V
Output duty cycle	98	%
Max. total power dissipation	0.75	W
Operating temperature range		
SE5561	−55 to +125	°C
NE5561	0 to 70	°C

NOTE 1: See Voltage/Current fed supply characteristic curve.

BLOCK DIAGRAM

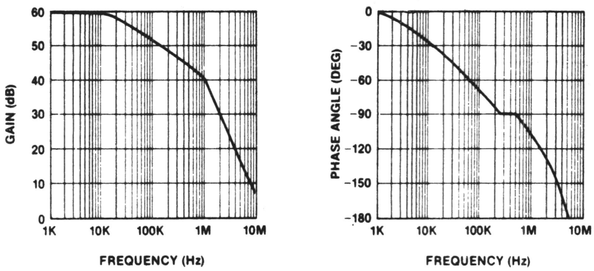

RT, CT
5
REF VOLTAGE
SAWTOOTH GENERATOR
ERROR AMP
+
−
FEED BACK 3
GAIN 4
PWM
0.5V
CURRENT SENSE 6
S
LATCH
R
VCC
7
OUTPUT
STABILIZED SUPPLY
8.2V
2
VZ
1
8
VCC
GND

DC ELECTRICAL CHARACTERISTICS V_{CC} = 12V, T_A = 25°C unless otherwise specified.

SYMBOL AND PARAMETER	TEST CONDITIONS		SE5561			NE5561			UNIT
			Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION									
V_{REF} Internal ref voltage	T_A = 25°C		3.69	3.75	3.84	3.57	3.75	3.96	V
	Over temp.		3.65		3.88	3.55		3.98	V
V_Z, Internal zener ref	*I_L = 7mA		7.8	8.2	8.8	7.8	8.2	8.8	V
Temp coefficient of V_{REF}				± 100			± 100		ppm/°C
Temp. coefficient of V_Z				± 200			± 200		ppm/°C
OSCILLATOR SECTION									
Frequency range	Over temp.		50		100k	50		100k	Hz
Initial accuracy				12			12		%
Duty cycle range	f_o = 20kHz		0		98	0		98	%
CURRENT LIMITING (I_{IN})									
	Pin 6 = 250mV	T_A = 25°C		− 2	− 10		− 2	− 10	μA
		Over temp.			− 20			− 20	μA
Single pulse inhibit delay	Inhibit delay time for 20% overdrive at	I_{OUT} = 20mA		0.88	1.10		0.88	1.10	μs
		I_{OUT} = 40mA		0.7	0.8		0.7	0.8	μs
Current limit trip level			.400	.500	.600	.400	.500	.600	V
ERROR AMPLIFIER									
Open loop gain				60			60		dB
Feedback resistor			10k			10k			Ω
Small signal bandwidth				3			3		MHz
Output voltage swing (V_{OH})			6.2			6.2			V
Output voltage swing (V_{OL})					0.7			0.7	V
OUTPUT STAGE									
Output current	Over temp.		20			20			mA
V_{ce} Sat	I_C = 20mA, Over temp.				0.4			0.4	V
SUPPLY VOLTAGE/CURRENT									
I_{CC}	I_Z = 0, voltage forced	T_A = 25°C			10.0			10.0	mA
		Over temp.			13.0			13.0	mA
V_{CC}	I_{CC} = 10mA, current fed		20.0	21.0	22.0	19.0	21.0	24.0	V
	I_{CC} = 30mA current		20.0		30.0	20.0		30.0	V
LOW SUPPLY PROTECTION									
Pin 1 threshold			8	9	10.5	8	9	10.5	V

TYPICAL PERFORMANCE CHARACTERISTICS

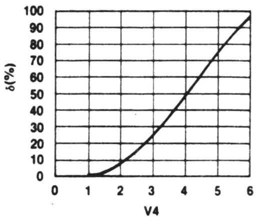
ERROR AMPLIFIER



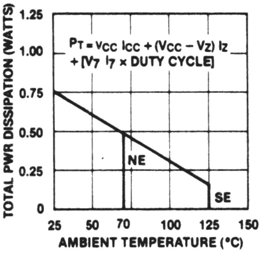
OPEN LOOP GAIN

OPEN LOOP PHASE

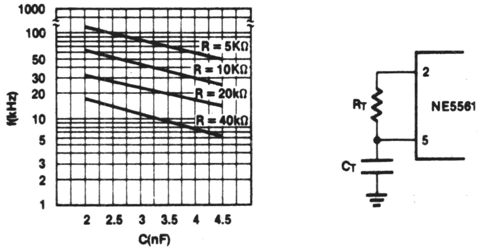
TRANSFER CURVE OF PULSE-WIDTH MODULATOR DUTY CYCLE VS INPUT VOLTAGE



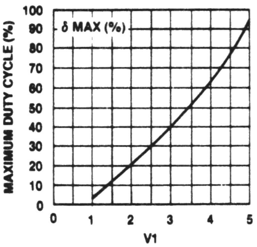
POWER DERATING CURVE



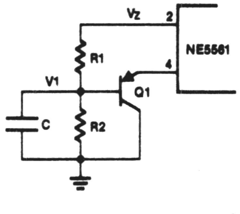
TYPICAL FREQUENCY PLOT VS R_T AND C_T



MAXIMUM DUTY CYCLE VS BASE VOLTAGE ON Q1

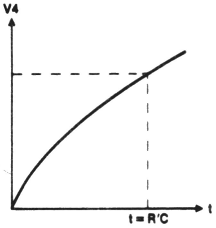


START-UP CIRCUIT



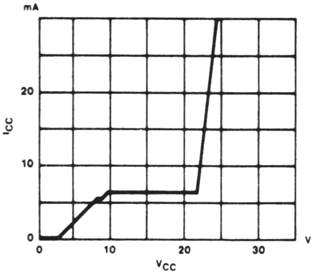
δ max is a function of f $\left[\frac{R2}{R1 + R2} \quad V_Z + V_{BE\,Q1}\right]$

SLOW START VOLTAGE

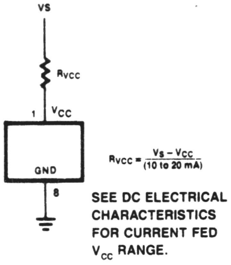


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

NE5561 VOLTAGE/CURRENT FED SUPPLY CHARACTERISTICS



CURRENT FED DROPPING RESISTOR


VS
R_{VCC}
1
V_{CC}
GND
8
$R_{VCC} = \frac{V_S - V_{CC}}{(10 \text{ to } 20 \text{ mA})}$

SEE DC ELECTRICAL CHARACTERISTICS FOR CURRENT FED V_{CC} RANGE.

NE5561 Start-Up

The start-up, or initial turn on, of this device requires some degree of external protective duty cycle limiting to prevent the duty cycle from initially going to the extreme maximum ($\delta > 90\%$). Either over-current limit or slow start circuitry must be employed to limit duty cycle to a safe value during start-up. Both may be used if desired.

To implement slow-start, the start-up circuit can be used. The divider R1 and R2 sets a voltage, buffered by Q1, such that the output of the error amplifier is clamped to a maximum output voltage, thereby limiting the maximum duty cycle. The addition of capacitor C will cause this voltage to ramp up slowly when power is applied, causing the duty cycle to ramp up simultaneously.

Over-current limit may be used also. To limit duty cycle in this mode, the switch current is monitored at pin 6 and the output of the 5561 is disabled on a cycle by cycle basis when current reaches the programmed limit. With current limit control of slow-start, the duty cycle is limited to that value just allowing maximum switch current to flow. (Approximately 0.50V measured at pin 6.)

APPLICATIONS

5V, 0.5A Buck Regulator Operates from 15V

The converter design shows how simple it is to derive a TTL supply from a system supply of 15V (see Figure 1). The NE5561 drives a 2N4920 PNP transistor directly to provide switching current to the inductor.

Overall line regulation is excellent and covers a range of 12V to 18V with minimal change (< 10 mV) in the output operating at full load.

As with all NE5561 circuits, the auxiliary slow start and δ_{max} circuit is required, as evidenced by Q1. The δ_{max} limit may be calculated by using the relationship (Figure 5a, b).

$$\frac{R2}{R1 + R2}(8.2V) = V_{\delta(max)}.$$

The maximum duty cycle is then determined from the pulse-width modulator transfer graph, and R1, R2 are defined from the desired conditions.

SWITCHED-MODE POWER SUPPLY CONTROL CIRCUIT SE/NE5562

Preliminary

DESCRIPTION

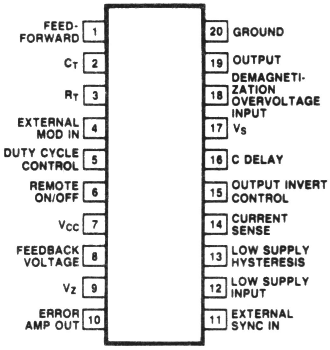
The SE/NE5562 is a single output control circuit for Switched Mode Power Supplies. This single monolithic IC contains all control and protection features needed for full featured Switched Mode Power Supplies.

FEATURES

- Stabilized power supply
- Temperature compensated reference source
- Sawtooth generator
- Pulse width modulator
- Remote on/off switching
- Current limiting (2 levels)
- Low supply voltage, with adjustable hysteresis
- Loop fault protection
- Demagnetization/over voltage protection
- Duty cycle adjust and clamp
- Feed forward control
- External synchronization
- Total shutdown after adjustable number of overcurrent faults

PIN CONFIGURATION

D, F, N PACKAGE


FEED-FORWARD 1
C_T 2
R_T 3
EXTERNAL MOD IN 4
DUTY CYCLE CONTROL 5
REMOTE ON/OFF 6
V_{CC} 7
FEEDBACK VOLTAGE 8
V_Z 9
ERROR AMP OUT 10
20 GROUND
19 OUTPUT
18 DEMAGNETIZATION OVERVOLTAGE INPUT
17 V_S
16 C DELAY
15 OUTPUT INVERT CONTROL
14 CURRENT SENSE
13 LOW SUPPLY HYSTERESIS
12 LOW SUPPLY INPUT
11 EXTERNAL SYNC IN

TOP VIEW

ORDER NUMBERS

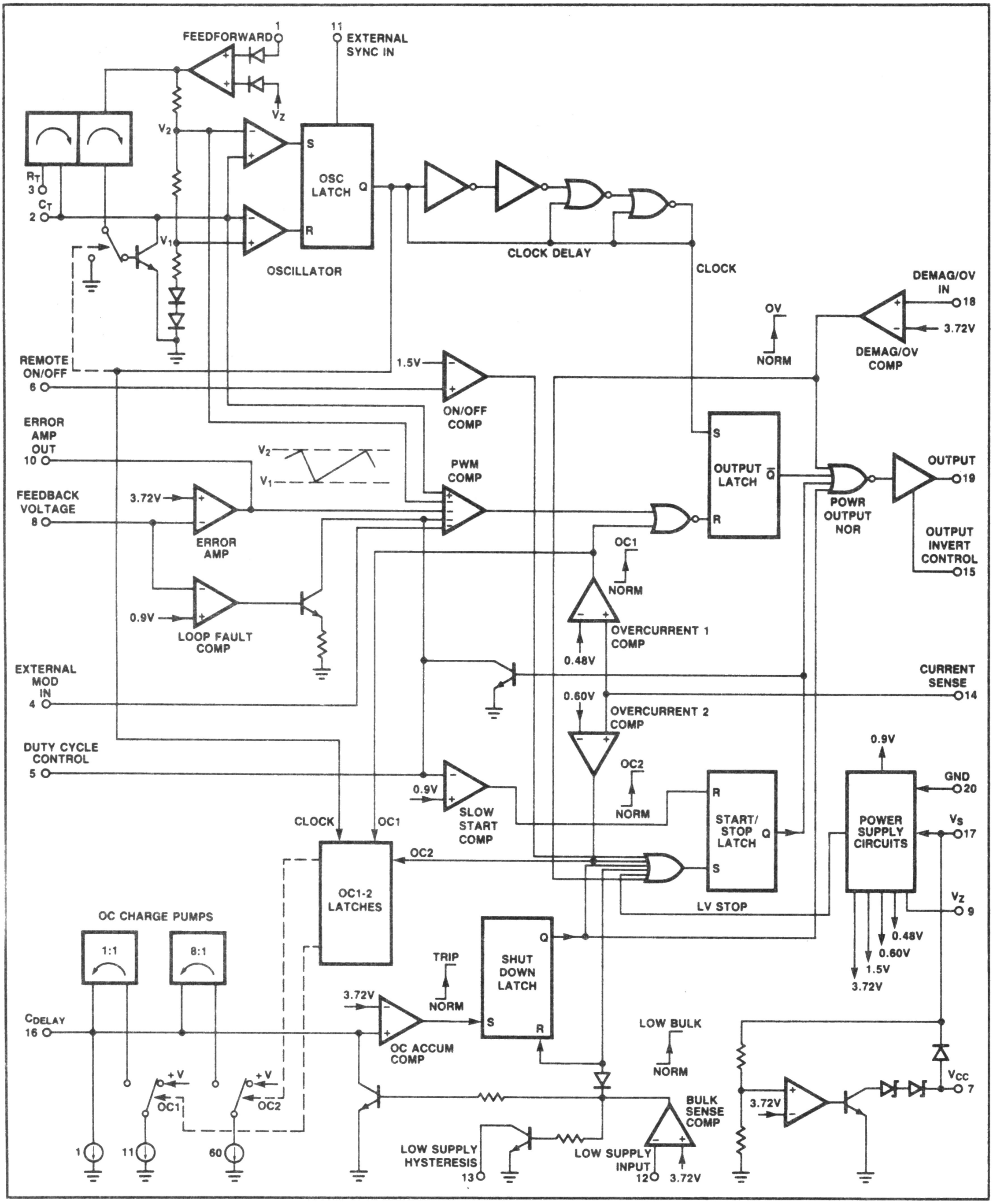
NE5562D, NE5562F, NE5562N
SE5562F, SE5562N

ABSOLUTE MAXIMUM RATINGS

SYMBOL AND PARAMETER	RATING	UNIT
Supply (pin 15)		
Voltage sourced	+15	V
Current sourced	30	mA
Output transistor		
Output current	100	mA
Sync (pin 11) positive		
negative		
Remote on/off (pin 6) positive		
negative		
Feedback pin (pin 8) positive		
negative		
External mod in (pin 4) positive		
negative		
Feedforward (pin 1) positive		
negative		
Error amp out (pin 10) positive		
negative		
Demag/O.V. in (pin 18) positive		
negative		
Current sense (pin 14) positive		
negative		
Low supply sense and hysteresis (Pin 12, 13) positive		
negative		

Preliminary

BLOCK DIAGRAM


FEEDFORWARD
1
11
EXTERNAL SYNC IN
V_Z
R_T
3
C_T
2
V_2
V_1
S
R
OSC LATCH
Q
OSCILLATOR
CLOCK DELAY
CLOCK
DEMAG/OV IN
18
3.72V
DEMAG/OV COMP
OV
NORM
REMOTE ON/OFF
6
1.5V
ON/OFF COMP
ERROR AMP OUT
10
V_2
V_1
PWM COMP
FEEDBACK VOLTAGE
8
3.72V
ERROR AMP
S
OUTPUT LATCH
$\overline{Q}$
R
POWR OUTPUT NOR
OUTPUT
19
OUTPUT INVERT CONTROL
15
OC1
NORM
0.9V
LOOP FAULT COMP
OVERCURRENT 1 COMP
0.48V
EXTERNAL MOD IN
4
CURRENT SENSE
14
0.60V
OVERCURRENT 2 COMP
OC2
NORM
DUTY CYCLE CONTROL
5
0.9V
SLOW START COMP
R
START/ STOP LATCH
Q
S
0.9V
GND
20
POWER SUPPLY CIRCUITS
Vs
17
V_Z
9
CLOCK
OC1
OC2
OC1-2 LATCHES
LV STOP
0.48V
0.60V
1.5V
3.72V
OC CHARGE PUMPS
1:1
8:1
TRIP
NORM
SHUT DOWN LATCH
Q
S
R
3.72V
CDELAY
16
OC ACCUM COMP
LOW BULK
NORM
+V
OC1
+V
OC2
BULK SENSE COMP
3.72V
V_{CC}
7
1
11
60
LOW SUPPLY HYSTERESIS
13
LOW SUPPLY INPUT
12
3.72V

SWITCHED-MODE POWER SUPPLY CONTROL CIRCUIT SE/NE5562

Preliminary

DC ELECTRICAL CHARACTERISTICS: V_{CC} = 12V unless otherwise specified

SYMBOL AND PARAMETER	TEST CONDITIONS	SE5562			NE5562			UNIT
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Reference Voltage V_R	25°C ± 50 ppm/°C (±1%) Over Temp	3.68	3.72	3.76		3.72		V
Zener Voltage V_Z	IL = 7mA	7.22	7.60	7.98		7.60		V
OSCILLATOR SECTION								
Frequency Range				300			300	kHz
MODULATOR SECTION								
Modulator Input Current	Over Temp V_{IN} = 1V		2	20		2	20	μA
HOUSEKEEPING FUNCTIONS								
Deltamax Input Current	Over Temp V_{IN} = 1V		2	20		2	20	μA
Accuracy of Duty Cycle Control	f = 15kHz to 150kHz V_{IN} = 55% of V_Z		50			50		% of Duty Cycle
Low Supply Voltage Shutdown	V_S for Restart Condition	V_Z+.2	V_Z+.7	V_Z+1.5	V_Z+.2	V_Z+.7	V_Z+1.7	V
Loop Fault Protection Threshold		.72	.9	.98	.72	.9	.98	V
Demag/Over Voltage Threshold Voltage		3.60	3.72	3.84	3.60	3.72	3.84	V
Over Voltage Input Bias Current			1	10		1	10	μA
FEED FORWARD FUNCTION								
Duty Cycle Reduction at 50% Duty Cycle	Feedforward Voltage V_{FF} V_{FF} = 2V_Z		12.785			12.8		% of Duty Cycle
Feedforward Bias Current	Feedforward Voltage V_{FF} V_{FF} = 2V_Z		.2	5		.2	5	μA
EXTERNAL SYNC								
"ON" Input voltage		.2		.8	.2		.8	V
"OFF" Input Voltage		2		V_Z	2		V_Z	V
Input Low Current	V_{IN} = 0V		1	10		1	10	μA
ERROR AMPLIFIER SECTION								
Amplifier Open Loop Gain	$R_L \geq$ 100K	60	80		60	80		dB
Amplifier Bias Current			.5	5		5	5	μA
Amplifier Output Current		−1		+1	−1		+1	μA
Amplifier Output Swing		1		V_Z−1	1		V_Z−1	V
REMOTE ON/OFF								
"OFF" Input Voltage		0		.8	0		.8	V
"ON" Input Voltage		2		V_Z	2		V_Z	V
Input Low Current	V_{IN} = 0V		1	10		1	10	μA
LOW SUPPLY SHUTDOWN								
Comparator Input Bias Current	V_{IN} = 0V		2	10		2	10	μA
Comparator Threshold Voltage		3.50	3.72	3.90		3.72		V
V_{CE} Sat. of Hysteresis Transistor	I_{OUT} = 1.0mA V_{IN} = 3.0V		.3	.6		.3		V
C_{DELAY} Discharge Current	V_C = 1.0V V_{IN} = 3.0V	1	10		1	10		mA

SWITCHED-MODE POWER SUPPLY CONTROL CIRCUIT SE/NE5562

Preliminary

DC ELECTRICAL CHARACTERISTICS: V_{CC} = 12V unless otherwise specified (cont)

SYMBOL AND PARAMETER	TEST CONDITIONS	SE5562			NE5562			UNIT
		Min	Typ	Max	Min	Typ	Max	
CURRENT SENSE								
OC1 Threshold Voltage		.456	.480	.504		.480		V
OC1 C_{DELAY} Charge Current	V_{ISENS} = .510V		10			10		μA
OC2 Threshold Voltage		.570	.600	.630	.560	.600	.640	V
OC2 C_{DELAY} Charge Current	V_{ISENS} = .640V		490			490		μA
C_{DELAY} Discharge Current	V_{ISENS} = 0V	.5	1	1.5	.4	1	1.6	μA
OUTPUT STAGE								
$V_S - V_{OH}$	$11 \leq V_S \leq 15V$ I_O = 100mA						2	V
V_{OL}	$11 \leq V_S \leq 15V$ I_O = 100mA			1.5			1.5	V
V_{OL}	$11 \leq V_S \leq 15V$ I_O = 2mA			4			.4	V
SUPPLY VOLTAGE/CURRENT								
I_{CC}	I_Z = O, V_S = 15V		7.5			7.5		mA
CURRENT FEED SHUNT REGULATOR								
V_S	I_{IN} = 10mA	14.25			14			V
V_S	I_{IN} = 20mA			16			16	V

SWITCHED-MODE POWER SUPPLY CONTROLLER NE5568

DESCRIPTION

The NE5568 is a control circuit for use in switched mode power supplies. It contains an internal temperature-compensated supply, PWM, sawtooth oscillator, over-current sense latch, and output stage. The device is intended for low-cost SMPS applications where extensive housekeeping functions are not required. The NE5568 is a selected version of the NE5561.

FEATURES

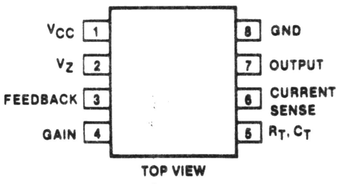
- **Micro-miniature (D) package**
- **Pulse width modulator**
- **Current limiting (cycle by cycle)**
- **Sawtooth generator**
- **Stabilized power supply**
- **Double pulse protection**
- **Internal temperature-compensated reference**

APPLICATIONS

- **Switch mode power supplies**
- **DC motor controller inverter**
- **DC/DC converter**

PIN CONFIGURATION

D, FE, N PACKAGES



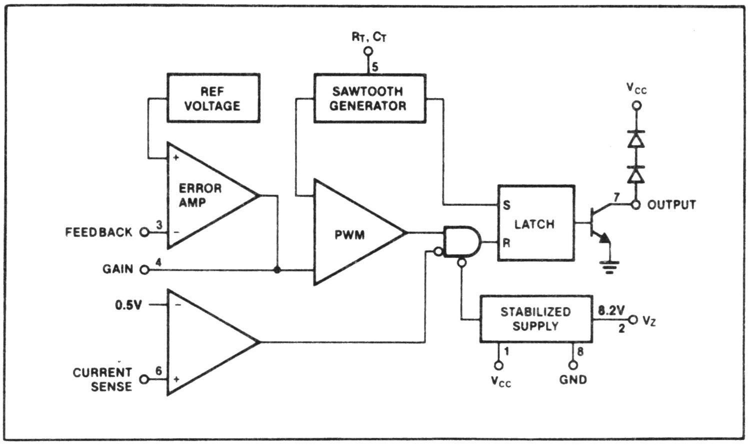
V_{CC} 1
V_Z 2
FEEDBACK 3
GAIN 4
8 GND
7 OUTPUT
6 CURRENT SENSE
5 R_T, C_T
TOP VIEW

ORDER NUMBERS
NE5568D, NE5568FE, NE5568N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage, V_{CC}	18	V
Output current	40	mA
Output duty cycle	98	%
Max total power dissipation	0.75	W
Operating temperature range	0 to 70	°C

BLOCK DIAGRAM



R_T, C_T
5
REF VOLTAGE
SAWTOOTH GENERATOR
V_{CC}
ERROR AMP
+
-
FEEDBACK 3
GAIN 4
PWM
S
LATCH
R
7
OUTPUT
0.5V
CURRENT SENSE 6
STABILIZED SUPPLY
8.2V
2
V_Z
1
8
V_{CC}
GND

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 12V$, $T_A = 25°C$ unless otherwise specified.

SYMBOL AND PARAMETER	TEST CONDITIONS		NE5568 Min	NE5568 Typ	NE5568 Max	UNIT
Reference Section V_{REF}, Internal ref voltage	$T_A = 25°C$		3.69	3.75	3.84	V
	Over temperature		3.66		3.87	V
V_Z, Internal zener ref	$I_L = 7mA$		7.8	8.2	8.8	V
Temperature coefficient of V_{REF}				± 100		ppm/°C
Temperature coefficient of V_Z				± 200		ppm/°C
Oscillator Section Frequency range	Over temperature		50		100k	Hz
Initial accuracy				12		%
Duty cycle range	$f_O = 20kHz$		0		98	%
Current Limiting (I_{IN})	Pin 6 = 250mV	$T_A = 25°C$		− 2	− 10	μA
		Over temp.			− 20	μA
Single pulse inhibit delay	Inhibit delay time for 20% overdrive at	$I_{OUT} = 20mA$		0.88	1.10	μs
		$I_{OUT} = 40mA$		0.7	0.8	μs
Current limit trip level			0.400	0.500	0.600	V
Error Amplifier Open loop gain				60		dB
Feedback resistor			10k			Ω
Small signal bandwidth				3		MHz
V_{OH}, Output voltage swing			6.2			V
V_{OL}, Output voltage swing					0.7	V
Output Stage Output current	Over temperature		20			mA
V_{CE}, Saturation	$I_C = 20mA$, over temperature				0.4	V
	$I_C = 40mA$, over temperature				0.5	V
Supply Voltage/Current I_{CC}	$I_Z = 0$, voltage fed	$T_A = 25°C$			10.0	mA
		Over temp.			13.0	mA
V_{CC}	$I_S = 10mA$, current fed		19.0	21.0	24.0	V
	$I_{CC} = 30mA$, current fed		20.0		30.0	V
Low Supply Protection Pin 1 threshold			8.0	9.0	10.5	V

NOTE
All curves and applications of NE5561 apply exactly.

SWITCHED-MODE POWER SUPPLY CONTROL CIRCUITS SG1526A/2526A/3526A

Preliminary

DESCRIPTION

SPECIFICALLY DESIGNED for use in fixed-frequency switching regulators and other power control applications, these Switched-Mode Power Supply Control Circuits can be used to implement single-ended or push-pull switching regulators of either polarity, both transformerless and transformer coupled.

Included in these monolithic integrated circuits are a temperature-compensated voltage reference, sawtooth oscillator, error amplifier, pulse-width modulator, pulse metering and steering logic, and two 200 mA source/sink power drivers. Also included are housekeeping functions such as soft-start and low supply voltage lockout, digital current limiting, double-pulse inhibit, a data latch for single-pulse metering, adjustable deadtime, and provision for symmetry correction inputs.

For ease of interface, all digital inputs are TTL and CMOS compatible. Active LOW logic allows wired-OR connections for maximum flexibility.

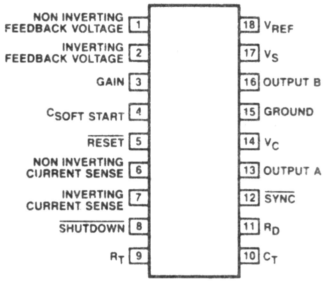
The SG1526A is supplied in an 18-pin glass/ceramic (cer-DIP) hermetic package and is characterized for operation over the full temperature range of −55°C to +125°C, allowing its use in military and aerospace applications. The SG2526A is rated for operation over the extended range of −40°C to +85°C recommending it for many industrial applications. The low-cost SG3526A is rated for continuous operation over the commercial temperature range of 0°C to +70°C. The extended and commercial versions are furnished in either the cer-DIP package or a dual in-line plastic package with copper alloy lead frame for improved heat dissipation.

FEATURES

- **8 to 35 V Operation**
- **Dual 100 mA Source/Sink Outputs**
- **Stabilized Power Supply**
- **Current Limiting**
- **Temperature Compensated Reference Source**
- **Sawtooth Generator**
- **Low Supply Voltage Protection**
- **External Synchronization**
- **Double-Pulse Suppression**
- **Programmable Deadtime**
- **Programmable Soft Start**
- **18-Pin Dual In-Line Plastic Package Or 18-Pin Cer-DIP Hermetic Package**

PIN CONFIGURATION

F,N PACKAGES



TOP VIEW

ORDER NUMBERS
SG1526A F,N
SG2526A F,N
SG3526A F,N

ABSOLUTE MAXIMUM RATINGS

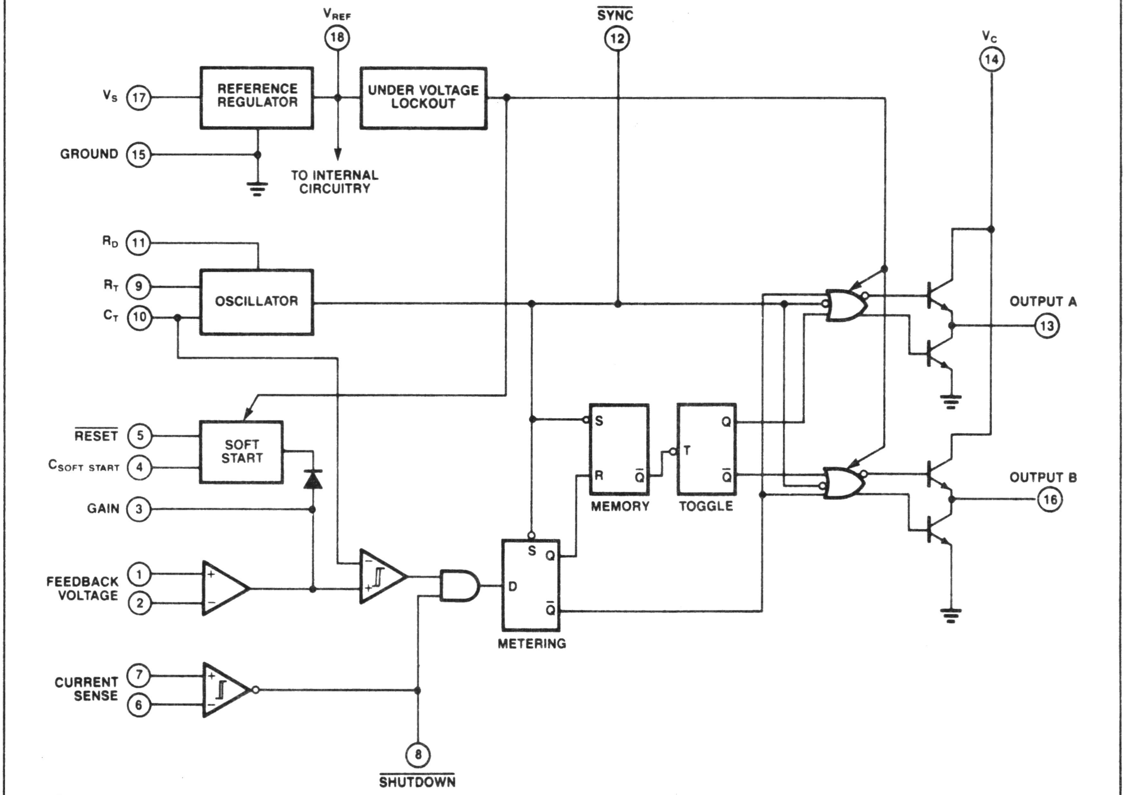
PARAMETER	RATING	UNIT
Supply Voltage, V_S	40	V
Collector Supply Voltage, V_C	40	V
Logic Input Voltage Range, V_{IN}	−0.3 to +5.5	V
Analog Input Voltage Range, V_{IN}	−0.3 V to V_S	V
Output Current, I_O	±200	mA
Reference Load Current, I_{REF}	50	mA
Logic Sink Current, I_{IN}	15	mA
Package Power Dissipation, P_D (Plastic DIP) (Cer-DIP)	2.3 1.9	W[*1] W[*1]
Storage Temperature Range, T_S	−65 to +150	°C

NOTE:
[*1] Derate linearly to 0 watts at T_A = +150°C.

SWITCHED-MODE POWER SUPPLY CONTROL CIRCUITS SG1526A/2526A/3526A

Preliminary

BLOCK DIAGRAM


VREF
18
SYNC
12
VC
14
VS 17
REFERENCE REGULATOR
UNDER VOLTAGE LOCKOUT
GROUND 15
TO INTERNAL CIRCUITRY
RD 11
RT 9
CT 10
OSCILLATOR
OUTPUT A
13
RESET 5
CSOFT START 4
SOFT START
GAIN 3
S Q
MEMORY
R Q̄
T
Q
Q̄
TOGGLE
OUTPUT B
16
FEEDBACK VOLTAGE 1 2
S Q
D
Q̄
METERING
CURRENT SENSE 7 6
8
SHUTDOWN

Preliminary

ELECTRICAL CHARACTERISTICS over operating temperature range, V_S 15 V (unless otherwise noted).

CHARACTERISTIC	TEST PINS	TEST CONDITIONS	LIMITS SG1526A & SG2526A Min.	Type.	Max.	SG3526A Min.	Typ.	Max.	UNITS
REFERENCE SECTION (L_L =0 mA)									
Reference Voltage	18	T_A = +25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
		Over Recommended Conditions	4.90	5.00	5.10	4.85	5.00	5.15	V
Ref. Volt. Regulation	18	V_S =8 to 35 V	—	10	20	—	10	30	mV
		I_L = 0 to 20 mA	—	10	30	—	10	50	mV
		Over Oper. Temp. Range	—	15	50	—	15	50	mV
Short Circuit Current	18	V_{REF} = 0 V	25	50	100	25	50	100	mA
Standby Current	17	V_S=35 V, R_T=4.22 kΩ, V_S=0.4 V	—	18	—	—	18	—	mA
OSCILLATOR SECTION (f = 40 kHz, R_T = 4.22 kΩ, C_T = 0.01 μF, R_D = 0 Ω)									
Oscillator Frequency	9, 10	R_T =150Ω, C_T = 20 μF	—	—	1.0		—	1.0	Hz
		R_T = 2kΩ, C_T = 0.001 μF	400	—	—	400	—	—	kHz
Initial Osc. Accuracy	9, 10	T_A = +25° C	—	3.0	—	—	3.0	—	%
Osc. Stability	9, 10	V_S = 8 to 35 V	—	0.5	—	—	0.5	—	%
		Over oper. Temp. Range	—	1.0	—	—	1.0	—	%
		Other Recommended Conditions	—	2.0	—	—	2.0	—	%
Sawtooth Peak Voltage	12	V_S = 35 V	—	3.0	3.5	—	3.0	3.5	V
Sawtooth Valley Volt.	12	V_S = 8.0 V	0.5	1.0	—	0.5	1.0	—	V
Sync. Pulse Width	12	C_L = 15 pF	—	500	—	—	500	—	ns
ERROR AMPLIFIER (V_{CM} = 0 to 5.2 V)									
Input Offset Voltage	1, 2	R_S = 2 kΩ	—	2.0	5.0	—	2.0	5.0	mV
Input Bias Current	1, 2		—	−350	−1000	—	−350	−2000	nA
Input Offset Current	1, 2		—	35	100	—	35	200	nA
Error Amp Gain	1–3	Open Loop, R_L = 10 MΩ	64	72	—	60	72	—	dB
Small Signal BW	1–3	C_L = 30 pF	0.7	1.0	—	0.7	1.0	—	MHz
Output Voltage Swing	3	Positive Limit, R_L = 50 kΩ	3.6	4.2	—	3.6	4.2	—	V
		Negative Limit, R_T = 50 kΩ	—	0.2	0.4	—	0.2	0.4	V
Common Mode Range	1, 2	V_S = 8.0 V	0	—	5.2	0	—	5.2	V
Common Mode Rejection	1, 2	R_S = 10 kΩ	70	94	—	70	94	—	dB
Error Amp. V_S Rej.	3	f = 120 Hz, ΔV_S = 1 Vrms	66	80	—	66	80	—	dB
HOUSEKEEPING FUNCTIONS									
Logic Voltage Levels	5, 8, 12	Logic HIGH, I_{SOURCE} = −40 μA	2.4	4.0	—	2.4	4.0	—	V
		Logic LOW, I_{SINK} = 3.6 mA	—	0.2	0.4	—	0.2	0.4	V
Input Current	5, 8, 12	V_{IN} =2.4 V	—	−125	−200	—	−125	−200	μA
		V_{IN} = 0.4 V	—	−225	−360	—	−225	−360	μA
Shutdown Delay	8–13, 16	100mV step, 5mV overdrive, R_S=50Ω	—	300	—	—	300	—	ns
CURRENT LIMITING									
Common Mode Range	6, 7	V_S = 18 V	0	—	15	0	—	15	V
Sense Voltage	6, 7	V_{CM} = 0 to 15 V	—	100	—	—	100	—	mV
Input Current	6, 7	V_{CM} = 0 to 15 V	—	−3.0	—	—	−3.0	—	μA
Voltage Gain	7–8	I_S = 360 μA	—	68	—	—	68	—	dB

Preliminary

ELECTRICAL CHARACTERISTICS over operating temperature range, V_S 15 V (unless otherwise noted). (Cont'd)

CHARACTERISTIC	TEST PINS	TEST CONDITIONS	LIMITS						UNITS
			SG1526A & SG2526A			SG3526A			
			Min.	Type.	Max.	Min.	Typ.	Max.	
SOFT START SECTION									
Error Clamp Voltage	—	$V_5 = 0.4$ V	—	100	400	—	100	400	mV
C_S Charging Current	4	$V_5 = 2.4$ V	—	100	—	—	100	—	µA
OUTPUT DRIVERS ($V_C = 15$ V)									
Output Voltage	12, 16	$I_{OUT} = -20$ mA	12.5	13.5	—	12.5	13.5	—	V
		$I_{OUT} = -100$ mA	—	13	—	—	13	—	V
		$I_{OUT} = 20$ mA	—	0.2	0.3	—	0.2	0.3	V
		$I_{OUT} = 100$ mA	—	1.2	—	—	1.2	—	V
Leakage Current	12, 16	$V_C = 40$ V	—	0.1	100	—	0.1	100	µA
Rise Time	12, 16	$C_L = 1000$ pF	—	300	—	—	300	—	ns
Fall Time	12, 16	$C_L = 1000$ pF	—	200	—	—	200	—	ns

NOTES:
Negative current is defined as coming out of (sourcing) the specified device pin.
*Commercial, extended, and full temperature range devices are defined on page 2.

RECOMMENDED OPERATING CONDITIONS

Logic Supply Voltage, V_S .... 8 V to 35 V
Collector Voltage, V_C .... 4.5 V to 35 V
Output Load Current, I_O .... 0 to ±100 mA
Reference Load Current, I_L .... 0 to 20 mA
Oscillator Frequency, f .... 1 Hz to 400 kHz
Oscillator Timing Resistance, R_T .... 2 kΩ to 150 kΩ
Oscillator Timing Capacitance, C_T .... 0.001 µF to 20 µF
Programmed Deadtime .... 3% to 50%

SMPS CONTROL CIRCUIT

SG3524

DESCRIPTION

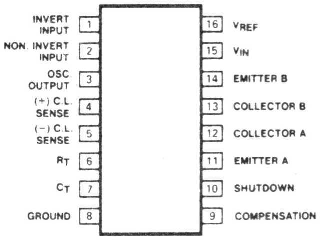
This monolithic integrated circuit contains all the control circuitry for a regulating power supply inverter or switching regulator. Included in a 16-pin dual-in-line package is the voltage reference, error-amplifier, oscillator, pulse width modulator, pulse steering flip-flop, dual alternating output switches and current limiting and shut-down circuitry. This device can be used for switching regulators of either polarity, transformer coupled DC to DC converters, transformerless voltage doublers and polarity converters, as well as other power control applications. The SG3524 is designed for commercial applications of 0°C to +70°C.

FEATURES

- **Complete PWM power control circuitry**
- **Single ended or push-pull outputs**
- **Line and load regulation of 0.2%**
- **1% maximum temperature variation**
- **Total supply current is less than 10mA**
- **Operation beyond 100kHz**

PIN CONFIGURATION

D,F,N PACKAGE

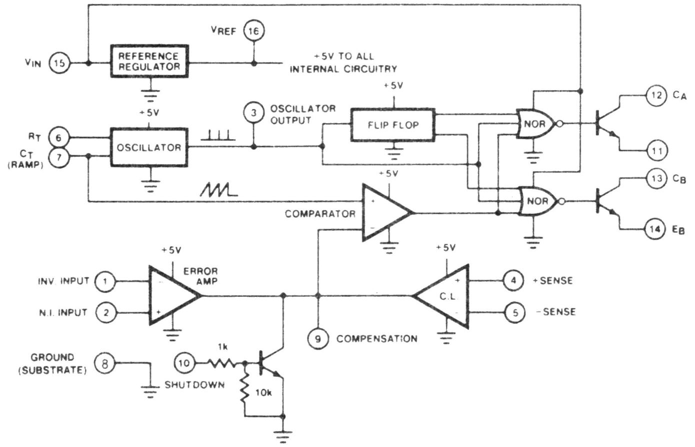

INVERT INPUT 1
NON. INVERT INPUT 2
OSC OUTPUT 3
(+) C.L. SENSE 4
(−) C.L. SENSE 5
RT 6
CT 7
GROUND 8
16 VREF
15 VIN
14 EMITTER B
13 COLLECTOR B
12 COLLECTOR A
11 EMITTER A
10 SHUTDOWN
9 COMPENSATION

ORDER PART NUMBERS:
SG3524F, SG3524D,
SG3524N

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Input voltage	40	V
Output current (each output)	100	mA
Reference output current	50	mA
Oscillator charging current	5	mA
Power dissipation		
Package limitation	1000	mW
Derate above 25°C	8	mW/°C
Operating temperature range	0 to +70	°C
Storage temperature range	−65 to +150	°C

BLOCK DIAGRAM


VREF 16
VIN 15
REFERENCE REGULATOR
+5V TO ALL INTERNAL CIRCUITRY
+5V
3 OSCILLATOR OUTPUT
FLIP FLOP
RT 6
CT 7 (RAMP)
OSCILLATOR
NOR
NOR
12 CA
11
13 CB
14 EB
COMPARATOR
ERROR AMP
INV. INPUT 1
N.I. INPUT 2
C.L.
4 +SENSE
5 −SENSE
9 COMPENSATION
GROUND (SUBSTRATE) 8
10 SHUTDOWN
1k
10k

SMPS CONTROL CIRCUIT SG3524

DC ELECTRICAL CHARACTERISTICS (T_A = 0°C to + 70°C, V_{ON} = 20V, and f = 20kHz unless otherwise specified.)

PARAMETER	TEST CONDITIONS	SG3524			UNIT
		Min	Typ	Max	
Reference Section Output voltage		4.6	5.0	5.4	V
Line regulation	V_{IN} = 8 to 40V		10	30	mV
Load regulation	I_L = 0 to 20mA		20	50	mV
Ripple rejection	f = 120Hz, T_A = 25°C		66		dB
Short circuit current limit	V_{REF} = 0, T_A = 25°C		100		mA
Temperature stability	Over operating temperature range		0.3	1	%
Long term stability	T_A = 25°C		20		mV/kHr
Oscillator Section Maximum frequency	C_T = .001 mfd, R_T = 2kΩ		300		kHz
Initial accuracy	R_T and C_T constant		5		%
Voltage stability	V_{IN} = 8 to 40V, T_A = 25°C			1	%
Temperature stability	Over operating temperature range			2	%
Output amplitude	Pin 3, T_A = 25°C		3.5		V_P
Output pulse width	C_T = .01 mfd, T_A = 25°C		0.5		μs
Error Amplifier Section Input offset voltage	V_{CM} = 2.5V		2	10	mV
Input bias current	V_{CM} = 2.5V		2	10	μA
Open loop voltage gain		68	80		dB
Common mode voltage	T_A = 25°C	1.8		3.4	V
Common mode rejection ratio	T_A = 25°C		70		dB
Small signal bandwidth	A_V = 0dB, T_A = 25°C		3		MHz
Output voltage	T_A = 25°C	0.5		3.8	V
Comparator Section Duty cycle	% each output "ON"	0		45	%
Input threshold	Zero duty cycle		1		V
Input threshold	Maximum duty cycle		3.5		V
Input bias current			1		μA
Current Limiting Section Sense voltage	Pin 9 = 2V with error amplifier set for maximum out, T_A = 25°C	180	200	220	mV
Sense voltage T.C.			0.2		mV/°C
Common mode voltage		−1		+1	V
Output Section (each output) Collector-emitter voltage (breakdown)		40			V
Collector-leakage current	V_{CE} = 40V		0.1	50	μA
Saturation voltage	I_C = 50mA		1	2	V
Emitter output voltage	V_{IN} = 20V	17	18		V
Rise time	R_C = 2kΩ, T_A = 25°C		0.2		μs
Fall time	R_C = 2kΩ, T_A = 25°C		0.1		μs
Total standby current (excluding oscillator charging current, error and current limit dividers, and with outputs open)	V_{IN} = 40V		8	10	mA

THEORY OF OPERATION

Voltage Reference

An internal series regulator provides a nominal 5 volt output which is used both to generate a reference voltage and is the regulated source for all the internal timing and controlling circuitry. This regulator may be bypassed for operation from a fixed 5 volt supply by connecting pins 15 and 16 together to the input voltage. In this configuration, the maximum input voltage is 6.0 volts.

This reference regulator may be used as a 5 volt source for other circuitry. It will provide up to 50mA of current itself and can easily be expanded to higher currents with an external PNP as shown in Figure 1.

EXPANDED REFERENCE CURRENT CAPABILITY

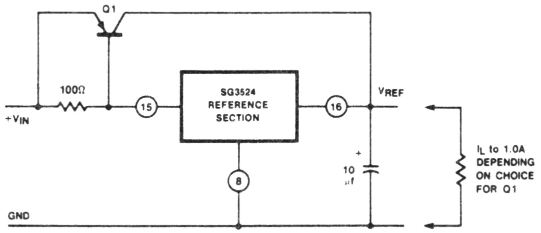
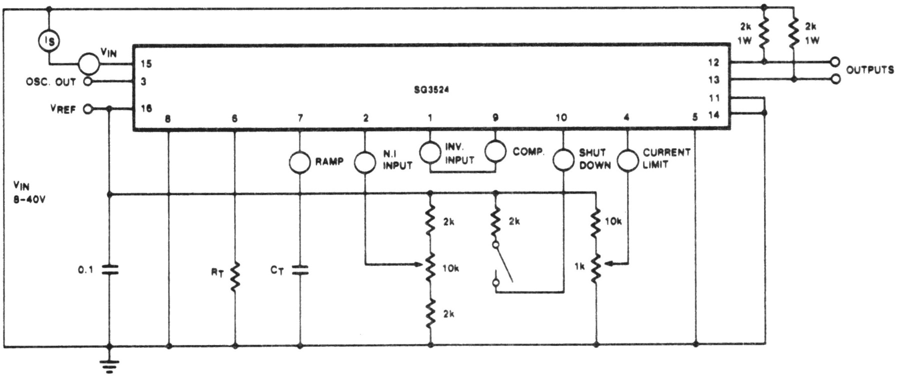

Q1
100Ω
+VIN
15
SG3524
REFERENCE
SECTION
16
VREF
+
10
μf
8
GND
I_L to 1.0A
DEPENDING
ON CHOICE
FOR Q1

Figure 1

TEST CIRCUIT


IS
VIN
OSC. OUT
VREF
15
3
16
SG3524
8
6
7
2
1
9
10
4
5
12
13
11
14
2k
1W
2k
1W
OUTPUTS
RAMP
N.I
INPUT
INV.
INPUT
COMP.
SHUT
DOWN
CURRENT
LIMIT
VIN
8-40V
0.1
RT
CT
2k
10k
2k
2k
10k
1k

SMPS CONTROL CIRCUIT SG3524

OUTPUT STAGE DEAD TIME AS A FUNCTION OF THE TIMING CAPACITOR VALUE

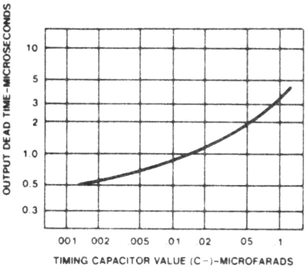


Figure 2

OSCILLATOR PERIOD AS A FUNCTION OF R_T AND C_T

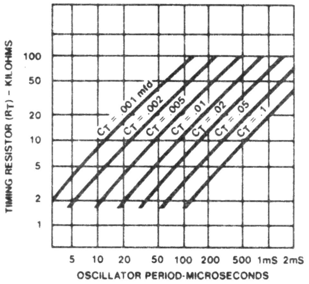


Figure 3

AMPLIFIES OPEN-LOOP GAIN AS A FUNCTION OF FREQUENCY AND LOADING ON PIN 9

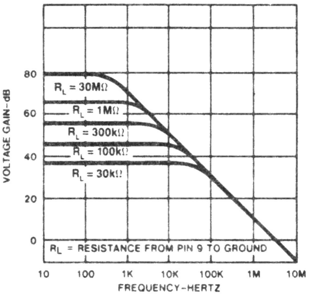


Figure 4

Oscillator

The oscillator in the SG3524 uses an external resistor (R_T) to establish a constant charging current into an external capacitor (C_T). While this uses more current than a series connected RC, it provides a linear ramp voltage on the capacitor which is also used as a reference for the comparator. The

charging current is equal to 3.6V ÷ R_T and should be kept within the range of approximately 30μA to 2mA, i.e., $1.8K < R_T < 100K$.

The range of values for C_T also has limits as the discharge time of C_T determines the pulse width of the oscillator output pulse. This pulse is used (among other things) as a blanking pulse to both outputs to insure that there is no possibility of having both outputs on simultaneously during transitions. This output dead time relationship is shown in Figure 2. A pulse width below approximately 0.5 microseconds may allow false triggering of one output by removing the blanking pulse prior to the flip-flops reaching a stable state. If small values of C_T must be used, the pulse width may still be expanded by adding a shunt capacitance (≈100pF) to ground at the oscillator output. (Note: Although the oscillator output is a convenient oscilloscope sync input, the cable and input capacitance may increase the blanking pulse width slightly.) Obviously, the upper limit to the pulse width is determined by the maximum duty cycle acceptable. Practical values of C_T fall between .001 and 0.1 microfarad.

The oscillator period is approximately $t = R_TC_T$ where t is in microseconds when R_T = ohms and C_T = microfarads. The use of Figure 3 will allow selection of R_T and C_T for a wide range of operating frequencies. Note that for series regulator applications, the two outputs can be connected in parallel for an effective 0-90% duty cycle and the frequency of the oscillator is the frequency of the output. For push-pull applications, the outputs are separated and the flip-flop divides the frequency such that each outputs duty cycle is 0-45% and the overall frequency is one-half that of the oscillator.

External Synchronization

If it is desired to synchronize the SG3524 to an external clock, a pulse of ≈+3 volts may be applied to the oscillator output terminal with R_TC_T set slightly greater than the clock period. The same considerations of pulse width apply. The impedance to ground at this point is approximately 2K ohms.

If two or more SG3524s must be synchronized together, one must be designated as master with its R_TC_T set for the correct period. The slaves should each have an R_TC_T set for approximately 10% longer period than the master with the added requirement that C_T (slave) = one-half C_T (master). Then connecting Pin 3 on all units together will insure that the master output pulse—which occurs first and has a wider pulse width—will reset the slave units.

Error Amplifier

This circuit is a simple differential-input, transconductance amplifier. The output is the compensation terminal, pin 9, which is a high impedance node ($R_L \approx 5M\Omega$). The gain is

$$A_V = gmR_L = \frac{8\ I_C\ R_L}{2kT} \approx .002\ R_L$$

and can easily be reduced from a nominal of 10,000 by an external shunt resistance from pin 9 to ground, as shown in Figure 4.

In addition to DC gain control, the compensation terminal is also the place for AC phase compensation. The frequency response curves of Figure 4 show the uncompensated amplifier with a single pole at approximately 200Hz and a unity gain cross-over at 5MHz.

Typically, most output filter designs will introduce one or more additional poles at a significantly lower frequency. Therefore, the best stabilizing network is a series R-C combination between pin 9 and ground which introduces a zero to cancel one of the output filter poles. A good starting point is 50kΩ plus .001 microfarad.

One final point on the compensation terminal is that this is also a convenient place to insert any programming signal which is to override the error amplifier. Internal shutdown and current limit circuits are connected here, but any other circuit which can sink 200μA can pull this point to ground thus shutting off both outputs.

While feedback is normally applied around the entire regulator, the error amplifier can be used with conventional operational amplifier feedback and is stable in either the inverting or non-inverting mode. Regardless of the connections, however, input common-mode limits must be observed or output signal inversions may result. For conventional regulator applications, the 5 volt reference voltage must be divided down as shown in Figure 5. The error amplifier may also be used in fixed duty cycle applications by using the unity gain configuration shown in the open loop test circuit.

Current Limiting

The current limiting circuitry of the SG3524 is shown in Figure 6.

By matching the base-emitter voltages of Q1 and Q2, and assuming negligible voltage drop across R_1:

$$\text{Threshold} = V_{BE}(Q1) + I_1 R_2 - V_{BE}(Q2)$$
$$= I_1 R_2 \approx 200\text{mV}$$

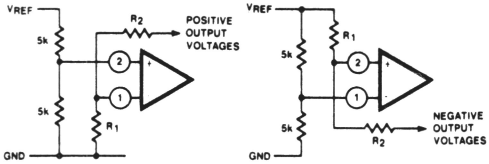
Although this circuit provides a relatively small threshold with a negligible temperature coefficient, there are some limitations to its use, the most important of which is the ±1 volt common mode range which requires sensing in the ground line. Another factor to consider is that the frequency compensation provided by R_1C_1 and Q1 provides a roll-off pole at approximately 300Hz.

Since the gain of this circuit is relatively low, there is a transition region as the current limit amplifier takes over pulse width control from the error amplifier. For testing purposes, threshold is defined as the input voltage to get 25% duty cycle with the error amplifier signaling maximum duty cycle.

In addition to constant current limiting, pins 4 and 5 may also be used in transformer-coupled circuits to sense primary current and shorten an output pulse, should transformer saturation occur. (Refer to Figure 11.) Another application is to ground pin 5 and use pin 4 as an additional shutdown terminal: i.e., the output will be off with pin 4 open and on when it is grounded. Finally, foldback current limiting can be provided with the network of Figure 7. This circuit can reduce the short-circuit current (I_{SC}) to approximately one-third the maximum available output current (I_{MAX}).

***For additional information, consult the Applications Section.**

ERROR AMPLIFIER BIASING CIRCUITS



$V_O = \frac{2.5V\,(R + R_2)}{R_1}$

$\frac{R_1 R_2}{R_2 + R_2} = 2.5k\Omega$

Note change in input connections for opposite polarity outputs.

Figure 5

CURRENT LIMITING CIRCUITRY OF THE SG3524

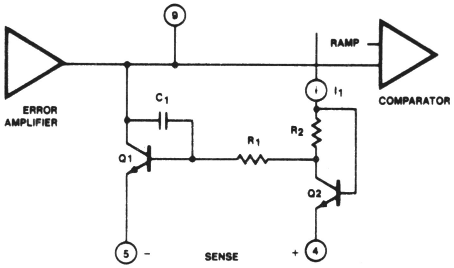
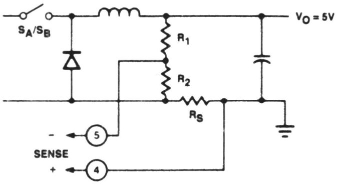


Figure 6

FOLDBACK CURRENT LIMITING



$I_{MAX} = \frac{1}{R_S} \quad V_{TH} + \frac{V_O R_2}{R_1 + R_2}$

$I_{SC} = \frac{V_{TH}}{R_S}$ WHERE

$V_{TH} = 200$ mV

Foldback current limiting can be used to reduce power dissipation under shorted output conditions.

Figure 7

PRECISION VOLTAGE REGULATOR

μA723/723C/SA723C

DESCRIPTION

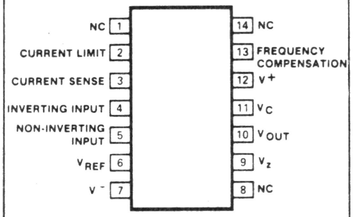
The μA723/SA723C is a Monolithic Precision Voltage Regulator capable of operation in positive or negative supplies as a series, shunt, switching or floating regulator. The 723 contains a temperature compensated reference amplifier, error amplifier, series pass transistor, and current limiter, with access to remote shutdown.

FEATURES

- **Positive or negative supply operation**
- **Series, shunt, switching or floating operation**
- **.01% line and load regulation**
- **Output voltage adjustable from 2 to 37 volts**
- **Output current to 150mA without external pass transistor**
- **μA723 MIL STD 88 3A, B, C available**

PIN CONFIGURATIONS

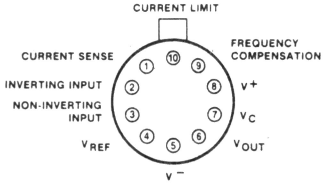
D,F,N PACKAGE


NC 1
CURRENT LIMIT 2
CURRENT SENSE 3
INVERTING INPUT 4
NON-INVERTING INPUT 5
V_{REF} 6
V⁻ 7
14 NC
13 FREQUENCY COMPENSATION
12 V+
11 V_C
10 V_{OUT}
9 V_Z
8 NC

TOP VIEW

ORDER NUMBERS
μA723F,N μA723CF,CN
SA723CN μA723CD

H PACKAGE*


CURRENT LIMIT
CURRENT SENSE
FREQUENCY COMPENSATION
INVERTING INPUT
NON-INVERTING INPUT
V_{REF}
V⁻
V+
V_C
V_{OUT}
①
②
③
④
⑤
⑥
⑦
⑧
⑨
⑩

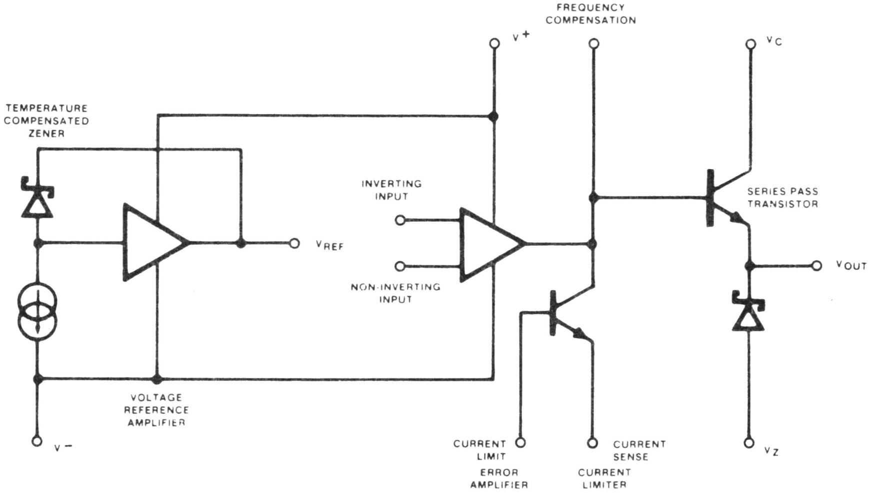
ORDER NUMBERS
μA723H μA723CH

*Metal cans (H) not recommended for new designs

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Pulse voltage from V+ to V- (50 ms)	50	V
Continous voltage from V+ to V-	40	V
Input-output voltage differential	40	V
Maximum output current	150	mA
Current from V_{REF}	15	mA
Current from V_Z	25	mA
Internal power dissipation[1]	800	mw
Operating temperature range		
μA723	-55 to +125	°C
μA723C	0 to 70	°C
SA723C	-40 to +85	°C
Storage temperature range	-65 to +150	°C
Lead temperature	300	°C

EQUIVALENT CIRCUIT


FREQUENCY COMPENSATION
V+
V_C
TEMPERATURE COMPENSATED ZENER
INVERTING INPUT
SERIES PASS TRANSISTOR
V_{REF}
NON-INVERTING INPUT
V_{OUT}
VOLTAGE REFERENCE AMPLIFIER
V−
CURRENT LIMIT
CURRENT SENSE
V_Z
ERROR AMPLIFIER
CURRENT LIMITER

PRECISION VOLTAGE REGULATOR

µA723/723C/SA723C

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$ unless otherwise specified.[1]

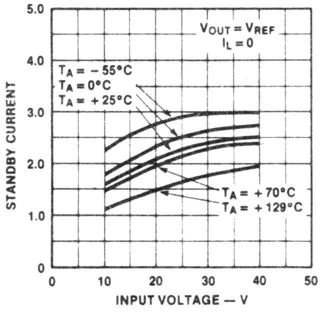
PARAMETER	TEST CONDITIONS	µA723 Min	µA723 Typ	µA723 Max	µA723C/SA723C Min	µA723C/SA723C Typ	µA723C/SA723C Max	UNIT
Line regulation[2]	$V_{IN} = 12V$ to $V_{IN} = 15V$ $V_{IN} = 12V$ to $V_{IN} = 40V$		0.01 0.02	0.1 0.2		0.01 0.1	0.1 0.5	$\%V_{OUT}$ $\%V_{OUT}$
Load regulation[2]	$I_L = 1mA$ to $I_L = 50mA$ f = 50Hz to 10kHz, $C_{REF} = 0$ f = 50Hz to 10kHz, $C_{REF} = 5\mu F$		0.03 74 86	0.15		0.03 74 86	0.2	$\%V_{OUT}$ dB dB
Short circuit current limit	$R_{SC} = 10\Omega$, $V_{OUT} = 0$		65			65		mA
Reference voltage		6.95	7.15	7.35	6.80	7.15	7.50	V
Output noise voltage	BW = 100Hz to 10kHz, $C_{REF} = 0$ BW = 100Hz to 10kHz, $C_{REF} = 5\mu F$		20 2.5			20 2.5		µVrms µVrms
Long term stability			0.1			1	0.1	%/1000hrs.
Standby current drain	$I_L = 0$, $V_{IN} = 30V$		2.3	3.5		2.3	4.0	mA
Input voltage range		9.5		40	9.5		40	V
Output voltage range		2.0		37	2.0		37	V
Input-output voltage differential		3.0		38	3.0		38	V
The following specifications apply over the operating temperature ranges Line regulation				0.3			0.3	$\%V_{OUT}$
Load regulation				0.6			0.6	$\%V_{OUT}$
Average temperature coefficient of output voltage	$V_{IN} = 12V$ to $V_{IN} = 15V$ $I_L = 1mA$ to $I_L = 50mA$		0.002	0.015		0.003	0.015	%/°C

NOTES

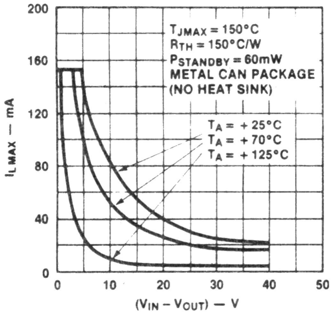
1. $V_{IN} = V+ = V_C = 12V$, $V- = 0V$, $V_{OUT} = 5V$, $I_L = 1mA$, $R_{SC} = 0$, $C_1 = 100pF$, $C_{REF} = 0$ and divider impedance as seen by error amplifier ≤ 10kΩ when connected as shown in Figure 3.
2. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

TYPICAL PERFORMANCE CHARACTERISTICS

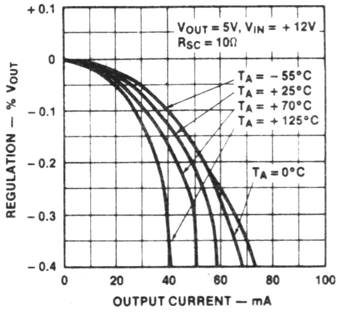
STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE



MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING

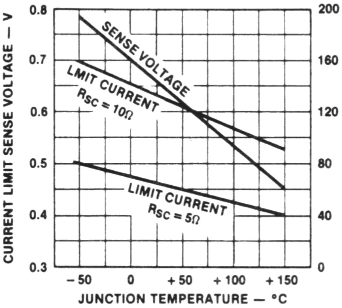


PRECISION VOLTAGE REGULATOR

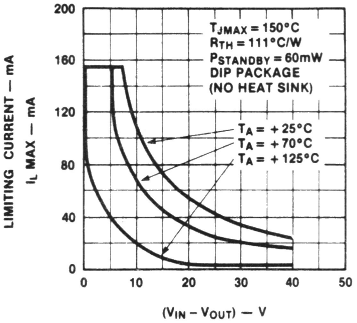
µA723/723C/SA723C

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

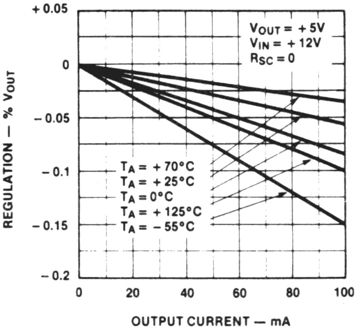
CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



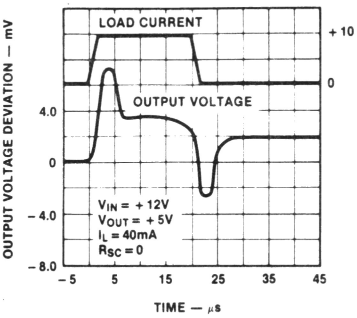
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



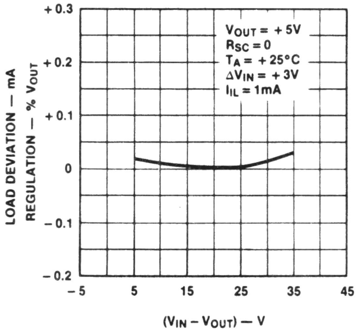
LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



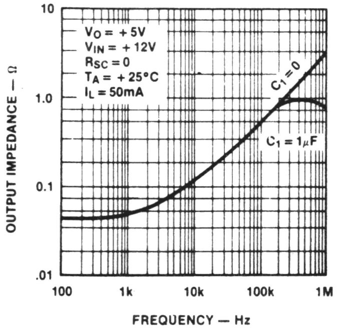
LOAD TRANSIENT RESPONSE



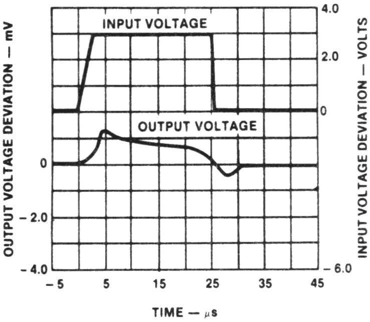
LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



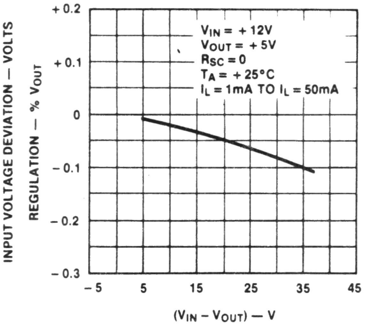
OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY



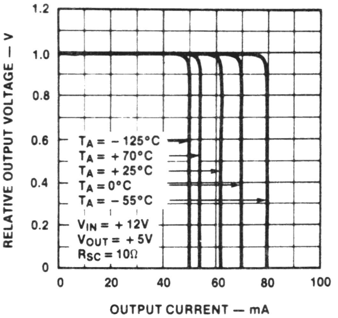
LINE TRANSIENT RESPONSE



LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

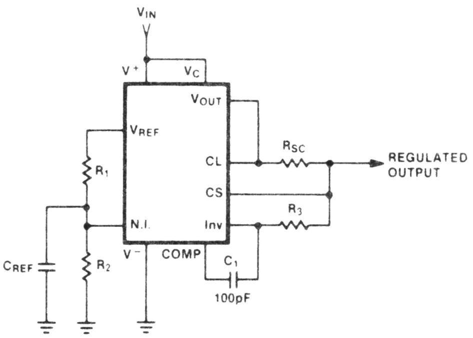


CURRENT LIMITING CHARACTERISTICS



TYPICAL APPLICATIONS

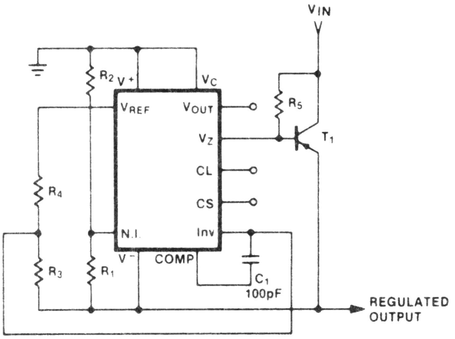
LOW VOLTAGE REGULATOR (V OUT = 2 TO 7 VOLTS)


VIN
V+
VC
VOUT
VREF
CL
CS
N.I.
Inv
V−
COMP
RSC
REGULATED OUTPUT
R3
R1
R2
CREF
C1
100pF

$$V_{OUT} = \left[V_{REF} \times \frac{R_2}{R_1 + R_2}\right]$$

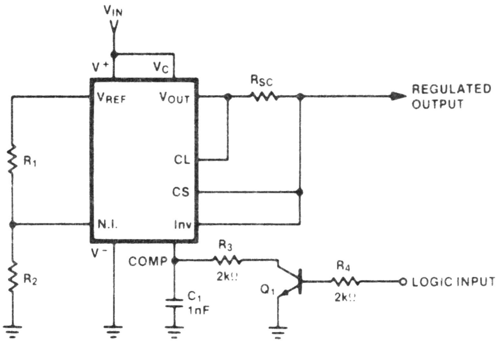
$R_3 = \frac{R_1 R_2}{R_1 + R_2}$ for minimum temperature drift

NEGATIVE VOLTAGE REGULATOR


VIN
R2
V+
VC
VREF
VOUT
VZ
CL
CS
N.I.
Inv
V−
COMP
R5
T1
R4
R3
R1
C1
100pF
REGULATED OUTPUT

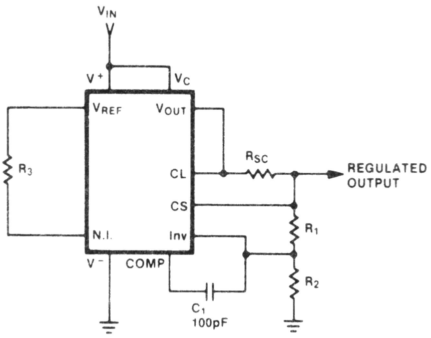
$$V_{OUT} = \left[\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1}\right];\ R_3 = R_4$$

REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING (V OUT = 2 TO 7 VOLTS)


VIN
V+
VC
VREF
VOUT
CL
CS
N.I.
Inv
V−
COMP
RSC
REGULATED OUTPUT
R1
R2
R3
2kΩ
Q1
R4
2kΩ
LOGIC INPUT
C1
1nF

$$V_{OUT} = \left[V_{REF} \times \frac{R_2}{R_1 + R_2}\right]$$

HIGH VOLTAGE REGULATOR (V OUT = 7 TO 37 VOLTS)


VIN
V+
VC
VREF
VOUT
CL
CS
N.I.
Inv
V−
COMP
R3
RSC
REGULATED OUTPUT
R1
R2
C1
100pF

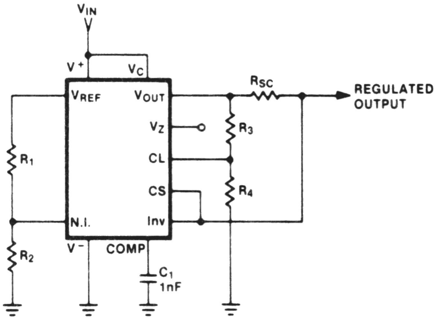
$$V_{OUT} = \left[V_{REF} \times \frac{R_1 + R_2}{R_2}\right]$$

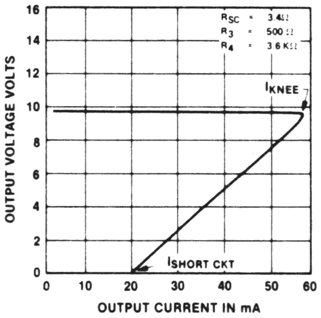
$R_3 = \frac{R_1 R_2}{R_1 + R_2}$ for minimum temperature drift

R3 may be eliminated for minimum component count

TYPICAL APPLICATIONS (Cont'd)

FOLDBACK CURRENT LIMITING REGULATOR
(V_{OUT} = 2 TO 7 VOLTS)


V_{IN}
V^+
V_C
V_{REF}
V_{OUT}
V_Z
CL
CS
N.I.
Inv
V^-
COMP
R_{SC}
REGULATED OUTPUT
R_1
R_2
R_3
R_4
C_1
1nF



$$I_{KNEE} = \left[\frac{V_{OUT}\,R_3}{R_{SC}\,R_4} + \frac{V_{SENSE}\,(R_3 + R_4)}{R_{SC}\,R_4}\right]$$

$$V_{OUT} = \left[V_{REF} \times \frac{R_1 + R_2}{R_2}\right]$$

$$I_{SHORT\ CKT} = \left[\frac{V_{SENSE}}{R_{SC}} \times \frac{R_3 + R_4}{R_4}\right]$$

$$\frac{R_4}{R_3} = \frac{V_{OUT}\,I_{SC}}{V_{SENSE}\,(I_{KNEE} - I_{SHORT\ CKT})} - 1$$

$$R_{SC} = \frac{V_{SENSE}}{I_{SC}}\left[1 + \frac{R_3}{R_4}\right]$$

Section 8
Applications

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SECTION 8 — APPLICATIONS

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AN OVERVIEW OF DATA CONVERTERS

AN100

INTRODUCTION

Large systems are comprised of many different subsystems, all of which must interface to complete the system. All types of circuits, including linear, digital and discrete are often used in the subsystems.

Interface circuits provide the necessary function of tying the parts of a system together. These circuits are usually not purely linear or digital but contain both types of circuit functions. For instance, sense amplifiers are designed for interface between low level memory outputs and bipolar levels, while differential comparators are designed for interface between analog systems and TTL/DTL systems. In general, this section will cover such devices as comparators, sense amplifiers, line drivers/receivers, and display drivers.

CONVERTERS

Digital communications, digital instruments and displays have created a demand for low cost reliable converters. Key factors in this demand are:

- The need to communicate with digital computers for processing and storage of analog signals.
- Severe limitations encountered in reliable analog data transmission over any considerable distance.
- The need for more easily readable displays.

General application areas for converters include: Data processing, data transmission, graphics and displays, audio systems, control systems and arithmetic operations.

Specific Applications

Test Systems

- Transistor tester (Force I_B and I_C)
- Resistor matching
- Programmable power supplies
- Programmable pulse generators
- Programmable current source
- Function generators (ROM drive)

Arithmetic Operations

- Analog division by a digital word
- Analog quotient of 2 digital words
- Analog product of 2 digital words—squaring
- Addition and subtraction with analog output
- Magnitude comparison of 2 digital words
- Digital quotient of 2 analog variables
- Arithmetic operations with words from different logic families

Graphics and Displays

- Polar to rectangular conversion
- CRT character generation
- Chart recorder driver
- CRT display driver

Data Transmission

- Modem transmitter
- Differential line driver
- Party line multiplexing of analog signals
- Multi-level 2-wire data transmission
- Secure communications (constant power dissipation)

Control Systems

- Reference level generator for setpoint controllers
- Positive peak detector
- Negative peak detector
- Disc drive head positioner
- Microfilm head positioner

Audio Systems

- Digital AVC and reverberation
- Music distribution
- Organ tone generator
- Audio tracking A/D
- Speech compression and expansion
- Audio digitizing and decoding

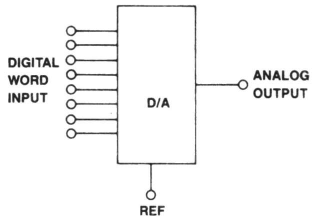
DAC Building Blocks

The actual implementation of a D/A system contains four separate parts: A reference quantity; a set of binary switches to simulate binary coefficients $B_1 \ldots B_N$; a weighting network; and an output summing means.

Binary-Weighted Ladder Employing Voltage Switching

The disadvantages of a binary-weighted ladder employing voltage switching include: A wide range of resistor values which are used in weighting the network; and nodal capacitances which are charged/discharged during conversion. See Figure 2.

CONVERSION OF A DIGITALLY CODED SIGNAL INPUT INTO AN ANALOG SIGNAL OUTPUT



Output = Ref. x digital word

$$\text{Output} = \text{Ref.} \times \left(\frac{B_1}{2} + \frac{B_2}{4} + \ldots + \frac{B_N}{2^N}\right)$$

Figure 1

R-2R Ladder Network Employing Current Switching

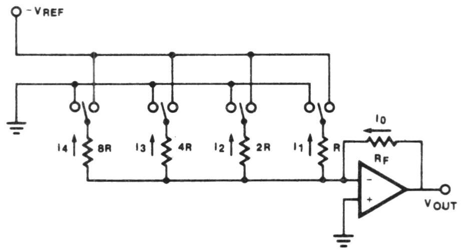
The advantages of this type of network include: No need for a wide range of resistor values; and current switching eliminates transients in nodal parasite capacitances. See Figure 3.

KEY SPECIFICATIONS

Speed

The conversion process should represent the input signal with the highest fidelity and minimal lag in time (Real time applications).

BINARY-WEIGHTED LADDER EMPLOYING VOLTAGE SWITCHING



$$V_{OUT} = \frac{R_F}{R} V_{REF} \times \left(b_1 + \frac{b_2}{2} + \frac{b_4}{4} + \frac{b_8}{8}\right)$$

Figure 2

AN OVERVIEW OF DATA CONVERTERS

DAC PRODUCTS SUMMARY

	MC1408 7-8	DAC08 Series	SE/NE5018/19	SE/NE5118/19	NE5020	MC3410 /NE5410	AM6012
Resolution	8 bit	8 bit	8 bit	8 bit	10 bit	10 bit	12 bit
Relative Accuracy	.39/ .19	.39/ .19/ .1	.19/ .1	.19/ .1	.05	.05	.05
Settling Time	300ns	60ns	2μs	200ns	4μs	250ns	500ns
Output	I	I & $\overline{I}$	V	I	V	I	±V
Features	Standard	Complementary Current Outputs	Bus Compatible input latches ref voltage	High speed current out version of NE5018	8 bit bus compatible	10 bit accuracy	Com-plementary Current Outputs

Table 1

Settling Time

Settling time is a measure of a converter's speed and is defined as the elapsed time after a code transition for DAC output to reach final value within specified limits, usually ±1/2 L.S.B. See Figure 4.

Errors

Offset Error —The output voltage of DAC with zero code input. Offset can and usually is trimmed to zero with an offset zero adjust potentiometer. See Figure 5.

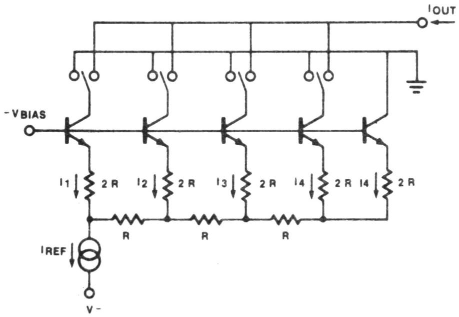
Gain Error —Deviation in output voltage from correct level when the input calls for a full scale output. This error may be trimmed to zero. See Figure 6.

Relative Accuracy—The maximum deviation of the DAC output relative to an ideal straight line drawn from zero to full scale -1 L.S.B. See Figure 7.

Differential Non-Linearity— Incremental error from any ideal L.S.B. analog output change when the digital input is changed 1 L.S.B.. See Figure 8.

Monotonicity—As the input code is incremented from one code to the next in sequence, the analog output will either increase or remain constant. See Figure 9.

R-2R LADDER NETWORK
EMPLOYING CURRENT SWITCHING



$I_{OUT} = I_{REF} \times \left(b_1 + \frac{b_2}{2} + \frac{b_3}{4} + \frac{b_4}{8}\right)$

Figure 3

Stability

Stability is a measure of the independence of converter parameters with respect to variations in external conditions such as temperature and supply voltage.

Temperature Coefficient —The effects of temperature changes of the output. Specified as %F.S. change.

Supply Rejection —Ability to resist changes in the output with supply changes, specified as % full scale change.

Long Term Stability —Measure of how stable the output is over a long period of time.

SETTLING TIME

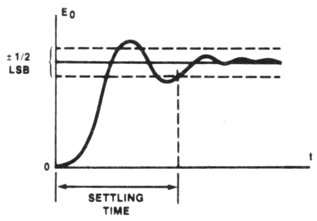


Figure 4

OFFSET ERROR

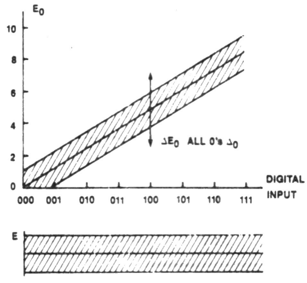


Figure 5

GAIN ERROR

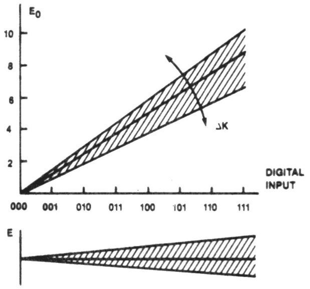


Figure 6

RELATIVE ACCURACY

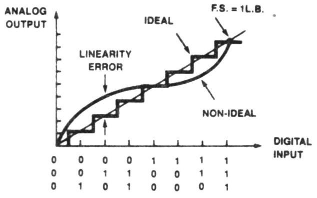


Figure 7

DIFFERENTIAL NON-LINEARITY

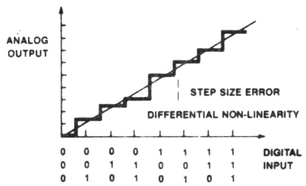


Figure 8

NON-MONOTONIC (Must be > ±1/2 LSB Non-Linear)

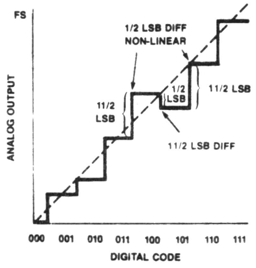


Figure 9

A/D CONVERTER CIRCUITS

Analog-to-Digital conversion schemes generally fall into one of three categories:

1. Feedback
   - Counting
   - Tracking (up-down)
   - Successive approximation
2. Integrating
   - Single slope
   - Dual slope
   - Triple slope
3. Multiple comparator (Flash)

The type of converter chosen for a given application depends upon many things: the accuracy required, the conversion speed necessary, the necessary immunity to noise, and cost are some of these considerations.

The successive approximation technique is the one most widely used, mainly because of its excellent tradeoffs in resolution, speed, accuracy, and cost. All of the A/D converters (ADCs) presently manufactured by Signetics are successive approximation types.

Figure 10 shows a simplified block diagram of a successive approximation A/D converter. Upon receiving the start signal, the successive approximation register (SAR) is cleared and the most significant bit (MSB) of that register is set. The SAR output is connected to the input of the DAC, the output of which is compared with the unknown input. If the input is less than the DAC output, the MSB is cleared and the next bit is set; if the input is greater than the DAC output, the MSB is left high and the next bit is set. The input is again compared with the DAC output and the second bit cleared or left high, based on the same criteria as for the MSB. This process continues until all bits have been determined.

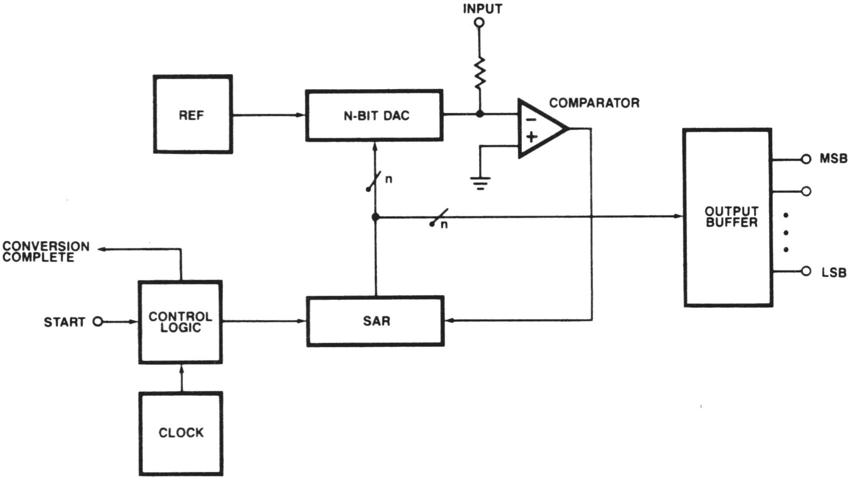


Figure 10. Block Diagram of a Successive Approximation A/D Converter.

The analog input should not change appreciably during the conversion time. If it did change during this time, the converted output would not be a true indication of the analog input. For this reason, it is common practice to use a sample-and-hold circuit at the converter analog input to hold the input value constant during the conversion process. A sample-and-hold circuit is not necessary if the signal at the input of the converter varies slowly enough and has a noise level low enough so that the input will not change a significant amount during the conversion. The allowable input change during this conversion is generally accepted as the value of 1/2 LSB (for n-bit accuracy).

Accuracy and speed are determined primarily by the properties of the DAC and the comparator. Linearity is determined primarily by the linearity of the DAC. If the DAC is non-monotonic, one or more codes will be missing from the A/D converter's output range.

Figure 11 is the transfer function of a 3-bit binary coded A/D converter with a 0 to + 10V input range. A 3-bit ADC is shown for simplicity but the principle applies to ADCs of any resolution. Note that there is a 1/2 LSB offset at the input such that the first count occurs with the input is equal the 1/2 LSB. The center of the range for the first step occurs, therefore, when the input is equal to the value of one LSB, and the error at the switch point is limited to 1/2LSB. This error is known as the quantization error as it is derived from the smallest input quantity that can be resolved. If an ADC has a specified error of 1/2 LSB maximum, this means that any transition point can be as far as 1/2 LSB from where it should be.

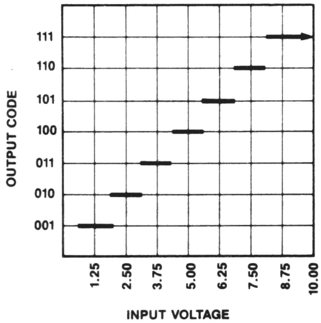


Figure 11. Transfer function of an ideal 3-bit ADC with a 0 to 10V input range.

AN OVERVIEW OF DATA CONVERTERS

CONSIDERATIONS FOR A/D CONVERTERS

- Analog input signal range and resolution required
- Linearity requirement and stability
- Conversion speed required
- Monotonicity requirement: Can missing codes be tolerated?
- Character of input signal: Is it noisy, sampled, filtered, slowly varying?
- Transfer characteristics (Type of coding)

A/D CONVERTER TERMS

Resolution

Resolution is the input change required to increment the output between the two adjacent codes. This term also refers to the number of bits in the output word and; hence, the number of discrete output codes the input analog signal can be broken into. Expressed in "bits" resolution.

Transfer Characteristic

The Transfer Characteristic is the relationship of the output digital word (code) to the input analog signal, i.e., Binary, BCD.

Conversion Speed

The Conversion Speed is the speed at which an ADC can make repetitive data conversions.

Quantizing Error

Quantizing Error is an inherent error in the conversion process due to finite resolution (discrete output). See Figure 12.

Offset Error

An Offset Error is shown in Figure 13.

Gain Error

A Gain Error is shown in Figure 14.

Relative Accuracy

Relative Accuracy is the deviation of an actual bit transition from the ideal transition value at any level over the range of the ADC (% F.S.). See Figure 15.

Hysteresis Error

A Hysteresis Error is the code transition voltage dependence relative to the direction from which the transition is approached.

Monotonicity

Monotonicity is when the output code either increases or remains the same for increasing analog input signals. The opposite is true in the reverse direction.

Missing Codes

A Missing Code is a code combination that is skipped. See Figure 16.

QUANTIZING ERRORS

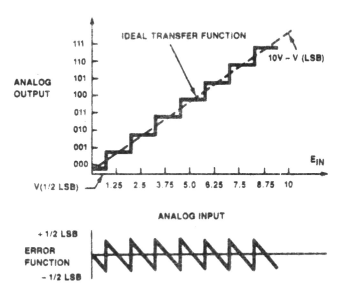


Figure 12

OFFSET ERROR

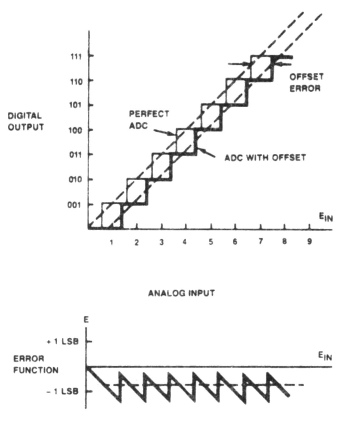
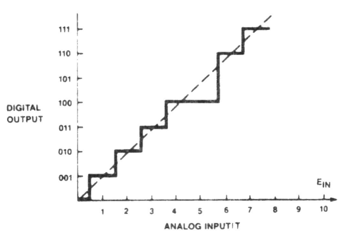


Figure 13

MISSING CODES



(SHOWS A MISSING CODE AT 101)

Figure 16

GAIN ERROR

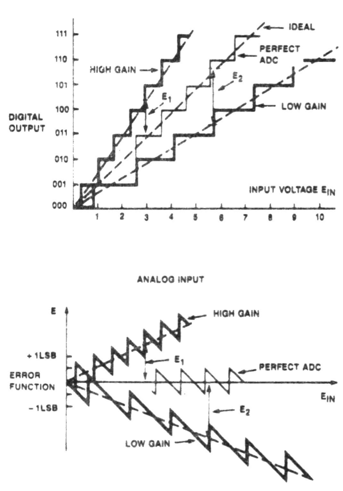


Figure 14

RELATIVE ACCURACY

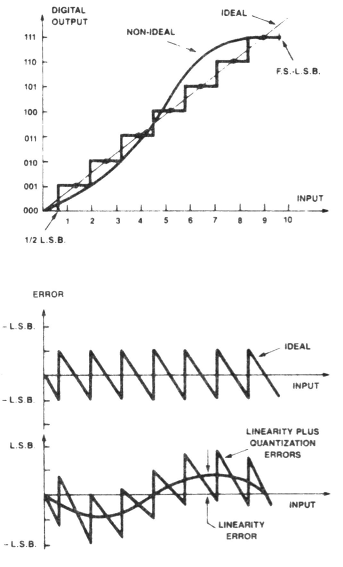


Figure 15

DAC08 SERIES

Reference Amplifier Setup

The DAC08 Series is a multiplying D-to-A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +4.0mA. The full scale output current is a linear function of the reference current and is given by this equation where $I_{REF} = I_{14}$.

$$I_{FS} = \frac{255}{256} \bullet I_{REF}$$

In positive reference applications shown in Figure 1, an external positive reference voltage forces current through R14 into the V_{REF} (+) terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to V_{REF} (−) at pin 15, shown in Figure 2. Reference current flows from ground through R14 into V_{REF}(+) as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R15 (nominally equal to R14) is used to cancel bias current errors. R15 may be eliminated with only a minor increase in error.

Bipolar references may be accommodated by offsetting V_{REF} or pin 15 as shown in Figure 3. The negative common mode range of the reference amplifier is given by the following equation.

$$V_{CM-} = V- + (I_{REF} \bullet 1k\Omega) + 2.5V$$

When a dc reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a refernce R14 should be split into 2 resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications, a +10.0V reference is recommended for optimum full scale temperature coefficient performance. This will minimize the contributions of reference amplifier V_{OS} and TCV_{OS}. For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full scale trimming may be accomplished by adjusting the value of R14, or by using a potentiometer for R14. An improved method of full scale trimming which eliminates potentiometer T.C. effects is shown Figure 4.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common mode range. The recommended range for operation with a dc reference current is +0.2mA to +4.0mA.

The reference amplifier must be compensated by using a capacitor from pin 16 to V−. For fixed reference operation, a 0.01μF capacitor is recommended. For varible reference applications, see section entitled Reference Amplifier Compensation for Multiplying Applications.

Multiplying Operation

The DAC08 Series provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 4mA to 4μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 4.0mA.

Reference Amplifier Compensation for Multiplying Applications

AC reference applications will require the reference amplifier to be compensated using a capacitor from pin 16 to V−. The value of this capacitor depends on the impedance presented to pin 14. For R_{14} values of 1.0, 2.5 and 5.0KΩ, minimum values of C_C are 15, 37 and 75pF. Larger values of R_{14} require proportionately increased values of C_C for proper phase margin.

For fastest multiplying response, low values of R_{14} enabling small C_C values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the preceding values will suffice and the amplifier must be heavily compensated, which will decreased overall bandwidth and slew rate. For $R_{14} = 1k\Omega$ and $CC = 15pF$, the reference amplifier slews at 4mA/μs enabling a transition from $I_{REF} = 0$ to $I_{REF} = 2mA$ in 500ns.

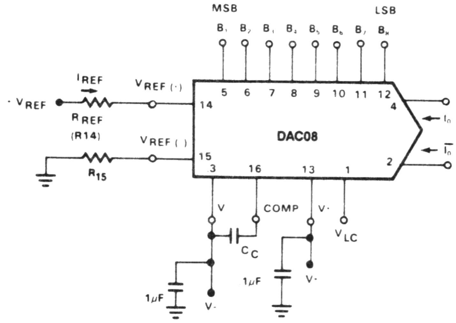
Operation with pulse inputs to the reference amplifier may be accommodated by an alternate compensation scheme shown in Figure 5. This technique provides lowest full scale transition times. Full scale transition (0 to 2mA) occurs in 120ns when the equivalent impedance at pin 14 is 200Ω and $C_C = 0$. This yields a reference slew rate of 16mA/μs, which is relatively independent of R_{IN} and V_{IN} values.

Logic Inputs

The DAC08 design incorporates a logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2μA logic input current and completely adjustable logic threshold voltage. For V− = −15V, the logic inputs may swing between −11V and +18V. This enables direct interface with +15V CMOS logic, even when the DAC08 is powered from a +5V supply. Minimum input logic swing is given by following the equation.

$$V- + (I_{REF} \bullet 1k\Omega) + 2.5V$$

BASIC POSITIVE REFERENCE OPERATION

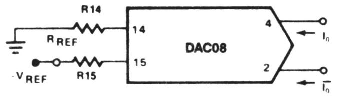


$$I_{FS} \approx +\frac{V_{REF}}{R_{REF}} \times \frac{255}{256} \quad I_O + \overline{I_O} = I_{FS} \text{ for all logic states}$$

For fixed reference, TTL operation typical values are:
$V_{REF} = +10.000V$, $R_{REF} = 5.000\Omega$ R15 ≈ R_{REF},
$C_C = 0.01\mu F$, $V_{LC} = 0V$ (ground)

Figure 1

BASIC NEGATIVE REFERENCE OPERATION

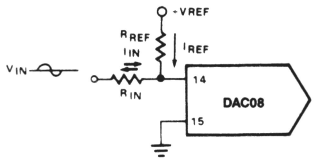


$$I_{FS} = \frac{-V_{REF}}{R_{REF}} \times \frac{255}{256}$$

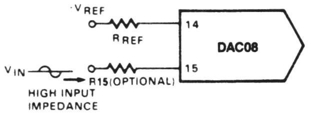
R_{REF} sets I_{FS}, R15 is for bias current cancellation.

Figure 2

ACCOMMODATING BIPOLAR REFERENCES



$I_{REF} \geq$ Peak Negative Swing of I_{IN}



$+V_{REF}$ must be above Peak Positive Swing of V_{IN}

Figure 3

RECOMMENDED FULL SCALE ADJUSTMENT CIRCUIT

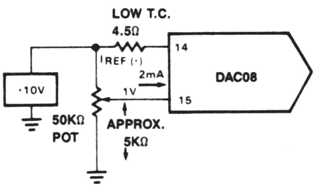


Figure 4

The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control in (pin 1, V_{LC}). Figure 6 shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4 above V_{LC}. For TTL and DTL interface, simply ground pin 1. When interfacing ECL, an I_{REF} = 1mA is recommended. For interfacing other logic families, see Figure 7. For general setup of the logic control circuit, it should be noted that pin 1 may source up to 200μA. External circuitry should be designed to accommodate this current.

Fastest settling times are obtained when pin 1 sees a low impedance. If pin 1 is connected to a 1kΩ divider, for example, it should be bypassed to ground by a 0.01μF capacitor.

Analog Output Currents

Both true and complemented output sink currents are provided, where $I_O + \overline{I_O} = I_{FS}$. Current appears at the true output when a 1 is applied to each logic input. As the binary count increases, the sink current at pin 4 increases proportionally, in the fashion of a positive logic D-to-A converter. When a 0 is applied to any input bit, that current is turned off at pin 4 and turned on at pin 2. A decreasing logic count increases I_O as in a negative or inverted logic D-to-A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FS}. Do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above V− and is independent of the positive supply. Negative compliance is given by the equation:

$$V- + (I_{REF} \bullet 1k\Omega) + 3.0V$$

Note that lower values of I_{REF} will allow a greater output compliance.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as balanced bridge A/D circuits as well as driving center-tapped coils and transformers.

Power Supplies

The DAC08 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating at supplies of ±5V or less, $I_{REF} \leq$ 1mA is recommended.

PULSED REFERENCE OPERATION

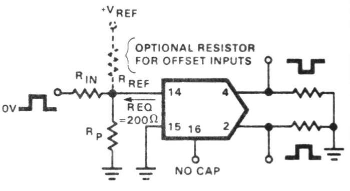


Figure 5

Low reference current operation decreases power consumption and increases negative compliance, reference amplifier negative common mode range, negative logic input range, and negative logic threshold range. Consult the various figures for guidance. For example, operation at −4.5V with I_{REF} = 2mA is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible; however, at least 8V total must be applied between pins 2 and 4, and pin 3 to insure turn-on of the internal bias network.

Symmetrical supplies are not required, as the DAC08 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be useful to insure logic swings, etc., remain between acceptable limits.

Power consumption may be calculated by this equation.

$$P_D = (I+)(V+) + (I+)(V-) + (2I_{REF})(V-)$$

A useful feature of the DAC08 design is that supply current is constant and independent of input logic states. This is useful in cryptographic applications and further serves to reduce the size of the power supply bypass capacitors.

Temperature Performance

The linearity and monotonicity specifications of the DAC08 are guaranteed to apply over the entire rated operating temperature range. Full scale output current drift is low, typically ±10ppm/°C, with zero scale output current and drift essentially negligible compared to 1/2 LSB.

Full scale output drift performance will be best with +10.0V references, as V_{OS} and TCV_{OS} of the reference amplifier will be very small compared to 10.0V. The temperature

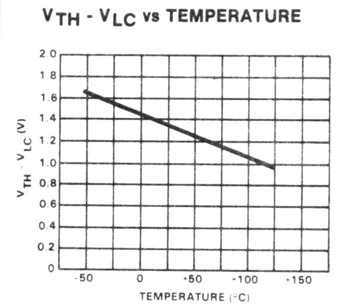


Figure 6

coefficient of the reference resistor R14 should match and track that of the output resistor for minimum overall full scale drift. Settling times of the DAC08 decrease approximately 10% at −55°C and an increase of about 15% at +125°C is typical.

Settling Time

The DAC08 is capable of extremely fast settling times (typically 85ns at $I_{REF} = 2.0mA$). Judicious circuit design and careful board layout must be employed to obtain full performance potential during testing and application. The logic switch design enables propagation delays of only 35ns for each of the 8 bits. Settling time to within 1/2 LSB of the LSB is therefore 35ns, with each progressively larger bit taking successively longer. The MSB settles in 85ns, thus determining the overall settling time of 85ns. Settling to 6-bit accuracy requires about 65 to 70 ns. The output capacitance, including the package, is approximately 15pF. Therefore the output RC time constant dominates settling time if RL >500Ω.

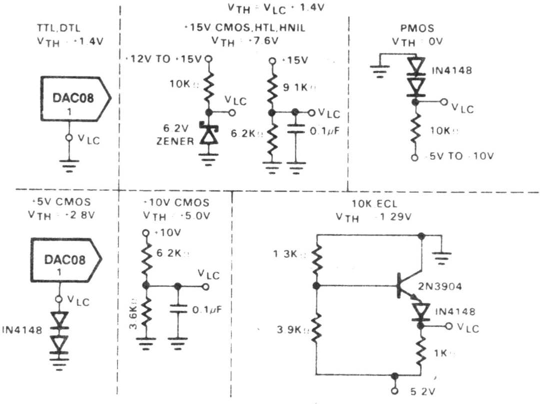
Settling time and propagation delay are relatively insensitive to logic input amplitude and rise and fall times due to the high gain of the logic switches. Settling time also remains essentially constant for I_{REF} values down to 1.0mA, with gradual increases for lower I_{REF} values. The principal advantage of higher I_{REF} values lies in the ability to attain a given output level with lower load resistors, thus reducing the output RC time constant.

Measurement of settling time requires the ability to accurately resolve ±4μA. Therefore a 1kΩ load is needed to provide adequate drive for most oscilloscopes. The settling time fixture of Figure 8 uses a cascode design to permit driving a 1kΩ load with less than 5pF of parastic capacitance at the measurement node. At I_{REF} values of less than 1.0mA, excessive RC damping of the output is difficult to prevent while maintaining adequate sensitivity. However, the major carry from 01111111 to 10000000 provides an accurate indicator of settling time. This code change does not require the normal 6.2 time constants to settle to within ±0.2% of the final value; thus, settling time may be observed at lower values of I_{REF}.

The DAC08 switching transients or glitches are very low and may be further reduced by small capacitive loads at the output at a minor sacrifice in settling time.

Fastest operation can be obtained by using short leads, minimizing output capacitance and load resistor values, and by adequate bypassing at the supply, reference and V_{LC} terminals. Supplies do not require large electrolytic bypass capacitors as the supply current drain is dependent of input logic states. 0.1μF capacitors at the supply pins provide full transient performance.

INTERFACING WITH VARIOUS LOGIC FAMILIES



NOTE

Do not exceed negative logic input range of DAC

Figure 7

SETTLING TIME MEASUREMENT

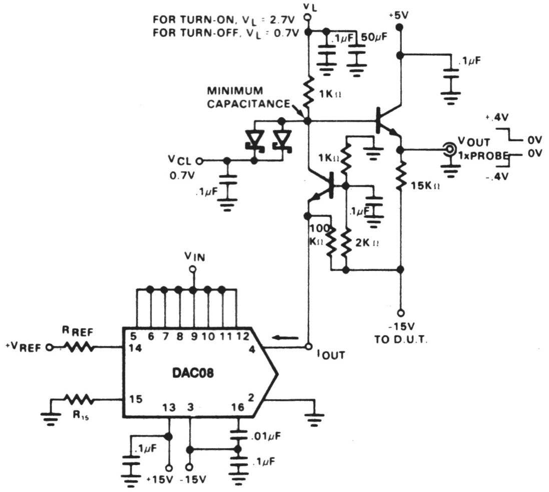
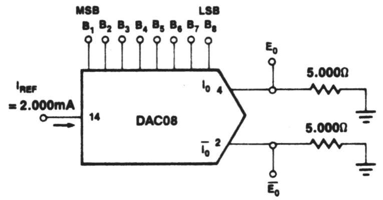

VL
FOR TURN-ON, VL = 2.7V
FOR TURN-OFF, VL = 0.7V
.1µF
50µF
+5V
.1µF
MINIMUM CAPACITANCE
1KΩ
+.4V
VOUT
1xPROBE
0V
0V
-.4V
VCL
0.7V
.1µF
1KΩ
15KΩ
.1µF
100KΩ
2KΩ
VIN
-15V TO D.U.T.
RREF
+VREF
5 6 7 8 9 10 11 12
14
4
IOUT
DAC08
15
13 3
16
2
R15
.1µF
+15V -15V
.01µF
.1µF

Figure 8

TYPICAL APPLICATIONS

BASIC UNIPOLAR NEGATIVE OPERATION

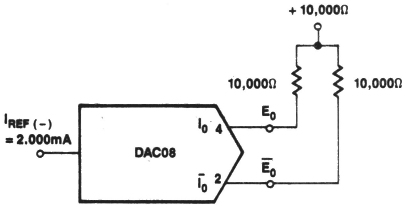

MSB
LSB
B_1 B_2 B_3 B_4 B_5 B_6 B_7 B_8
E_0
I_{REF} = 2.000mA
14
DAC08
I_0 4
$\overline{I_0}$ 2
5.000Ω
5.000Ω
$\overline{E_0}$

	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	I_OmA	$\overline{I_O}$mA	E_O	$\overline{E_O}$
Full scale	1	1	1	1	1	1	1	1	1.992	000	-9.960	.000
Full scale - LSB	1	1	1	1	1	1	1	0	1.984	.008	-9.920	-.040
Half scale + LSB	1	0	0	0	0	0	0	1	1.008	.984	-5.040	-4.920
Half scale	1	0	0	0	0	0	0	0	1.000	.992	-5.000	-4.960
Half scale - LSB	0	1	1	1	1	1	1	1	.992	1.000	-4.960	-5.000
Zero scale + LSB	0	0	0	0	0	0	0	1	.008	1.984	-.040	-9.920
Zero scale	0	0	0	0	0	0	0	0	.000	1.992	.000	-9.960

Figure 9

TYPICAL APPLICATIONS (Cont'd)

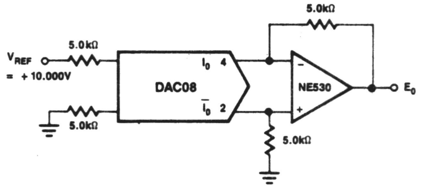
BASIC BIPOLAR OUTPUT OPERATION


+ 10,000Ω
10,000Ω
10,000Ω
I_{REF} (−) = 2.000mA
DAC08
I_0 4
$\bar{I}_0$ 2
E_0
$\bar{E}_0$

	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	E_O	$\overline{E_O}$
POS full scale	1	1	1	1	1	1	1	1	-9.920	+10.000
POS full scale - LSB	1	1	1	1	1	1	1	0	-9.840	+9.920
Zero scale + LSB	1	0	0	0	0	0	0	1	-0.080	+0.160
Zero scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero scale - LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg full scale + LSB	0	0	0	0	0	0	0	1	+9.920	-9.840
Neg full scale	0	0	0	0	0	0	0	0	+10.000	-9.920

Figure 10

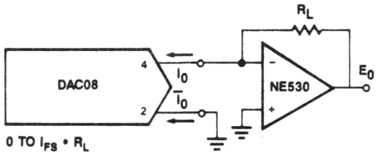
SYMMETRICAL OFFSET BINARY OPERATION


5.0kΩ
V_{REF} = + 10.000V
5.0kΩ
5.0kΩ
DAC08
I_0 4
$\bar{I}_0$ 2
NE530
−
+
5.0kΩ
E_0

	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	E_O
POS full scale	1	1	1	1	1	1	1	1	+9.920
POS full scale - LSB	1	1	1	1	1	1	1	0	+9.840
(+) Zero scale	1	0	0	0	0	0	0	0	+0.040
(-) Zero scale	0	1	1	1	1	1	1	1	-0.040
Neg full scale + LSB	0	0	0	0	0	0	0	1	-9.840
Neg full scale	0	0	0	0	0	0	0	0	-9.920

Figure 11

POSITIVE LOW IMPEDANCE OUTPUT OPERATION

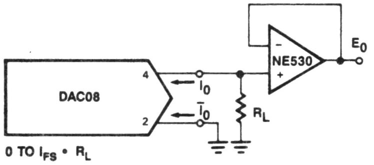

R_L
DAC08
4
2
I_O
Ī_O
NE530
-
+
E_O
0 TO I_FS • R_L

$$I_{FS} \cong \frac{255}{256} I_{REF}$$

For complementary output (operation as negative logic DAC), connect inverting input of OP-amp to I_O (pin 2), connect $\overline{I}_O$ (pin 4) to ground.

Figure 12

NEGATIVE LOW IMPEDANCE OUTPUT OPERATION


DAC08
4
2
I_O
Ī_O
R_L
NE530
-
+
E_O
0 TO I_FS • R_L

$$I_{FS} \cong \frac{255}{256} I_{REF}$$

For complementary output (operation as a negative logic DAC), connect non-inverting input of OP-amp to I_O (pin 2); connect I_O (pin 4) to ground.

Figure 13

LOW COST 8-BIT 1 MICROSECOND A-TO-D CONVERTER

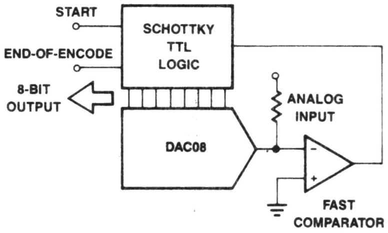
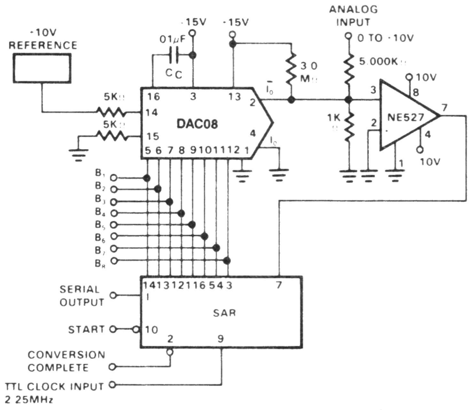

START
END-OF-ENCODE
8-BIT OUTPUT
SCHOTTKY TTL LOGIC
DAC08
ANALOG INPUT
-
+
FAST COMPARATOR

Figure 14

3 IC LOW COST A-TO-D CONVERTER

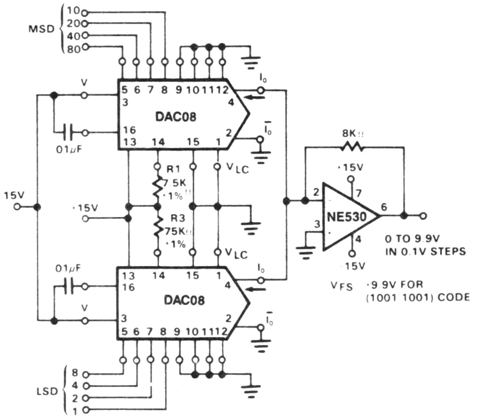

-10V REFERENCE
-15V
-15V
ANALOG INPUT
0 TO -10V
.01μF
Cc
5K
5K
16
14
15
3
13
2
4
1
DAC08
5 6 7 8 9 10 11 12
I0
3.0 MΩ
5.000KΩ
1K
NE527
+10V
-10V
B1
B2
B3
B4
B5
B6
B7
B8
SERIAL OUTPUT
START
CONVERSION COMPLETE
TTL CLOCK INPUT 2.25MHz
14 13 12 11 6 5 4 3
7
1
10
2
9
SAR

NOTE

Connect "start" to "conversion complete" for continuous conversions.

Figure 15

LOW COST 2-DIGIT BCD DAC

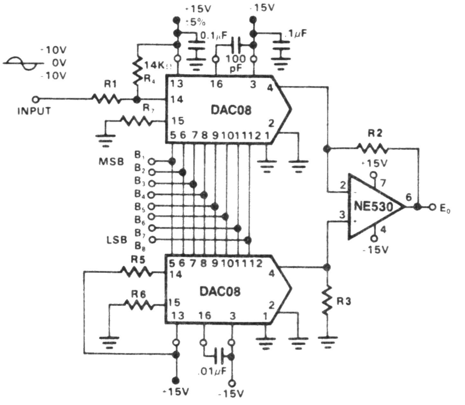

MSD
10
20
40
80
V
5 6 7 8 9 10 11 12
3
DAC08
16
13 14 15 1
.01μF
I0
R1 7.5K ±1%
R3 75KΩ ±1%
VLC
15V
-15V
.01μF
13 14 15 1
16
DAC08
3
5 6 7 8 9 10 11 12
LSD
8
4
2
1
8KΩ
-15V
NE530
2
3
7
6
4
15V
0 TO 9.9V IN 0.1V STEPS
VFS = 9.9V FOR (1001 1001) CODE

NOTE

Output is directly proportional to positive power supply.

Figure 16

DC-COUPLED DIGITAL ATTENUATOR/ PROGRAMMABLE GAIN AMPLIFIER


+10V
0V
-10V
INPUT
R1
R7
14KΩ
R4
-15V ±5%
15V
0.1μF
100 pF
1μF
13 16 3 4
14
15
DAC08
5 6 7 8 9 10 11 12 1
2
MSB
B1
B2
B3
B4
B5
B6
B7
B8
LSB
R5
R6
5 6 7 8 9 10 11 12
14
15
DAC08
13 16 3 1
4
2
R2
R3
+15V
NE530
E0
-15V
.01μF
-15V
-15V

Bipolar input offset binary output } Performs 2 quadrant multiplications—AC input controls output polarity.

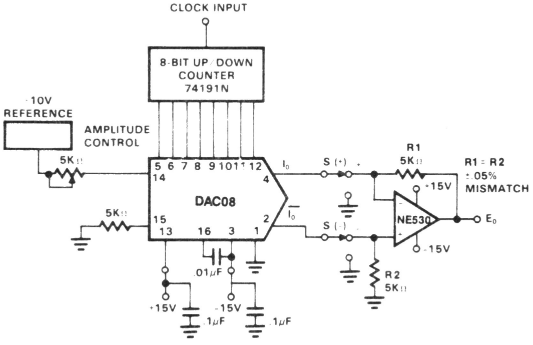
NOTES

1. R1 = R2 = R3
2. R4 = R5
3. Eo DC to 20KHz = ±5V
4. Eo DC to 10KHz = ±10V

Figure 17

HIGH SPEED WAVEFORM GENERATOR

OUTPUT TYPE (EO)	SWITCH S(+)	CONDITIONS S(-)
Unipolar positive	+	GND
Unipolar negative	GND	-
Bipolar	+	-


CLOCK INPUT
8-BIT UP/DOWN COUNTER 74191N
-10V REFERENCE
AMPLITUDE CONTROL
5KΩ
5KΩ
5 6 7 8 9 10 11 12
14
15
13 16 3 1
DAC08
4
2
I0
S(+)
S(-)
R1 5KΩ
R2 5KΩ
+15V
-15V
NE530
E0
R1 = R2 ±.05% MISMATCH
.01μF
-15V
-15V
.1μF
.1μF

NOTES

1. Bipolar output is symmetrical around zero, adjustable peak to peak amplitude.
2. For triangle wave, count up to full, reverse and count down.
3. For positive-going sawtooth, count up to full, clear, repeat.
4. For negative-going sawtooth, count down, clear, repeat.
5. For other waveforms, use a ROM programmed with the desired function.

Figure 18

DIGITAL ATTENUATOR

Figure 1 shows a D-C coupled Digital Attenuator or Programmable Gain Amplifier.

Pin 14 of the DAC is a Virtual Ground. Current must always flow into Pin 14, so the current through R4 must be greater than that through R1 when the input signal is at its most negative usable value. If the input signal value goes low enough to cause the current through R1 to be greater than that through R4, output clipping will occur.

To extend the operating frequency range, the compensation cap, C_C, needs to be minimized, which implies that the resistance at Pin 14 (R1 and R4) must be minimized. If the voltage to which R4 and R5 are returned has any noise on it at all, R4 and R5 should be formed of two series resistors with the junction of them bypassed with 0.1μF to ground. Pin 15 could be grounded with a small sacrifice in accuracy and temperature drift. R6 and R7 compensate for reference amplifier input offset.

R1 and R4 should be chosen such that, when the input is at peak usable signal, the total current into Pin 14 does not exceed 4mA. When the input is most negative, R1 current must be less than R4 current (remember, pin 14 is always at 0V). Also, when the input is at its absolute positive peak value, current into pin 14 should not exceed 5mA. Minimum compensation capacitor, C_C, in pF is 15 times the parallel combination of R1 and R4 in K-ohms.

With a single DAC, there is a D C offset at the circuit output that varies with the digital word input. To eliminate this, we use a second DAC to subtract this offset at the sum node of the op-amp.

Example 1: Input signal is to be 20V p-p, centered at 0V. Maximum input frequency is to be 15kHz. Power supplies available are +/−15V, both regulated. Determine values of all resistors for maximum gain of unity.

Solution 1: At minimum input (−10V), reference current, I_{REF} is

$$I_{REF} = \frac{15V}{R4} + \frac{(-10V)}{R1}$$

If minimum $I_{REF} = 0$, then

$$\frac{15V}{R4} = \frac{10V}{R1}$$

and R4 = (1.5)(R1),

Therefore, 60 percent of I_{REF} comes through R4. If we let I_{REF} go to about 3.9mA (4mA is max recommended), R4 current is found to be

$$I_{R4} = (0.6)\ (3.9mA) = 2.34mA$$

and R4 = 6.4K.

The balance of the reference current I_{R1} is found to be

$$I_{R1} = 3.9mA - I_{R4}$$

or

$$I_{R1} = 3.9mA - 234mA = 1.56mA$$

and

R1 = 6.4K

Using commonly available values, and remembering that R4 current must exceed R1 current, we set

R1 = 6.8K

and R4 = 6.2K.

Maximum reference current is now

$$I_{REF}\ (max) = \frac{15V}{6.2K} + \frac{10V}{6.8K} = 3.9mA.$$

The parallel combination of R1 and R4 is found to be 3.24K, so minimum compensation capacitor value is

$$C_C\ (min) = (3.24)(15)pF = 48.6pF.$$

If we use 50pF, from the graph we find $F_{(max)}$ to be 370kHz. For unity gain,

R2 = R1 = 6.8K
R3 = R2 = 6.8K
R5 = R1 = 6.8K

$$R6 = R7 = \frac{(R1)\ (R4)}{R1 + R4} = 3.24K$$

(use 3.3K)

Example 2: Usable input signal is 12V p-p, centered at 0V, with occasional excursion to twice this amplitude, which we do not care about. Maximum input frequency is to be 500kHz. Available power supplies are +5V logic supply, +15V, −15V, all regulated. Determine values of all resistors and C_C for maximum gain of 2.

Solution 2: To extend the frequency response, we want minimum compensation capacitor value, therefore need minimum R1 and R4 values, for which reason we want to return R4 to as low a regulated supply as is possible; we will use the 5V logic supply.

At minimum usable input,

$$I_{REF} = \frac{5V}{R4} - \frac{6V}{R1}$$

or, for $I_{REF} = 0$,

$$\frac{5V}{R4} = \frac{6V}{R1}$$

therefore, 55 percent of $I_{(REF)}$ comes through R4, and

$$R4 = (5/6)R1.$$

Because peak input goes to +12V, this condition should not cause $I_{(REF)}$ to exceed 5mA, and

$$\frac{12V}{R1} + \frac{5V}{R4} = 5mA$$

Recall that R4 = (5/6) R1

$$\frac{12V}{R1} + \frac{5}{(5/6)\ (R1)} = 5mA$$

$$\frac{12V}{R1} + \frac{6V}{R1} = 5mA$$

R1 = 3.6K

and R4 = (5/6) R1 = 3.0K

Because the reference source will be the 5V logic supply, which will be noisy, we will split R4 into two resistors and bypass their junction with 0.1μF to ground. Furthermore, to be sure that R4 current exceeds R1 current, we will increase R1 to 4.3K. The absolute maximum reference current is now

$$I_{REF}\ (max) = \frac{12V}{4.3K} + \frac{5V}{3K} = 4.46mA.$$

The parallel combination of R1 and R4 is 1.77K, so minimum compensation capacitor is

$$C_C(min) = (15)(1.77) = 26.5pF$$

If we use 27pF, the graph tells us the maximum frequency is about 490kHz, which is 2 percent lower than desired. If we wanted to further extend this frequency range, we find that we can reduce R4 to two resistors of 1.1K and 1.2K, bringing the absolute maximum reference current to

$$I_{REF}\ (max) = \frac{12V}{4.3K} + \frac{5V}{2.3K} = 4.96mA$$

and the maximum usable reference current becomes

$$I_{REF} = \frac{6V}{4.3K} + \frac{5V}{2.3K} = 3.57mA,$$

below the 5mA and 4mA respective desired maximum values. Now the resistance at pin 14 is the parallel combination of R1 and R4, or 1.4K, and the minimum compensation capacitor becomes

$$C_C(min) = (15)(1.4)pF = 21pF.$$

If we use 22pF, the graph tells us we can just go to 500kHz.

USING THE DAC08 WITHOUT A NEGATIVE SUPPLY AN106

USING THE DAC08 WITHOUT A NEGATIVE SUPPLY

The DAC08 can be used without a negative supply if a few precautions are observed:

1. V_{CC} must be in the range of 10V to 30V.
2. $V_{REF(-)}$ must be at least 3V more positive than pin 3 at all times.
3. Pins 2 and 4 must always be at least 5 volts above pin 3 for reference currents up to 2mA, and at least 8 volts above pin 3 for reference currents above 2mA.
4. Pin 1 must be at least 5 volts above pin 3.

Figure 1 shows the DAC08 in a circuit without a negative supply with two MC1489's used as level shifters. The need for level shifters is implied from requirement 4 above, since the logic threshold is about 1.35 volts above pin 1. V_O must be the same potential as the positive logic supply because of the internal circuitry of the MC1489.

If $V_{REF(+)}$ is a very stable source with no ripple or noise, R1 and R2 can be a single resistor. The same is true of R3 and R4 if $V_{REF(-)}$ is a very stable source. Resistor values are determined as follows:

$$R1 + R2 = \frac{V_{REF(+)} - V_{REF(-)}}{I_{REF}}$$

$$R3 + R4 = R1 + R2$$

where I_{REF} is reference current through R1 and R2 (pin 14 is at $V_{REF(-)}$ potential)

The value of the compensation capacitor, C_C, is determined by the relationship:

$$C_C = 15\,(R1 + R2)$$

where C_C is in pF and R1 and R2 are in Kilohms.

V_O (DAC08 pin 1 and MC1489 pin 7) must be at least 5 volts for DAC08 reference currents at or below 2mA, and at least 8 volts for reference currents above 2mA. V_O must also be equal to the positive potential of the logic supply, as mentioned above. It should be noted that the MC1489 inverts the logic inputs.

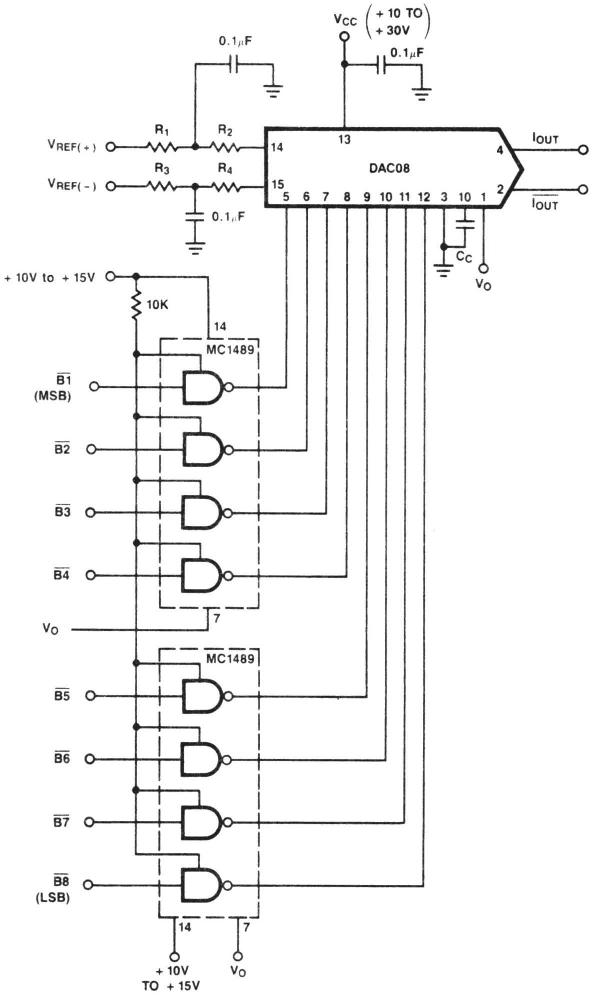
EXAMPLE

Power supply voltages of +5V and +15V are available and the input logic is TTL. The need is for a DAC with a full scale output of 2mA.

- V_O is set to +5V
- V_{CC} for the DAC08 and the MC1489 are set to +15V
- If $V_{REF(+)}$ and $V_{REF(-)}$ are set to +15V and +5V respectively,

$$R1 + R2 = \frac{15 - 5}{I_{REF}} = \frac{10V}{2mA} = 5K$$

- R3 + R4 should also add up to 5 Kilohms.
- C_C is 15(5)pF = 75pF.



VCC (+10 TO +30V)
0.1μF
0.1μF
R1
R2
R3
R4
VREF(+)
VREF(−)
0.1μF
14
13
15
DAC08
5 6 7 8 9 10 11 12 3 10 1
4
2
IOUT
$\overline{I_{OUT}}$
CC
VO
+10V to +15V
10K
14
MC1489
$\overline{B1}$ (MSB)
$\overline{B2}$
$\overline{B3}$
$\overline{B4}$
VO
7
MC1489
$\overline{B5}$
$\overline{B6}$
$\overline{B7}$
$\overline{B8}$ (LSB)
14
7
+10V TO +15V
VO

Figure 1. Using the DAC08 without a negative supply.

MICROPROCESSOR COMPATIBLE DACs AN109

DAC products are designed to convert a digital code to an analog signal. Since a common source of digital signals is the data bus of a μ processor, DAC circuits that are bus compatible ease the design engineer's interface problems.

WHAT FEATURES MAKE A DEVICE BUS COMPATIBLE?

The five conditions which determine processor bus compatibility are:

- **Inputs must be low loading**
- **Addressing must be provided**
- **Inputs must be latched**
- **Logic thresholds must be compatible**
- **Timing requirements should be adequate (<1 μ sec)**

Signetics microprocessor compatible DACs, the NE5018 series, meet these requirements. In addition, they provide an internal reference source. The NE5018 provides a scaled voltage output, eliminating the need for an external op amp. The NE5118 is identical to the NE5018, except it provides the user with a current output. Figure 1 shows a typical microprocessor system with analog I/O using the NE5018 to provide a programmable voltage and an NE5118 to provide a programmable current.

The following discussions detail the operation of the NE5018 and NE5118 series DAC's.

LATCH CIRCUIT

The latch circuits of the NE5018 and NE5118 are identical. Both the data inputs and latch enable ($\overline{LE}$) input feature ultra-low loading for ease of interfacing. The eight bit-data latch, controlled by the latch enable input, is static and level sensitive. When ($\overline{LE}$) is low, all the latches become transparent and the output changes as the bit pattern changes on the data bus. When the latch enable returns to its high state, the last set of inputs are held by the latch and a unique output corresponding to the binary word in the latch is produced. While the latch enable is high, the latch inputs represent a high impedance load on the data bus and changes on the data bus have no effect on the DAC output.

The digital logic input for the NE5018 and NE5118 series DAC's utilize a differential input logic system with a threshold level of + 1.4 volts with respect to the voltage level on the digital ground pin (Pin 1).
To be compatible with microprocessors, the DAC should respond in as short a period as possible to insure full utilization of the μP and I/O data bus lines. Figure 2 gives the typical timing requirements of the latch circuits in the NE5018 and NE5118.

The voltage levels on the data bus should be stable for approximately 150ns before latch enable returns to high level. The timing diagram shows 100ns is required for set-up time and the information on the data lines should remain valid for another 50ns.

REFERENCE INTERFACE

The NE5018 and NE5118 contain an internal bandgap voltage reference which is designed to have a very low temperature coefficient and excellent long term stability characteristics.

The internal bandgap reference (1.23V) is buffered and amplified to provide the 5 volt reference output. Providing a V_{REF} (ADJ) (pin 12) allows easy trimming of the reference output (pin 13). Use of a 10K pot and series resistor, as shown in Figure 3, adjusts the gain of the buffer amplifier therefore varying the output reference voltage level.

This network can then be used as a full scale output adjust. A variation in the V_{REF} OUT of $\sim$.8V, results in a corresponding 1.6V variation in the full scale output. This is more than adequate since the untrimmed V_{REF} OUT is typically within 200mv of the nominal 5 volts. The V_{REF} OUT will provide a maximum of 5mA drive and can be used as a reference voltage for other system components, if required.

Since a potential need exists to use the NE5018 and NE5118 as multiplying DAC's, the V_{REF} is not connected internally, allowing the use of external reference sources. To utilize the internal reference, the V_{REF} OUT (pin 13) must be jumper connected to the V_{REF} IN (pin 14). This also makes it possible to use a common reference for other D/A or A/D circuits in a system.

INPUT AMPLIFIER OF THE NE5018

The DAC reference amplifier has been designed to eliminate the need for compensation when operating from the internal reference or from an external reference which is buffered by an op amp or low impedance

INTERFACING TO A μPROCESSOR

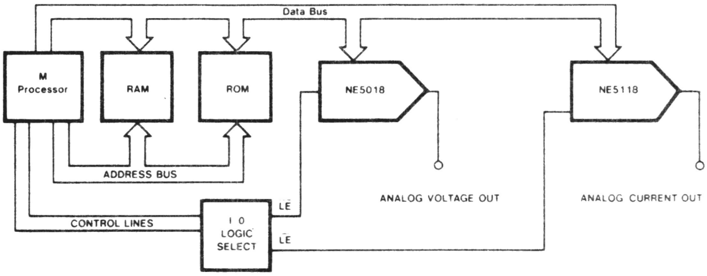


Figure 1

LATCH ENABLE ($\overline{LE}$) TIMING DIAGRAM for the NE5018 and NE5118

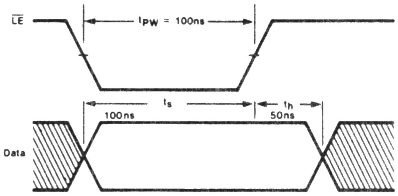


Figure 2

source. Compensation is required, however, when operating from a high impedance source. The addition of an external resistance reduces the phase margin of the amplifier making if less stable. Compensation, when required, is a single capacitor from pin 16 to ground.

Figure 4 details the input reference amplifier and current ladder. The voltage to current converter of the DAC amp will generate a 1mA reference current through Q_R with a 5 volt V_{REF}. This current sets the input bias to the ladder network. Data bit 7 (DB_7) Q_7, when turned on, will mirror this current and will contribute 1mA to the output. DB_6 (Q_6) will contribute 1/2 of that value or .5mA, and so on. If all bits are on, the output current will be 2mA - 1 LSB. The full scale V_{OUT} will be ($I_{OUT}R_S$) or (2mA - 1 LSB × 5K) = (10V - 1 LSB) = 9.961V. The overall input/output expression for the NE5018 is:

$$V_{OUT} = 2V_{REF} \times \left(\frac{DB7}{2} + \frac{DB6}{4} + \frac{DB5}{8} + \frac{DB4}{16} + \frac{DB3}{32} + \frac{DB2}{64} + \frac{DB1}{128} + \frac{DB0}{256}\right)$$

The minimum current for the ladder network to be operative in the linear region is 100μA. Therefore the minimum V_{REF} input is 500mV. The slew rate of the reference amplifier is typically .7V/μs without compensation. The input structure of the NE5118 is slightly different and will be discussed in greater detail later. Q_T provides a termination for the R-2R ladder network and does not contribute to I_{OUT}.

OUTPUT INTERFACE OF THE NE5018

The NE5018 has an internal op amp which provides a voltage output, while the NE5118 is a current output device. The NE5018 output op amp is a two stage design with feed-forward compensation. Having a slew rate 10V/μs, it provides a voltage output from 0 to 10V (±.2%) typically within 2μs (the time allowed for the output voltage to settle to within 1/2 LSB). Compensation must be provided externally as shown in Figure 5.

The addition of the optional diode between the summing node (Pin 20) and ground prevents the DAC current switches from driving the op amp into saturation during large signal transitions which would increase the settling time.

Zero adjust circuits such as the one shown in Figure 5 may also be connected to the summing node to provide a means to zero the output when all zeros are present on the input. Not all applications require a zero adjust circuit since the untrimmed zero scale is typically less than 5mV. Excess stray capacitance at the sum node of the output op amp may necessitate the use of a feedback capacitor from V_{OUT} to the sum node (C_{FF}) to insure stability of the op amp. Typical values of C_{FF} range from 15 to 22pF. The rated load of the op amp is ~ 2Kohm. For stability, the load capacitance should be minimized (50pF max).

REFERENCE ADJUST CIRCUIT

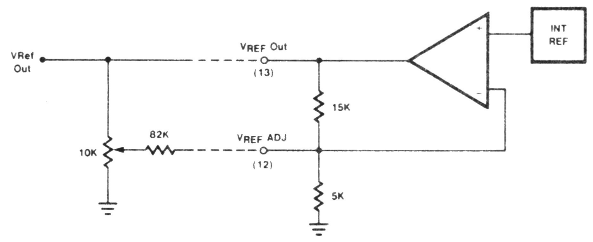
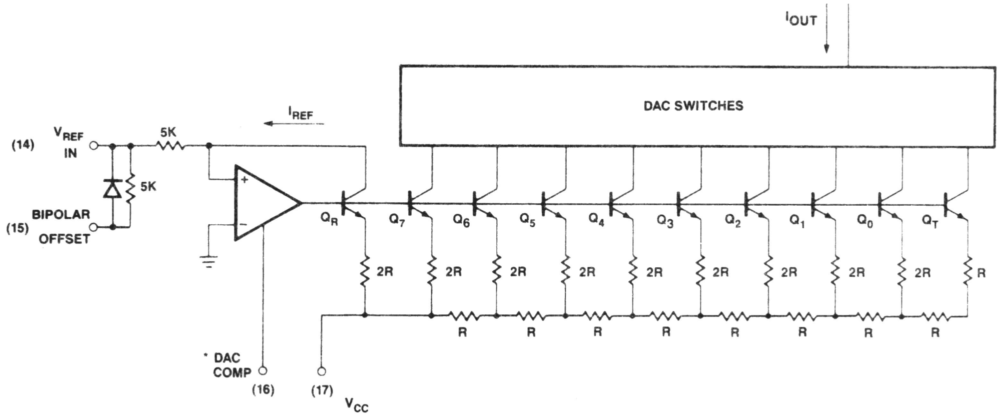


Figure 3

R - 2R LADDER NETWORK DEVELOPS A SCALED REFERENCE CURRENT VALUE INTO THE DAC SWITCHING NETWORK



NOTE
DAC compensation may be required if V_{REF} resistance exceeds 10K ohm.

Figure 4

MICROPROCESSOR COMPATIBLE DACs

MODES OF OPERATION OF THE NE5018

The NE5018 has two basic modes of operation: unipolar and bipolar. When operating in the unipolar mode the output range is 0 to + 10 volts. To change from unipolar to bipolar operation the bipolar offset pin is connected to the summing node. This provides the 5 volt offset required for this mode of operation. The output now will have a range from − 5 to + 5 volts. Figure 6 details the connection of the NE5018 in the bipolar mode of operation.

With the bipolar offset pin (15) connected to the sum node pin (20), it forms a unity gain inverter with an input of + V_{REF}. The bipolar offset develops an I_{REF} current through the internal 5K resistor. This current is then fed to the sum node of the output amplifier where it is summed with the current output of the DAC ladder network. Assume for the moment that the current output of the ladder network is 0mA. With a V_{REF} equal to + 5 volts, I_{REF} is 1mA and the output of the op amp is converted to − 5V. If the DAC switches are now set to full scale, the current from the DAC ladder is 2mA. This is summed against the 1mA I_{REF} and causes the output of the op amp to swing from − 5V to + 5 volts.

$(I_{DAC} - I_{REF})\,5K = (2mA - 1mA)\,5K = +5$ volts

Since the bipolar offset resistor is monolithic, tracking with the 5K feedback resistor of the output amplifier is excellent.

Note that the bipolar offset pin could not be used when using the DAC in a multiplier application since the V_{OUT} would reflect an inverted input signal.

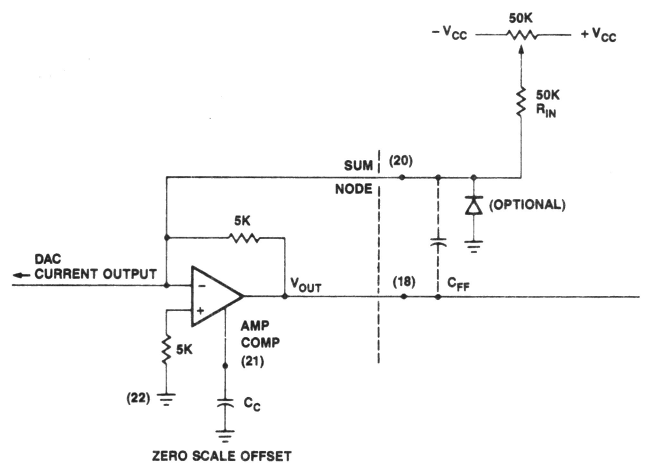


Figure 5

BIPOLAR OUTPUT

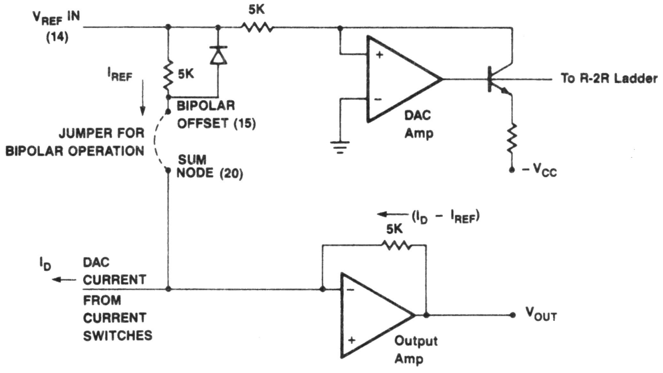


Figure 6

NOTES ON THE NE5118 CURRENT OUTPUT DAC

The basic operation of the NE5118 current output DAC is the same as the NE5018. The current output structure allows the user to provide a programmable current sink (I_{OUT} max of 2mA). Several jumper options provide a variety of operational modes. Figure 7 is a block diagram of the NE5118. The input logic and V_{REF} portions are identical to the NFE5018.

REFERENCE INPUT AMPLIFIER

The characteristics of the reference input amplifier are identical to the NE5018; however, extended versatility of the input structure allows for both current (via pin 14) or voltage (via pin 15) reference inputs.

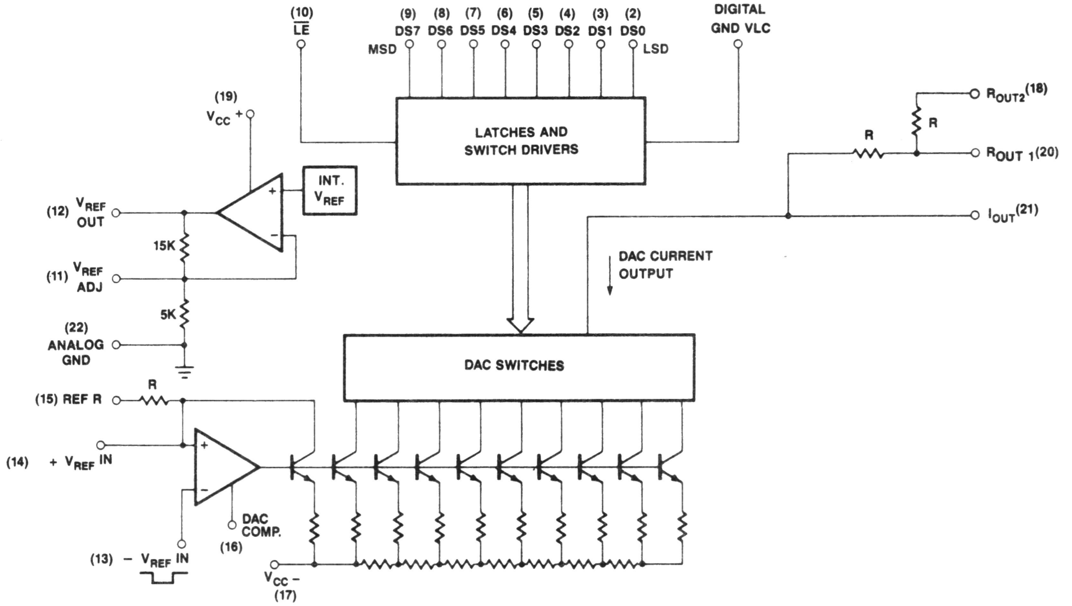
The maximum DAC output current is 2mA. The DAC has an internal gain of 2, limiting the maximum usable input current to 1mA. (Note: The absolute maximum input current should be limited to 5mA to prevent damage to the input reference amplifier). Figure 8 shows the basic operating mode of the NE5118 using an external current reference resistor (R_1) and a positive reference voltage.

This voltage can be provided by either an internal or external reference voltage. Figure 9 shows a typical connection using a voltage input directly via pin 15.

Besides a reduced parts count, use of the internal R_{REF} provides excellent tracking characteristics with the R_{OUT} resistor (pin 20) when developing a high slew rate voltage output. The negative V_{REF} input must be returned to ground directly or through R_2. R_2 is optional and is used to cancel minor errors developed by the input bias currents of the reference amplifier ($R_2 = R_1$). A negative voltage can be the reference by using the − V_{REF} input pin as shown in Figure 10.

The positive V_{REF} is returned to ground via R_{IN} (pin 15). As with the NE5018, a compensation capacitor on Pin 16 is not required if the V_{REF} is supplied by a low impedance source.

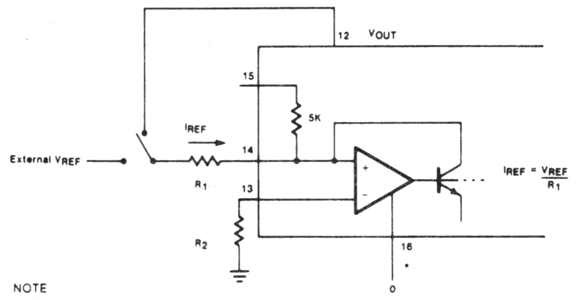
BLOCK DIAGRAM


(10)
LE
(9) (8) (7) (6) (5) (4) (3) (2)
DS7 DS6 DS5 DS4 DS3 DS2 DS1 DS0
MSD
LSD
DIGITAL
GND VLC
(19)
V_{CC} +
LATCHES AND
SWITCH DRIVERS
INT.
V_{REF}
(12) V_{REF} OUT
15K
(11) V_{REF} ADJ
5K
(22) ANALOG GND
R
(15) REF R
(14) + V_{REF} IN
DAC COMP.
(16)
(13) − V_{REF} IN
V_{CC} −
(17)
R_{OUT2} (18)
R
R
R_{OUT} 1(20)
I_{OUT} (21)
DAC CURRENT
OUTPUT
DAC SWITCHES

All R values are equal 5kΩ and are thermally matched.

Figure 7

POSITIVE I_{REF}


12
V_{OUT}
15
5K
I_{REF}
External V_{REF}
14
R_1
13
R_2
16
0
$I_{REF} = \frac{V_{REF}}{R_1}$

NOTE
DAC compensation

Figure 8

OUTPUT STRUCTURE

The output of the NE5118 is a current sink with a capacity of 2mA (full scale) capable of settling to .2% in 200ns. Internal bias and feedback resistors are also made available to ease the designer's task of interfacing.

Figure 11 shows the NE5118 using a current to voltage converter at the output to provide a high slew rate voltage output. Using the NE538 as shown can provide 60V/µs slew rate output. The diode at the inverting node of the op amp improves the response time by preventing saturation of the op amp during large signal transitions. The feedback resistor R_{OUT1} (pin 20) is provided internally; this provides excellent thermal tracking characteristics with the R_{REF} on the input.

Bipolar operation can be accomplished by connecting the $V_{REF\ OUT}$ (Pin 12) to the R_{OUT} resistor (Pin 20)(Figure 12). The principal is the same as the NE5018 bipolar operation. The internal resistors exhibit excellent thermal tracking characteristics.

An alternate method of bipolar output operation is shown in Figure 12. The R_{REF} and R_{OUT} set up a current to voltage converter while two (2) external resistors provide a bipolar offset. R_{EXT_1} and R_{EXT_2} should have similar thermal tracking characteristics.

The NE5118 can provide a voltage output directly when driving a high impedance load as shown in Figure 13. With a full scale current of 2mA, pin 20 tied to +10V and a digital input of zero, the high impedance load will see +10V. For a full scale digital input, the load will see 0 volts. Since the load and the internal resistor form a voltage divider, their ratio determines full scale accuracy.

By connecting the R_{OUT} resistor (pin 20) to ground (Figure 13), the output voltage seen by the load ranges from 0 volts as zero scale to −10 volts as full scale. Only a few of the many possible output configurations have been shown to demonstrate the NE5118 flexibility.

CIRCUIT EXAMPLES

Now that the basics of the NE5018 and the NE5118 have been discussed, let's examine some specific circuits. Figure 14 is a microprocessor controlled programmable gain amplifier, using the NE5018. The V_{REF} output is fed to the non-inverting input to a differential amplifier. $R_1 + R_2$ set the differential gain to 0.5. This places 2.5V DC bias on the V_{REF} input. R_2 can be made adjustable to precisely control the DC reference input. The analog input is fed to the inverting input of the differential amplifier with a gain of unity. An input of ± 2V will provide a ± 4 volt output full scale. With a maximum input of ± 2 volts. V_{REF} IN will vary from .5 volts to 4.5 volts. The current ladder is always kept in the linear operating range and the output will not become distorted.

No compensation is required for the DAC reference amplifier since the $V_{REF\ IN}$ is fed from a low impedance source. With a compensation cap of 30pF on the output amplifier, the frequency response of the output is linear to at least 20kHz with less than .1% distortion with an input amplitude of 1V p.p. The NE5018 is seen by the μ processor as an I/O device.

In Figure 15, the N5018 and NE5118 provide a method of summing two digital words of equal weight and generating a voltage output. The latch enable feature of both devices direct connection to a data bus, using address decoding. These devices greatly reduced the total component count required to perform this operation.

The reference voltage is common to both DAC's, being provided by the NE5018. The bipolar offset resistor of the NE5018 provides the 1mA current reference for the NE5118. Using the internal resistor of the NE5018 to develop the reference current enhances the thermal tracking since the current to voltage resistor of the output op amp is also in the NE5018. Both DAC's can be addressed by a μprocessor using an address decoder to select DAC A or DAC B.

Figure 16 is a schematic of the NE5118 and NE527 as a high speed programmable limit sensor (or A/D converter). A 4.8 volt zener diode is used on the comparator input to insure the input voltage range of the comparator is not exceeded. The outputs of the NE527 comparator are complementary, easing the logic interface requirement. If the strobe function is not used, the strobe inputs should be tied high, through a 10KΩ resistor.

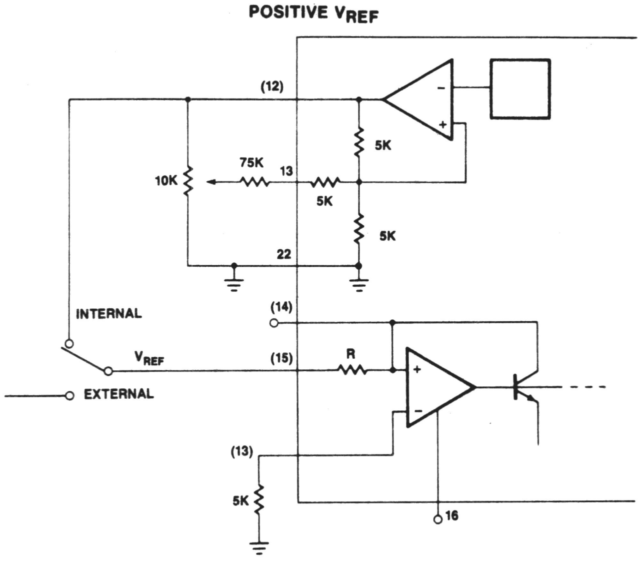

POSITIVE VREF
(12)
5K
75K
13
10K
5K
5K
22
INTERNAL
(14)
VREF
(15)
R
EXTERNAL
(13)
5K
16

Figure 9

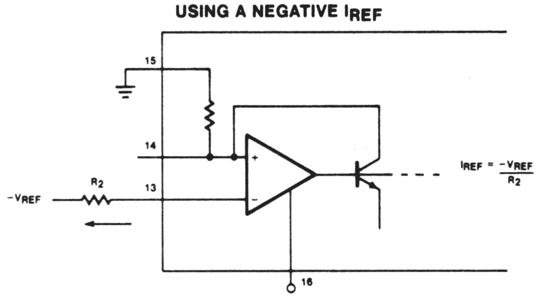

USING A NEGATIVE IREF
15
14
R2
13
-VREF
IREF = -VREF/R2
16

Figure 10

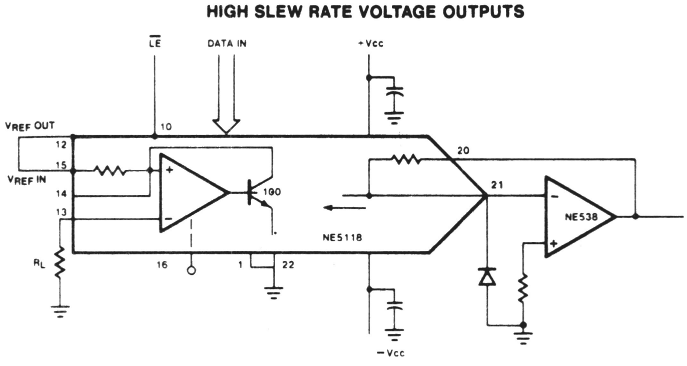

HIGH SLEW RATE VOLTAGE OUTPUTS
LE
DATA IN
+Vcc
VREF OUT
10
12
15
VREF IN
14
13
100
20
21
NE538
NE5118
RL
16
1
22
-Vcc

Figure 11

BIPOLAR OPTIONS OF THE NE 5118

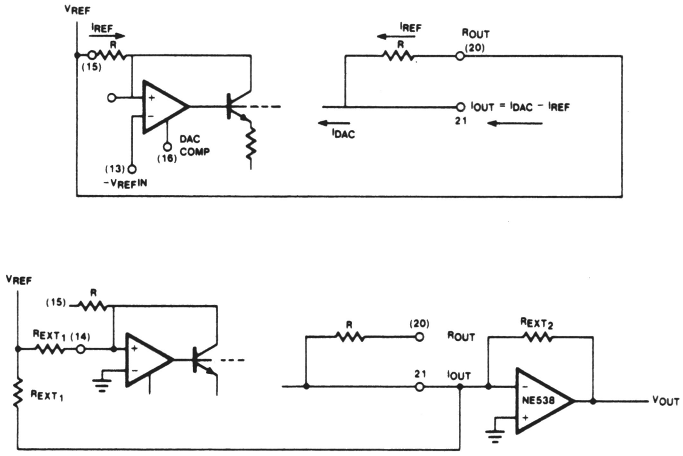

VREF
IREF
R
(15)
+
−
DAC COMP
(16)
(13)
−VREF IN
IREF
R
ROUT
(20)
IOUT = IDAC − IREF
21
IDAC
VREF
R
(15)
REXT1 (14)
REXT1
R
(20)
ROUT
21
IOUT
REXT2
NE538
VOUT

Figure 12

+10 TO 0 VOLTS **0 TO −10 VOLTS**

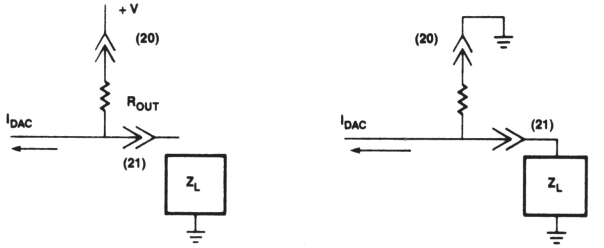

+V
(20)
ROUT
IDAC
(21)
ZL
(20)
IDAC
(21)
ZL

Figure 13

PROGRAMMABLE GAIN AMPLIFIER

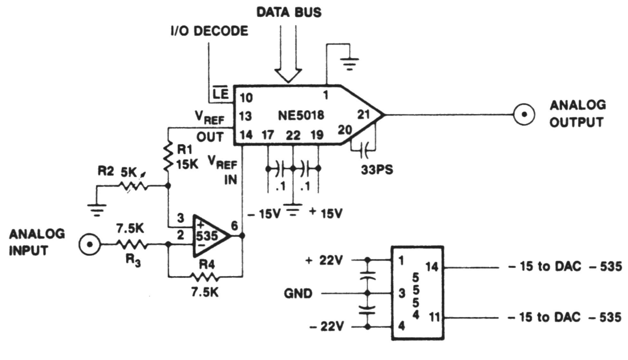

DATA BUS
I/O DECODE
LE
10
1
VREF
13
NE5018
21
OUT
14 17 22 19
20
R1
15K
VREF
IN
.1
.1
33PS
R2 5K
−15V
+15V
3
2
535
6
ANALOG INPUT
7.5K
R3
R4
7.5K
ANALOG OUTPUT
+22V
GND
−22V
1
3
4
5554
14
11
−15 to DAC −535
−15 to DAC −535

Figure 14

ANALOG SUMMATION WITH DIGITAL INPUTS

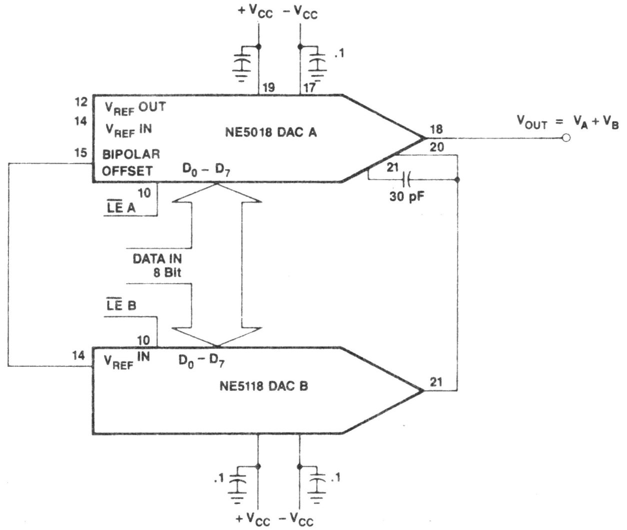

+V$_{CC}$
−V$_{CC}$
.1
19
17
12
14
15
V$_{REF}$ OUT
V$_{REF}$ IN
BIPOLAR OFFSET
NE5018 DAC A
D$_0$ − D$_7$
10
LE A
18
20
21
30 pF
V$_{OUT}$ = V$_A$ + V$_B$
DATA IN 8 Bit
LE B
10
14
V$_{REF}$ IN
D$_0$ − D$_7$
NE5118 DAC B
21
.1
.1
+V$_{CC}$
−V$_{CC}$

Figure 15

PROGRAMMABLE LIMIT COMPARATOR

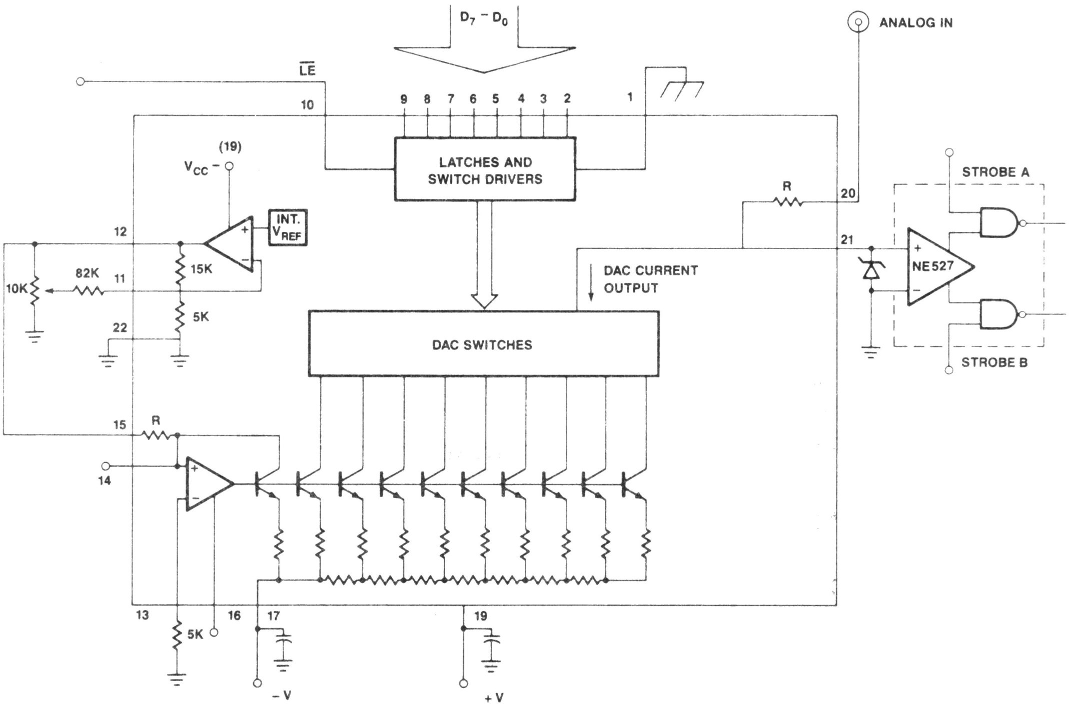

D$_7$ − D$_0$
ANALOG IN
LE
10
9 8 7 6 5 4 3 2
1
(19)
V$_{CC}$ −
LATCHES AND SWITCH DRIVERS
R
20
STROBE A
12
INT. V$_{REF}$
21
NE527
82K
11
15K
10K
DAC CURRENT OUTPUT
5K
22
DAC SWITCHES
STROBE B
15
R
14
13
16
17
19
5K
−V
+V

Figure 16

LED DECODER DRIVERS: USING THE NE587 AND NE589 AN112

LED DECODER DRIVER NE587 and 589

The NE587 and 589 are latchable decoder drivers for L.E.D. displays. Figure 1 provides a summary of their features.

NE 587/589 LED DRIVERS

- **Strobed Latch**
- **Inputs compatible with NMOS, CMOS, DMOS, TTL**
- **Single 5 volt supply**
- **Constant Current Outputs**
- **Inputs are compatible with microprocessor bus**
- **BCD Inputs—Hexadecimal Outputs**
- **Programmable segment current**

Figure 1

The programmable constant current supplies (fixed or adjustable) are essentially independent of output voltage, power supply voltage, and temperature.

The data (BCD) and $\overline{LE}$ (latch enable) inputs are low loading and thus are compatible with a data bus system.

Figure 2 shows a block diagram of the NE587. Seven segment decoding is implemented using a ROM so that alternate decoding fonts can be made available.

L.E.D. Drivers and Power Dissipation Consideration

The following discussion refers to the NE587, but is also applicable for the 589.

LED displays are power hungry devices, and, inevitably, somewhat inefficient in their use of the power supply necessary to drive them. Duty cycle control does afford one way of improving display efficiency, provided that the LEDs are not driven too far into saturation, but the improvement is marginal. Operation at higher peak currents has the added advantage of giving much better matching of light output, both from segment-to-segment and digit-to-digit.

When designing a display system, particular care must be taken to minimize power dissipation within the IC display driver. Since the NE587 output is a constant programmed current source, all the remaining supply voltage, which is not dropped across the LED (and the digit driver, if used) will appear across the output of the NE587. Thus the power dissipation in the NE587 will go up sharply if the display power supply voltage rises. Clearly, then, it is good design practice to keep the display supply voltage as low as possible consistent with proper operation of the output current sources. Inserting a resistor or diode in series with the display supply is a good way of reducing the power dissipation within the integrated circuit segment driver, although, of course, total system power remains the same.

Power dissipation within the NE587 may be calculated as follows. Referring to Figure 3, the two system power supplies are V_{CC} and V_S. In many cases, these will be the same voltage. Necessary parameters are:

• V_{CC}	Supply voltage to driver
• V_S	Supply voltage to display
• I_{CC}	Quiescent supply current of driver
• I_{SEG}	LED segment current
• V_F	LED segment forward voltage at I_{seg}
• K_{DC}	% Duty cycle

V_F, the forward LED drop, depends upon the type of LED material (hence the color) and the forward current. The actual forward

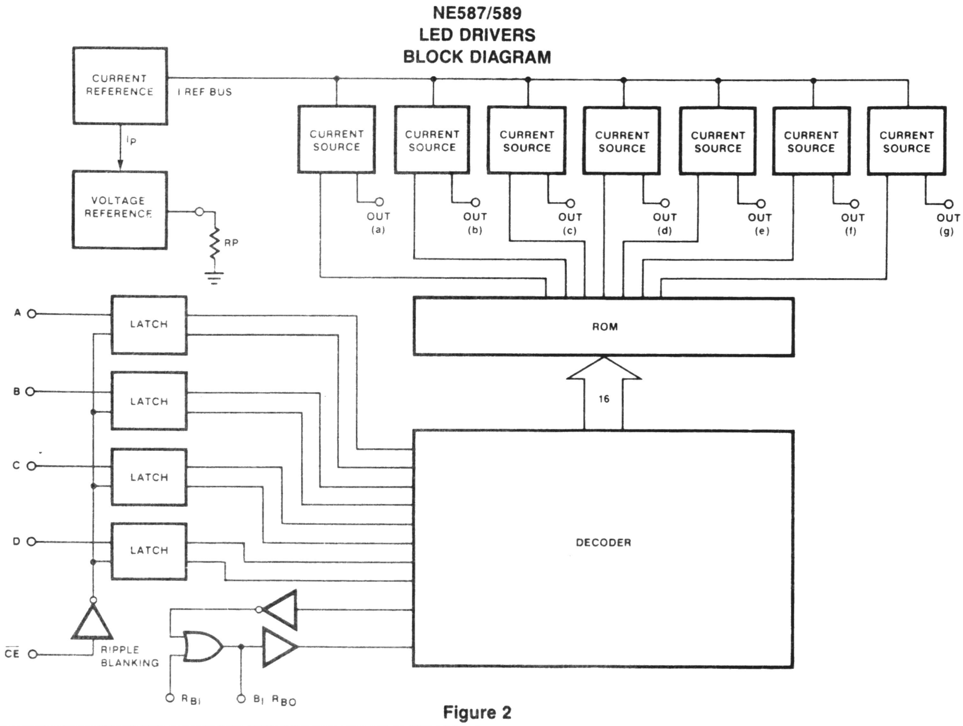
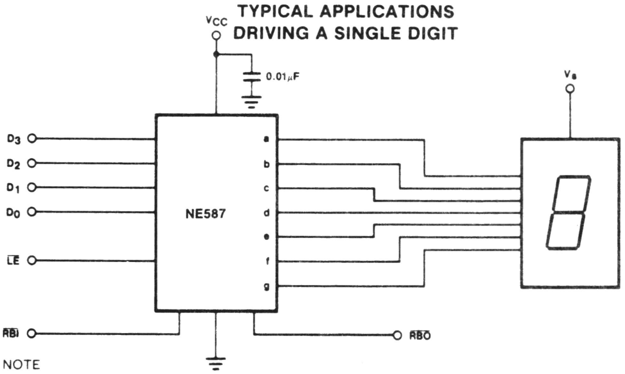

NE587/589
LED DRIVERS
BLOCK DIAGRAM

Figure 2

TYPICAL APPLICATIONS DRIVING A SINGLE DIGIT



NOTE
Decoupling capacitor on VCC should be 0.01µF ceramic

Figure 3

MAXIMUM POWER DISSIPATION VS TEMPERATURE

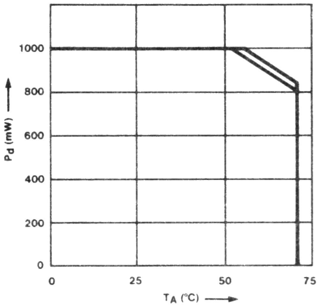


Figure 4

voltage drops should be obtained from the LED display manufacturers literature for the peak segment current selected. However, approximate voltages at nominal rated currents are:

Red	1.6 to 2.0V
Orange	2.0 to 2.5V
Yellow	2.2 to 3.5V
Green	2.5 to 3.5V

These voltages are all for single diode displays. Some early red displays had 2 series LEDs per segment, hence the forward voltage drop was around 3.5V.

Thus a maximum power dissipation calculation when all segments are on, is:

$$P_d = V_{CC} \times I_{CC} + (V_S - V_F) \times 7 \times I_{seg} \times K_{DC} \text{ mW} \quad (1)$$

Assuming $V_S = V_{CC} = 5.25V$
$V_F = 2.0V$
$K_{DC} = 100\%$
$I_{seg} = 30mA$

$$\begin{aligned} \text{Pd max} &= 5.25 \times 50 + 3.25 \times 7 \times 30 \text{ mW} \\ &= 945 \text{ mW} \end{aligned}$$

However, the average power dissipation will be considerably less than this. Assuming 5 segments are on (the average for all output code combinations), then

$$\begin{aligned} P_{d\,av} &= 5.0 \times 30 + 3.00 \times 5 \times 25 \text{ mW} \\ &= 525 \text{ mW} \end{aligned}$$

Operating temperature range limitations can be deduced from the power dissipation graph in Figure 4.

However, a major portion of this power dissipation ($P_{d\,max}$) is because the current source output is operating with 3.25V across it. In practice, the outputs operate satisfactorily down to 0.5V, and so the extra voltage may be dropped external to the integrated circuit.

Suppose the worst case V_{CC}/V_S supply is 4.75 to 5.25V, and that the maximum V_F for the LED display is 2.25V. Only 2.75V is required to keep the display active, and hence 2.0V may be dropped externally with a resistor from V_{CC} to V_S. The value of this resistor is calculated by using equation 2.

$$R_S = \frac{V_{DROP}}{I_{seg} \times \# \text{ of seg}} \quad (2)$$

or $R_S = \dfrac{2.0}{7 \times I_{seg}} \approx 10\Omega$ (1/2 W rating)

assuming worst case I_{seg} of 30mA
Hence now:

$$\begin{aligned} P_{d\,max} &= V_{CC} \times I_{CC} + (V_S - V_V - R_X \times 7 \times I_{seg}) \times 7 \times I_{seg} \times K_{DC} \\ &= 5.25 \times 50 + 1.25 \times 7 \times 30\text{mW} \\ &= 525\text{mW} \end{aligned} \quad (3)$$

and $P_{d\,av} = 5.0 \times 30 + 1.25 \times 5 \times 25$
$= 306$mW

If a diode (or 2) is used to reduce voltage to the display, then the voltage appearing across the display driver will be independent of the number of "ON" segments and will be equal to

$V_S - V_F - nV_d$, $V_D \approx 0.8V$

Where n is the number of diodes used, and so power dissipation can be calculated in a similar manner.

In a multiplexed display system, the voltage drop across the digit driver must also be considered in computing device power dissipation. It may even be an advantage to use a digit driver which drops an appreciable voltage, rather than the saturating PNP transistors shown in Figure 5. For example a Darlington PNP or NPN emitter follower may be preferable. Figure 6 shows the NE591 as the digit driver in a multiplexed display system. The NE591 output drops about 1.8V which means that the power dissipation is evenly distributed between the two integrated circuits.

Where V_S and V_{CC} are two different supplies, the V_S supply may be optimized for minimum system power dissipation and/or cost. Clearly, good regulation in the V_S supply is totally unnecessary, and so this supply can be made much cheaper than the regulated 5V supply used in the rest of the

4-DIGIT MULTIPLEXED LED DISPLAY

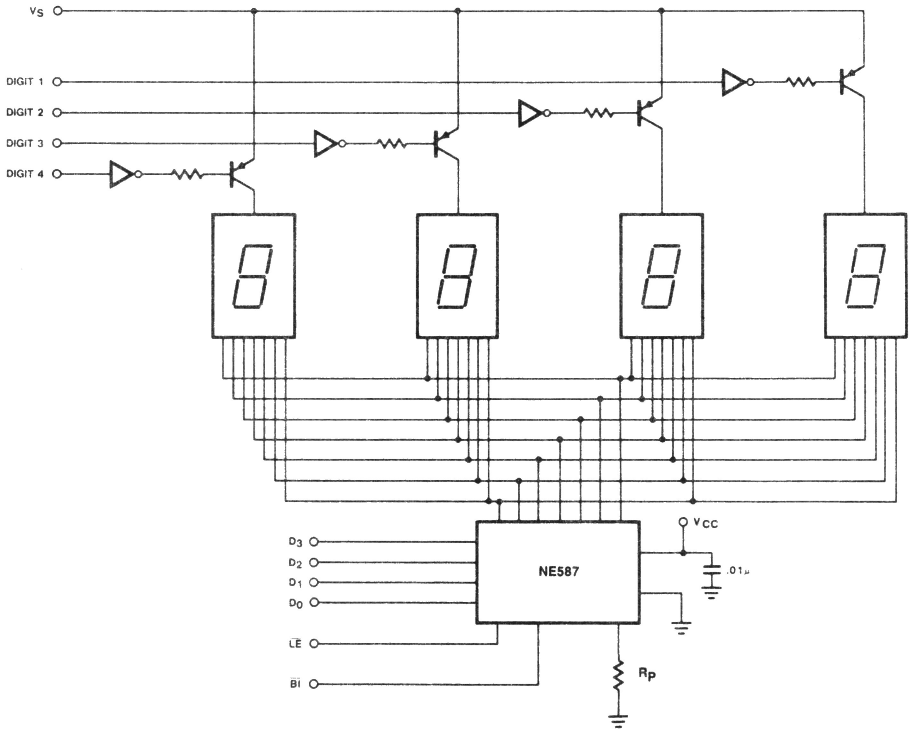

VS
DIGIT 1
DIGIT 2
DIGIT 3
DIGIT 4
D3
D2
D1
D0
$\overline{LE}$
$\overline{BI}$
NE587
VCC
.01μ
RP

Figure 5

LED DECODER DRIVERS: USING THE NE587 AND NE589

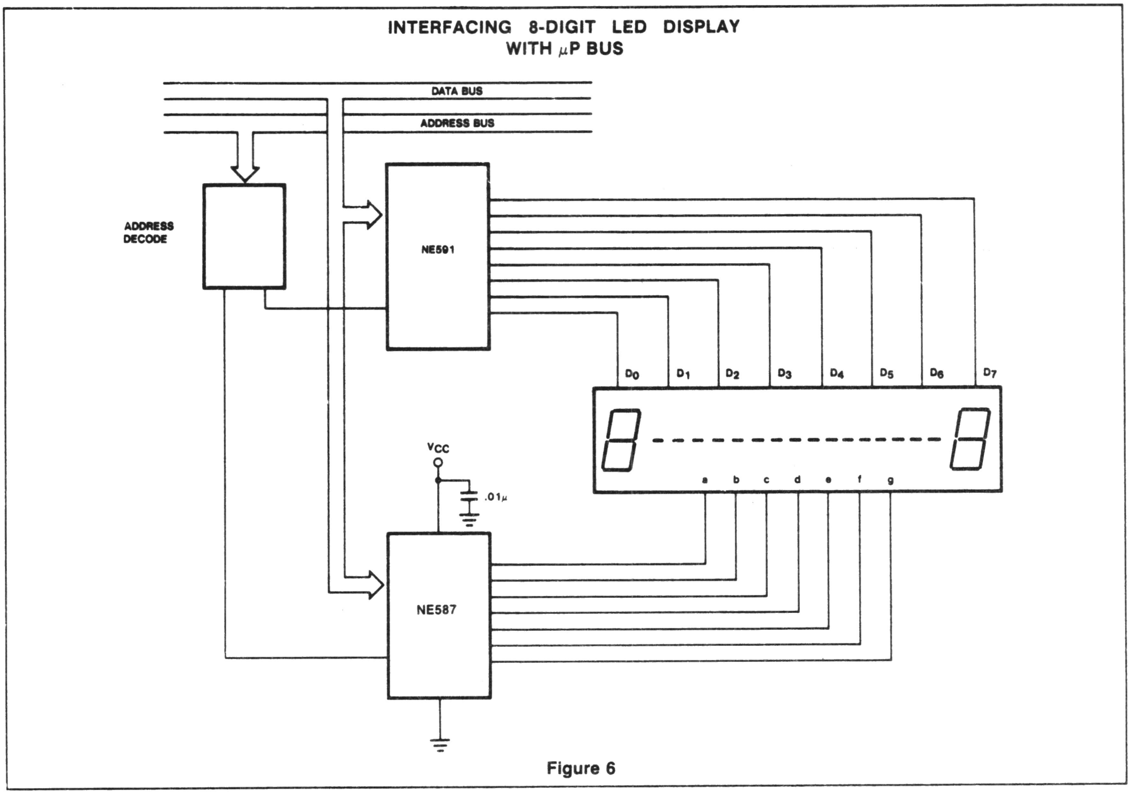


Figure 6

system. In fact a simple unsmoothed full-wave rectified sine wave works extremely well if a slight loss in brightness can be tolerated. A transformer voltage of about 3-4.5Vrms works well in most LED display systems. Waveforms are shown in Figure 7.

The duty cycle for this system depends upon V_S, V_F and the output characteristics of the display driver.

With

$V_S = 4.9V$ pk.
$V_F = 2.0V$

The duty cycle is approximately 60%.

V_S in this example was derived by the circuit shown in Figure 7. Remember that the forward voltage drop of the rectifying diode must be subtracted to arrive at the exact peak of the V_S voltage.

Figure 8 shows other typical application schemes for multiplexing LED diplays.

ADDRESSABLE PERIPHERAL DRIVERS SUPPORT μP-BASED SYSTEMS

The Signetics NE590 and NE591 addressable peripheral drivers (APDs) greatly facilitate interfacing a variety of support circuits to microprocessor based systems.

The APDs are designed to eliminate the need for many of the buffers, latches, TTL ICs, and discrete transistors currently needed to drive peripheral devices.

Figure 9 shows that each driver includes a set of input latches, a 1-of-8 demultiplexer, and a set of high current drive outputs together with the assorted chip enable and clear logic.

The low loading inputs of these drivers (typically $I_{IL} = 15\mu A$ and $I_{IH} = 1\mu A$) allow direct interfacing to the μP-bus. Eight addressable latches, which are addressed by a three bit binary code and (set/reset) by a single binary bit, allow storage of each output condition (ON/OFF), allowing the μP to continue processing after the APD has been addressed.

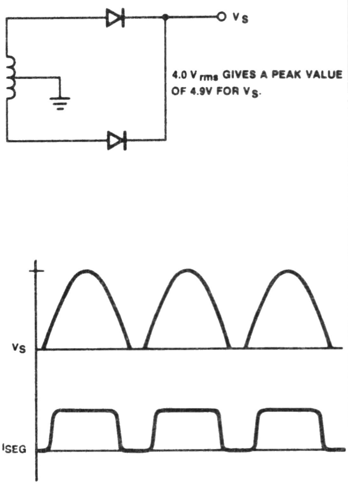
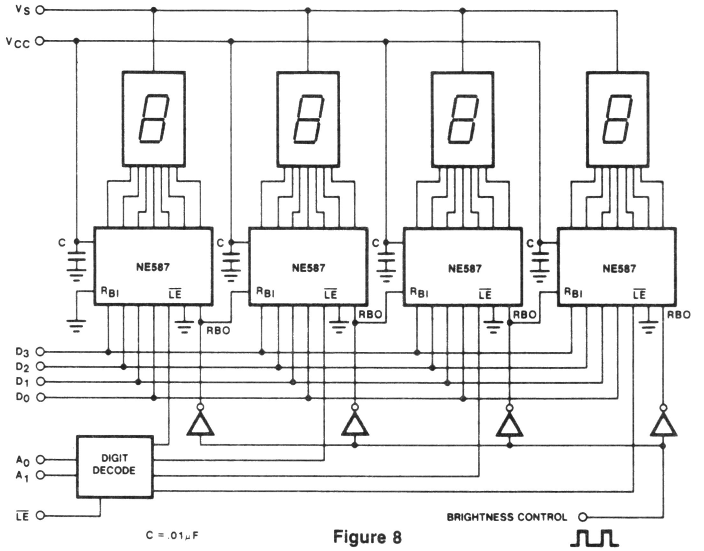


Figure 7

4-DIGIT DISPLAY WITH BRIGHTNESS CONTROL AND LEADING EDGE RIPPLE BLANKING.



V S
V CC
C
NE587
R BI
LE
RBO
D 3
D 2
D 1
D 0
A 0
A 1
DIGIT DECODE
LE
BRIGHTNESS CONTROL
C = .01µF

Figure 8

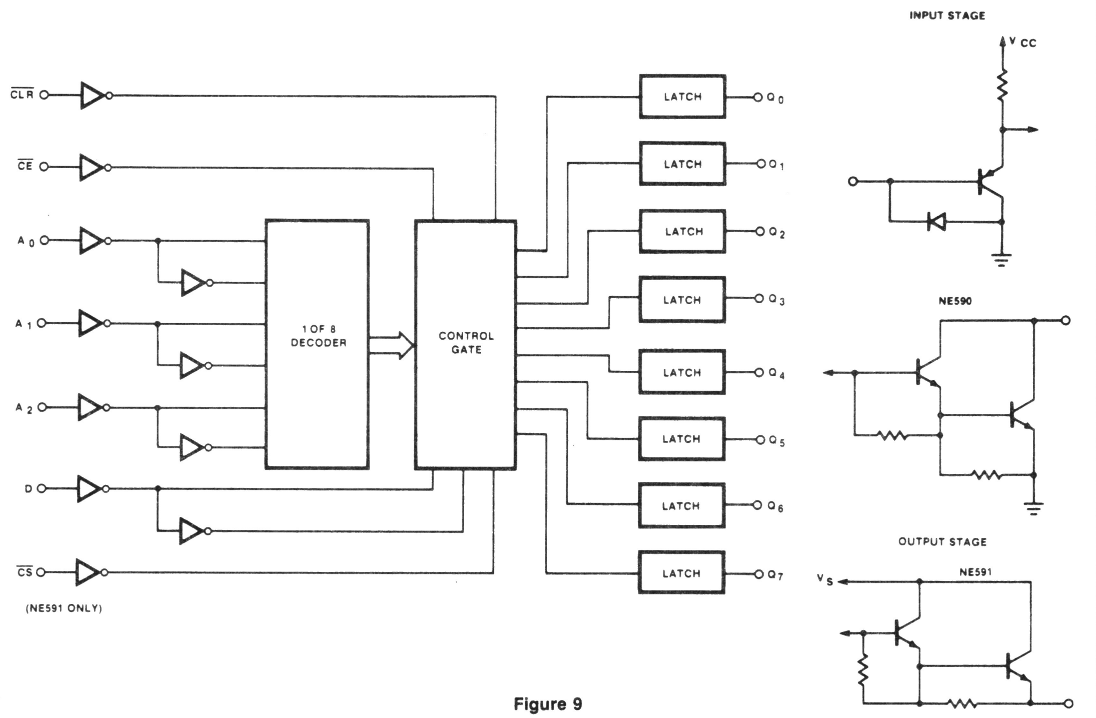
Driver selection is accomplished with a low active chip enable which may be derived from the I/O decoder common to all I/O devices. A low active master clear is also provided to reset all outputs simultaneously. This signal may be generated from the I/O decoder or set high when not required.

The high-current outputs of the drivers (250mA sinking with the NE590 and 250mA sourcing with the NE591) allows direct interfacing to relays, motors, lamps, LED's, and other devices or systems requiring high current drive capabilities.

Figure 10 demonstrates the use of APD's in a uP-based system. When driving LED displays, a single 8-bit word contains all the data required for defining both digit location and segment selection. The APD uses four bits—three to address one of 8 outputs and one to set the output to an ON or OFF state.

When using he NE590, ON refers to the output low state in which the output is

BLOCK DIAGRAM



INPUT STAGE
V CC
CLR
CE
A 0
A 1
A 2
D
CS
(NE591 ONLY)
1 OF 8 DECODER
CONTROL GATE
LATCH
Q 0
Q 1
Q 2
Q 3
Q 4
Q 5
Q 6
Q 7
NE590
OUTPUT STAGE
NE591
V S

Figure 9

MICROPROCESSOR BASED SYSTEM

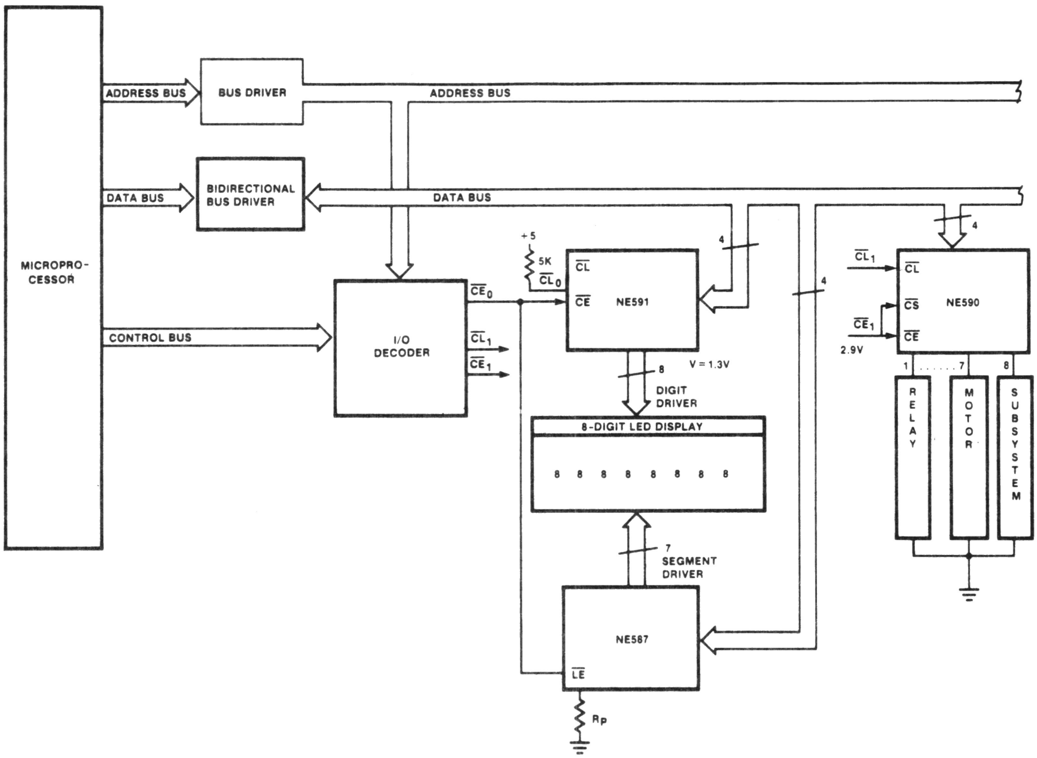

MICROPROCESSOR
ADDRESS BUS
BUS DRIVER
ADDRESS BUS
DATA BUS
BIDIRECTIONAL BUS DRIVER
DATA BUS
CONTROL BUS
I/O DECODER
CE0
CL1
CE1
+5
5K
CL0
CL
CE
NE591
4
4
4
8
V = 1.3V
DIGIT DRIVER
8-DIGIT LED DISPLAY
8 8 8 8 8 8 8 8
7
SEGMENT DRIVER
NE587
LE
Rp
CL1
CL
CS
NE590
CE1
CE
2.9V
1 7
8
RELAY
MOTOR
SUBSYSTEM

Figure 10

capable of sinking a maximum of 250mA. The clear ($\overline{CL}$) pin may be tied high and would normally not be required in this application.

The four remaining data bits are required by the NE589 which supplies segment data. These four BCD data bits are converted into seven-segment data used for driving the anodes of the LED's. Data is strobed into the latches by the LATCH ENABLE INPUT at the same time that information is being supplied to the NE590. Since the NE589 provides a constant current source, uniform brightness is obtained from each segment in the display. The NE589 is capable of supplying up to 50 mA/segment. Segment currents are set by a single programming resistor.

Figure 10 shows several devices connected to the NE591: a relay, a motor, and a D-C subsystem. Each device is selected in the same manner as the LED digits: that is, three bits are used to select the output and one bit is used to turn the output ON or OFF.

An output may be cleared in one of two ways:

1) By direct selection and clearing of the individual latch,
   or
2) By clearing all outputs through the use of the clear input.

The latter method does not require addressing.

The examples shown in Figure 10 clearly demonstrate the advantages that can be derived from using the NE590 and NE591 APDs in microprocessor-based systems. These devices provide easy interfacing and minimize the number of interfacing components; they also provide the logic interface to the microprocessor and the switch function and high-current drive required by the peripheral units.

USING THE MC1488/1489 LINE DRIVERS AND RECEIVERS AN113

LINE DRIVERS AND RECEIVERS

Many types of line drivers and receivers are available today. Each device has been designed to meet specific criteria. For instance, the device may be extremely wide band or be intended for use in party line systems. Some include built in hysteresis in the receiver while others do not.

The EIA Standard

The Electronic Industries Association has produced a set of specifications dealing with the transmission of data between data terminal and communications equipment. This is EIA Standard RS-232-C and delineates much information about signal levels and hardware configurations in data systems.

MC1488/1489

As line driver and receiver the MC1488 and MC1489 meet or exceed the RS-232 specification.

Standard RS-232 defines the voltage level as being from 5 to 15 volts with positive voltage representing a logic 0. The MC1488 meets these requirements when loaded with resistors from 3k to 7k ohms.

Output slew rates are limited by RS-232 to 30 volts per microsecond. To accomplish this specification the MC1488 is loaded at its output by capacitance as shown by the typical hookup diagram of Figure 1. A graph of slew rate vs output capacitance is given in Figure 2. For the standard 30V/μs a capacitance of 400pF is selected.

The short circuit current charges the capacitance with the relationship.

$$C = \frac{I_{SC} \Delta T}{\Delta V}$$

Where C is the required capacitor, I_{SC} is the short circuit current value, and $\Delta V/\Delta T$ is the slew rate.

Using the worst case output short circuit current of 12mA in the above equation, calculations result in a required capacitor of 400pF connected to each output to limit the output slew rate to 30V/μs in accordance with the EIA standard.

The EIA standard also states that output shorts to any other conductor of the cable must not damage the driver. Thus the MC1488 is designed such that the output will withstand shorts to other conductors indefinitely even if these conductors are at worst case voltage levels. In addition to output protection, the MC1488 includes a 300 ohm resistor to ensure that the output impedance of the driver will be at least 300 ohms even if the power supply is turned off. In cases where power supply malfunction produces a low impedance to ground, the 300 ohm resistors are shorted to ground also. Output shorts then can cause excessive power dissipation. To prevent this, series diodes should be included in both supply lines as pictured in Figure 3.

The companion receiver, MC1489, is also designed to meet RS-232 specifications for receivers. It must detect a voltage from ± 3 to ± 25 volts as logic signals but cannot generate an input differential voltage of greater than 2 volts should its inputs become open circuited. Noise and spurious signals are rejected by incorporating positive feedback internally to produce hysteresis. Featured also in the receiver is an external response node so that the threshold may be externally varied to fit the application. Figure 4 shows the shift in high and low trip points as a function of the programming resistance.

APPLICATIONS

The design of the MC1488 and MC1489 makes them very versatile with many possible applications. The MC1488 output current limiting enables the user to define the output voltage levels independent of supply voltages. Figure 5 shows the MC1488 as a TTL to MOS Translator, while Figures 6 and 7 illustrate TTL to HTL and TTL to MOS Translator.

The MC1489 response control node allows the user to modify the input threshold voltage levels. This is accomplished by adding a resistor between the response control pin and an external power supply. Figure 4 shows the shift thus provided. This feature and the fact that the inputs are designed to withstand ± 30 volts permit the use of the MC1489 for level translation as shown in the MOS to TTL translator of Figure 8. This feature is also useful for level shifting, as illustrated in Figure 9.

The response control node can also be used to filter out high frequency, high energy noise pulses. Figures 10 and 11 give typical noise pulse rejection curves for various sized external capacitors.

TYPICAL LINE DRIVER-RECEIVER APPLICATION

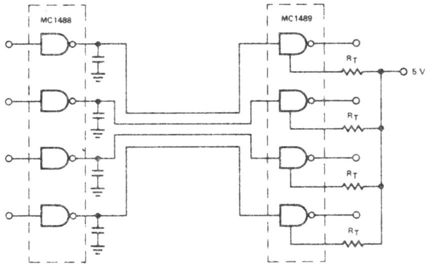

MC1488
MC1489
R_T
R_T
R_T
R_T
5 V

Figure 1

OUTPUT SLEW RATE vs. LOAD CAPACITANCE

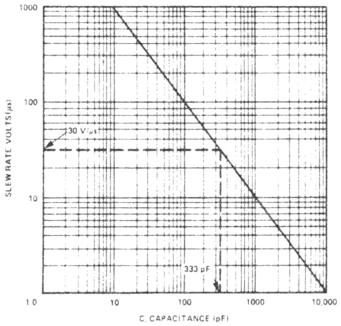


Figure 2

PROTECTION FROM POWER SUPPLY MALFUNCTION

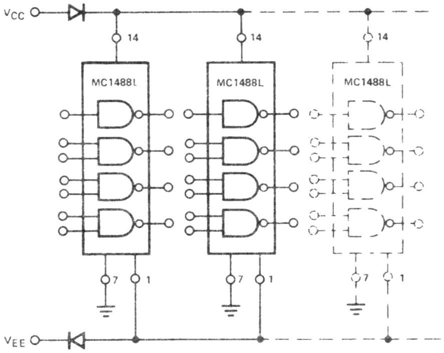

V_{CC}
14
14
14
MC1488L
MC1488L
MC1488L
7
1
7
1
7
1
V_{EE}

Figure 3

HYSTERESIS AS A FUNCTION OF PROGRAMMING RESISTANCE

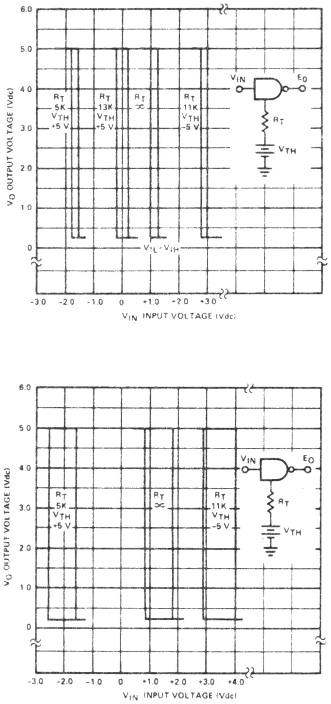


Figure 4

USING THE MC1488/1489 LINE DRIVERS AND RECEIVERS

TTL-TO-MOS TRANSLATOR

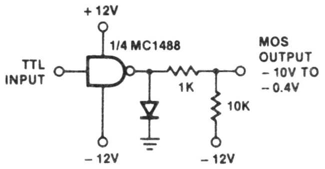

+12V
1/4 MC1488
TTL INPUT
MOS OUTPUT −10V TO −0.4V
1K
10K
−12V
−12V

Figure 5

TTL-TO-HTL TRANSLATOR

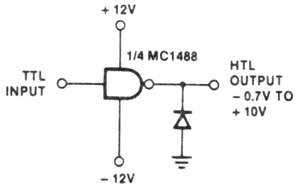

+12V
1/4 MC1488
TTL INPUT
HTL OUTPUT −0.7V TO +10V
−12V

Figure 6

TTL-TO-MOS TRANSLATOR

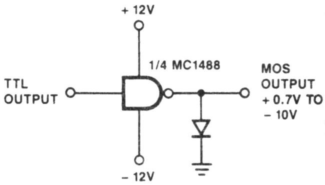

+12V
1/4 MC1488
TTL OUTPUT
MOS OUTPUT +0.7V TO −10V
−12V

Figure 7

MOS-TO-TTL TRANSLATOR

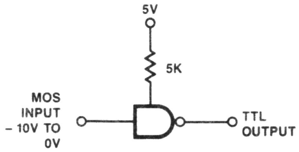

5V
5K
MOS INPUT −10V TO 0V
TTL OUTPUT

Figure 8

LEVEL SHIFTER

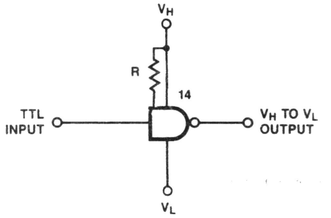

V_H
R
14
TTL INPUT
V_H TO V_L OUTPUT
V_L

Figure 9[1]

NOTE:
1. $V_2 \le 5V$; $3V \le V_H - V_L \le 10V$.

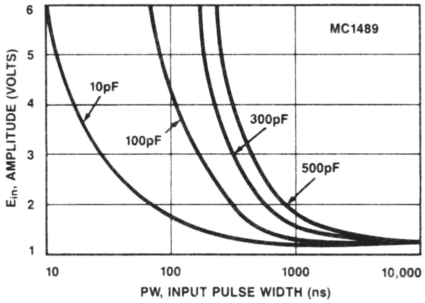


Figure 10. Turn-on Threshold versus Capacitance from response control pin to gnd

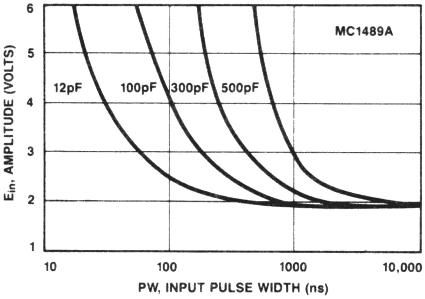


Figure 11. Turn-on Threshold versus Capacitance from response control pin to gnd

APPLICATIONS FOR THE NE521/522/527/529 AN116

COMPARATORS

Voltage compartors are high gain differential input—logic output devices. They are specifically designed for open loop operation with a minimum of delay time. Although variations of the comparator are used in a host of applications, all uses depend upon the basic transfer function of Figure 1. As shown, device operation is simply a change of output voltage dependent upon whether the signal input is above or below the threshold input. The threshold in this example is 0 volts.

Comparator inputs are customarily marked with plus or minus signs to indicate their polarity. For example the circuit of Figure 2 produces a logic 1 level when the non-inverting input is more positive than the reference voltage.

DEFINITIONS

Many similarities exist between operational amplifiers and the amplifier section of voltage comparators. In fact op amps can be used to implement the comparator function at low frequencies.

Thus, the characteristic definitions presented here are similar to those reveiwed for op amps.

Input Offset Voltage

As with operational amplifiers, the non-ideal comparator possesses some offset voltage. The definition differs slightly in that the output structure of comparators is digital rather than linear. Hence, input offset voltage is defined for comparators as the dc voltage required at the input to force the output to the logic threshold of ensuing devices (1.2 volts for TTL).

Input Offset Current

Imbalances of input bias current arise from small variances of the junction geometry of the differential input amplifier. As for op amps, the imbalance is referred to as input offset current.

Bias Current

As with op amps the input structure of comparators is usually a differential bipolar stage. Input bias current is the average of the two input currents.

Common Mode Range

When specifying voltage comparators one of the key parameters is common mode range, which is defined as the range of voltages over which both inputs can be varied simultaneously without abnormal output voltage transitions or device degradation. This parameter must be kept uppermost in the designer's mind because the reference and signal voltages become common mode signals at threshold. All ranges of input signals thus must be within the common mode range of the input amplifier.

Voltage Gain

Specifications of voltage gain refer to the overall gain of the device, the bulk of which occurs in the amplifier section.

In general, higher gains would be advantageous for resolving smaller input signals. Of course, the propagation delay suffers due to the more severe saturation of the transistors. Typical gains for TTL output devices are set for 5000 volts per volt. This gain provides 5 volts of output swing with 1mV input signal change for reasonable accuracy but does not contribute severely to the overload recovery delay.

Propagation Delay

Voltage comparisons of analog signals with a reference voltage usually require that the operation take as little time as possible. Long delays in the comparator cause a pulse position error at the output since the analog signal in the meantime has changed value. At low frequencies the delay is of small consequence but, at higher frequencies, transit time becomes intolerable. Design of voltage comparator devices includes, as a prime goal, the minimizing of transit times.

TRANSFER FUNCTION OF LM119

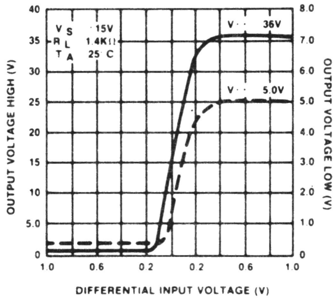


Figure 1

BASIC COMPARATOR CIRCUIT

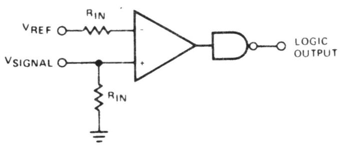


Figure 2

Propagation delay testing is done under worst case conditions. The recovery from saturation varies depending upon the initial state of the amplifier and the overdrive. Worst case conditions begin by applying a 100mV signal on the reference terminal. With no signal applied the amplifier is in saturation in one direction. A step input pulse on the signal line of 100mV ± V_{OS} will bring the amplifier to a threshold level. Propagation delay at this point is undefined since the output has not switched.

To attain output switching a small overdrive is necessary. Propagation delay is tested in a configuration such as Figure 3. The input is a step function of 100mV plus a specified excess or overdrive signal. This causes the amplifier to be exercised from saturation in one direction to saturation in the other for worst case propagation delay. Note that larger overdrive reduces delay time as can be seen in Figure 4. An overdrive of 5mV causes 12ns delay, whereas a 100mV overdrive improves transit time to only 6ns.

PROPAGATION DELAY TEST SETUP

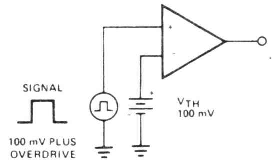


Figure 3

RESPONSE TIME FOR NE/SE521 COMPARATOR FOR VARIOUS INPUT OVERDRIVES

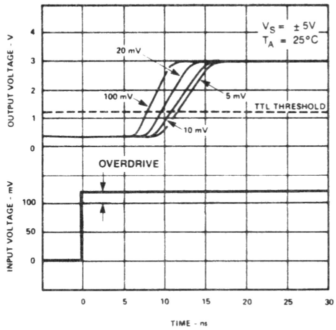


Figure 4

If the measurement were made without initial saturation (less than 100mV V threshold) the delay time would be less, due to the decreased storage times of unsaturated transistors.

STATE-OF-THE-ART

Comparator design has always been optimized for four basic parameters. They are:

1. High Speed
2. Wide Input Voltage Range
3. Low Input Current
4. Good Resolution

Unfortunately these four parameters are not compatible. For instance gain and input current can be improved by using thinner diffusions for higher beta, but only at the expense of input voltage range. Higher gain also means higher saturation for an increase in delay time. So it becomes obvious that older comparators such as the 710 were designed with the best compromises in mind using standard processing.

One method of improving overall response adds gold doping to the processing flow. The gold dopant causes a decrease in minority carrier lifetime which aids the recombination process and shortens the saturation recovery time. Unfortunately, the transistor beta is adversely affected by gold causing slightly higher bias and offset currents.

It was not until advent of the Schottky clamp that a vast improvement in speed without input degradation was possible. A very familiar term in the semiconductor industry, the Schottky barrier diode's (SBD) location is illustrated in Figure 5.

SCHOTTKY CLAMPED TRANSISTOR

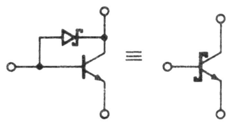


Figure 5

The Schottky clamped transistor is formed by parallelling the Schottky diode with the base-collector junction of the npn transistor. Without the clamp, as base drive is increased the collector voltage falls until hard saturation occurs. At this point the collector voltage is very near the emitter voltage, and stored charges in the junctions causes slow recovery from saturation after base drive has been removed. The forward voltage drop of the Schottky diode is 0.4 volts—less than the forward drop of silicon diodes. This difference in forward drop is used by placing the diode across the transistor base-collector junction. The Schottky diode becomes forward biased when the collector voltage falls 0.4 volts below the base voltage. Excess base drive is then shunted into the collector circuit prohibiting the transistor from reaching classic saturation. With almost no stored charge in either the SBD or the transistor, there is a large reduction in storage time. Thus, transistor switching time is significantly reduced.

A cross sectional area of the Schottky diode is shown in Figure 6.

SCHOTTKY CLAMPED TRANSISTOR GEOMETRY

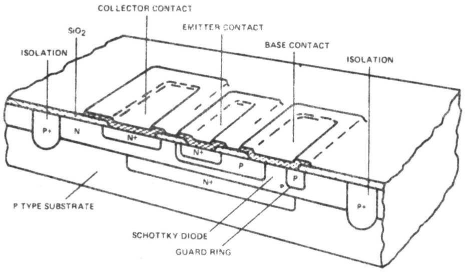


Figure 6

COMPARATOR SELECTION GUIDE

Device	Propagation Delay (ns)	V_{OS} (mV)	I_{OS} (μA)	I_{bias} (μA)	Gain	CMR (V)	Benefits
NE521	12	7.5	5	20	5000	±3	Dual, very fast, standard supplies, TTL compatible, individual & common strobe.
NE522	15	7.5	5	20	5000	±3	Same as NE521 plus open collector outputs for additional decoding.
NE527	26	6	0.75	2	5000	±6	Fast, very low input current, differential outputs, flexible surplus wide common mode range.
NE529	22	6	5	20	5000	±6	Same as NE527 but with faster response.
LM311	200	7.5	0.05	0.25	200K	±30	High common mode input range, ±5V to ±15V supply, strobe input, open collector output.
LM319	80	8	0.2	1.2	40K	±5	Low input bias, dual, +5V to ±15V supply, open collector output.
LM339	1300	2	0.05	0.25	200K	V+ −1.5V	High common mode input range, low input bias, quad, +5V to ±15V supply, open collector output.
LM393	1300	2	0.05	0.25	200K	V+ −1.5V	Same as LM339 but dual.

Figure 7

NOTE Parameters are based on min/max limits at 25° C as defined in the individual data sheet.

COMPARING THE COMPARATORS

Presently available comparator ICs range from the ultra fast SE/NE521 to the general purpose comparator fashioned from an inexpensive op amp. Selection of the device depends upon the application in which it will be used. Speed of conversion is often of primary importance to minimize pulse position errors of high frequency signals. At other times the requirements are much less stringent allowing the use of a general purpose comparator.

A handy reference guide to the major parameters is summarized in Figure 7. The necessary parameters can be chosen to select the proper device.

A general description of the comparator devices is included here to familiarize the user with available devices and their advantages.

SE/NE521/522 Comparators

Processed with state-of-the-art Schottky barrier diodes, the NE521/522 series' devices provide good input characteristics while providing the fastest analog to TTL conversion to date. Total delay from input to output is typically 6ns with a guaranteed speed of 12ns. Additional features of this device include the dual configuration and individual output strobes to simplify system logic. The NE522, although sacrificing some speed, features open collector outputs for party line or wired-OR configurations for additional system flexibility.

NE/SE527 Comparator

Featuring darlington inputs for very low bias current, the NE527 is generically related to the NE529 comparator. Emitter follower inputs to the differential amplifier are used to trade better input parameters for slightly less speed. As Figure 7 shows, a factor of 10 improvement in I_{BIAS} is gained with a propagation delay increase of only 4ns maximum.

NE529 Comparator

The NE529 is manufactured using Schottky technology. Although a few nano seconds slower than the NE521, the NE529 features variable supplies from ± 5 to ± 10 volts with a high common mode range of ± 6 volts. Both the NE527 and NE529 Schottky comparators boast complimentary logic outputs with output A being in phase with input A. In addition, the supplies of both the NE527 and NE529 may be non-symmetrical to produce a desired shift in the common mode range.

This technique is illustrated by the ECL to TTL and TTL to ECL transistor of Figures 17 and 18 respectively. The only major requirement of the supplies is that the negative supply be at least 5 volts more negative than the ground terminal of the gate. This is necessary to insure that the internal bias arrangement has sufficient voltage to operate normally.

APPLICATIONS

Today's state-of-the-art ultra-high speed comparators are capable of making logic decisions in less than 10 nano seconds. They are easily applied and possess good input and power supply noise rejection. As with all linear ICs however, some preliminary steps should be taken in their use.

General Precautions

Layout

The comparator is capable of resolving submillivolt signals. To prevent unwanted signals from appearing at signal ports, good physical layout is required. For any high speed design, ground planes should be used to guard against ground loops and other sources of spurious signals. At high frequencies hidden signal paths become dominant. Distributed capacitance is a particular nuisance. If care is not taken to isolate output from input, distributed capacitance can couple a few millivolts into the input, causing oscillation.

Another source of spurious signals is ground current. Input structures are relatively high impedance while the gate structures of comparators run with large signal and ground currents. If this gate ground current is allowed to pass near the input signal path, the small impedances of the ground circuit will cause millivolt changes in reference or signal voltages producing errors, sustained oscillation, ringing, or excessive V_{OS}. A ground plane arranged such that output currents do not flow near input areas is highly recommended.

Power Supplies

Another general precaution that should always be execised is power supply bypassing. As mentioned the name of the game is speed. Very high speed gates are used to produce the desired output logic levels. Maximizing response speed also requires higher current levels, giving rise to power supply noise. For this reason, good power supply bypassing very close to the device itself is always mandatory. A tantalum capacitor of 1 to 10μF in parallel with 500 to 1000pF will prove effective in most cases. Lead lengths should be as short as physically possible to preserve low impedances at high frequency.

Unused Inputs

Some currently available comparators such as the NE521 and NE522 are dual devices. Most often both sections of these devices will be utilized. Should a system utilize one device, the unused inputs should be biased in a known condition. The high gain-bandwidth may otherwise cause oscillations in the unused comparator section. A low impedance should be provided from both unused inputs to ground. A resistor of relatively high impedance may then be used to supply a differential input on the order of 100mV to insure the comparator assumes a known state.

If the inverting input is tied to the positive differential voltage the gate output will be low. The strobe inputs then provide a means of utilizing the Schottky gate for other system logic functions.

If the strobe inputs are not used, they should be connected to the output of a logic gate that is always high, or to the +5 volt supply through a 5 to 10 K-ohm resistor. They should never be tied directly to the +5 volt supply as the relatively minor spiking on the supply may damage these inputs.

Common Mode Signals

Manufacturers specify the maximum voltage range over which the inputs may be taken. In addition the maximum differential voltage that may be safely applied to the inputs is specified. In the case of the NE529 comparator the differential voltage is restricted to less than ± 5 volts, with a common mode of ± 6 volts. That these two quantities interact cannot be overlooked. For instance, with both inputs at ± 4 volts the common mode restriction is satisfied. If V_{ref} is now left at +4 volts the signal input may not be taken more than 1 volt below ground because the differential signal becomes 5 volts.

It is important to observe this maximum rating since exceeding the differential input voltage limit and drawing excessive current in breaking down the emitter-base junctions of the input transistors could cause gross degradation in the input offset current and bias current parameters.

Exceeding the absolute maximum positive input voltage limit of the device will saturate the input transistor and possibly cause damage through excessive current. However, even if the current is limited to a reasonable value so that the device is not damaged, erratic operation can result.

Input Impedance

The differential bias and offset currents of comparators are minimized by design. As was pointed out for op amps, the input resistance seen by both inputs should be equal. This reduces to a minimum the contribution of offset current to threshold error. Unbalanced input impedance also adds to the offset error due to the difference in voltage drop across the input resistances.

BASIC APPLICATIONS

The basic comparator circuit and its transfer function were presented by Figures 1 and 2.

When the input exceeds the reference voltage, the output switches either positive or negative, depending on how the inputs are connected.

The vast majority of specific applications involve only the basic configuration with a change of reference voltage. A to D converters are realized by applying the signal to one terminal and the voltage derived from a ladder network to the other. Limit detectors are likewise made from only the very basic circuit. Both are only a small deviation from the basic level detector.

Hysteresis

Normally saturated high or low, the amplifiers used in voltage comparators are seldom held in their threshold region.

They possess high gain-bandwidth products and are not compensated to preserve switching speed. Therefore, if the compared voltages remain at or near the threshold for long periods of time, the comparator may oscillate or respond to noise pulses. For instance, this is a common problem with successive approximation D/A converters where the differential voltage seen by the comparator becomes successively smaller until noise signals cause indecision. To avoid this oscillation in the linear range, hysteresis can be employed from output to input. Figure 8 defines the arrangement. Both positive and negative feedback is provided by R_{IN} and R_f.

Hysteresis occurs because a small portion of the "one" level output voltage is fed back in phase and added to the input signal. This feedback aids the signal in crossing the threshold. When the signal returns to the threshold, the positive feedback must be overcome by the signal before switching can occur. The switching process is then assured and oscillations cannot occur. The threshold "dead zone" created by this method, illustrated in Figure 9, prevents output chatter with signals having slow and erratic zero crossings.

As shown in Figure 8, the voltage feedback is calculated from the expression:

$$V_{HYST} = \frac{E_{OUT} \bullet R_{IN}}{R_{IN} + R_f}$$

where E_{OUT} is the gate high output voltage. The hysteresis voltage is bounded by the common mode range and the ability of the gate to source the current required by the feedback network. If symmetrical hysteresis is desired an additional inverting gate is required if the comparator does not have differential outputs. The NE527 and NE529 devices provide inverted signals from differential outputs while the NE521 and NE522 devices will require the inverter. Care should be taken in the selection of the inverter that propagation delay is minimum, especially for very high speed comparators such as the NE521.

Line Receiver

Retrieving signals which have been transmitted over long cables in the presence of high electrical noise is a perfect application for differential comparators. Such systems as automated production lines and large computer systems must transmit high frequency digital signals over long distances.

If the twisted pair of the system is driven differentially from ground, the signals can be reclaimed easily via a differential line receiver.

Since the electrical noise imposed upon a pair of wires takes the form of a common mode signal, the very high common mode rejection of the NE521/522 makes the unit ideal for differential line receivers. Figure 10 depicts the simple schematic arrangement. The NE521 is used as a differential amplifier having a logic level output. Because common mode signals are rejected, noise on the cable disappears and only the desired differential signal remains. Figure 11 illustrates the NE521 response to the 200mV peak to peak 10MHz differential signal. In Figure 12 the same signal has been buried in 5 volts peak to peak of 1HMz common mode "noise."

The circuit suffers no degradation of signal. If desired several NE522 comparators may be "wire OR'd," or latched output can be built as shown in Figure 10.

The NE521 and NE529 comparators have the advantage of wider bandwidth to permit higher data rates.

Double Ended Limit (Window) Detector

Many system designs require that it be known when a signal level lies between two limits. This function is easily accomplished with a single NE522 package. The schematic and transfer curve of the circuit is shown in Figure 13.

Each half of the NE522 is referenced to the desired upper or lower voltage limit producing the desired transfer curve shown. Taking advantage of the dual configuration and the open collectors of the NE522 minimize external components and connections.

Crystal Oscillator

Any device with a reasonable gain can be made to oscillate by applying positive feedback in controlled amounts. The NE521 will lend itself to crystal control easily, provided the crystal is used in its fundamental mode. Figure 14 shows a typical oscillator circuit.

The crystal is operated in its series resonant mode, providing the necessary feedback through the capacitor to the input of the NE521. The resistor R_{adj} is used to control the amount of feedback for symmetry. Oscillations will start whenever a circuit disturbance such as turning on the power supplies occurs. The NE521 will oscillate up to 70MHz. However, crystals wth frequencies higher than about 20MHz are usually operated in one of their overtones. To build an oscillator for a specific overtone requires tuned circuits in addition to the crystal to provide the necessary mode suppression. If the spurious modes are not tuned out the crystal will oscillate at the fundamental frequency. Higher frequency oscillators could be realized using

LEVEL DETECTOR WITH HYSTERESIS

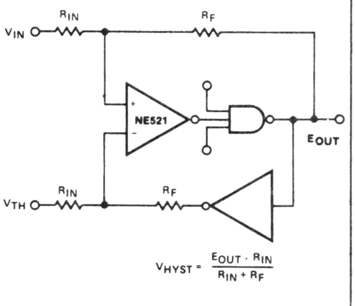


Figure 8

0 VOLT LEVEL DETECTOR WITH ± 10mV HYSTERESIS

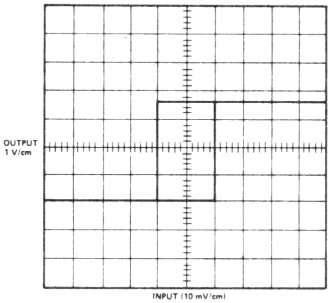


Figure 9

APPLICATIONS FOR THE NE521/522/527/529

LINE RECEIVER

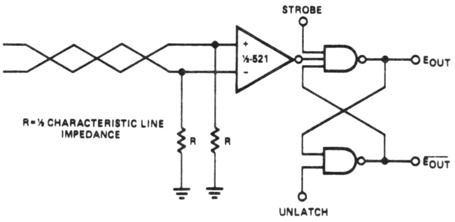

STROBE
½-521
+
-
EOUT
$\overline{E_{OUT}}$
R=½ CHARACTERISTIC LINE IMPEDANCE
R
R
UNLATCH

Figure 10

LINE RECEIVER RESPONSE

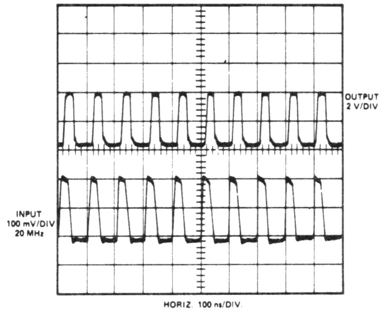


Figure 11

RESPONSE DURING COMMON MODE NOISE

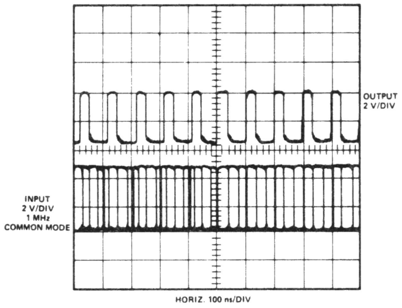


Figure 12

DOUBLE ENDED LIMIT DETECTOR

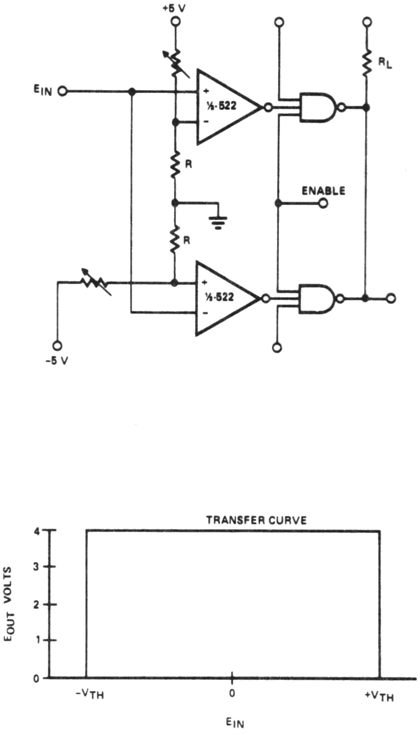

+5 V
EIN
+
-
½-522
RL
R
ENABLE
R
½-522
-5 V
TRANSFER CURVE
EOUT VOLTS
4
3
2
1
0
-VTH
0
+VTH
EIN

Figure 13

CRYSTAL OSCILLATOR

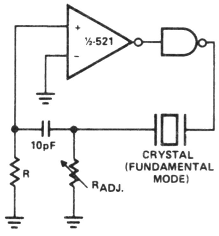

+
-
½-521
10pF
CRYSTAL
(FUNDAMENTAL MODE)
R
RADJ.

Figure 14

input and output mode suppression or tuning. The NE522 is especially desirable since the open collector topology allows the output to be collector tuned readily.

Analog to Digital Converter

There are many types of A to D converter designs, each having its own merits. However, where speed of conversion is of prime interest the multi-threshold conversion type is used exclusively. It is apparent from Figure 15, that the conversion speed of this design is the sum of the delay through the comparator and the decoding gates.

The sacrifices which must be made to obtain speed are the number of components, bit accuracy and cost. The number of comparators needed for an N-bit converter is 2n-1. Although the NE521 provides two comparators per package, the length of parallel converters is usually limited to less than 4 bits. Accuracy of multi-threshold A-D converters also suffers since the integrity of each bit is dependent upon comparator threshold accuracy.

The implementation of a 3-bit parallel A-D converter is shown in Figure 16 with a 3-bit digital equivalent of an analog input shown in Figure 15.

Reference voltages for each bit are developed from a precision resistor ladder network. Values of R and 2R are chosen so that the threshold is one half of the least significant bit. This assures maximum accuracy of ±1/2 bit.

It is apparent from the schematic that the individual strobe line and duality features of the NE521 have greatly reduced the cost and complexity of the design. The speed of the converter is graphically illustrated by the photo of Figure 15. All 3-bit outputs have settled and are true a mere 15ns after the input step of 3 volts has arrived. The output is usually strobed into a register only after a certain time has elapsed to insure that all data has arrived.

Logic Interface

During the design of the NE527 and NE529 devices, particular attention was paid to the biasing network so that balanced supplies need not be provided. For example, if the "ground" terminal is set at -5.2 volts and the other supplies are adjusted accordingly, the output logic 1 state will be at -1.5 volts and logic 0 will be at -5.0 volts. With this freedom of power supply voltage, the user may adjust the output swings to match the desired logic levels even if that logic is other than TTL levels.

ECL to TTL Interface

Emitter coupled logic is very popular due to its speed. Systems are often built around standard TTL logic with those portions requiring higher speed being implemented with emitter coupled logic. As soon as such a decision is made the problem of interfacing TTL to ECL logic levels is encountered.

The standard logic output swings of ECL are −0.8V to −1.8V at room temperature. Converting these signals to TTL levels is accomplished simply by using the basic voltage comparator circuit with slight modifications. Figure 17 reveals that the power supplies have been shifted in order to shift the common mode range more negative. This insures

PARALLEL A-D RESPONSE

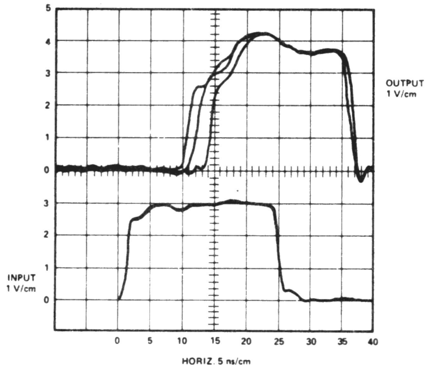


Figure 15

3-BIT PARALLEL A-D CONVERTER

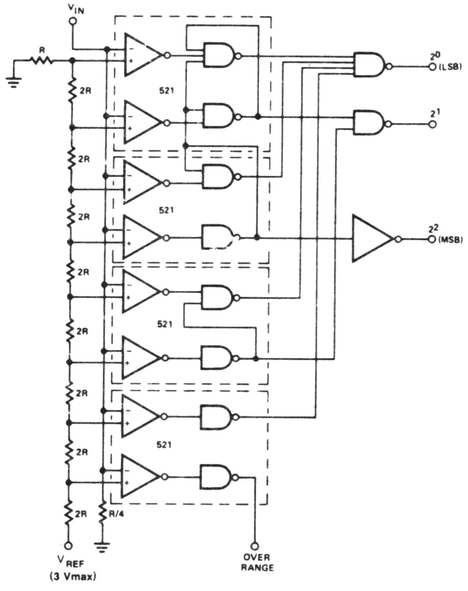


Figure 16

that the common mode range is not exceeded by the logic inputs. Since ECL is extremely fast the NE529 is usually selected because of its superior speed so that a minimum of time is lost in translation.

TTL to ECL

Operating in the reverse, TTL levels can also be converted to ECL levels by the NE529. Again the NE529 is selected as the fastest converter with the necessary power supply flexibility to accomplish the level shifting with a minimum of effort and cost.

A check of output voltage for the NE529 reveals that the voltage is slightly less than required by the ECL logic for fast switching R2 and the diode of Figure 18 raises the gate supply voltage and therefore the NE529 output voltage by 0.7 sufficient to guarantee fast switching of the translator. Resistive pull up from the NE529 output to V_{CC} can also be used with the gate supply grounded. This method is dependent upon RC time constants of distributed capacitance and is the therefore much slower.

Photo Diode Detector

Responding to the presence or absence of light, the photo diode increases or decreases the current through it. Detecting the changes becomes a matter of converting light and dark currents to voltage across a resistor as shown in Figure 19. R1 is selected to be large enough to generate detectable differences between light and dark conditions. Once the signal levels are defined by R1 and the diode characteristics, the average between light and dark signals is used for V reference and is produced by the resistive divider consisting of R1 and R2. The comparator then produces an output dependent upon the presence or absence of light upon the diode.

SENSE AMPLIFIERS

Closely related to the comparator is the sense amplifer. Signals derived from the many sources, such as transducers, are not of sufficient amplitude to be compatible with subsequent logic. It then becomes necessary to amplify and convert the signal to TTL levels, which is the responsibility of the sense amplifier.

Some transducers produce an output current. It remains, then, for the user to convert these currents to TTL levels. A terminating resistor from the drain to ground provides a voltage output proportional to the current and the resistor size. Larger signals can be produced by larger resistors; but in practice resistors larger than 1k ohm are avoided because of increasing access time. Distributed capacitance forms a time constant with this output resistance causing slow rise and fall times when the resistor is large, adding to the access time.

Virtually any voltage comparator or sense amplifier can be used. Since total time is the sum of all delays, the sense amplifier is most often the fastest available. Signetics comparators NE521 and NE522 are ideal in this application because of low input offset voltages and very fast response. Using these Schottky clamped comparators significantly reduces the total cycle time of the memory.

Design of the sense amplifier network depends upon the transducer used and the input characteristics of the sense amplifier. The significant specifications are given in Table 1.

Consideration must first be given to the differential input voltage requirements of the sense amplifier. The required reference voltage is calculated from the relationship:

$$V_{ref} \leq (I_1 - I_B)\, R1 - V_{diff}$$

Table 1
IMPORTANT SENSE AMPLIFIER PARAMETERS

DEVICE	V_{OS} (mV)	I_B (μA)	V_{IN} (MIN)(mV)	SPEED (NS) (V_{IN} = 100mV)	GAIN
521	10	40	15	12	5000
522	10	40	15	15	5000

ECL TO TTL TRANSLATOR

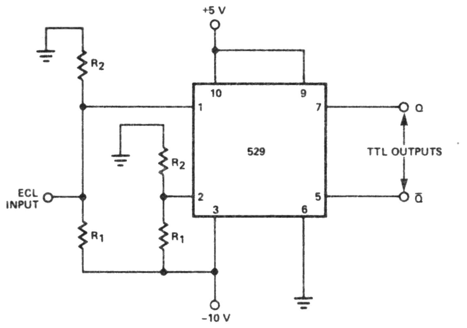


Figure 17

TTL TO ECL TRANSLATOR

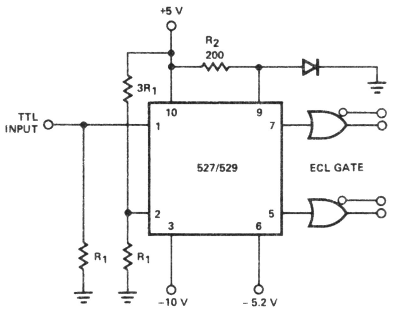


Figure 18

PHOTO DIODE DETECTOR

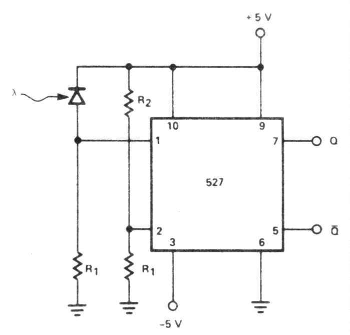

+5 V
λ
R2
10
9
1
7
Q
527
2
3
5
6
Q̄
R1
R1
-5 V

Figure 19

Where I_t is the transducer output current, I_B is sense amplifier bias current and V_{diff} is minimum differential voltage to switch the sense amplifier.

In large systems, noise coupled into the sense lines by stray capacitance can be very troublesome. Judicious layout patterns with sense lines as short as possible will help, but will not always be sufficient. One method of eliminating noise is to use a balance sense line as shown in Figure 20.

A dummy line should be run parallel to the actual sense line in as close proximity as possible. One end is connected to the sense amplifier at the V_{ref} point while the other end is left open. The normal sense line is connected as usual. Electrical noise imposed upon the pair of sense lines takes the form of a common mode signal and will be rejected by the sense amplifier. Signal currents in the sense line, on the other hand, form differential signals at the sense amp causing the output to switch.

BALANCED SENSE LINE TO REDUCE NOISE

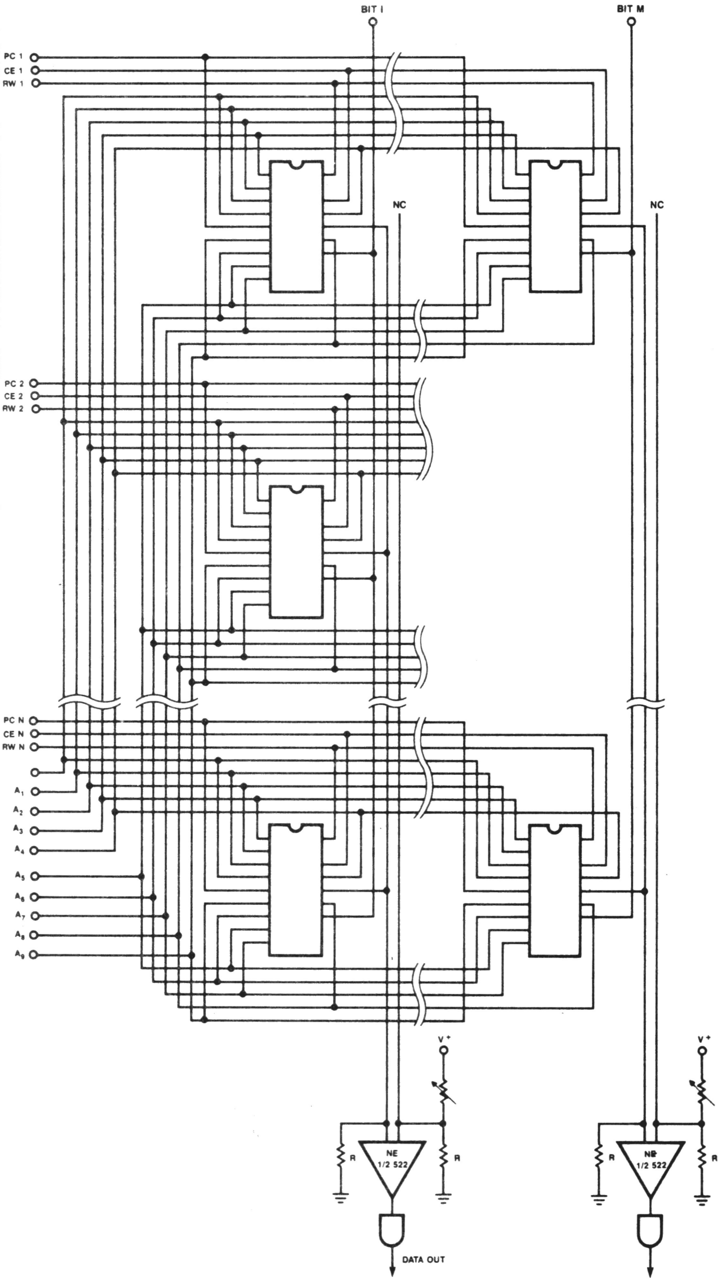

BIT I
BIT M
PC 1
CE 1
RW 1
NC
NC
PC 2
CE 2
RW 2
PC N
CE N
RW N
A1
A2
A3
A4
A5
A6
A7
A8
A9
V+
V+
R
NE 1/2 522
R
R
NE 1/2 522
R
DATA OUT

Figure 20

USING THE LVDT SIGNAL CONDITIONER

AN118

ALL PIN NUMBERS REFER TO N PACKAGE

INTRODUCTION

An LVDT is an electromechanical transducer which makes possible the measurement of very small motion in a structure or mechanical device. Mechanical motion is translated to an electrical signal which contains position information much as a radio frequency carrier contains sound information. The position information from the LVDT is contained in the phase and amplitude of the output AC waveform. In order to remove the position information (demodulation), a system such as is shown in block form in Figure 1 must be used. Once signal demodulation is achieved the position data may be read out on a meter or digital display in addition to being processed by microprocessor or computer. The Signetics NE5520 is a new *Monolithic LVDT Driver-Demodulator* designed to interface with most LVDT's presently being used in the industry.

Uses will range over a large number of potential applications including the accurate measurement of position, pressure, load weight, angular position and even acceleration. Historically, LVDT's have been used in the following applications:

- Load cell
- Linear motion
- Torque cell
- Vibration
- Fluid pressure
- Accelerometer
- Inclinometer
- Seismic load cell

MOTION MAY-BE

- Linear
- Rotary

The NE5520 provides sinusoidal drive to the Linear Variable Differential Transformer (LVDT), the output of which is buffered, rectified and phase demodulated to obtain both direction and displacement information in the form of a DC output signal (Figure 2).

THE LVDT WITH SINEWAVE EXCITATION AND SYNCHRONOUS DEMODULATION

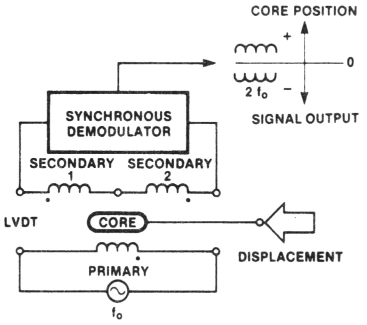


Figure 1

LVDT SYSTEM TRANSFER FUNCTION

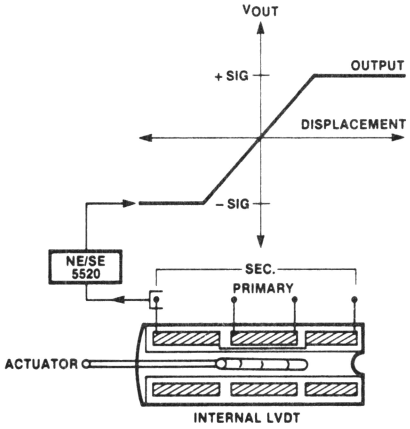


Figure 2

LVDT LOADING

Due to the loosely coupled characteristics of the typical LVDT, loading effects versus frequency may be critical to a successful design. The graph (Figure 3A) shows this relationship in the form of a family of curves relative to LVDT core displacement for 400Hz and 2500Hz. From the curves it is obvious that the linearity and output level versus displacement is superior for an LVDT operated at 2500Hz with a very high impedance load (0.5 meg ohm). The **NE5520 demodulator presents a very high input impedance to the LVDT secondary for maximum linearity. (Fig. 3B)**

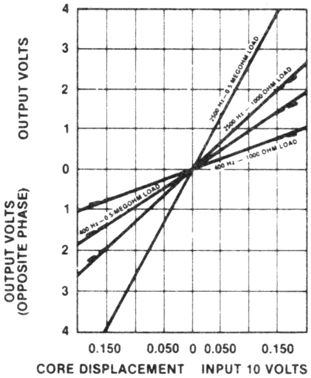
LVDT INTERFACING: SIGNAL CONDITIONING IS REQUIRED

In order to obtain usable information from the LVDT a series of signal conditioning circuit operations are required. First, a stable source of constant frequency excitation voltage must be applied to the primary of the LVDT.

Next some form of demodulator is needed to extract position information from the LVDT secondary output signal. A full wave rectifier will provide usable amplitude information when adequately filtered, however, relative phase information is lacking. In order to obtain both phase and amplitude information synchronous demodulation is needed. This type of demodulator

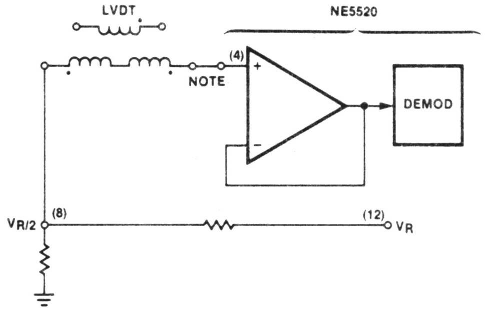
USING THE LVDT SIGNAL CONDITIONER

OUTPUT CHARACTERISTICS OF A TYPICAL LVDT FOR VARIOUS LOADS AND EXCITATION FREQUENCIES



BY PERMISSION SCHAEVITZ ENGINEERING
"HANDBOOK OF MEASUREMENT AND CONTROL" BY HERCEG.

Figure 3a



NOTE: INTERNAL BUFFER AMP PROVIDES HIGH IMPEDANCE LOAD TO SECONDARY.

Figure 3b

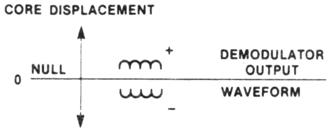


Figure 3c

exists in the Signetics NE5520. Once phase and amplitude information is obtained in the form of a polar full wave rectified signal (see Figure 3C) from the synchronous demodulator, the carrier component (actually 2nd harmonic of the carrier plus higher order spectral components) must be filtered out leaving only the true position information. This is accomplished by passing the demodulated signal through a low-pass active filter. An auxiliary operational amplifier is provided for this purpose within the NE5520, in addition to adjustable signal gain for proper full scale output (span adjustment). In addition, DC offsets are nulled by a simple offset adjustment at the auxiliary amplifier. The resulting system is a complete LVDT signal conditioner. Figure 4 shows a block diagram of the NE5520. The device will operate in a single supply range from 5 to 20 volts DC or with split supplies of ± 5 to ± 10 volts DC. A device current, I_{CC}, of 10 milliamperes at an operating voltage of 10 volts is typical.

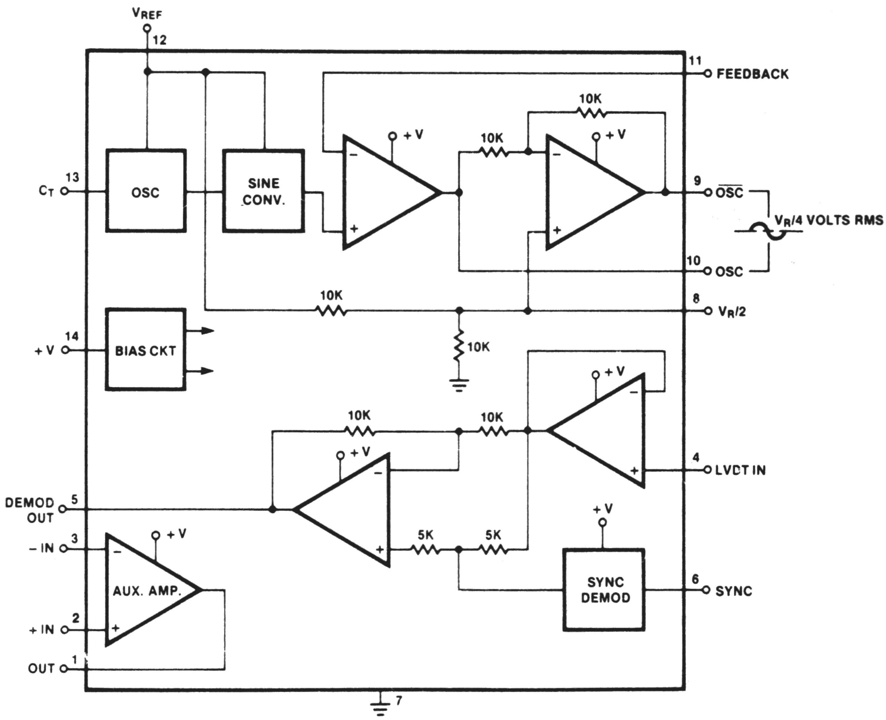
DESCRIPTION OF THE NE5520 (Figure 4)

The NE5520 oscillator consists of a triangle wave generator, a current source-sink circuit which switches when the capacitor voltage reaches discrete levels at 1/4 and 3/4 V_{REF}. The total swing being $V_{REF/2}$ volts p-p. The triangle wave is fed into a non-linear load which generates a sinusoidal waveform with low distortion. The sine wave output is then buffered by two op amps, the output of which appear on pins 9 and 10 in phase opposition. This then is the excitation signal for the LVDT primary.

The second major functional portion of the NE5520 is the synchronous demodulator and this section performs full wave rectification in phase synchronism (pin 6) with the above oscillator output. In order to extract true position information, the phase relationship of the LVDT secondary must be obtained. This means that as the LVDT core passes through null an abrupt 180° phase change occurs. Once full wave rectification is accomplished, the resulting signal carrier frequency must be removed by filtering. Demodulator output appears on pin 5. This is accomplished by an active filter incorporating the auxiliary op amp (pins 1, 2, 3). The original position information then appears ripple free on pin 1 of the auxiliary amplifier.

USING THE LVDT SIGNAL CONDITIONER

BLOCK DIAGRAM



NOTE:
Pin numbers for for N package.

Figure 4

Other functions include buffer amplifier feedback in the oscillator circuit. The loop is closed with negative feedback around both amplifiers (pin 10 to 11) operating at unity gain.

The oscillator timing capacitor controls the frequency as shown in the graph, Figure 5. The frequency is related by the equation $f_{OSC} = 110/C_{\mu F}$ Absolute output frequency will vary slightly with supply voltage.

BIASING THE REFERENCE V_{REF} (PIN 12)

The manner in which the V_R pin is biased will effect the output voltage function of the NE5520 and consideration must be given to this in order to arrive at an optimum system design. There are two basic modes of operation involved as listed below:

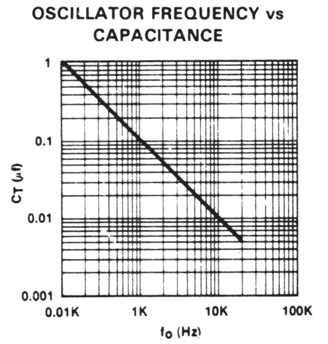


Figure 5

1) Ratiometric
2) Fixed Reference

With the *ratiometric mode*, pin 12 (V_{REF}) is connected to pin 14 (+V). Since V_R controls the DC common mode voltage of the demodulator and the oscillator rms output, these magnitudes will now change with supply voltage. The DC output from pin 1, using a single ground referenced supply, will be ratiometric with the supply voltage and centered within the common mode range of the output amplifier when the LVDT transducer is at null. Single or dual supply operation will be ratiometric when +V is connected to V_R.

The alternate method of biasing is the *fixed reference* mode with pin 12 (V_R) connected to a fixed reference voltage such as +10 volts and pin 14 (+V) allowed to vary with an incoming poorly regulated supply. This might occur in automotive applications where battery voltage may vary from 10 to 14 volts. However, with a fixed reference driving V_R, DC voltage at the output will not vary with supply but will vary within the common mode limits of the amplifier as the LVDT core traverses its path. Output voltage of pin 1 at LVDT null will be $V_R/2$. Thus, for the case mentioned with $V_R = 10$ volts, the null voltage will be +5 volts. The maximum linear swing would be 1.5-8.5 volts around this value. The fixed reference mode may be used with single or dual supply operation.

DUAL SUPPLY OPERATION

When connected to a typical LVDT transducer as shown in Figure 6, the NE5520 will exhibit an extremely linear transfer function. Very important to precision position measurement is the inherent repeatability of the system. The graphs in Figure 7A, B illustrate the highly linear transfer function and its repeatable accuracy with different supply voltages, in this case ±6 and ±10 volts. The transducer motion was over a range of ±150 milli-inches each side of the LVDT null. Typical DC output signal is shown with an output amplifier gain of X10 in both cases. Note that linearity remains constant, however, full scale output varies with supply voltage. This is due to the increased excitor drive to the LVDT with increased reference voltage. LVDT ouput is a linear function of excitor amplitude on the primary winding. The addition of a single gain control may easily be added between pins 1 and 3 to reduce gain in order to retain constant output for different supply voltages (see Figure 8) or V_R may be connected to a fixed voltage. (See 'Biasing.')

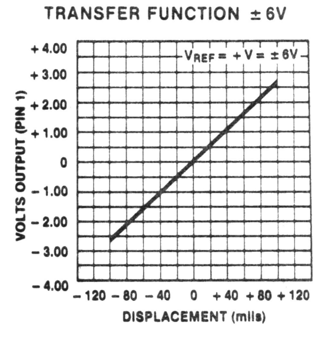

TRANSFER FUNCTION ±6V

Figure 7a

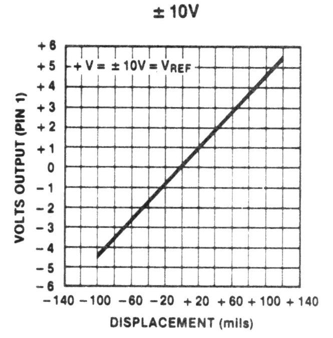

± 10V

Figure 7b

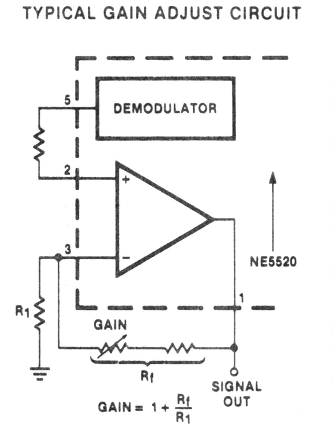

TYPICAL GAIN ADJUST CIRCUIT

Figure 8

It is strongly recommended that dual output tracking regulated supplies be used in this type of application in order to minimize system DC offset and impaired measurement accuracy due to power supply unbalance. An optional circuit capable of automatically tracking and nulling power supply offset is shown in Figure 9. The bipolar output signal is referenced to ground.

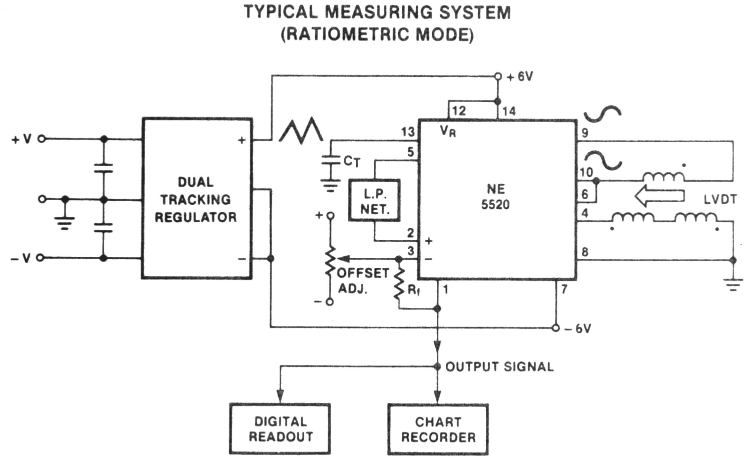

TYPICAL MEASURING SYSTEM
(RATIOMETRIC MODE)

Figure 6

USING THE LVDT SIGNAL CONDITIONER

AUTO PSRR FOR USE WITH NON-TRACKING SUPPLIES

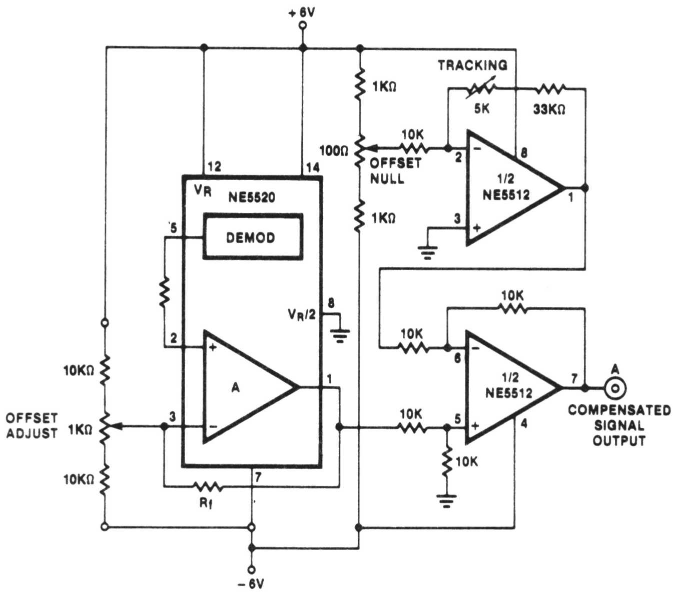

+6V
1KΩ
TRACKING
5K
33KΩ
100Ω
10K
OFFSET NULL
2
8
1/2 NE5512
1
3
1KΩ
12
14
VR
NE5520
5
DEMOD
VR/2
8
10K
2
10KΩ
10K
6
1/2 NE5512
7
A
COMPENSATED SIGNAL OUTPUT
1
OFFSET ADJUST
1KΩ
3
10K
5
4
10K
10KΩ
7
Rf
−6V

Figure 9

NULLING PROCEDURE (Ref Fig. 9)

1. Null transducer position by observing pin 4 waveform. Set supply voltage for ± 6.00 volts.
2. **Set offset adjust pot (feeds pin 3 of NE5520) for 0.00 volts DC at pin 1 of NE5520.**
3. Adjust offset null pot (NE5512) for zero output on Terminal A.
4. Check for equal voltage ± deflection when transducer is displaced equal distances from physical null position.
5. Adjust tracking control for minimum DC output change when either supply is varied over operating range at 'A'.

SINGLE SUPPLY OPERATION

Single ended supply operation requires a different circuit approach to obtain measurement system interface. Figure 10 shows a typical circuit using a single 10-volt supply. Note that the output (pin 1) of the NE5520 is now floating above ground at approximately $V_R/2$. Simple measuring circuits may be realized (Figures 11A, B, C) by placing a DC microammeter between pin 1 and a resistive divider

TYPICAL SINGLE SUPPLY LVDT CIRCUIT

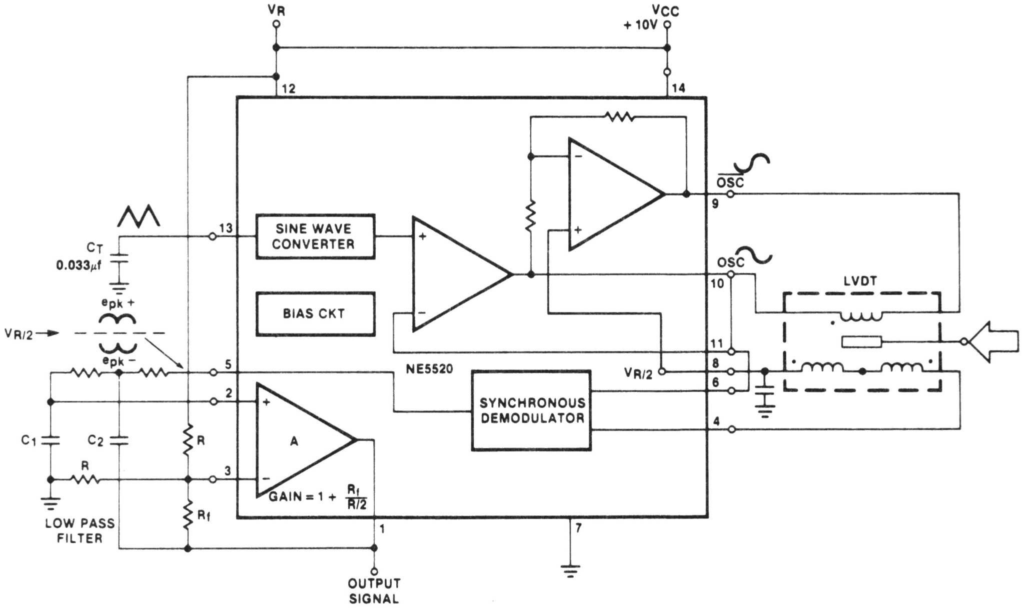

VR
VCC
+10V
12
14
OSC
9
13
CT
0.033µf
SINE WAVE CONVERTER
BIAS CKT
OSC
10
LVDT
epk +
VR/2
epk −
11
NE5520
VR/2
8
5
SYNCHRONOUS DEMODULATOR
6
2
4
C1
C2
R
A
R
3
GAIN = 1 + Rf/R/2
LOW PASS FILTER
Rf
1
7
OUTPUT SIGNAL

Figure 10

creating a bridge readout which is ratiometric with supply voltage variations. In case more precision is necessary, a buffer amplifier may be added between the voltage divider or $V_R/2$ and the readout circuit in order to minimize offset due to measuring circuit loading. DC offset due to internal tracking error in the NE5520 may be reduced by using the nulling circuit shown in Figure 12. Offset sensitivity and its effect on system accuracy will be inversely proportional to full scale signal output of the NE5520 which is a function of the DC gain of the auxiliary amplifier and LVDT output. A typical full scale output with 10-volt supply operation is $V_R/2 \pm 3.5$ volts with gain equal to 10.

OUTPUT INTERFACING EXAMPLES

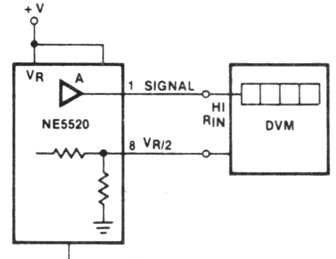


Figure 11a

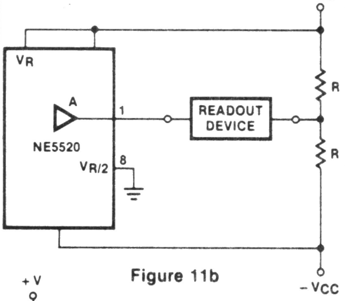


Figure 11b

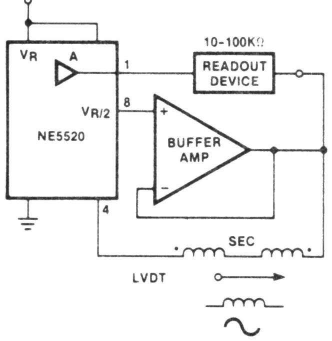


Figure 11c

D.C. OFFSET ADJUST

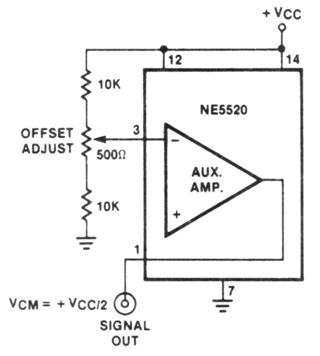


Figure 12

MATCHING THE NE5520 TO LOW IMPEDANCE LVDT's

The NE5520 exciter output is capable of driving LVDT primary windings with a minimum impedance of 1K ohm. When a significantly lower impedance primary is driven by the device some form of step-down impedance matching or a power buffer is recommended. Figure 13 shows a step-down matching transformer approach. A transformer with primary impedance of approximately 1K ohm (audio type) with the proper secondary impedance to match the LVDT primary is used to couple oscillator excitation. Depending on the output efficiency of the LVDT, output signal losses may occur with a corresponding loss in measuring sensitivity. The auxiliary amplifier gain may be increased to offset this loss.

A second approach makes use of a power buffer amplifier constructed from discrete transistors (2N2222, 2N3644). This circuit (Figure 14) results in less signal loss and is inexpensive. A DC decoupling capacitor must be used to prevent DC offset currents from flowing in the LVDT primary winding. A 3dB signal reduction is noted when driving a 15-ohm load to 6 volts peak to peak (10-volt operation); and 12 volts peak to peak for 20-volt supply.

NE5520 TEMPERATURE COMPENSATION

Internal offset voltages originating in the NE5520 synchronous demodulator require external compensation to obtain best measurement accuracy when operating over the full temperature range. The circuits shown (Figures 15A, B) give a simple approach using a thermistor inserted in series with the offset null resistors to reduce voltage drift to a reasonable level. These tolerances are based on ± 3.5 volts full scale output for LVDT displacements each side of physical null. A thermistor having a positive coefficient of +0.7%/°C is used. Obviously, if the total divider resistance is changed a different thermistor resistance will be required.

DRIVING LOW Z LVDT'S WITH THE NE/SE5520

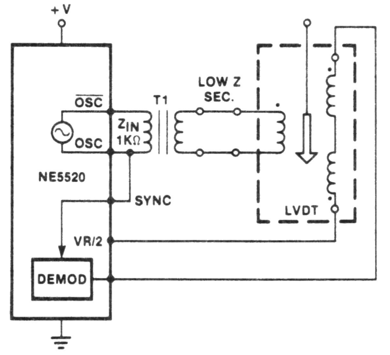


Figure 13

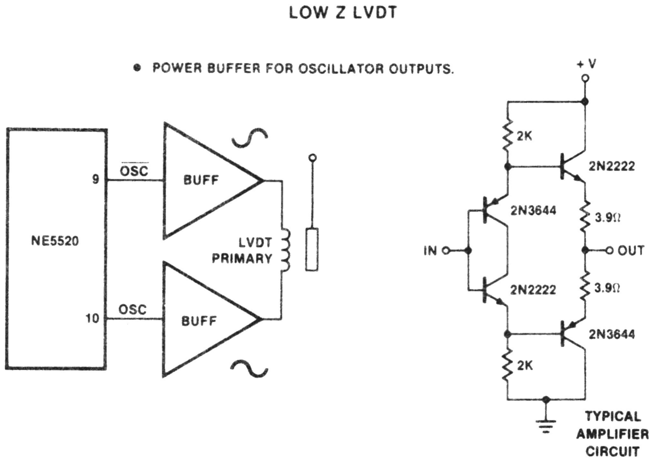

LOW Z LVDT
• POWER BUFFER FOR OSCILLATOR OUTPUTS.
NE5520
9
OSC
10
OSC
BUFF
BUFF
LVDT PRIMARY
+V
2K
2N2222
2N3644
3.9Ω
IN
OUT
2N2222
3.9Ω
2N3644
2K
TYPICAL AMPLIFIER CIRCUIT

Figure 14

DEMODULATOR DISTORTION (OVERDRIVE)

When the demodulator input exceeds 2 volts peak to peak clipping distortion will increase and must be avoided by controlling oscillator drive to the primary of the LVDT. Figure 16 shows an example of a circuit for attenuating primary excitation using a 1K ohm potentiometer.

The procedure for adjusting the level is simply to:

1. Set LVDT core position for maximum output from the secondary.
2. Monitor the waveform on (pin 5 demodulator output) and adjust oscillator level for the amplitude just below clipping. Normally this should result in a maximum of 2 volts peak to peak at pin 4 of the NE5520 (25°C).

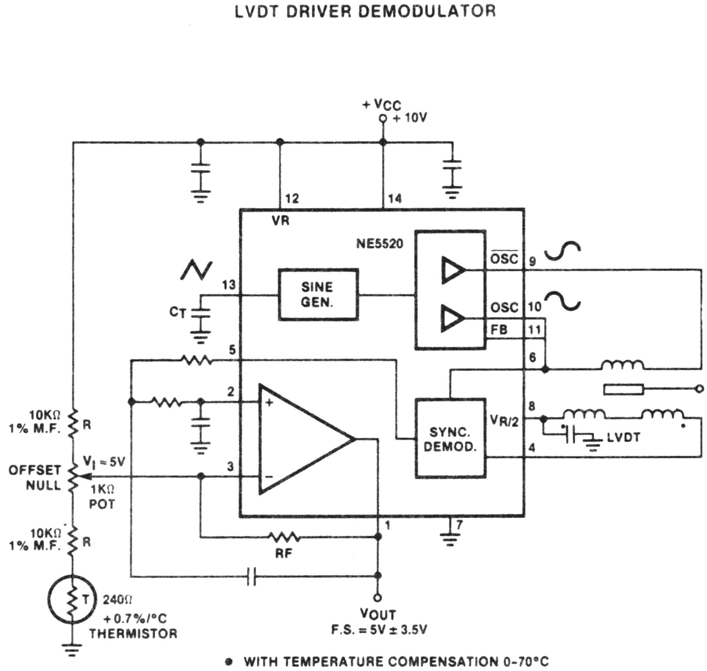

LVDT DRIVER DEMODULATOR
+VCC
+10V
12
14
VR
NE5520
SINE GEN.
13
CT
5
2
3
OSC 9
OSC 10
FB 11
6
8
VR/2
4
SYNC. DEMOD.
LVDT
10KΩ 1% M.F. R
OFFSET NULL
VI ≈ 5V
1KΩ POT
10KΩ 1% M.F. R
T 240Ω +0.7%/°C THERMISTOR
1
7
RF
VOUT F.S. = 5V ± 3.5V
• WITH TEMPERATURE COMPENSATION 0-70°C

Figure 15a

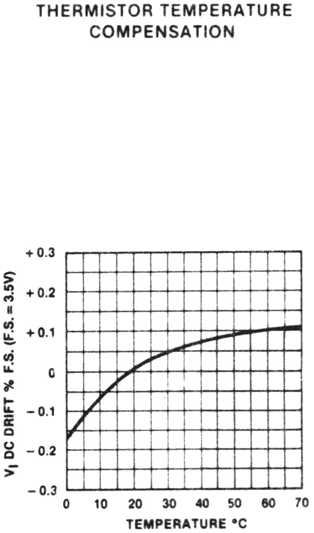


Figure 15b.

LVDT SECONDARY PHASE ANGLE COMPENSATION BY EXCITATION FREQUENCY

The LVDT has a frequency dependent phase shift associated with the particular characteristics of the device and its excitation frequency. This phase shift is in addition to the 180° shift which occurs when passing through null position.

By adjusting the frequency of the sine wave excitation a condition results which causes secondary voltage to be in phase with primary excitation. The adjustment of relative primary and secondary phase angles has several effects. First, if the primary excitation is referenced to the synchronous demodulator, as in the NE5520, optimum rectification occurs at zero phase differential between secondary AC phase and demodulator switching relative to the waveform zero crossings. Second, "Exciting an LVDT at its zero phase angle frequency results in minimum sensitivity to frequency and temperature variations" (Schaevitz Handbook of Measurement and Control, 1976).

LIMITING LVDT EXCITATION TO PREVENT DEMODULATOR DISTORTION

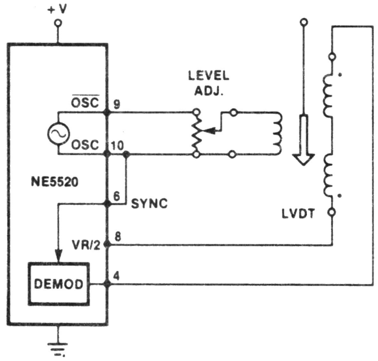


Figure 16

DEMODULATOR SYNC PHASE

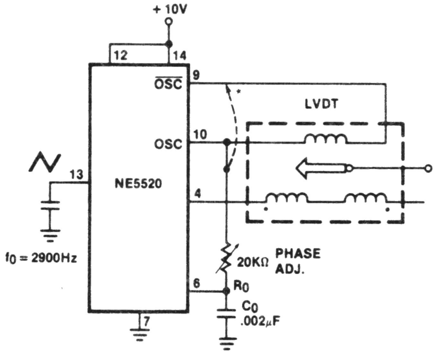
A second method of phase compensation of the NE5520 versus the LVDT is to use a variable phase shift network between the *oscillator* output and the *sync* input to the NE5520. This is shown in Figure 17. The oscillator frequency remains fixed and the pot is tuned for optimum demodulator phasing.

It is emphasized that an external phasing adjustment as outlined above is not always necessary. Some LVDT's operating in the 1-5kHz range will be near zero phase and will need no phase compensation. Experimental evaluation of the prototype design combined with system specifications will be the best means of making this decision.

Waveform photo in Figure 18A-B, shows the demodulator output signal when phasing of the synchronous demodulator is correct (A) and improperly adjusted (B).

Proper phasing of the sync signal to the demodulator results in optimum sensitivity and linearity.

EXTERNAL PHASE ADJUSTMENT



EXAMPLE: $R_0 = 10K\Omega$ $f_0 = 2900Hz$
$C_0 = 2nf$ $\Delta\phi = -\tan^{-1}\omega RC$
$= -20°$

*Alternate connection may be required for some LVDT's.

Figure 17

NE5520 DEMODULATOR PHASING

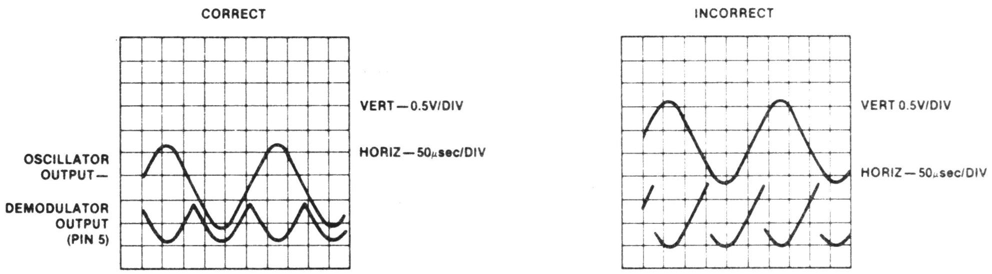


Figure 18a

Figure 18b

NE5520 LVDT DRIVER DEMODULATOR APPLICATIONS

OPERATED WITH A SINGLE POWER SUPPLY

The NE5520 may be operated with a single ended power supply ranging from +5 to 20 volts.

A very simple motion transducer may be constructed using the circuit shown in Figure 19A, B. The output is biased to one-half the supply voltage. This requires special interface circuitry for the signal readout. One simple method is to use a zero center meter in a bridge configuration as shown. Displacement now may be measured as a positive or negative meter reading. Readout sensitivity is a function of the particular LVDT and of the gain of the error amplifier. DC offsets may be nulled by using a simple offset adjustment circuit as indicated.

The transducer is centered in its displacement and the *offset adjust* pot set for a zero meter reading. Once this procedure is completed, the circuit is capable of making measurements based on transducer displacement. Displacement sensitivity is a function of the LVDT transducer rated in volts-per-inch in addition to the transfer gain of the NE5520 demodulator. The input excitation is generally a fixed level as is the LVDT transducer transformer ratio. However, the auxiliary gain stage may be used to adjust the overall system sensitivity. This section of the device is also used to obtain a low-pass active filter for the smoothing of demodulator ripple. The design examples use a simple VCVS low-pass filter which allows gain and cut-off frequency to be adjusted independently. Gain equals ten in the example.

Note that using a single supply results in a DC common mode voltage at the output of one-half the reference voltage on pin 12. *This voltage V_R may be equal to but not greater than the supply voltage on pin 14.*

LVDT MEASURING CIRCUIT USING A DUAL SUPPLY

A second mode of operation makes use of dual power supply. A common choice may be ±5, ±6, or ±10 volts. Special consideration must be made in properly biasing the internal circuitry to operate under these conditions. Figure 20 shows a simple design for working with ±6-volt supplies. Special provisions for minimizing DC power supply offsets may be made by using the NE5512 dual op amp as a tracking voltage source and difference amplifier-output buffer (see Figure 9). A second method is to use a dual tracking regulator to supply the NE5520.

LVDT IN CLOSED LOOP SERVO

The LVDT provides an excellent method of obtaining position information for closed loop servo drive systems. Pressure rollers, hydraulic drivers, and motor driven linear motion transducers are a few of the general applications which may benefit from the accuracy and speed of response inherent in the LVDT sensor.

A simple block diagram (Figure 21A) shows one possible application in which the NE5520 with LVDT sensor provides accurate position control in a closed loop servo. Linear motion from millimeters to inches of translational motion are possible using the LVDT technique.

In practice the position voltage may be the output of a D/A converter which in turn is activated digitally from a controlling microprocessor. Keyboard information or software commands are translated directly into mechanical motion (Figure 21B).

LVDT MEASURING GAUGE

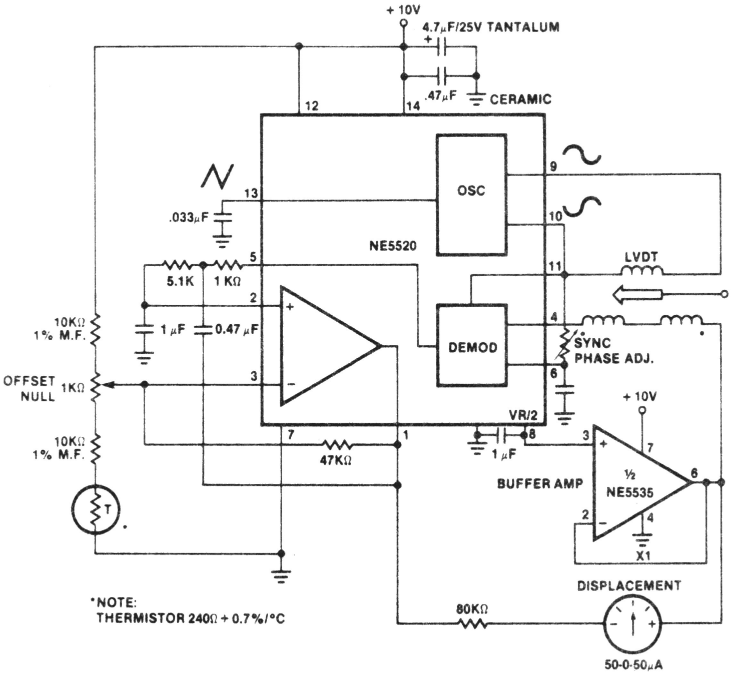
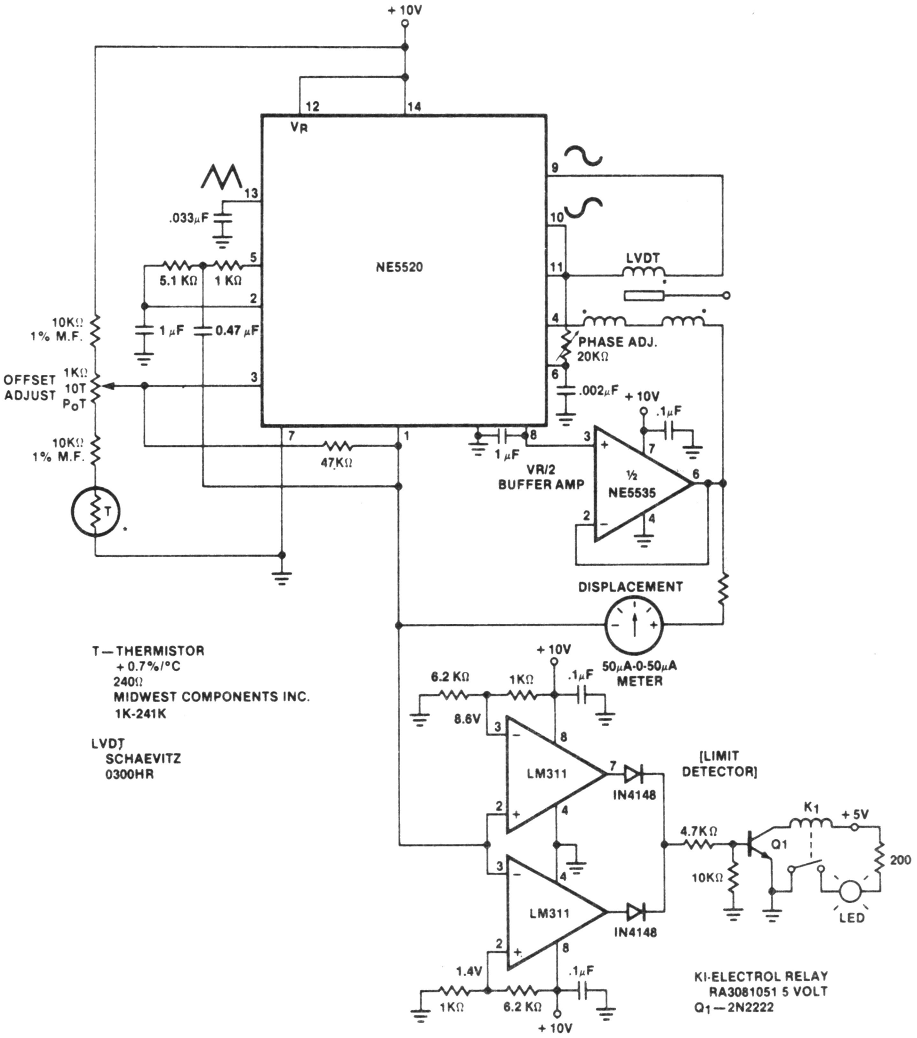

+ 10V
4.7μF/25V TANTALUM
+
.47μF
CERAMIC
12
14
13
.033μF
OSC
NE5520
9
10
11
LVDT
5
5.1K
1 KΩ
2
+
1 μF
0.47 μF
DEMOD
4
SYNC
PHASE ADJ.
6
10KΩ
1% M.F.
OFFSET
NULL
1KΩ
3
–
VR/2
8
7
1
47KΩ
1 μF
10KΩ
1% M.F.
T
3
+ 10V
BUFFER AMP
½
NE5535
7
6
2
4
X1
DISPLACEMENT
80KΩ
50-0-50μA
*NOTE:
THERMISTOR 240Ω + 0.7%/°C

Figure 19a

NE5520 LVDT MEASURING CIRCUIT WITH LIMIT DETECTOR


+10V
12
14
VR
NE5520
13
.033μF
5
5.1 KΩ
1 KΩ
2
1 μF
0.47 μF
10KΩ 1% M.F.
OFFSET ADJUST
1KΩ 10T PoT
3
10KΩ 1% M.F.
T
7
47KΩ
1
9
10
11
LVDT
4
PHASE ADJ. 20KΩ
6
.002μF
+10V
.1μF
8
1 μF
VR/2 BUFFER AMP
3
7
½ NE5535
6
2
4
DISPLACEMENT
50μA-0-50μA METER
+10V
6.2 KΩ
1KΩ
.1μF
8.6V
3
8
LM311
7
IN4148
[LIMIT DETECTOR]
2
4
4.7KΩ
Q1
K1
+5V
200
10KΩ
3
4
LM311
IN4148
LED
2
8
1.4V
1KΩ
6.2 KΩ
.1μF
+10V

T—THERMISTOR
+0.7%/°C
240Ω
MIDWEST COMPONENTS INC.
1K-241K

LVDT
SCHAEVITZ
0300HR

KI-ELECTROL RELAY
RA3081051 5 VOLT
Q1—2N2222

Figure 19b

NE5520 LVDT DRIVER-DEMODULATOR <f_o = 2900Hz>

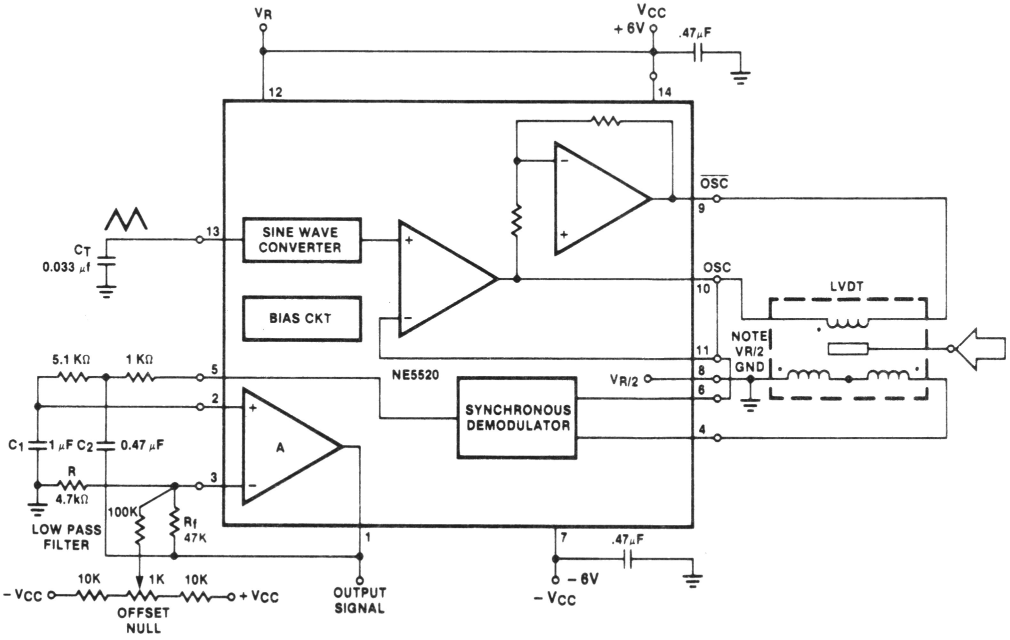

VR
VCC
+6V
.47μF
12
14
13
SINE WAVE CONVERTER
BIAS CKT
CT
0.033 μf
OSC
9
OSC
10
LVDT
11
NOTE
VR/2
GND
8
6
4
VR/2
NE5520
SYNCHRONOUS DEMODULATOR
5.1 KΩ
1 KΩ
5
2
3
A
C1
1 μF
C2
0.47 μF
R
4.7kΩ
LOW PASS FILTER
100K
Rf
47K
1
7
.47μF
−6V
−VCC
10K
1K
10K
−VCC
+VCC
OFFSET NULL
OUTPUT SIGNAL

Figure 20

NE5520 POSITION SERVO WITH LVDT SENSOR

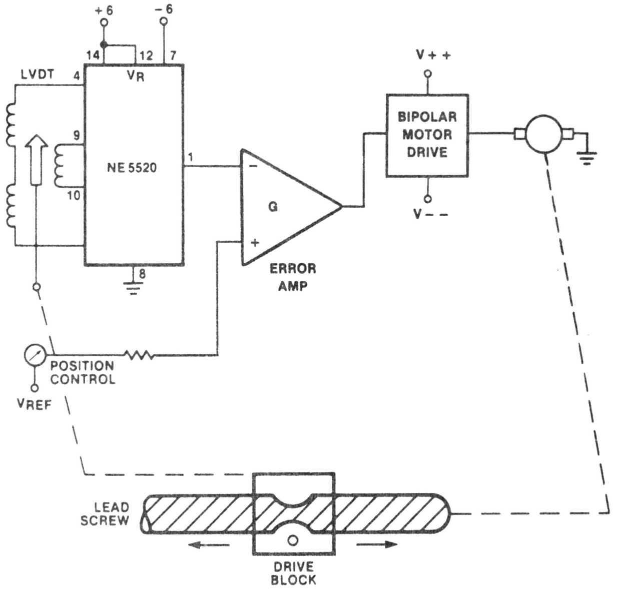


Figure 21a

MICROPROCESSOR CONTROL INTERFACE

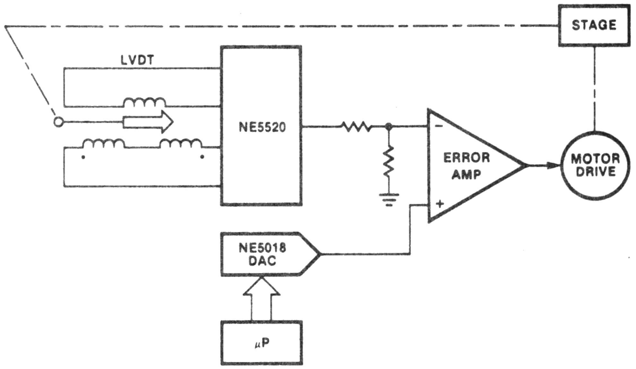


Figure 21b

LVDT SIGNAL TRANSMISSION BY CURRENT LOOP

In certain situations the demodulated output signal must be transmitted over long wires or cables before reaching the signal monitoring equipment. The receiver end may consist of chart recorders, digital panel meters and computers or microprocessors. In some systems many LVDT signals must be monitored from different locations thus requiring variable wire length between transmitter and receiver, thus a different line resistance in each case. If voltage feed were used, signal accuracy would be affected by line resistance. This need for accurate signal transmission necessitates the use of a current loop. A current loop develops a current exactly in proportion to the demodulated LVDT output voltage. It is not affected by line resistance within certain limits governed by the current generator.

One method of current loop transmission uses the $V_{R/2}$ common mode reference to create a null balance signal circuit which is converted to a bipolar current signal corresponding to the LVDT transducer null (i.e. physical displacement center null position at which zero current occurs). This method is shown in Figure 22 and requires the use of an external dual op amp, half of which is used to provide a buffered reference ($V_{R/2}$) voltage return for the current loop. With $R_2 = 200$ ohms the current loop sensitivity is 5 milliamperes per volt of input signal. In all cases, the current output to the loop receiver will remain constant with fixed input voltage (LVDT demodulator) even for varying line resistance up to 600 ohms. This resistance must include all wire and load drops in the loop. Various full scale current limits require different supply voltages and without external supplies will be limited by op amp swing characteristics, for to force a given current across $R_L + R_2$ results in an ultimate voltage limit from the op amp output in the current converter as total resistance increases.

Another method uses an external supply and discrete transistor controlled by the closed loop op amp referenced to shunt resistor R_{SH} in the emitter return circuit. This of course is a unipolar current loop. See Figure 23.

NE5520 WITH BIPOLAR CURRENT LOOP OUTPUT ± 10mA F.S. — SINGLE SUPPLY OPERATION

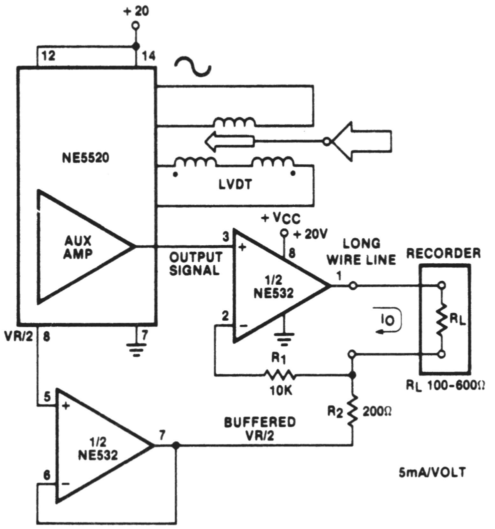
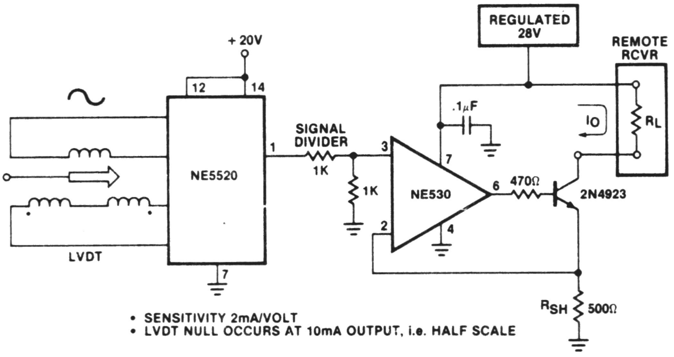

+20
12
14
NE5520
LVDT
AUX AMP
OUTPUT SIGNAL
+VCC
+20V
3
8
2
1
1/2 NE532
LONG WIRE LINE
RECORDER
IO
RL
R1
10K
R2
200Ω
RL 100-600Ω
VR/2
8
7
5
6
1/2 NE532
BUFFERED VR/2
5mA/VOLT

Figure 22

NE5520 WITH UNIPOLAR CURRENT SOURCE


+20V
12
14
NE5520
LVDT
1
7
SIGNAL DIVIDER
1K
1K
REGULATED 28V
REMOTE RCVR
.1μF
IO
RL
3
7
2
4
6
NE530
470Ω
2N4923
RSH
500Ω

- SENSITIVITY 2mA/VOLT
- LVDT NULL OCCURS AT 10mA OUTPUT, i.e. HALF SCALE

Figure 23

USING THE LVDT SIGNAL CONDITIONER AN118

Some systems in common use require two wire source to include both the device operating current and the signal loop current. Thus the quiescent device current must be nulled out at the receiver end leaving the residual signal loop current. **The NE5520 is not well suited to this particular application since the device standby current is approximately 10 milliamperes.**

A current loop operated from supply voltage sources at the transducer location is a better choice for the operation of an output signal loop where long lines must carry locally generated LVDT signals after demodulation back to the monitor site.

POSITIONING THE NE5520 LVDT 3-WIRE REMOTE DRIVER DEMODULATOR SENSING HEAD

The NE5520 may be placed in close proximity to the LVDT transducer provided the environment stays within device specifications. This physical arrangement allows only DC supply and low frequency signal lines (3 wires) being run between the transducer-conditioner unit and the signal processing station as shown in Figure 24.

POSITIONING THE NE/SE5520 LVDT 3 WIRE REMOTE DEMODULATOR SENSING HEAD

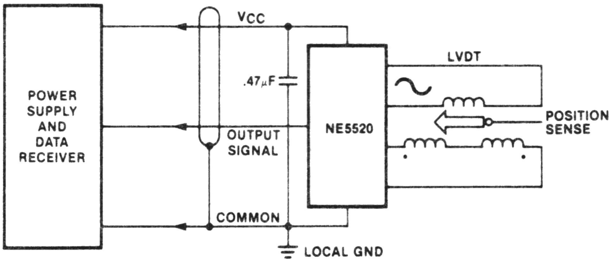


Figure 24

MULTIPLE TRANSDUCER OPERATION — SYNCHRONOUS OSCILLATOR MODE

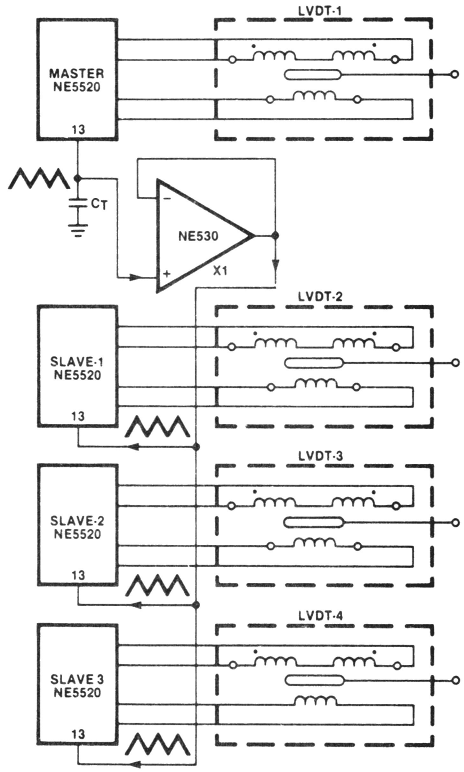

LVDT-1
MASTER NE5520
13
CT
NE530
X1
LVDT-2
SLAVE-1 NE5520
13
LVDT-3
SLAVE-2 NE5520
13
LVDT-4
SLAVE 3 NE5520
13

Figure 25

REFERENCES

Handbook of Measurement and Control, Revised Edition 1976, by Edward Herceg, Schaevitz Engineering Publication, Pennsauken, New Jersey.

Handbook of Integrated-Circuit Operational Amplifiers, by George B. Rutkowski, Prentice Hall 1975, Englewood Cliffs, New Jersey.

NE555 AND NE556 APPLICATIONS AN170

INTRODUCTION

In mid 1972, Signetics introduced the 555 timer, a unique functional building block that has enjoyed unprecedented popularity. The timer's success can be attributed to several inherent characteristics foremost of which are versatility, stability and low cost. There can be no doubt that the 555 timer has altered the course of the electronics industry with an impact not unlike that of the I.C. operational amplifier.

The simplicity of the timer in conjunction with its ability to produce long time delays in a variety of applications has lured many designers from mechanical timers, op amps, and various discrete circuits into the ever increasing ranks of timer users.

DESCRIPTION

The 555 timer consists of two voltage comparators, a bistable flip-flop, a discharge transistor, and a resistor divider network. To understand the basic concept of the timer let's first examine the timer in block form as in Figure 1.

555/556 TIMER FUNCTIONAL BLOCK DIAGRAM

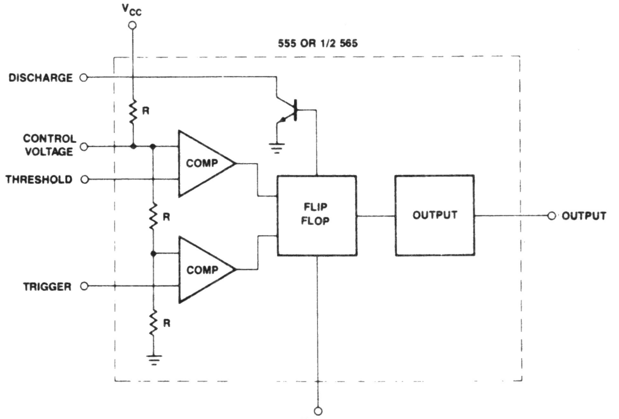


Figure 1

The resistive divider network is used to set the comparator levels. Since all three resistors are of equal value, the threshold comparator is referenced internally at 2/3 of supply voltage level and the trigger comparator is referenced at 1/3 of supply voltage. The outputs of the comparators are tied to the bistable flip-flop. When the trigger voltage is moved below 1/3 of the supply, the comparator changes state and sets the flip-flop driving the output to a high state. The threshold pin normally monitors the capacitor voltage of the RC timing network When the capacitor voltage exceeds 2/3 of the supply, the threshold comparator resets the flip-flop which in turn drives the output to a low state. When the output is in a low state, the discharge transistor is "on", hereby discharging the external timing capacitor. Once the capacitor is discharged, the timer will await another trigger pulse, the timing cycle having been completed.

The 555 and its complement, the 556 Dual Timer, exhibit a typical initial timing accuracy of 1% with a 50ppm/°C timing drift with temperature. To operate the timer as a one shot, only two external components are necessary; resistance & capacitance. For an oscillator, only one additional resistor is necessary. By proper selection of external components, oscillating frequencies from one cycle per half hour to 500KHz can be realized. Duty cycles can be adjusted from less than one percent to 99 percent over the frequency spectrum. Voltage control of timing and oscillation functions is also available,

Timer Circuitry

The timer is comprised of five distinct circuits; two voltage comparators, a resistive voltage divider reference, a bistable flip-flop, a discharge transistor, and an output stage that is the "totem pole" design for sink or source capability. Q_{10} - Q_{13} comprise a Darlington differential pair which serves as a trigger comparator. Starting with a positive voltage on the trigger; Q_{10} and Q_{11} turn on when the voltage at pin 2 is moved below one third of the supply voltage. The voltage level is derived from a resistive divider chain consisting of R_7, R_8 and R_9. All three resistors are of equal value (5K ohms). At fifteen volts supply, the triggering level would be five volts. When Q_{10} and Q_{11} turn on, they provide a base drive for Q_{15}, turning it on. Q_{16} and Q_{17} form a bistable flip-flop. When Q_{15} is saturated, Q_{16} is 'off' and Q_{17} is saturated. Q_{16} and Q_{17} will remain in these states even if the trigger is removed and Q_{15} is turned 'off'. While Q_{17} is saturated, Q_{20} and Q_{14} are turned off.

The output structure of the timer is a "totem pole"design, with Q_{22} and Q_{24} being large geometry transistors capable of providing 200mA with a fifteen volt supply. While Q_{20} is 'off', base drive is provided for Q_{22} by Q_{21}, thus providing a high output.

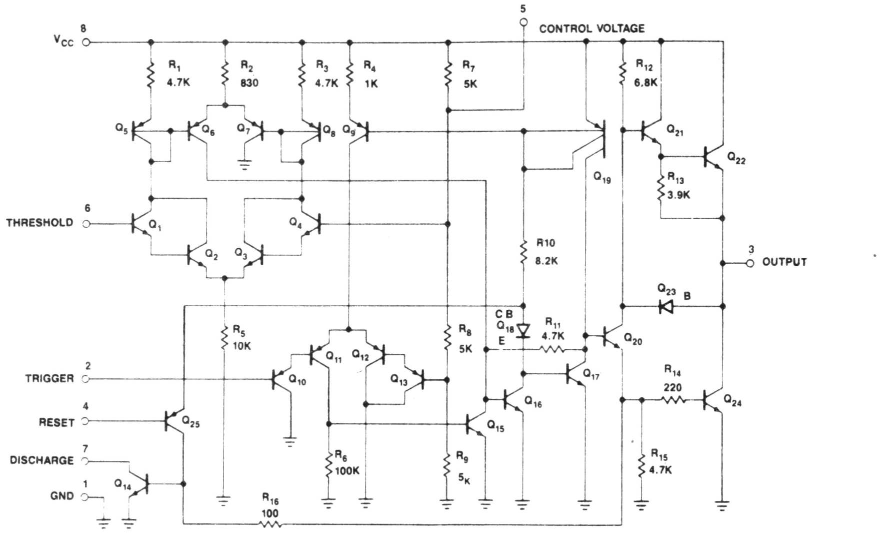
For the duration that the output is in a high state, the discharge transistor is 'off'. Since the collector of Q_{14} is typically connected to the external timing capacitor, C, while Q_{14} is off the timing capacitor now can charge thru the timing resistor, R_A.

The capacitor voltage is monitored by the threshold comparator (Q_1 - Q_4) which is a Darlington differential pair. When the capacitor voltage reaches two thirds of the supply voltage, the current is directed from Q_3 and Q_4 thru Q_1 and Q_2. Amplification of the current change is provided by Q_5 and Q_6. Q_5 - Q_6 and Q_7 - Q_8 comprise a diode-biased amplifier. The amplified current change from Q_6 now provides a base drive for Q_{16} which is part of the bistable flip-flop to change states. In doing so, the output is driven "low", and Q_{14} the discharge transistor is turned "on" shorting the timing capacitor to ground.

The discussion to this point has only encompassed the most fundamental of the timer's operating modes and circuitry. Several points of the circuit are brought out to the real world which allow the timer to function in a variety of modes. It is important; more than that, it is essential that one understands all the variations possible in order to utilize this device to its fullest extent.

NE555 AND NE556 APPLICATIONS

SCHEMATIC 555 OR 1/2 556 DUAL TIMER


5
CONTROL VOLTAGE
8
V_{CC}
R_1 4.7K
R_2 830
R_3 4.7K
R_4 1K
R_7 5K
R_{12} 6.8K
Q_5
Q_6
Q_7
Q_8
Q_9
Q_{19}
Q_{21}
Q_{22}
R_{13} 3.9K
6
THRESHOLD
Q_1
Q_2
Q_3
Q_4
R10 8.2K
3
OUTPUT
Q_{23} B
C B
Q_{18}
E
R_{11} 4.7K
Q_{20}
R_5 10K
R_8 5K
Q_{11}
Q_{12}
Q_{17}
2
TRIGGER
Q_{10}
Q_{13}
R_{14} 220
Q_{24}
4
RESET
Q_{25}
Q_{16}
Q_{15}
7
DISCHARGE
R_6 100K
R_9 5K
R_{15} 4.7K
1
GND
Q_{14}
R_{16} 100

ALL RESISTOR VALUES ARE IN OHMS

Figure 2

Reset Function

Regressing to the trigger mode, it should be noted that once the device has triggered and the bistable flip-flop set, continued triggering will not interfere with the timing cycle. However, there may come a time when it is necessary to interrupt or halt a timing cycle. This is the function that the reset accomplishes.

In the normal operating mode the reset transistor, Q_{25}, is off with its base held high. When the base of Q_{25} is grounded, it turns on, providing base drive to Q_{14}, turning it on. This discharges the timing capacitor, resets the flip-flop at Q_{17}, and drives the output low. The reset overrides all other functions within the timer.

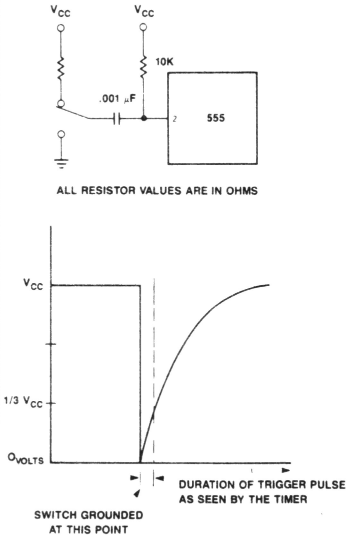
Trigger Requirements

Due to the nature of the trigger circuitry, the timer will trigger on the negative going edge of the input pulse. For the device to time out properly, it is necessary that the trigger voltage level be returned to some voltage greater than one third of the supply before the time out period. This can be achieved by making either the trigger pulse sufficiently short or by AC coupling into the trigger. By AC coupling the trigger, see Figure 3, a short negative going pulse is achieved when the trigger signal goes to ground. AC coupling is most frequently used in conjunction with a switch or a signal that goes to ground which initiates the timing cycle. Should the trigger be held low, without AC coupling, for a longer duration than the timing cycle the output will remain in a high state for the duration of the low trigger signal, without regard to the threshold comparator state. This is due to the predominance of Q_{15} on the base of Q_{16}, controlling the state of the bistable flip-flop. When the trigger signal then returns to a high level, the output will fall immediately. Thus, the output signal will follow the trigger signal in this case.

Control Voltage

One additional point of significance, the control voltage, is brought out on the timer. As mentioned earlier, both the trigger comparator, Q_{10} - Q_{13}, and the threshold comparator, Q_1 - Q_4, are referenced to an internal resistor divider network, R_7, R_8, R_9. This network establishes the nominal two thirds of supply voltage (Vcc) trip point for the threshold comparator and one third of

AC COUPLING OF THE TRIGGER PULSE


V_{CC}
V_{CC}
10K
.001 μF
2
555
V_{CC}
1/3 V_{CC}
0_{VOLTS}
DURATION OF TRIGGER PULSE AS SEEN BY THE TIMER
SWITCH GROUNDED AT THIS POINT

ALL RESISTOR VALUES ARE IN OHMS

Figure 3

Vcc for the trigger comparator. The two thirds point at the junction of R_7, R_8 and the base of Q_4 is brought out. By imposing a voltage at this point, the comparator reference levels may be shifted either higher or lower than the nominal levels of one third and two thirds of the supply voltage. Varying the voltage at this point will vary the timing. This feature of the timer opens a multitude of application possibilities such as using the timer as a voltage controlled oscillator, pulse width modulator, etc. For applications where the control voltage function is not used, it is strongly recommended that a bypass capacitor (.01μF) be place across the control voltage pin and ground. This will increase the noise immunity of the timer to high frequency trash which may monitor the threshold levels causing timing error.

Monostable Operation

The timer lends itself to three basic operating modes:

1. Monostable (one shot)
2. Astable (oscillatory)
3. Time delay

By utilizing any one or combination of basic operating modes and suitable variations it is possible to utilize the timer in a myriad of applications. The applications are limited only to the imagination of the designer.

One of the simplest and most widely used operating modes of the timer is the monostable (one shot). This configuration requires only two external components for operation (See Figure 4). The sequence of events starts when a voltage below one third Vcc is sensed by the trigger comparator. The trigger is normally applied in the form of a short negative going pulse. On the negative going edge of the pulse, the device triggers, the output goes high and the discharge transistor turns off. Note that prior to the input pulse, the discharge transistor is on, shorting the timing capacitor to ground. At this point the timing capacitor, C, starts charging thru the timing resistor, R. The voltage on the capacitor increases exponentially with a time constant T = RC. Ignoring capacitor leakage, the capacitor will reach the two thirds Vcc level in 1.1 time constants or

$$T = 1.1\ RC \tag{1}$$

where T is in seconds; R is in ohms and; C is in Farads. This voltage level trips the threshold comparator, which in turn drives the output low and turns on the discharge transistor. The transistor discharges the capacitor, C, rapidly. The timer has completed its cycle and will now await another trigger pulse.

MONOSTABLE OPERATION

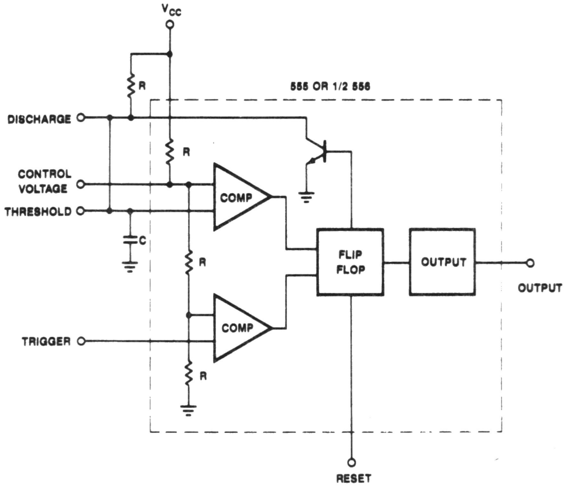


Figure 4

ASTABLE OPERATION

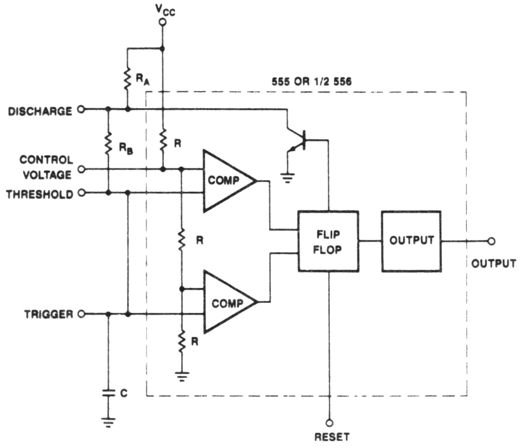


Figure 5

Astable Operation

In the astable (free run) mode, only one additional component, Rb is necessary. The trigger is now tied to the threshold pin. At power up, the capacitor is discharged, holding the trigger low. This triggers the timer, which establishes the capacitor charge path thru R_A and R_B. When the capacitor reaches the threshold level of 2/3 Vcc, the output drops low and the discharge transistor turns on.

The timing capacitor now discharges thru R_B. When the capacitor voltage drops to 1/3 Vcc, the trigger comparator trips, automatically retriggering the timer, creating an oscillator whose frequency is given by:

$$f = \frac{1.49}{(R_A + 2R_B)\ C} \qquad (2)$$

Selecting the ratios or R_A and R_B varies the duty cycle accordingly. Lo and behold, we have a problem. If a duty cycle of less than fifty percent is required, then what? Even if $R_A = 0$, the charge time cannot be made smaller than the discharge time because the charge path is $R_A + R_B$ while the discharge path is R_B alone. In this case it becomes necessary to insert a diode in parallel with R_B, cathode toward the timing capacitor. Another diode is desireable, but not mandatory, this one in series with R_B, cathode away from the timing capacitor. Now the charge path becomes R_A, thru the parallel diode into C. Discharge is thru the series diode and R_B to the discharge transistor. This scheme will afford a duty cycle range from less than 5% to greater than 95%. It should be noted that for reliable operation a minimum value of 3KΩ for R_B is recommended to assure that oscillation begins.

METHOD OF ACHIEVING DUTY CYCLES LESS THAN 50%

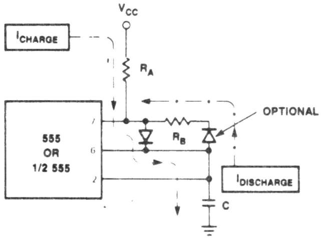


Figure 6

Time Delay

In this third basic operating mode, we aim to accomplish something a little different from monostable operation. In the monostable mode, when a trigger was applied, the output immediately changed to the high state, timed out, and returned to its pre-trigger low state. In the time delay mode, we require the output not to change state upon triggering, but at some precalculated time after trigger is received.

TIME DELAY OPERATION

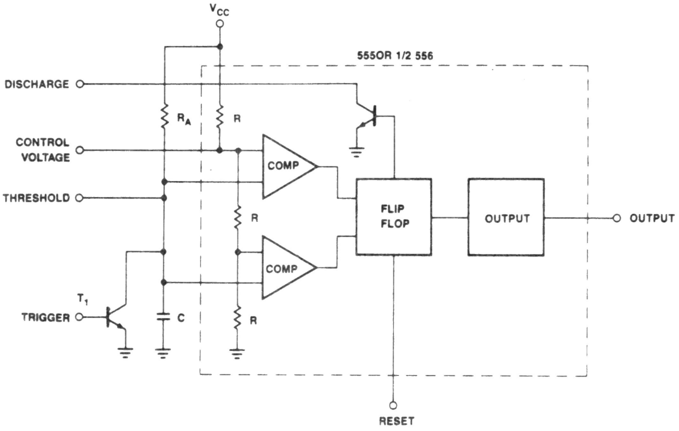


Figure 7

The threshold and trigger are tied together monitoring the capacitor voltage. The discharge function is not used. The operation sequence begins as transistor (T_1) is turned on, keeping the capacitor grounded. The trigger sees a low state and forces the timer output high. When the transistor is turned off the capacitor commences its charge cycle. When the capacitor reaches the threshold level, then and only then does the output change from its normally high state to the low state. The output will remain low until T_1 is again turned on.

GENERAL DESIGN CONSIDERATIONS

The timer will operate over a guaranteed voltage range of 4.5 volts to 15 volts DC, with 16 VDC being the absolute max. rating. Most of the devices, however, will operate at voltage levels as low as 3 VDC. The timing interval is independent of supply voltage since the charge rate and threshold level of the comparator are both directly proportional to supply. The supply volatage may be provided by any number of sources: however, several precautions should be taken. The most important, the one which provides the most headaches if not practiced, is good power supply filtering and adequate bypassing. Ripple on the supply line can cause loss of timing accuracy. The threshold level shifts causing a change of charging current. This will cause a timing error for that cycle.

Due to the nature of the output structure, a high power totem pole design, the output of the timer can exhibit large current spikes on the supply line. Bypassing is necessary to eliminate this phenomenon. A capacitor across the Vcc and ground, ideally, directly across the device is necessary. The size of capacitor will depend on the specific application. Values of capacitance from .01μF to 10μF are not uncommon. Note that the bypass capacitor would be as close to the device as physically possible.

Selecting External Components

In selecting the timing resistor and capacitor, there are several considerations to be taken into account.

Stable external components are necessary for the RC network if good timing accuracy is to be maintained. The timing resistor(s) should be of the metal film variety if timing accuracy and repeatability are important design criteria. The timer exhibits a typical initial accuracy of one percent. That is, with any one RC network, from timer to timer only one percent change is to be expected. Most of the initial timing error (i.e. deviation from the formula) is due to inaccuracies of external components. Resistors range from their rated values by .01% to 10 and 20 percent. Capacitors may have a 5 to 10 percent deviation from rated capacity. Therefore, in a system where timing is critical, an adjustable timing resistor or precision components are necessary. For best results, a good quality trim pot, placed in series with the largest feasible resistance will allow for best adjustability and performance.

The timing capacitor should be a high quality, stable component with very low leakage characteristics. *Under no circumstances should ceramic disc capacitors be used in the timing network!* Ceramic disc capacitors are not sufficiently stable in capacitance to operate properly in an RC mode. Several acceptable capacitor types are: silver mica, mylar, polycarbonate, polystyrene, tantulum or similar types.

The timer typically exhibits a small negative temperature coefficient (50ppm/°C). If timer accuracy over temperature is a consideration, timing components with a small positive temperature coefficient should be chosen. This combination will tend to cancel timing drift due to temperature.

In selecting the values for the timing resistors and capacitor, several points should be considered. A minimum value of threshold current is necessary to trip the threshold comparator. This value is .25μA. To calculate the maximum value of resistance, keep in mind that at the time the threshold current is required, the voltage potential on the threshold pin is two thirds of supply. Therefore:

$$\text{Vpotential} = V_{CC} - \text{Vcapacitor}$$

$$\text{Vpotential} = V_{CC} - 2/3\ V_{CC} = 1/3\ V_{CC}$$

Maximum resistance is then defined as

$$R_{max} = \frac{V_{CC} - V_{cap}}{I_{thresh}} \qquad (3)$$

Example: $V_{CC} = 15V$

$$R_{max} = \frac{15 - 10}{.25\ (10^{-6})} = 20M\Omega$$

$V_{CC} = 5V$

$$R_{max} = \frac{5 - 3.33}{.25\ (10^{-6})} \qquad 6.6M\Omega$$

NOTE: If using a large value of timing resistor, be certain that the capacitor leakage is significantly lower than the charging current available to minimize timing error.

On the other end of the spectrum, there are certain minimum values of resistance that should be observed. The discharge transistor, Q_{14}, is current limited at 35mA to 55mA internally. Thus, at the current limiting values, Q_{14}, establishes high saturation voltages. When examining the currents at Q_{14}, remember that the transistor, when turned on will be carrying two current loads. The first being the constant current thru timing resistor, R_A. The second will be the varying discharge current from the timing capacitor. To provide best operation the current contributed by the R_A path should be minimized so that the majority of discharge current can be used to reset the capacitor voltage. Hence it is recommended that a 5K ohm value be the minimum feasible value for R_A. This does not mean lower values cannot be used successfully in certain applications. Yet there are extreme cases that should be avoided if at all possible.

Capacitor size has not proven to be a legitimate design criteria. Values ranging from picofarads to greater than one thousand microfarads have been used successfully. One precaution need be utilized though. (It should be a cardinal rule that applies to the usage of all I C's.) Make certain that the package power dissipation is not exceeded. With extremely large capacitor values, a maximum duty cycle which allows some cooling time for the discharge transistor, may be necessary.

The most important characteristic of the capacitor should be as low a leakage as possible. Obviously any leakage will subtract from the charge count causing the calculated time to be longer than anticipated.

Control Voltage

Regressing momentarily, we recall that the control voltage pin is connected directly to the threshold comparator at the junction of R_7, or R_8. The combination of R_7, R_8 and R_9 comprise the resistive voltage divider network that establishes the nominal 1/3 Vcc trigger comparator level (junction R_8, R_9) and the 2/3 Vcc level for the threshold comparator (junction R_7, R_8).

For most applications, the control voltage function is not used and therefore is bypassed to ground with a small capacitor for noise filtering. The control voltage function, in other applications becomes an integral part of the design. By imposing a voltage at this pin, it becomes possible to vary the threshold comparator "set" level above or below the 2/3 Vcc nominal, hereby varying the timing. In the monostable mode, the control voltage may be varied from 45 percent to 90 percent of Vcc. The 45 to 90 percent figure is not firm, but only an indication to a safe usage. Control voltage levels below and above those stated have been used successfully in some applications.

In the oscillatory (free run) mode, the control voltage limitations are from 1.7 volts to Vcc. These values should be heeded for reliable operation. Keep in mind that in this mode the trigger level is also important. When the control voltage raises the threshold comparator level it also raise the trigger comparator level by one half that amount due to R_8 and R_9 of Figure 2. As a voltage controlled oscillator, one can expect ±25% around center frequency (f_o) to be virtually linear with a normal RC timing circuit. For wider linear variations around F_o it may be desireable to replace the charging resistor with a constant current source. In this manner the exponential charging characteristics of the classical configuration will be altered to linear charge time.

Reset Control

The only remaining function now is the reset. As mentioned earlier, the reset, when taken to ground, inhibits all device functioning. The output is driven low, the bistable flip-flop is reset, and the timing capacitor is discharged. In the astable (oscillatory) mode, the reset can be used to gate the oscillator. In the monostable it can be used as a timing abort to either interrupt a timing sequence or establish a standby mode (i.e. — device off during power up). It can also be used in conjunction with the trigger pin to establish a positive edge triggered circuit as opposed to the normal negative edge trigger mode. One thing to keep in mind when using the reset function is that the reset voltage (switching) point is between 0.4V and 1.0V (min/max). Therefore, if used in conjunction with the trigger, the device will be out of the reset mode prior to reaching 1 volt. At that point the trigger is in the "turn on" region, below 1/3 Vcc. This will cause the device to trigger immediately, effectively triggering on the positive going edge if a pulse is applied to pins 4 and 2 simultaneously.

FREQUENTLY ASKED APPLICATIONS QUESTIONS

The following is a harvest of various maladies, exceptions, and idiosyncracies that may exhibit themselves from time to time in various applications. Rather than cast aspersions, a quick review of this list may uncover a solution to the problem at hand.

1. In the oscillator mode when reset is released the *first time constant* is approximately *twice as long as the rest.* Why?

   Answer: In the oscillator mode the capacitor voltage fluctuates between 1/3 and 2/3 of the supply voltage. When reset is pulled down the capacitor discharges completely. Thus for the first cycle it must charge from ground to 2/3 Vcc which takes twice as long.

2. What is *maximum frequency of oscillations?*

   Answer: Most devices will oscillate about 1M Hz. However, in the interest of temperature stability one should operate only up to about 500kHz.

3. What is *temperature drift* for *oscillator mode?*

   Answer: Temperature drift of oscillator mode is 3 times that of one shot mode due to addition of second voltage comparator. Frequency always increases with an increasing temperature. Therefore it is possible to partially offset this drift with an offsetting temperature coefficient in the external resistor/capacitor combination.

4. Oscillator exhibits spurious *oscillations on cross over points.* Why?

   Answer: The 555 can oscillate due to feedback from power supply. Always bypass with sufficient capacitance close to the device for all applications.

5. Trying to drive a *relay* but 555 *hangs up.* How come?

   Answer: Inductive feedback. A clamp diode across the coil prevents the coil from driving pin 3 below a negative .6 volts. This negative voltage is sufficient in some cases to cause the timer to malfunction. The solution is to drive the relay through a diode thus preventing pin 3 from ever seeing a negative voltage.

6. Double triggering of the TTL loads sometimes occurs. Why?

   Answer: Due to the high current capability and fast rise and fall times of the output a totem pole structure different from the TTL classical structure was used. Near TTL threshold this output exhibits a cross over distortion which may double trigger logic. A 1000 pF capacitor from the output to ground will eliminate any false triggering.

7. What is the longest time I can get out of the timer?

   Answer: Times exceeding an hour are possible, but not always practical. Large capacitors with low leakage specs are quite expensive. It becomes cheaper to use a countdown scheme (see Figure 15) at some point dependent on required accuracy. Normally 20 to 30 min. is the longest feasible time.

DRIVING HIGH Q INDUCTIVE LOADS

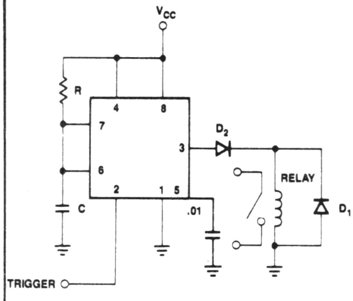
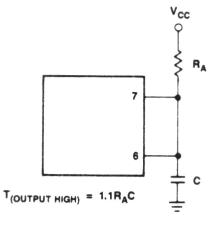


Figure 8

DESIGN FORMULAS

Before entering the section on specific applications it is advantageous to review the timing formulas. The formulas given here apply to the 555 and 556 devices.

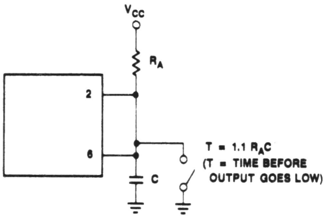
MONOSTABLE TIMING



$T_{(OUTPUT\ HIGH)} = 1.1 R_A C$

Figure 9a

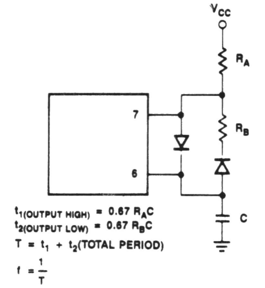
TRUE TIME DELAY



$T = 1.1 R_A C$
(T = TIME BEFORE OUTPUT GOES LOW)

Figure 9b

MODIFIED DUTY CYCLE (ASTABLE)



$t_{1(OUTPUT\ HIGH)} = 0.67\ R_A C$

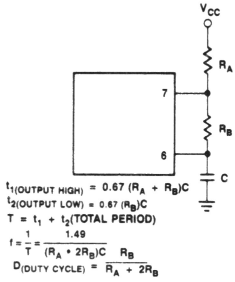
$t_{2(OUTPUT\ LOW)} = 0.67\ R_B C$

$T = t_1 + t_2 (TOTAL\ PERIOD)$

$f = \frac{1}{T}$

Figure 9c

ASTABLE TIMING



$t_{1(OUTPUT\ HIGH)} = 0.67\ (R_A + R_B)C$

$t_{2(OUTPUT\ LOW)} = 0.67\ (R_B)C$

$T = t_1 + t_2 (TOTAL\ PERIOD)$

$$f = \frac{1}{T} = \frac{1.49}{(R_A \bullet 2R_B)C}$$

$$D_{(DUTY\ CYCLE)} = \frac{R_B}{R_A + 2R_B}$$

Figure 9d

APPLICATIONS

The timer since introduction has spurred the imagination of thousands. Thus the ways in which this device has been used are far too numerous to present each one. A review of the basic operation and basic modes has previously been given. Presented here are some ingenious applications devised by our applications engineers and by some of our customers.

Missing Pulse Detector

Using the circuit of Figure 10a, the timing cycle is continuously reset by the input pulse train. A change in frequency, or a missing pulse, allows completion of the timing cycle which causes a change in the output level. For this application, the time delay should be set to be slightly longer than the normal time between pulses. Figure 10b shows the actual waveforms seen in this mode of operation.

SCHEMATIC DIAGRAM

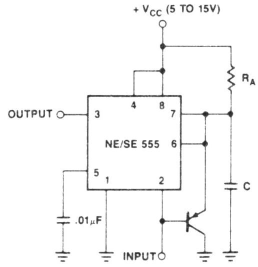

+VCC (5 TO 15V)
RA
OUTPUT
4
8
3
7
NE/SE 555
6
5
1
2
C
.01μF
INPUT

Figure 10a

EXPECTED WAVE FORMS

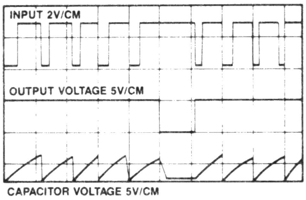


Figure 10b

Frequency Divider

If the input frequency is known, the timer can easily be used as a frequency divider by adjusting the length of the timing cycle.

SCHEMATIC DIAGRAM

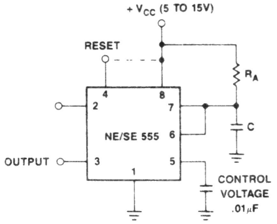

+VCC (5 TO 15V)
RESET
RA
4
8
2
7
NE/SE 555
6
C
OUTPUT
3
5
1
CONTROL
VOLTAGE
.01μF

Figure 11a

EXPECTED WAVE FORMS

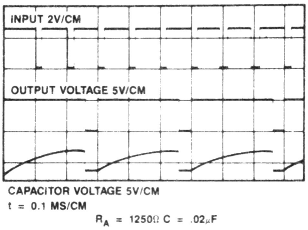


Figure 11b

Figure 11b shows the waveforms of the timer in Figure 11a when used as a divide by three circuit. This application makes use of the fact that this circuit cannot be retriggered during the timing cycle.

Pulse Width Modulation (PWM)

In this application, the timer is connected in the monostable mode as shown in Figure 12a. The circuit is triggered with a continuous pulse train and the threshold voltage is modulated by the signal applied to the control voltage terminal (pin 5). This has the effect of modulating the pulse width as the control voltage varies. Figure 12b shows the actual waveform generated with this circuit.

DEVICE SCHEMATIC

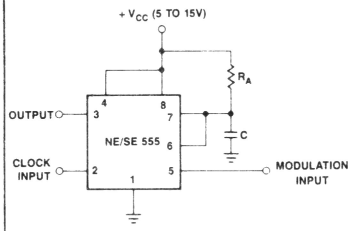

+VCC (5 TO 15V)
RA
OUTPUT
4
8
3
7
NE/SE 555
6
C
CLOCK
INPUT
2
5
1
MODULATION
INPUT

Figure 12a

EXPECTED WAVE FORMS

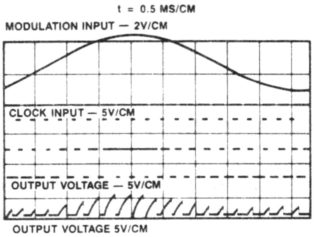


Figure 12b

Pulse Position Modulation (PPM)

This application uses the timer connected for astable (free-running) operation. Figure 13a, with a modulating signal again applied to the control voltage terminal. Now the pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. Figure 13b shows the waveform generated for triangle wave modulation signal.

SCHEMATIC DIAGRAMS

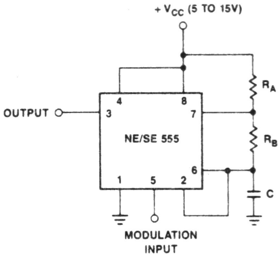

+VCC (5 TO 15V)
RA
OUTPUT
4
8
3
7
NE/SE 555
RB
6
1
5
2
C
MODULATION
INPUT

Figure 13a

EXPECTED WAVE FORMS

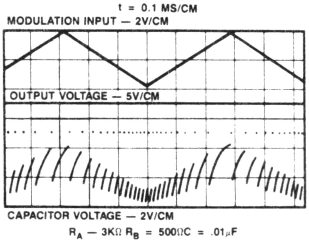
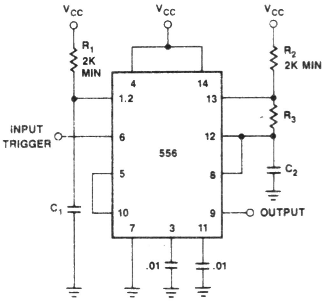


Figure 13b

TONE BURST GENERATOR


VCC
VCC
VCC
R1
2K
MIN
R2
2K MIN
4
14
1.2
13
R3
INPUT
TRIGGER
6
12
556
5
8
C2
C1
10
9
OUTPUT
7
3
11
.01
.01

ALL RESISTOR VALUES ARE IN OHMS

Figure 14

Tone Burst Generator

The 556 Dual Timer makes an excellent tone burst generator. The first half is connected as a one shot and the second half as an oscillator. (Figure 14)

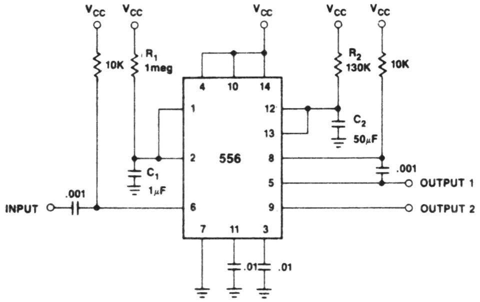
The pulse established by the one shot turns on the oscillator allowing a burst to be generated.

Sequential Timing

One feature of the dual timer is that by utilizing both halves it is possible to obtain sequential timing. By connecting the output of the first half to the input of the second half via a .001μfd coupling capacitor sequential timing may be obtained. Delay t_1 is determined by the first half and t_2 by the second half delay. (Figure 15)

The first half of the timer is started by momentarily connected pin 6 to ground. When it is timed out (determined by 1.1 R_1C_1) the second half begins. Its duration is determined by 1.1 R_2C_2.

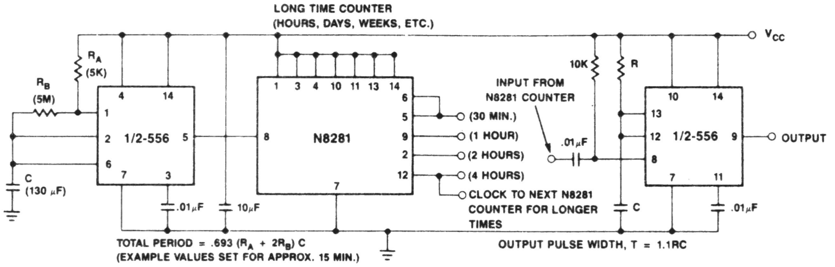
SEQUENTIAL TIMER


V_{CC}
V_{CC}
V_{CC}
V_{CC}
V_{CC}
10K
R_1 1meg
4
10
14
1
12
13
2
556
8
5
6
9
7
11
3
R_2 130K
10K
C_2 50μF
C_1 1μF
.001
.001
INPUT
OUTPUT 1
OUTPUT 2
.01
.01

ALL RESISTOR VALUES ARE IN OHMS

Figure 15

METHOD OF ACHIEVING LONG TIME DELAYS


LONG TIME COUNTER
(HOURS, DAYS, WEEKS, ETC.)
V_{CC}
R_A (5K)
R_B (5M)
4
14
1
2
1/2-556
5
6
7
3
C (130 μF)
.01μF
10μF
1
3
4
10
11
13
14
8
N8281
6
5
9
2
12
7
(30 MIN.)
(1 HOUR)
(2 HOURS)
(4 HOURS)
CLOCK TO NEXT N8281 COUNTER FOR LONGER TIMES
INPUT FROM N8281 COUNTER
10K
R
.01μF
C
10
14
13
12
1/2-556
9
8
7
11
OUTPUT
.01μF
TOTAL PERIOD = .693 (R_A + $2R_B$) C
(EXAMPLE VALUES SET FOR APPROX. 15 MIN.)
OUTPUT PULSE WIDTH, T = 1.1RC

ALL RESISTOR VALUES ARE IN OHMS

Figure 16

Long Time Delays

In the 556 timer the timing is a function of the charging rate of the external capacitor. For long time delays expensive capacitors with extremely low leakage are required. the practicality of the components involved limits the time between pulses to something in the neighborhood of twenty minutes.

To achieve longer time periods both halves may be connected in tandem with a "divide-by" network in between.

The first timer section operates in an oscillatory mode with a period of $1/f_o$. This signal is then applied to a "Divide-by-N" network to give an output with the period of N/f_o. This can then be used to trigger the second half of the 556. The total time is now a function of N and f_o (Figure 16).

Speed Warning Device (1)

Utilizing the "missing pulse detector" concept, a speed warning device, such as depicted, becomes a simple and inexpensive circuit (Figure 17a).

Car Tachometer (1)

The timer receives pulses from the distributor points. Meter M receives a calibrated current thru R_6 when the timer output is high. After time out the meter receives no current for that part of the duty cycle. Integration of the variable duty cycle by the meter movement provides a visible indication of engine speed (Figure 18).

SCHEMATIC OF SPEED WARNING DEVICE

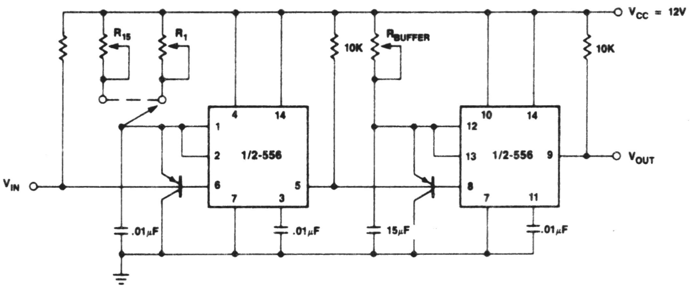

V_{CC} = 12V
R_{15}
R_1
10K
R_{BUFFER}
10K
4
14
1
2
1/2-556
6
5
7
3
10
14
12
13
1/2-556
9
8
7
11
V_{IN}
V_{OUT}
.01μF
.01μF
15μF
.01μF

Figure 17a

OPERATING WAVE FORMS OF SPEED WARNING DEVICE

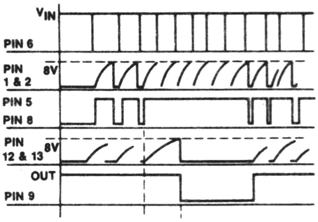
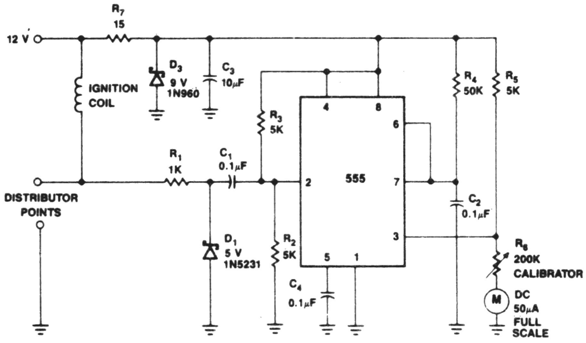


Figure 17b

TACHOMETER


R_7
15
12 V
D_3
9 V
1N960
C_3
10μF
IGNITION COIL
R_3
5K
4
8
6
555
2
7
3
5
1
R_4
50K
R_5
5K
R_1
1K
C_1
0.1μF
DISTRIBUTOR POINTS
D_1
5 V
1N5231
R_2
5K
C_4
0.1μF
C_2
0.1μF
R_6
200K
CALIBRATOR
M
DC
50μA
FULL SCALE

ALL RESISTOR VALUES ARE IN OHMS

Figure 18

Oscilloscope Triggered Sweep

The 555 timer holds down the cost of adding a triggered sweep to an economy oscilloscope. The circuit's input op amp triggers the timer, setting its flip-flop and cutting off its discharge transistor so that capacitor C can charge. When capacitor voltage reaches the timer's control voltage ($0.33V_{CC}$), the flip-flop resets and the transistor conducts, discharging the capacitor (Figure 19).

Greater linearity can be achieved by substituting a constant current source for the frequency adjust resistor (R).

Square Wave Tone Burst Generator (4)

Depressing the pushbutton provides square-wave tone bursts whose duration depends on the duration for which the voltage at pin 4 exceeds a threshold. Components R_1, R_2 and C_1 causes the astable action of the timer IC (Figure 6-20).

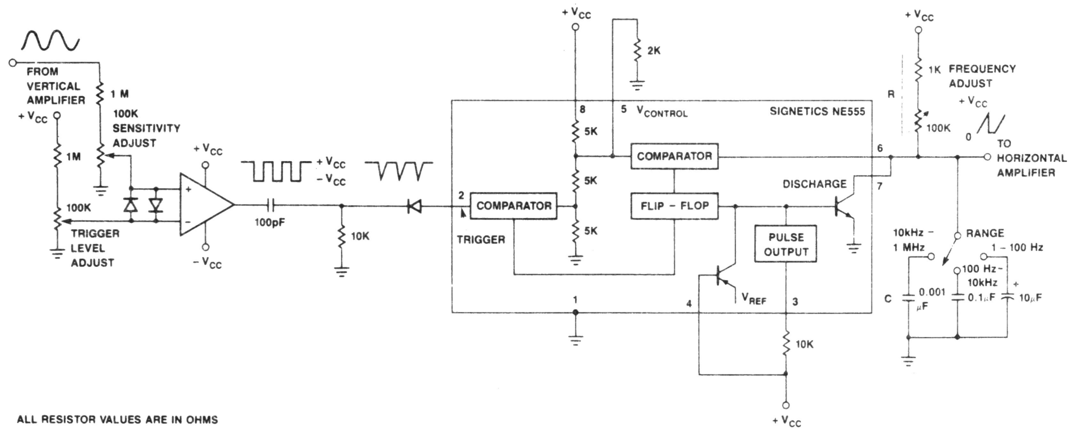
Regulated DC-to-DC Converter (2)

Regulated DC to DC converter produces 15V DC outputs from a +5V DC input. Line and load regulation is 0.1% (Figure 21).

Voltage to Pulse Duration Converter (1)

Voltage levels can be converted to pulse durations by combining an op amp and a timer IC. Accuracies to better than 1% can be obtained with this circuit (a) and the output signals (b) still retain the original frequency, independent of the input voltage (Figure 22).

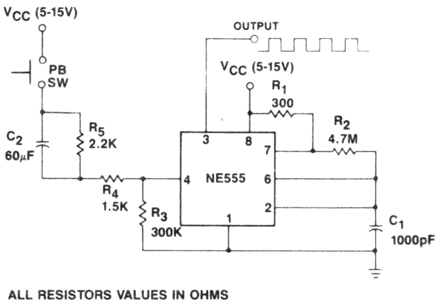
SCHEMATIC OF TRIGGERED SWEEP


FROM VERTICAL AMPLIFIER
1 M
+Vcc
100K SENSITIVITY ADJUST
1M
100K
TRIGGER LEVEL ADJUST
+Vcc
-Vcc
100pF
+Vcc
-Vcc
10K
+Vcc
2K
8
5 VCONTROL
SIGNETICS NE555
5K
COMPARATOR
5K
2
COMPARATOR
TRIGGER
FLIP - FLOP
5K
DISCHARGE
PULSE OUTPUT
1
4
VREF
3
10K
+Vcc
6
7
+Vcc
1K FREQUENCY ADJUST
R
+Vcc
100K
0
TO HORIZONTAL AMPLIFIER
10kHz - 1 MHz
RANGE
1 - 100 Hz
100 Hz - 10kHz
C
0.001 μF
0.1μF
10μF

ALL RESISTOR VALUES ARE IN OHMS

Figure 19

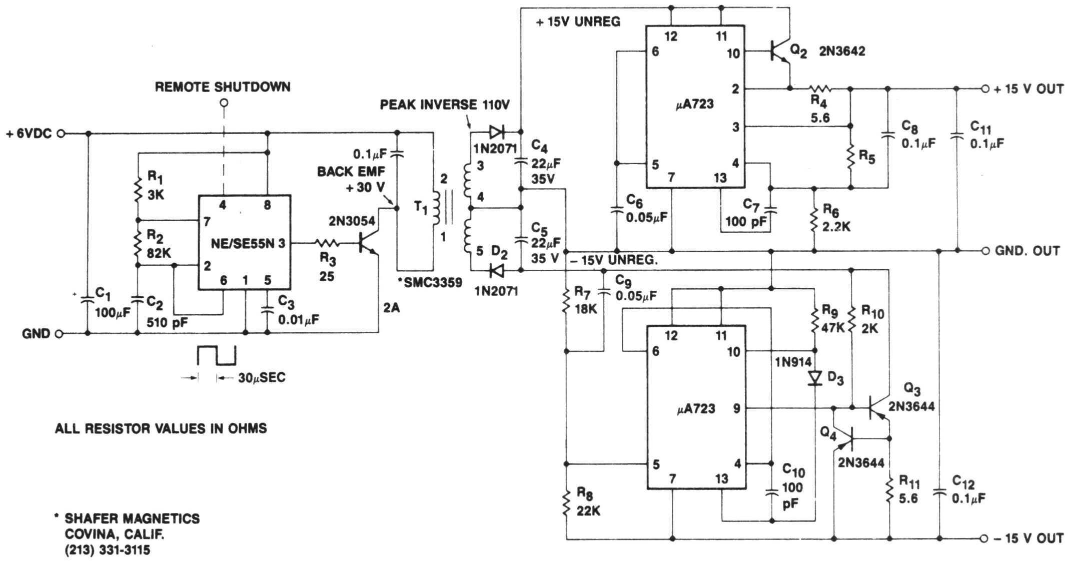
SQUARE WAVE TONE BURST GENERATOR


VCC (5-15V)
PB SW
C2 60μF
R5 2.2K
R4 1.5K
R3 300K
OUTPUT
VCC (5-15V)
R1 300
R2 4.7M
3
8
7
4
NE555
6
2
1
C1 1000pF

ALL RESISTORS VALUES IN OHMS

Figure 20

REGULATED DC TO DC CONVERTER

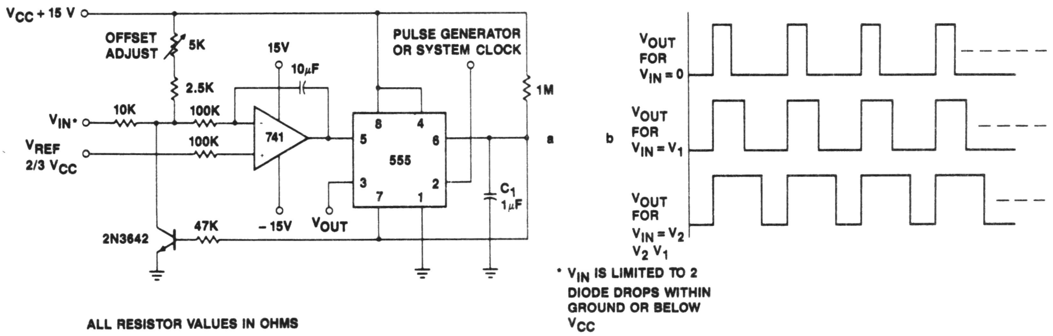

+15V UNREG
REMOTE SHUTDOWN
PEAK INVERSE 110V
+6VDC
0.1μF
BACK EMF
+30 V
R1
3K
R2
82K
4
8
7
NE/SE55N 3
2
6 1 5
2N3054
R3
25
T1
2
1
3
4
5
1N2071
C4
22μF
35V
C5
22μF
35 V
D2
1N2071
*SMC3359
2A
C1
100μF
C2
510 pF
C3
0.01μF
GND
30μSEC
12
11
6
10
Q2 2N3642
2
μA723
3
5
4
7
13
R4
5.6
R5
C8
0.1μF
C11
0.1μF
+15 V OUT
C6
0.05μF
C7
100 pF
R6
2.2K
−15V UNREG.
GND. OUT
R7
18K
C9
0.05μF
R9
47K
R10
2K
1N914
D3
μA723 9
Q3
2N3644
Q4
2N3644
C10
100
pF
R8
22K
R11
5.6
C12
0.1μF
−15 V OUT

ALL RESISTOR VALUES IN OHMS

* SHAFER MAGNETICS
COVINA, CALIF.
(213) 331-3115

Figure 21

VOLTAGE-TO-PULSE-DURATION CONVERTER


V_{CC} + 15 V
OFFSET
ADJUST
5K
2.5K
15V
10μF
PULSE GENERATOR
OR SYSTEM CLOCK
1M
V_{IN}*
10K
100K
100K
V_{REF}
2/3 V_{CC}
741
8
4
5
6
555
3
2
7
1
a
b
C1
1μF
2N3642
47K
−15V
V_{OUT}
V_{OUT}
FOR
V_{IN} = 0
V_{OUT}
FOR
V_{IN} = V_1
V_{OUT}
FOR
V_{IN} = V_2
V_2 V_1

* V_{IN} IS LIMITED TO 2 DIODE DROPS WITHIN GROUND OR BELOW V_{CC}

ALL RESISTOR VALUES IN OHMS

Figure 22

Servo System Controller (1)

To control a servo motor remotely, the 555 needs only six extra components (Figure 6-23).

Stimulus Isolator (5)

Stimulus isolator uses a photo-SCR and a toroid for shaping pulses of up to 200V at 200μA (Figure 24).

Voltage to Frequency Converter (0.2% Accuracy) (6)

Linear voltage-to-frequency converter (a) achieves good linearity over the 0 to − 10V. Its mirror image (b) provides the same linearity over the 0-to + 10V range but is not DTL/TTL compatible (Figure 25a & b).

SERVO SYSTEM CONTROLLER

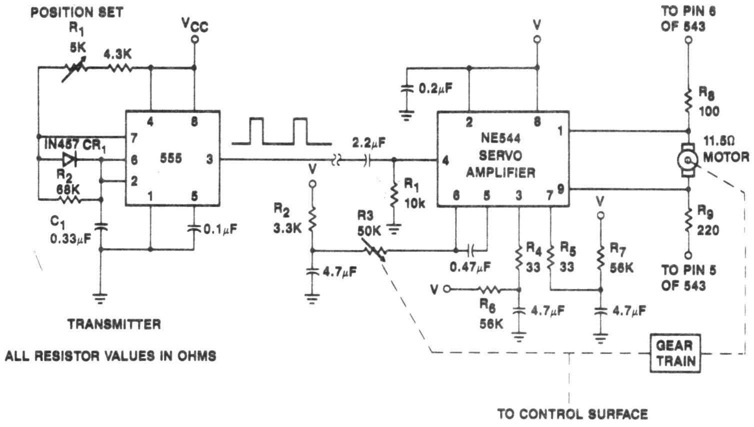

POSITION SET
R1
5K
4.3K
VCC
IN457 CR1
R2
68K
C1
0.33µF
555
0.1µF
TRANSMITTER
ALL RESISTOR VALUES IN OHMS
2.2µF
V
R2
3.3K
4.7µF
R3
50K
R1
10k
0.2µF
NE544
SERVO
AMPLIFIER
0.47µF
R4
33
R5
33
R7
56K
V
R6
56K
4.7µF
4.7µF
TO PIN 6
OF 543
R8
100
11.5Ω
MOTOR
R9
220
TO PIN 5
OF 543
GEAR
TRAIN
TO CONTROL SURFACE

Figure 23

STIMULUS ISOLATOR

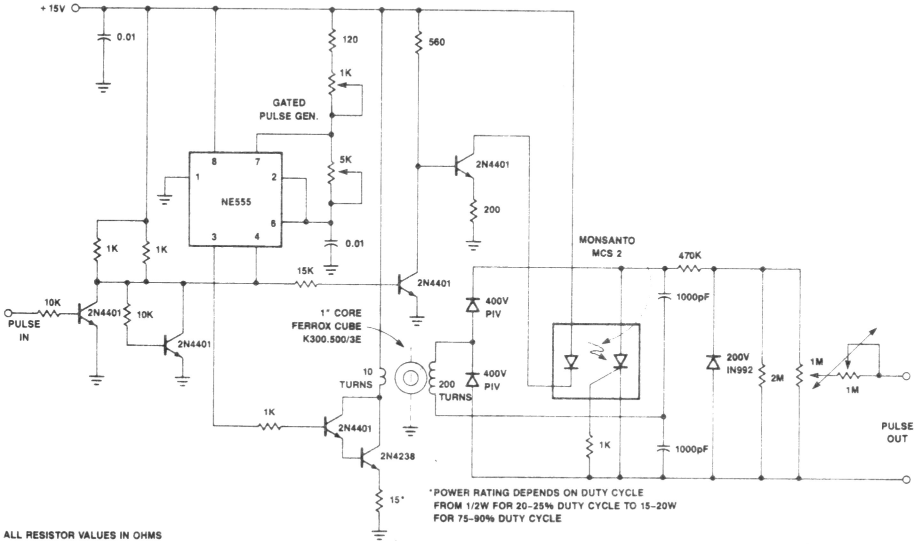
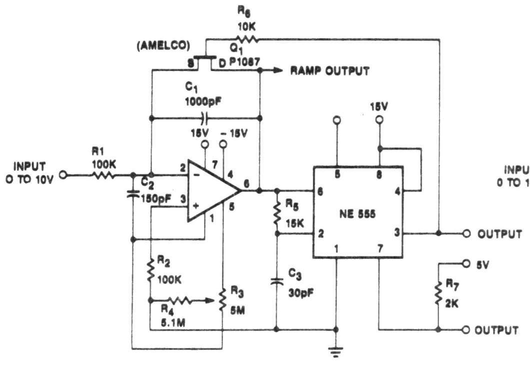

+15V
0.01
120
1K
GATED
PULSE GEN.
5K
0.01
NE555
560
2N4401
200
1K
1K
15K
2N4401
10K
PULSE
IN
2N4401
10K
2N4401
1" CORE
FERROX CUBE
K300.500/3E
10
TURNS
200
TURNS
400V
PIV
400V
PIV
1K
2N4401
2N4238
15*
MONSANTO
MCS 2
470K
1000pF
1K
1000pF
200V
IN992
2M
1M
1M
PULSE
OUT
*POWER RATING DEPENDS ON DUTY CYCLE
FROM 1/2W FOR 20-25% DUTY CYCLE TO 15-20W
FOR 75-90% DUTY CYCLE
ALL RESISTOR VALUES IN OHMS

Figure 24

VOLTAGE-TO-FREQUENCY CONVERTER (0.2% ACCURACY)


R6
10K
(AMELCO)
Q1
S
D P1087
RAMP OUTPUT
C1
1000pF
15V
15V
-15V
R1
100K
INPUT
0 TO 10V
C2
150pF
R5
15K
NE 555
OUTPUT
5V
R7
2K
R2
100K
R4
5.1M
R3
5M
C3
30pF
OUTPUT

ALL RESISTOR VALUES IN OHMS

Figure 25a

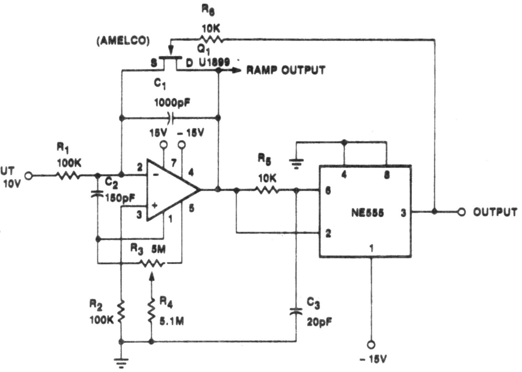

R6
10K
(AMELCO)
Q1
S
D U1899
RAMP OUTPUT
C1
1000pF
15V
-15V
R1
100K
INPUT
0 TO 10V
C2
150pF
R5
10K
NE555
OUTPUT
R3 5M
R2
100K
R4
5.1M
C3
20pF
-15V

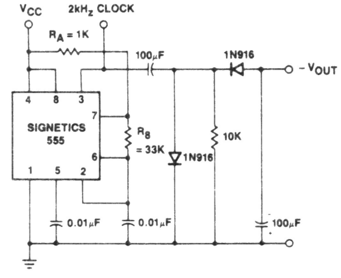
Figure 25b

Positive to Negative Converter (7)

Transformerless dc-dc converter derives a negative supply voltage from a positive. As a bonus the circuit also generates a clock signal.

The negative output voltage tracks the dc input voltage linearity (a), but its magnitude is about 3V lower. Application of a 500Ω load, (b), causes 10% change from the no-load value (Figure 26a, b, & c).

POSITIVE TO NEGATIVE CONVERTER


VCC
2kHz CLOCK
RA = 1K
100μF
1N916
-VOUT
SIGNETICS
555
R8
= 33K
10K
1N916
0.01μF
0.01μF
100μF

ALL RESISTOR VALUES ARE IN OHMS

Figure 26a

Auto Burglar Alarm (8)

Timer A produces a safeguard delay, allowing driver to disarm alarm and eliminating vulnerable outside control switch. The SCR prevents timer A from triggering timer B, unless timer B is triggered by strategically located sensor switches (Figure 27).

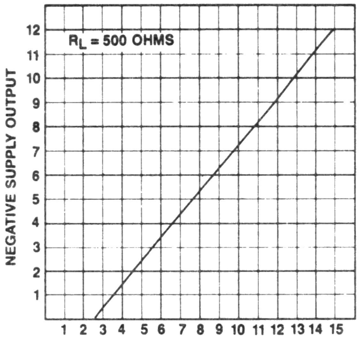


Figure 26b

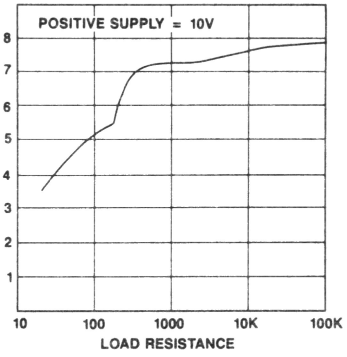


Figure 26c

Cable Tester (9)

Compact tester checks cables for open-circuit or short-circuit conditions. A differential transistor pair at one end of each cable line remains balanced as long as the same clock pulse-generated by the timer IC - appears at both ends of the line. A clock pulse just at the clock end of the line lights green light-emitting diode, and a clock pulse only at the other end lights a red LED (Figure 28).

Low Cost Line Receiver (10)

The timer makes an excellent line receiver for control applications involving relatively slow electro-mechanical devices. It can work without special drivers over single unshielded lines (Figure 29).

AUTO BURGLAR ALARM

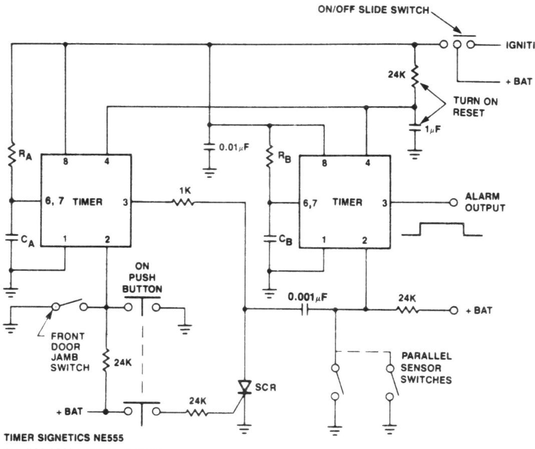

ON/OFF SLIDE SWITCH
IGNITION
+ BAT
24K
TURN ON RESET
1μF
0.01μF
R_A
R_B
8
4
6, 7 TIMER 3
1
2
1K
C_A
C_B
6,7 TIMER 3
ALARM OUTPUT
ON PUSH BUTTON
0.001μF
24K
+ BAT
FRONT DOOR JAMB SWITCH
24K
PARALLEL SENSOR SWITCHES
SCR
+ BAT
24K
TIMER SIGNETICS NE555
ALL RESISTOR VALUES IN OHMS

Figure 27

CABLE TESTER

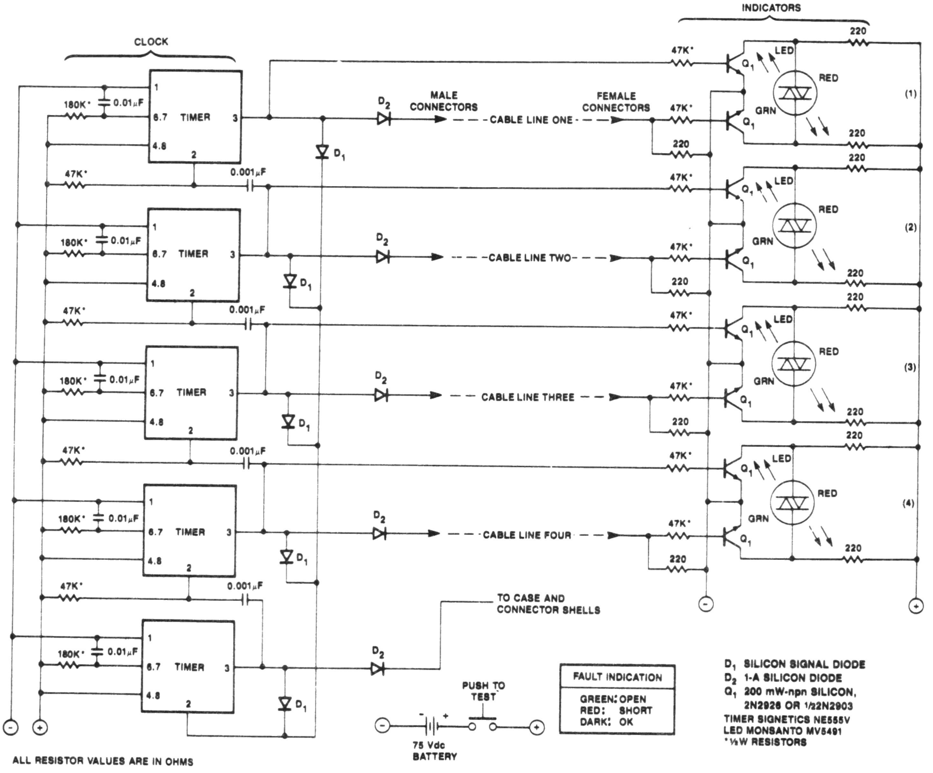
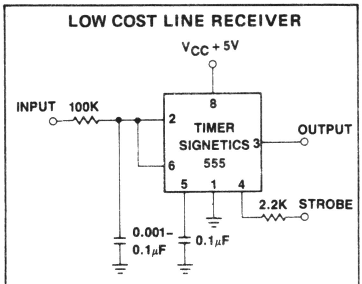

INDICATORS
CLOCK
220
47K*
LED
Q_1
RED
(1)
(2)
(3)
(4)
GRN
1
6.7 TIMER 3
4.8
2
180K*
0.01μF
47K*
0.001μF
D_1
D_2
MALE CONNECTORS
FEMALE CONNECTORS
CABLE LINE ONE
CABLE LINE TWO
CABLE LINE THREE
CABLE LINE FOUR
TO CASE AND CONNECTOR SHELLS
PUSH TO TEST
75 Vdc BATTERY
FAULT INDICATION
GREEN: OPEN
RED: SHORT
DARK: OK
D_1 SILICON SIGNAL DIODE
D_2 1-A SILICON DIODE
Q_1 200 mW-npn SILICON, 2N2926 OR 1/22N2903
TIMER SIGNETICS NE555V
LED MONSANTO MV5491
* ½W RESISTORS
ALL RESISTOR VALUES ARE IN OHMS

Figure 28


LOW COST LINE RECEIVER
VCC + 5V
INPUT 100K
8
2
TIMER
SIGNETICS 3
555
6
5 1 4
OUTPUT
2.2K STROBE
0.001-
0.1μF
0.1μF

ALL RESISTOR VALUES ARE IN OHMS

Figure 29

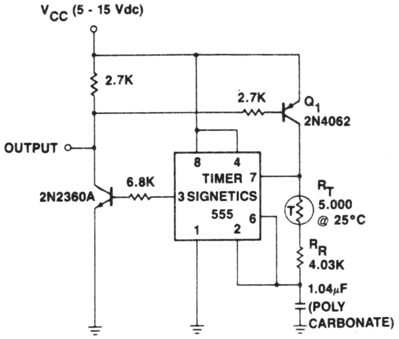
Temperature Control (11)

A couple of transistors and thermistor in the charging network of the 555-type timer enable this device to sense temperature and produce a corresponding frequency output. The circuit is accurate to within ±1 Hertz over a 78°F temperature range (Figure 30a & b).

Automobile Voltage Regulator (12)

Monolithic 555-type timer is the heart of this simple automobile voltage regulator. When the timer is off so that its output (pin 3) is low, the power Darlington transistor pair is off. If battery voltage becomes too low (less than 14.4 volts in this case), the timer turns on and the Darlington pair conducts (Figure 31).

TEMPERATURE CONTROL


VCC (5 - 15 Vdc)
2.7K
2.7K
Q1
2N4062
OUTPUT
8 4
TIMER 7
3 SIGNETICS
555 6
1 2
6.8K
2N2360A
RT
5.000
@ 25°C
T
RR
4.03K
1.04μF
(POLY
CARBONATE)

ALL RESISTOR VALUES ARE IN OHMS

Figure 30a

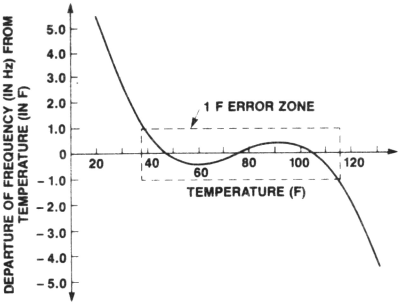
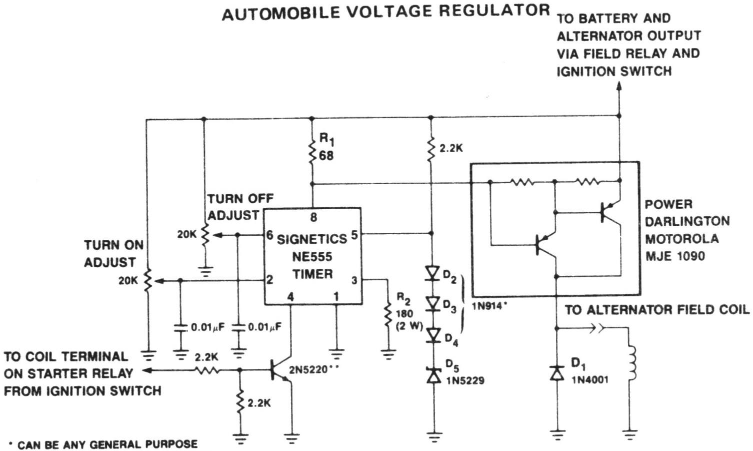


Figure 30b


AUTOMOBILE VOLTAGE REGULATOR
TO BATTERY AND ALTERNATOR OUTPUT VIA FIELD RELAY AND IGNITION SWITCH
R1
68
2.2K
TURN OFF ADJUST
20K
8
6 SIGNETICS 5
NE555
TIMER
2
3
4 1
TURN ON ADJUST
20K
0.01μF
0.01μF
R2
180
(2 W)
D2
D3
D4
1N914*
D5
1N5229
POWER DARLINGTON MOTOROLA MJE 1090
TO ALTERNATOR FIELD COIL
D1
1N4001
TO COIL TERMINAL ON STARTER RELAY FROM IGNITION SWITCH
2.2K
2N5220**
2.2K

* CAN BE ANY GENERAL PURPOSE SILICON DIODES OR 1N4157 DEVICE

** CAN BE ANY GENERAL PURPOSE SILICON TRANSISTOR

ALL RESISTOR VALUES ARE IN OHMS

Figure 31

Switching Regulator (13)

The basic regulator of Figure 32 is shown here with its associated timing and pulse generating circuitry. The block diagram illustrates how the over-all regulator works. The multivibrator determines switching frequency, and the error amplifier adjusts the pulse width of the modulator to maintain output voltage at the desired level. The output resistor divider provides the sensing voltage. (Figure 35).

DC-to-DC Converter (14)

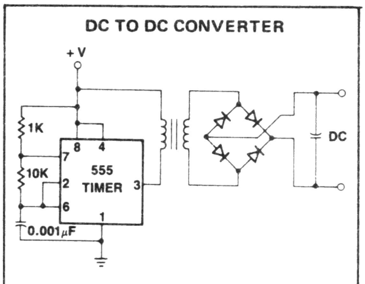

DC TO DC CONVERTER
+V
1K
10K
8
4
7
2
6
1
3
555
TIMER
0.001µF
DC

Figure 32

Ramp Generator (14)

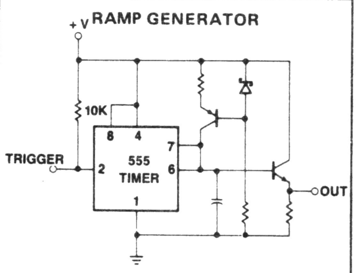

+V RAMP GENERATOR
10K
8
4
7
6
2
1
555
TIMER
TRIGGER
OUT

Figure 33

Audio Oscillator (14)

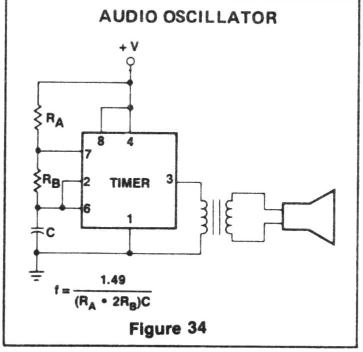

AUDIO OSCILLATOR
+V
R_A
R_B
C
8
4
7
2
6
1
3
TIMER
f = 1.49 / (R_A + 2R_B)C

Figure 34

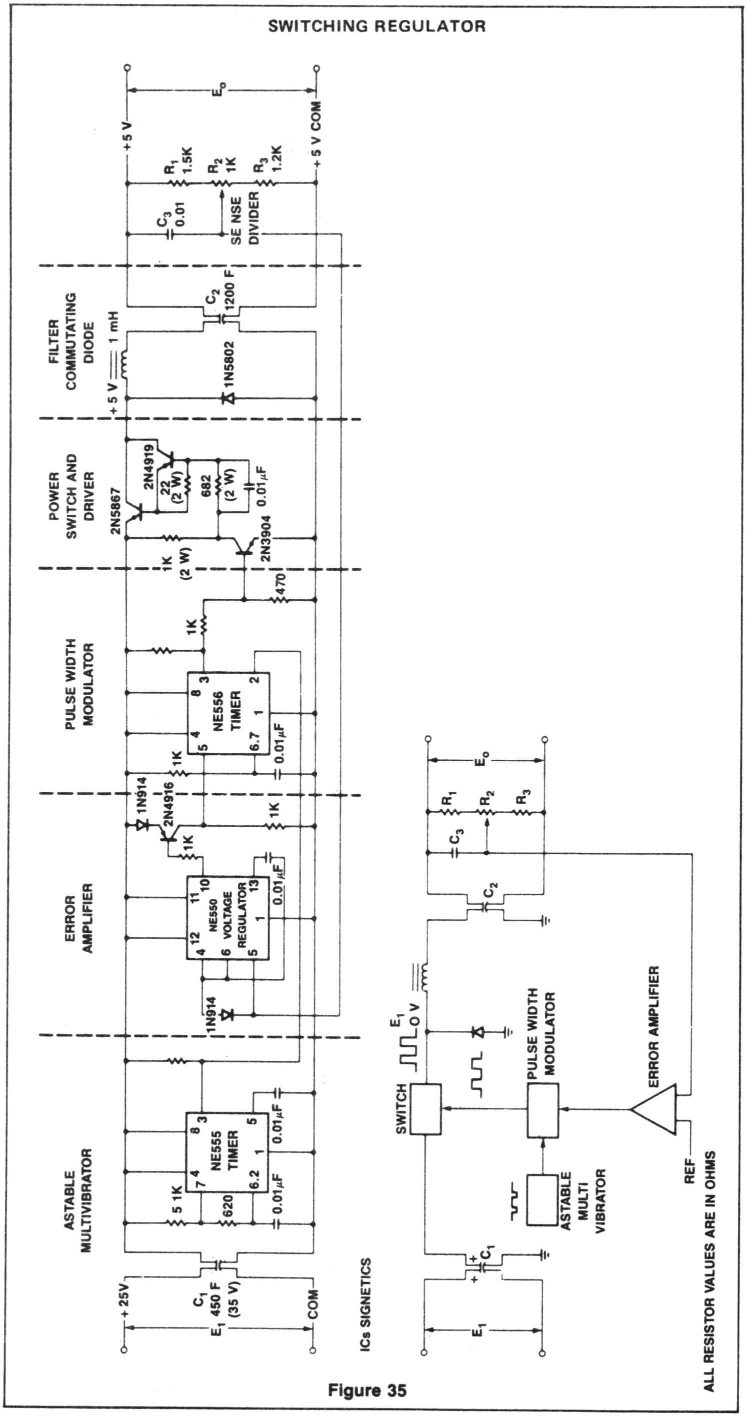

SWITCHING REGULATOR
E_o
+5 V
+5 V COM
R_1 1.5K
R_2 1K
R_3 1.2K
C_3 0.01
SE NSE DIVIDER
C_2 1200 F
1 mH
1N5802
FILTER COMMUTATING DIODE
POWER SWITCH AND DRIVER
2N5867
2N4919
22 (2 W)
682 (2 W)
0.01µF
2N3904
1K (2 W)
470
1K
PULSE WIDTH MODULATOR
NE556 TIMER
0.01µF
1N914
2N4916
1K
ERROR AMPLIFIER
NE550 VOLTAGE REGULATOR
0.01µF
1N914
ASTABLE MULTIVIBRATOR
NE555 TIMER
0.01µF
5 1K
620
+25V
C_1 450 F (35 V)
E_1
COM
ICs SIGNETICS
E_1
0 V
SWITCH
PULSE WIDTH MODULATOR
ERROR AMPLIFIER
ASTABLE MULTI VIBRATOR
REF
C_1
C_2
C_3
R_1
R_2
R_3
E_o
ALL RESISTOR VALUES ARE IN OHMS

Figure 35

Low Power Monostable Operation

In battery operated equipment where load current is a significant factor figure 36 can deliver 555 monostable operation at low standby power. This circuit interfaces directly with CMOS 4000 series and 74L00 series. During the monostable time, the current drawn is 4.5mA for T = 1.1RC. The rest of the time the current drawn is less than 50µA. Circuit submitted by Karl Imhof, Executone Inc., Long Island City, NY.

In other low power operations of the timer where Vcc is removed until timing is needed, it is necessary to consider the output load. If the output is driving the base of a PNP transistor, for example, and its power is not removed, it will sink current into pin 3 to ground and use excessive power. Therefore, when driving these types of loads, one should recall this internal sinking path of the timer.

LOW POWER MONOSTABLE

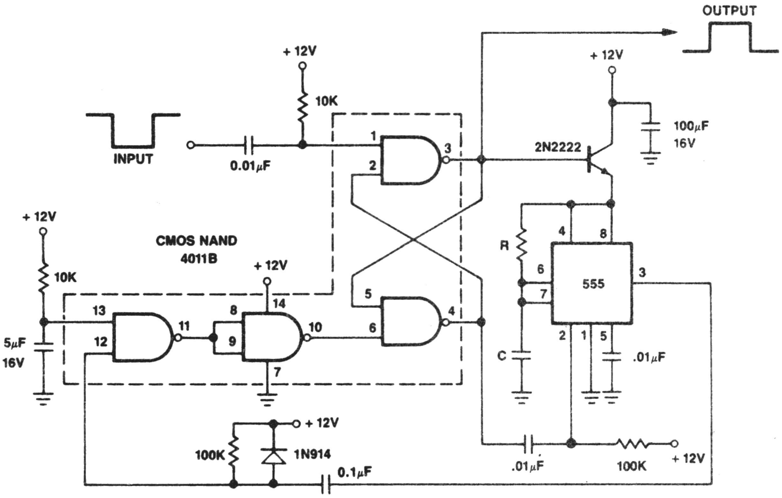


Figure 36

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9. **"Timer IC's And LEDs form Cable Tester"**, L. W. Herring, *Electronics*, May 10, 1973, pp. 115.
10. **"IC Timer Can Function As Low Cost Line Receiver"**, John Pate, *Electronics*, June 21, 1973, pp. 132.
11. **"IC Timer Plus Thermister Can Control Temperature"**, Donald Dekold, *Electronics*, June 21, 1973, pp. 132.
12. **"IC Timer Makes Economical Automobile Voltage Regulator"**, T. J. Fusar, *Electronics*, February 21, 1974, pp. 100.
13. **"Switching Regulators, The Efficient Way to Power"**, Robert Olla, *Electronics*, August 16, 1973, pp. 94-95.
14. **"Put The IC Timer To Work in A Myriad Of Ways"**, Eugene Hnatek, *EDN*, March 5, 1973, pp. 54-58.

NE558 APPLICATIONS

AN171

INTRODUCTION

The 558 is a monolithic Quad Timer designed to be used in the timing range from a few microseconds to a few hours. Four entirely independent timing functions can be acheived, using a timing resistor and capacitor for each section. Two sections of the quad may be interconnected for astable operation. All four sections may be used together, in tandem, for sequential timing applications up to several hours. No coupling capacitors are required when connecting the output of one timer section to the input of the next.

FEATURES

- **100mA OUTPUT CURRENT PER SECTION**
- **EDGE TRIGGERED (NO COUPLING CAPACITOR)**
- **OUTPUT INDEPENDENT OF TRIGGER CONDITIONS**
- **WIDE SUPPLY VOLTAGE RANGE 4.5V TO 16V**
- **TIMER INTERVALS FROM MICROSECONDS TO HOURS**
- **TIME PERIOD EQUALS RC**

CIRCUIT OPERATIONS

In the one shot mode of operation, it is necessary to supply a minimum of two external components, the resistor and capacitor for timing. The time period is equal to the product of R and C. An output load must be present to complete the circuit due to the output structure of the 558.

For astable operation, it is desirable to cross couple two devices from the 558 Quad. The outputs are direct coupled to the opposite trigger input. The duty cycle can be set by ratio of R_1C_1 to R_2C_2 from close to zero to almost 100%. An astable circuit using one timer is shown in Figure 5b.

OUTPUT STRUCTURE 558

The 558 structure is open collector which requires a pull-up resistor to Vcc and is capable of sinking 100mA per unit but not to exceed the power dissipation and junction temperature rating of the die and package. The output is normally low and is switched high when triggered.

RESET

A reset function has been made available to reset all sections simultaneously to an output low state. During reset the trigger is disabled. After reset is finished, the trigger voltage must be taken high and then low to implement triggering.

The reset voltage must be brought below 0.8V to insure reset.

THE CONTROL VOLTAGE

The control voltage is also made available on the 558 timer. This allows the threshold voltage to be modulated, therefore controlling the output pulse width and duty cycle with an external control voltage. The range of this control voltage is from about 0.5V to Vcc minus 1 volt. This will give a cycle time variation of about 50:1. In a sequential timer with voltage controlled cycle time, the timing periods remain proportional over the adjustment range.

TEST BOARD FOR 558

The circuit layout can be used to test and characterize the 558 timer. S2 is used to connect the loads to either Vcc or ground. The main precaution, in layout of the 558 circuit, is the path of the discharge current from the timing capacitor to ground (pin 12). The path must be direct to pin 12 and not on the ground bus. This is to prevent voltage spikes on the ground bus return due to current switching transient. It is also wise to use good power supply by passing when large currents are being switched.

558 TEST CIRCUIT

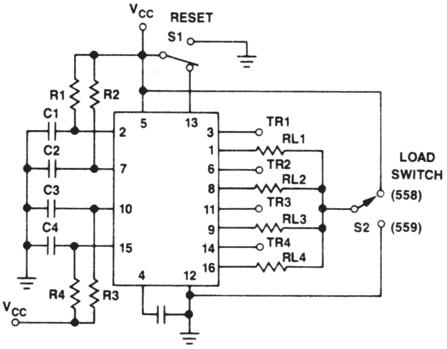


Figure 1

TEST BOARD LAYOUT

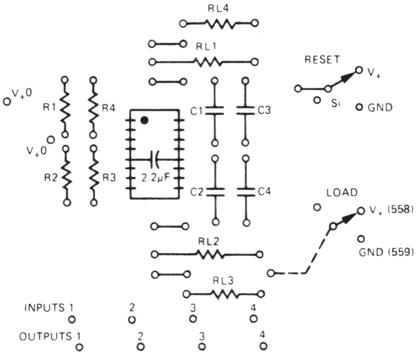

RL4
RL1
RESET
V+
S1
GND
V+0
R1
R4
C1
C3
V+0
R2
R3
2.2µF
C2
C4
LOAD
V+ (558)
GND (559)
RL2
RL3
INPUTS 1
2
3
4
OUTPUTS 1
2
3
4

Figure 2a

FOIL SIDE

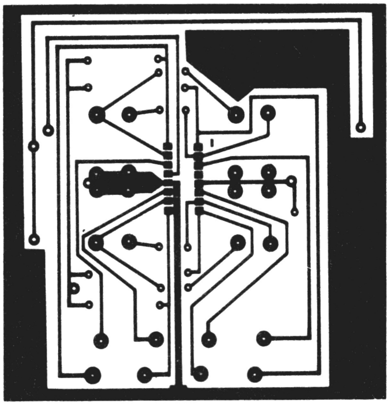
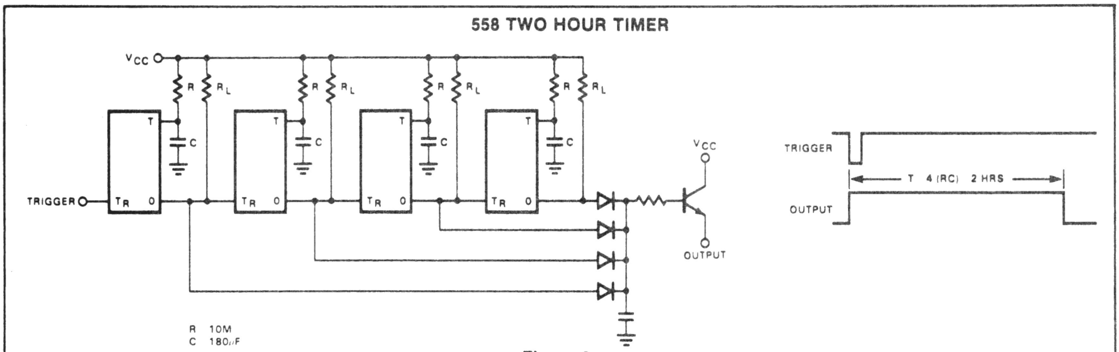


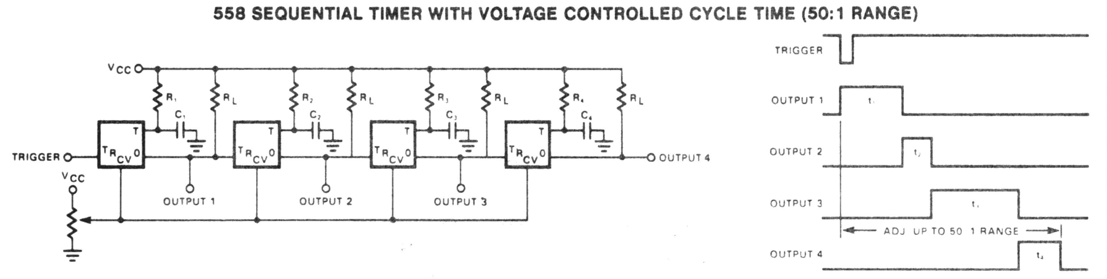
Figure 2b



558 TWO HOUR TIMER

VCC
R
RL
C
T
TR
O
TRIGGER
VCC
OUTPUT
TRIGGER
OUTPUT
T 4 (RC) 2 HRS
R 10M
C 180μF

Figure 3

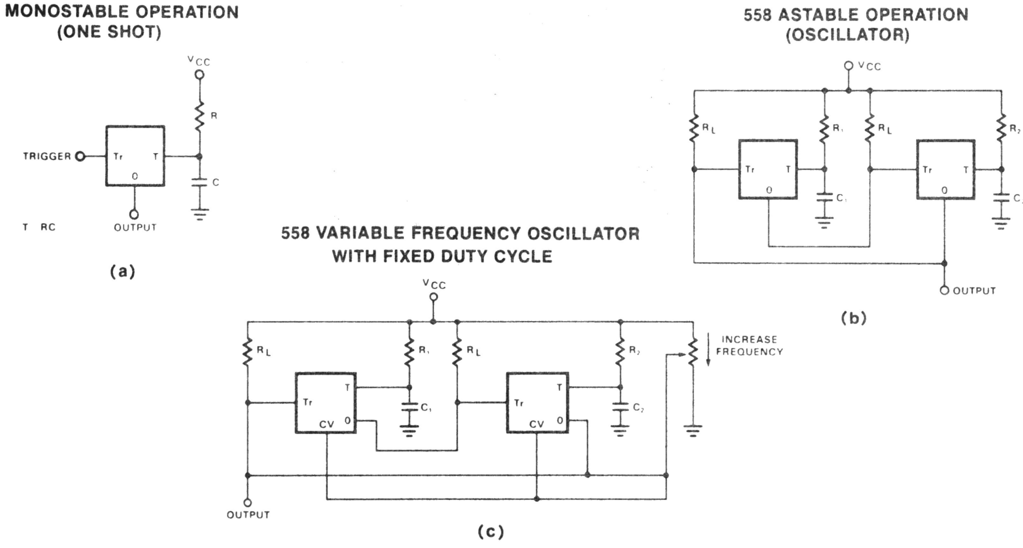


558 SEQUENTIAL TIMER WITH VOLTAGE CONTROLLED CYCLE TIME (50:1 RANGE)

VCC
R1
R2
R3
R4
RL
C1
C2
C3
C4
T
TR
CV
O
TRIGGER
VCC
OUTPUT 1
OUTPUT 2
OUTPUT 3
OUTPUT 4
TRIGGER
OUTPUT 1
OUTPUT 2
OUTPUT 3
OUTPUT 4
t1
t2
t3
t4
ADJ UP TO 50 1 RANGE

NOTE
t_1, t_2, t_3, t_4 remain proportional over entire adj. range.

Figure 4



MONOSTABLE OPERATION (ONE SHOT)

558 ASTABLE OPERATION (OSCILLATOR)

558 VARIABLE FREQUENCY OSCILLATOR WITH FIXED DUTY CYCLE

VCC
R
C
TRIGGER
Tr
T
O
OUTPUT
T RC
(a)
VCC
RL
R1
R2
C1
C2
OUTPUT
(b)
VCC
RL
R1
R2
C1
C2
CV
INCREASE FREQUENCY
OUTPUT
(c)

Figure 5

558 LONG-TIME DELAY

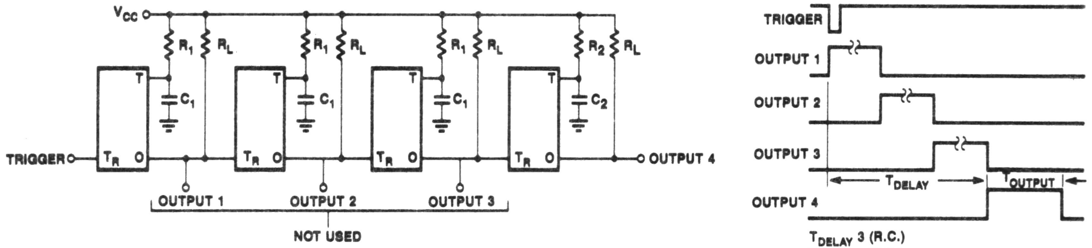
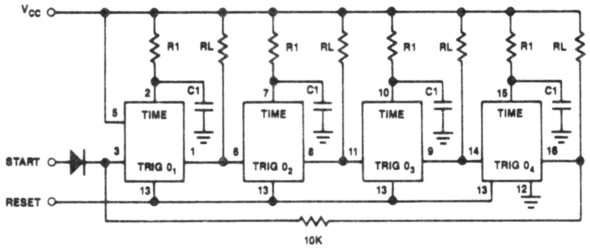

VCC
R1
RL
R2
C1
C2
T
TR
O
TRIGGER
OUTPUT 1
OUTPUT 2
OUTPUT 3
OUTPUT 4
NOT USED
TRIGGER
OUTPUT 1
OUTPUT 2
OUTPUT 3
OUTPUT 4
TDELAY
TOUTPUT
TDELAY 3 (R.C.)
TOUTPUT (R.C.)

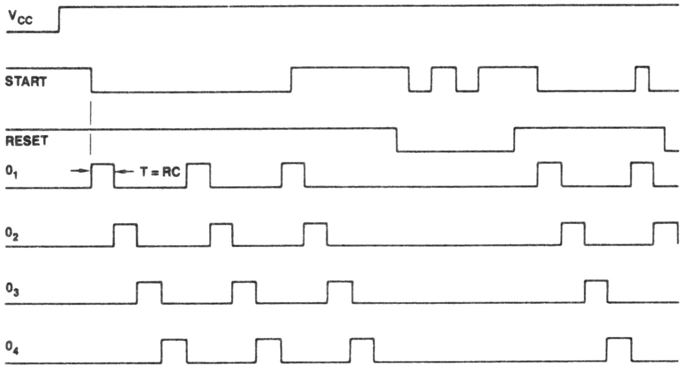
Figure 6

558 RING COUNTER


VCC
R1
RL
C1
TIME
TRIG O1
TRIG O2
TRIG O3
TRIG O4
START
RESET
2
5
3
1
13
7
6
8
10
11
9
15
14
16
12
10K

(a)

EXPECTED WAVEFORMS



(b)

Figure 7

NE558 APPLICATIONS

NE558 400 Hz SQUARE WAVE OSCILLATOR

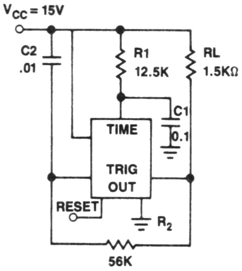

$V_{CC} = 15V$
C2
.01
R1
12.5K
RL
1.5KΩ
C1
0.1
TIME
TRIG
OUT
RESET
R_2
56K

Figure 8

A single section of the Quad time may be used as a non precision oscillator. The values given are for oscillation at about 400Hz. $T_1 \approx R_1 C_1$ and $T_2 \approx 2.25\ R_2 C_2$ for Vcc of 15 volts. The frequency of oscillation is subject to the changes in Vcc.

AN OVERVIEW OF PHASE LOCKED LOOP (PLL) AN177

2.1 An Overview of the Phase Locked Loop (PPL)

Portions of this Phase Locked Loop section were edited by Dr. J.A. Connelly

INTRODUCTION

The basic phase locked loop (PLL) concept has been known and widely utilized since first being proposed in 1922 (1). Since that time PLLs have been used in instrumentation, space telemetry, and many other applications requiring a high degree of noise immunity and narrow bandwidth. Techniques and systems involved in these applications frequently are quite complex, requiring a high degree of sophistication. Many of the PLL applications have been at microwave frequencies and employ complex phase shifters, signal splitters, modulation, and demodulation schemes such as biphase and quadraphase. Because of the high frequencies involved in microwave applications, most all components of these PLL systems are made from discrete as opposed to integrated circuits. However in other communication system applications such as FSK and FM and AM demodulation where frequencies are below approximately 100MHz, monolithic PLLs have found wide application because of their low cost versus high performance.

A block diagram representation of a PLL is shown in Figure 1. Phase locked loops operate by producing an oscillator frequency to match the frequency of an input signal, f_i. In this locked condition, any slight change in f_i first appears as a change in phase between f_i and the oscillator frequency. This phase shift then acts as an error signal to change the frequency of the local PLL oscillator to match f_i. The locking onto a phase relationship between f_i and the local oscillator accounts for the name phase locked loop.

A MECHANICAL ANALOG TO THE PLL

To better visualize the frequency and phase relationships in a PLL, consider the mechanical system shown in Figure 2 which is a dual to the electronic PLL. This mechanical system has two identical, heavy disks with two separate center shafts attached to each disk. Each staft is presumed to be mounted on a bearing that allows each massive disk to be rotated in either direction when some external force is applied. The shafts are coupled together by a spring whose end points are fixed to each shaft. This spring can be twisted in either direction depending upon the relative positions of the shafts. The spring cannot "kink up" due to the shafts passing through the center of the spring.

Now suppose the sequence of events shown on Figure 3 occurs to the mechanical system. The disks are simply represented like clock faces with positional reference markers. Initally both disks are stationary in a neutral position. Then the left disk, or input, is advanced slowly clockwise through an angle Θ_1 from the neutral position. The right disk, or output, initially doesn't move as the spring begins to tighten. As the input continues to move and when it reaches Θ_2, the output disk just begins to turn and tracks the input with a positional phase shift error of

$$\Theta_e = \Theta_2. \tag{1}$$

At any point in time with both disks slowly turning at the same speed, there will be some inherent phase error between the disks, or

$$\Theta_e = \Theta_3 - \Theta_4. \tag{2}$$

This positional phase error in the mechanical system is analogous to the phase error in the electronic PLL. When the input disk coasts to a stop, the output also gradually comes to a stop with a fixed phase error equal to that in Equation 2 or

$$\Theta_e = \Theta_5 - \Theta_6 = \theta_3 - \Theta_4. \tag{3}$$

The spring has a residual stored twist in one direction due to Θ_e.

Now consider that the disks are first returned to their neutral positions. Then the input disk is instantaneously rotated through an angle of Θ_1 as shown in Figure 4. The output disk can't respond instantaneously because of its large mass. It doesn't move instantaneously and the spring develops considerable torque. Then as shown in the sequence of events in Figure 4, the output disk begins accelerating after some delay due to the large phase error. It swings past the stopped position of the input disk due to its momentum, reaches a peak overshoot, and gradually oscillates about Θ_1 with a damped response, finally coming to rest with some small residual phase error. The input twist of Θ_1 represents the application of a step of position or phase to the system, and the response of the output disk is typical for a second-order, under-damped system. This same type of second-order behavior occurs in the PLL system for an instantaneous change of input phase.

As a final example, consider the events in Figure 5 where both disks are rotating at a constant rate. Applying a strobing light (strobotac) simultaneously to both disks

BLOCK DIAGRAM OF A PHASE LOCKED LOOP

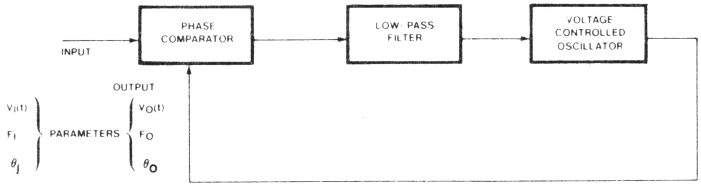


Figure 1

AN OVERVIEW OF PHASE LOCKED LOOP (PLL)

MECHANICAL ANALOG TO PLL

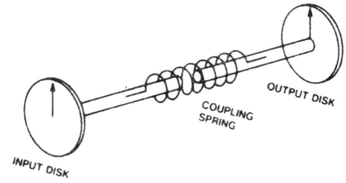

OUTPUT DISK
COUPLING SPRING
INPUT DISK

Figure 2

DISK SEQUENCE SHOWING OUTPUT TRACKING INPUT WITH PHASE ERROR

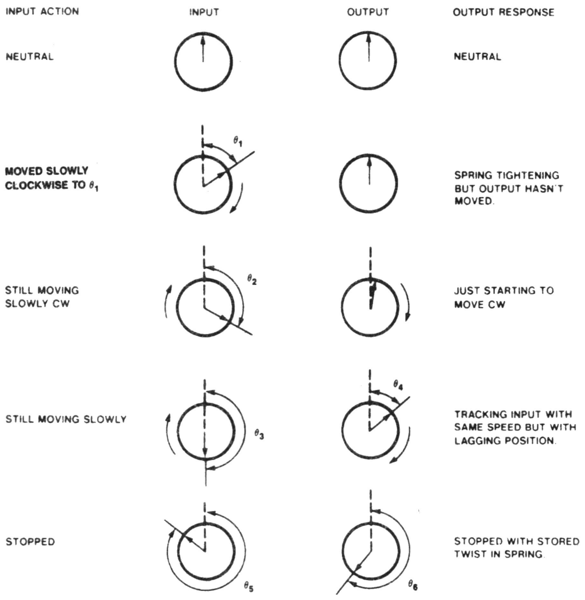

INPUT ACTION
INPUT
OUTPUT
OUTPUT RESPONSE
NEUTRAL
NEUTRAL
MOVED SLOWLY CLOCKWISE TO θ1
θ1
SPRING TIGHTENING BUT OUTPUT HASN'T MOVED.
STILL MOVING SLOWLY CW
θ2
JUST STARTING TO MOVE CW
STILL MOVING SLOWLY
θ3
θ4
TRACKING INPUT WITH SAME SPEED BUT WITH LAGGING POSITION.
STOPPED
θ5
θ6
STOPPED WITH STORED TWIST IN SPRING.

Figure 3

and adjusting its flashing rate to one flash per disk rotation will cause the positional markers to appear stationary. There will be a constant phase error in this case just as there was in Figure 3. Now suppose the revolution rate of the input disk gradually increases by a small amount to a new rate. The positional marker will appear to walk around the disk. The output first senses the increased rate of the input through an increase in the phase error. Then, after some delay, the rate of the output gradually increases to track the input. Both positional markers appear to be walking around each disk at the same rate until the strobotac is adjusted for the higher input and output rate. Then the strobe light again freezes the markers, producing a phase error at this higher rate that is larger than before the input rate was increased. This gradual increase in the input rate to the mechanical system simulates a ramp change in the input frequency to the PLL system. The response to the output disk simulates the behavior of the oscillator in the PLL.

If the rate of the input disk is alternately increased and decreased by some small amount compared to the nominal revolution rate, the positional markers will appear to walk both clockwise and counter clockwise, momentarily appearing stationary when the strobing light rate equals the disk revolution rate. This "walking" represents a changing phase error which is occurring at the modulation rate. Thus the phase error can be thought of as a useable demodulated output signal.

The disk-spring mechanical system is a helpful analog for visualizing frequency, phase, transient, and steady-state responses in the electronic phase locked loop system. In this example, the positions of the disk marker and rotation rates are analogous to phase and frequency in the electronic PLL system. The spring acts as a phase comparator to constantly sense the relative positions or phases of the disks. The torque developed in this spring acts as the driving force or input signal to turn the second disk.

Thus the spring torque simulates a voltage which controls the rate or frequency of the output disk or oscillator. Hence the second disk is analogous to a voltage-controlled oscillator (VCO). The large mass of the disks together with their angular momentum slows down the systems response time and simulates a low-pass filter in the electronic PLL system. This describes the lagging of the VCO free-running frequency to the input signal in an analog phase locked loop.

EXAMPLES OF PLL APPLICATIONS

Now consider the action of the voltage controlled oscillator, phase comparator and low pass filter in the PLL. The VCO generates a signal that is periodic. Normally, the rate or frequency of the VCO is primarily determined by the value of a capacitance connected to this oscillator. This action of starting the VCO running by itself is analogous to disconnecting the spring from one of the shafts in the mechanical system and starting the output disk rotating at a constant rate through some external means such as a motor. In the PLL system this frequency is called the oscillator's *free running frequency,* (f_o'), because it occurs when the system is unlocked and there is no coupling between input and output frequencies. With the PLL, the VCO frequency can be shifted above and below f_o' by applying a voltage to the optional fine tune input.* This signal generator property is just one of the many uses of the PLL. Specifically with integrated circuit PLLs, frequency ranges from less than 1.0Hz to more than 50MHz can be produced just by selecting the right value of capacitance from a chart on the data sheet.

Selecting f_o' and then changing it by a control voltage makes the VCO well suited for converting digital data that is represented by two different voltage levels into two different frequencies. A "1" voltage level can be related to a frequency called a mark, and an "0" level to a frequency called a space. This technique called *frequency shift keying*, or (FSK), is typical of data being transmitted over telephone and radio links where it is impractical to use dc voltage level shifts. Essentially this is what a modem (modulator-demodulator) does as it converts data to tones to go out of the system into a transmission link. Then it reverses the process and converts received tones to "1"'s and "0"'s at the receiver for the system to use. Sometimes confusion arises because different names are used for the same thing. For example,

A shift up in frequency = "1" = Mark
A shift down in frequency = "0" = Space

If voice or music is applied to the VCO instead of digital data, the oscillator's frequency will move or modulate with the voice or music. This is frequency modulation (FM) and is simply moving the frequency in relation to some input voltage which represents intelligence. Of course as in the modem case the process has to be reversed and the PLL can do this also. The PLL is a complete working system that can be used to

DISK SEQUENCE SHOWING OUTPUT RESPONSE TO A SUDDEN POSITION INPUT

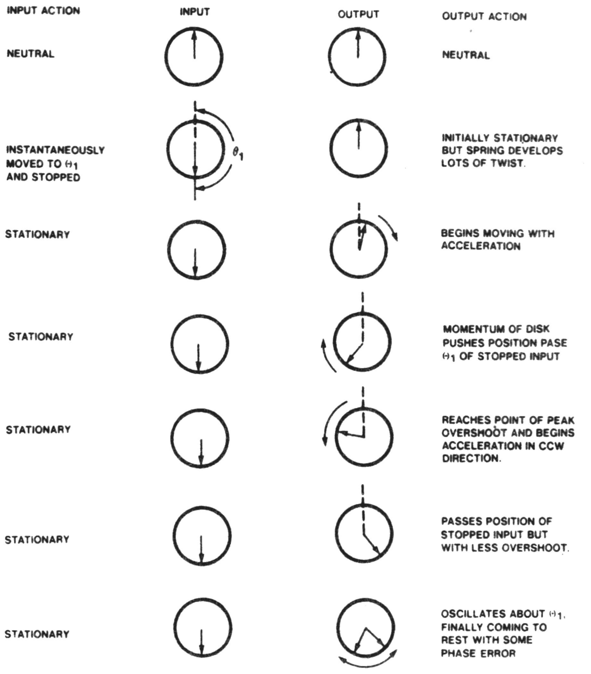

INPUT ACTION
INPUT
OUTPUT
OUTPUT ACTION
NEUTRAL
NEUTRAL
INSTANTANEOUSLY MOVED TO θ1 AND STOPPED
θ1
INITIALLY STATIONARY BUT SPRING DEVELOPS LOTS OF TWIST.
STATIONARY
BEGINS MOVING WITH ACCELERATION
STATIONARY
MOMENTUM OF DISK PUSHES POSITION PASE θ1 OF STOPPED INPUT
STATIONARY
REACHES POINT OF PEAK OVERSHOOT AND BEGINS ACCELERATION IN CCW DIRECTION.
STATIONARY
PASSES POSITION OF STOPPED INPUT BUT WITH LESS OVERSHOOT.
STATIONARY
OSCILLATES ABOUT θ1, FINALLY COMING TO REST WITH SOME PHASE ERROR

Figure 4

DISK SEQUENCE SHOWING OUTPUT BEHAVIOR DUE TO CHANGES IN INPUT SPEED

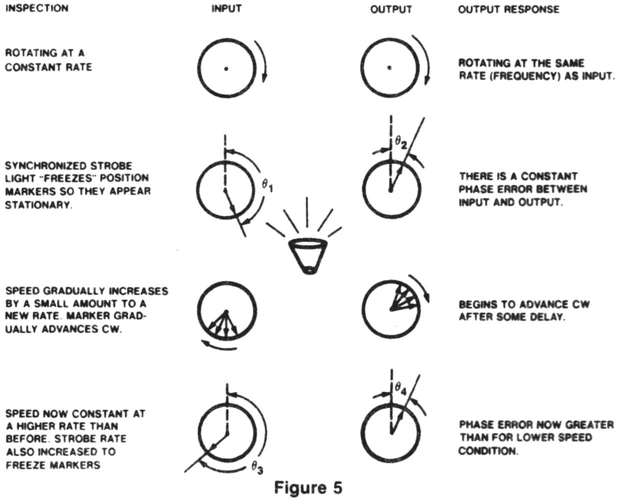

INSPECTION
INPUT
OUTPUT
OUTPUT RESPONSE
ROTATING AT A CONSTANT RATE
ROTATING AT THE SAME RATE (FREQUENCY) AS INPUT.
SYNCHRONIZED STROBE LIGHT "FREEZES" POSITION MARKERS SO THEY APPEAR STATIONARY.
θ1
θ2
THERE IS A CONSTANT PHASE ERROR BETWEEN INPUT AND OUTPUT.
SPEED GRADUALLY INCREASES BY A SMALL AMOUNT TO A NEW RATE. MARKER GRADUALLY ADVANCES CW.
BEGINS TO ADVANCE CW AFTER SOME DELAY.
SPEED NOW CONSTANT AT A HIGHER RATE THAN BEFORE. STROBE RATE ALSO INCREASED TO FREEZE MARKERS
θ3
θ4
PHASE ERROR NOW GREATER THAN FOR LOWER SPEED CONDITION.

Figure 5

---

*Some oscillators have frequencies controlled by an input current rather than a voltage and are referred to as current-controlled oscillators (CCO).

send and receive signals. In fact the PLL can create the signal, or select a signal, decode it and reproduce it. Now let's look at how this works.

The VCO is connected to a section where its frequency is put together with an incoming signal or signals. In a radio this is known as a "mixer" where signals are mixed together. In a PLL it is usually called a *Phase Comparator*. Other names for this function are *phase detector* or *multiplier* - either analog or digital. (Differences between analog and digital phase comparators will be explained later in this chapter). The purpose of this phase comparator is to produce an output which represents how far the VCO frequency is from that of the incoming signal. Comparing these frequencies and producing an error signal proportional to their difference allows the VCO frequency to shift from f_O' and become the same frequency as the input signal. This is exactly what happens with the VCO frequency - first "capturing" the input frequency, and then locking onto it. A similar type action can be visualized in the mechanical system by having the coupling spring disconnected at one end with the two disks rotating at different rates. When their rotation rates are approximately equal, the spring is suddenly connected, and the output disk's speed will gradually become equal to and track the inputs rate as in Figure 1.5.

When the VCO shifts frequency and locks to the input, the signal frequency is duplicated. If the input signal contains static or noise, the VCO output will be an exact reproduction of the signal frequency without the static or noise. Thus the PLL has accomplished signal reconditioning or reconstitution.

The error signal used to keep the VCO exactly synchronized with an incoming signal can be amplified, filtered, and used to "clock" the signal or give synchronizing information necessary to look at the signal. For example, in some digital memories and transmission systems, data are stored in a code and looked at or strobed at a rate which must be synchronized to the data. This strobing may be at twice or one-half the data rate. By setting f_O' equal to twice or one-half the data rate, the PLL will lock to the data and give an exact synchronized clock. This shows another application of the PLL for multiplying or dividing frequencies.

PLLs can separate a signal of one frequency from among many others as for example is done in television and radio reception. This selectivity or capture range is controlled in the PLL by the low-pass filter (LPF) which allows the PLL to only see signals close to the frequency of interest. The time constant of the LPF is set easily by the selection of a resistor and capacitor network. This network determines how far away in frequency an input signal can be from f_O' and still permit the PLL to respond and capture. Once locking is activated, the PLL system will continue to track the input frequency unless the instantaneous phase error exceeds the systems capability.

The error signal which drives the VCO and keeps the system locked is a usable output. In the FSK example the oscillator's frequency is shifted with each "1" or "0" digital input. Converting these frequency shifts back to the "1" and "0" signals automatically occurs in a PLL because a mark input generates an error signal to move the VCO up to that frequency. When the mark changes to a space, the error signal jumps suddenly down, forcing the VCO to follow. The error signal then is exactly the data that generated the FSK signals. *A PLL for FSK can convert data to tones for transmission to a remote point. Then another PLL can reconvert the data tones back to voltage levels, all without tuned circuits.*

The PLL system decodes FM signals in a similar way. The frequency variations caused by voltages from a microphone into one VCO serve as the input signal to another PLL which reverses the action since the error signal driving the second PLLs VCO is exactly the same as the original microphone voltage.

Decoding of an amplitude modulated (AM) input signal is another application of the PLL. This application is more involved than FM demodulation because a phase shift network, a second phase comparator, and another low-pass filter are required. This application is discussed in detail later in Chapters 4 and 5. However, it should be pointed out that AM demodulation with PLLs offers improved system linearity than the more commonly employed technique of nonlinear diode detection. Tone decoding is a special case of AM demodulation. When performed with PLLs, the second phase comparator is called a quadrature phase detector (QPD). The QPD produces a maximum output error voltage whenever the input and oscillator frequencies are locked to the free-running frequency, f_O', unlike the regular phase comparator which has a nominal zero error voltage under this same condition.

These application examples show that with the PLL is a system that can:

1 Generate a signal
2 Modulate a signal (encode)
3 Select a signal from among many
4 Demodulate (decode)
5 Recreate (reconstitute) a signal frequency with reduced noise
6 Multiply and divide frequency

TYPES OF PLLS

Generally speaking the monolithic PLLs can be classified into two groups - digital and analog. While both perform as PLLs, the digital circuits are more suitable for synchronization of digital signals, clock recovery from encoded digital data streams, and other digital applications. Analog monolithic PLLs are used quite extensively in communication systems since they maintain linear relationships between input and output quantities.

The phase comparator is perhaps the most important part of the PLL system since it is here that the input and VCO frequencies are simultaneously compared. Some digital PLLs employ a two-input Exclusive-Or gate as the phase comparator. When the digital loop is locked to f_O', there is an inherent phase error of 90° that is represented by asymmetry in the output waveform. Also the phase comparators output has a frequency component of twice the reference frequency. Because of the large logic voltage swings in digital systems, extensive filtering must be performed to remove the harmonic frequencies. For this reason, other types of digital phase comparators achieve locking by synchronizing the "edges" of the input and VCO frequency waveshapes. The phase comparator produces an error voltage that is proportional to the time difference between the edges, i.e., the phase error. This edge-triggering technique for the phase comparator produces lower output noise than with the Exclusive-Or approach. However time jitter on the input and VCO frequencies is translated into phase error jitter that may require additional filtering within the loop.

Triggering on the edges of digital signals means that only frequency (or period) is important and not duty cycle. This is a key consideration in PLL applications utilizing counters where waveshapes usually aren't symmetrical, i.e., 50% duty cycle. For the TTL family, it is easier to provide the edge matching function on the falling edges ("1" to "0") transition of the waveform. CMOS, I^2L, and ECL are better suited for leading edge triggering ("0" to "1").

Analog PLLs utilize a phase comparator which functions as a four-quadrant analog multiplier to mix the input and VCO signals. Since this mixing is true analog multiplication, the phase comparators output is a function of input and VCO signal amplitudes, frequencies, phase relationships, and duty cycles. The inherent linearity afforded by this analog multiplication makes the monolithic analog PLL well suited for many general purpose and communication system applications.

Another way of distinguishing between digital and analog phase comparators is by thinking of the similarities and differences between voltage comparators and operational amplifiers. Voltage comparators are specially designed for digital applications where response time between output levels has been minimized at the expense of system linearity. Feedback is seldom used to maintain linear system relationships, with the comparator normally running open loop. Op amps, on the other hand, are designed for a linear input-output relationship, with negative feedback being employed to further improve the system linearity.

PLL TERMINOLOGY

The following is a brief glossary of frequently encountered terms in PLL literature.

Free-running Frequency (f_o', ω_o').

Also called the *center frequency*, this is the frequency at which the loop VCO operates when not locked to an input signal. The "prime" superscripts are used to distinguish the free-running frequency from f_o and ω_o which are used for the general oscillator frequency. (Many references use f_o and ω_o for both the free-running and general oscillator frequency and leave the proper choice for the reader to infer from the context). The appropriate units for f_o' and ω_o' are Hz and radians per second respectively.

Lock Range ($2 f_L$, $2\omega_L$).*

The range of frequencies over which the loop will remain in lock. Normally the lock range is centered at the free-running frequency unless there is some nonlinearity in the system which limits the frequency deviation on one side of f_o'. The deviations from f_o' are referred to as the *Tracking Range* or *Hold-in Range*. (See Figure 1.6). The tracking range is therefore one-half of the lock range.

Capture Range ($2 f_c$, $2\omega_c$).**

Although the loop will remain in lock throughout its lock range, it may not be able to acquire lock at the tracking range extremes because of the selectivity afforded by the low-pass filter. The capture range also is centered at f_o' with the equal deviations called the *Lock-in* or *Pull-in Ranges. The capture range can never exceed the lock range.*

Lock-up Time (t_L).***

The transient time required for a free running loop to lock. This time depends principally upon the bandwidth selectivity designed into the loop with the low-pass filter. *The lock-up time is inversely proportional to the selectivity bandwidth.* Also, lock-up time exhibits a statistical spreading due to random initial phase relationships between the input and oscillator phases.

Phase Comparator Conversion Gain (K_d).

The conversion constant relating the phase comparators output voltage to the phase difference between input and VCO signals when the loop is locked. At low input signal levels, K_d is also a function of signal amplitude. K_d has units of volts per radian (V/rad).

LOCK AND CAPTURE RANGE RELATIONSHIPS

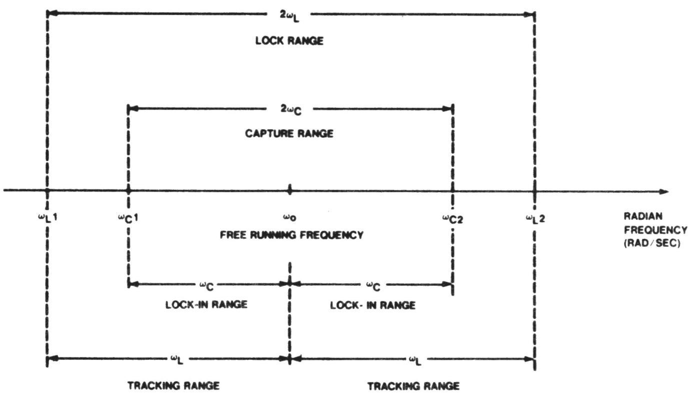


Figure 6

VCO Conversion Gain (K_o).

The conversion constant relating the oscillators frequency shift from f_o' to the applied input voltage. K_o has units of radians per second per volt (rad/sec/volt). K_o is a linear function of ω_o' and must be obtained using a formula or graph provided or experimentally measured at the desired ω_o'.

Loop Gain (K_v)

The product of K_d, K_o, and the low-pass filters gain at dc. K_d is evaluated at the appropriate input signal level and K_o at the appropriate ω_o'. K_v has units of $(\text{sec})^{-1}$.

Closed Loop Gain (CLG)

The output signal frequency and phase can be determined from a product of the CLG and the input signal where the CLG is given by

$$\text{CLG} = \frac{K_v}{1 + K_v} \tag{4}$$

Natural Frequency (ω_n).

The characteristic frequency of the loop, determined mathematically by the final pole positions in the complex plane or determined experimentally as the modulation frequency for which an underdamped loop gives the maximum frequency deviation from f_o' and at which the phase error swing is the greatest.

Damping Factor (ζ).

The standard damping constant of a second order feedback system. For the PLL, ζ refers to the ability of the loop to respond quickly to an input frequency step without excessive overshoot.

Loop Noise Bandwidth (B_L).

A loop property relating ω_n and ζ which describes the effective bandwidth of the received signal. Noise and signal components outside this bandwidth are greatly attenuated.

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* Also called Synchronization Range.

** Also called Acquisition Range.

*** Also called Acquisition Time.

MODELING THE PLL

INTRODUCTION

The phase locked loop is a feedback system comprised of a phase comparator, a low pass filter and an error amplifier in the forward signal path and a voltage-controlled oscillator (VCO) in the feedback path. The block diagram of a basic PLL system is shown in Figure 1. Perhaps the single most important point to realize when designing with the PLL is that it is a feedback system and, hence, is characterized mathematically by the same equations that apply to other, more conventional feedback systems. However, the parameters in the equations are somewhat different since the feedback error signal in the phase locked system is a phase rather than a current or voltage signal, as is usually the case in conventional feedback systems.

BLOCK DIAGRAM OF PHASE LOCKED LOOP

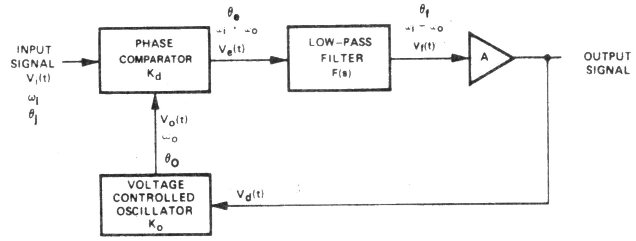


Figure 1

PHASE LOCKED LOOP OPERATION

The basic principle of the PLL operation can be briefly explained as follows:

With no signal input applied to the system, the VCO control voltage $V_d(t)$ is equal to zero. The VCO operates at a set frequency, f_o' (or the equivalent radian frequency ω_o') which is known as the free-running frequency. When an input signal is applied to the system, the phase comparator compares the phase and the frequency of the input with the VCO frequency and generates an error voltage $V_e(t)$ that is related to the phase and the frequency difference between the two signals. This error voltage is then filtered, amplified, and applied to the control terminal of the VCO. In this manner, the control voltage $V_d(t)$ forces the VCO frequency to vary in a direction that reduces the frequency difference between ω_o and the input signal. If the input frequency ω_i is sufficiently close to ω_o, the feedback nature of the PLL causes the VCO to synchronize or lock with the incoming signal. Once in lock, the VCO frequency is identical to the input signal except for a finite phase difference.

This net phase difference of Θ_e where

$$\Theta_e = \Theta_o - \Theta_i \tag{1}$$

is necessary to generate the corrective error voltage V_d to shift the VCO frequency from its free-running value to the input signal frequency ω_i and, thus, keep the PLL in lock. This self-correcting ability of the system also allows the PLL to track the frequency changes of the input signal once it is locked. The range of frequencies over which the PLL can maintain lock with an input signal is defined as the "lock range" of the system. The band of frequencies over which the PLL can acquire lock with an incoming signal is known as the "capture range" of the system and is never greater than the lock range.

Another means of describing the operation of the PLL is to observe that the phase comparator is in actuality a multiplier circuit that mixes the input signal with the VCO signal. This mix produces the sum and difference frequencies $\omega_i \pm \omega_o$ shown in Figure 1. *When the loop in in lock,* the VCO duplicates the input frequency so that the difference frequency component $(\omega_i \cdot \omega_o)$ is zero; *hence, the output of the phase comparator contains only a dc component.* The low pass filter removes the sum frequency component $(\omega_i + \omega_o)$ but passes the dc component which is then amplified and fed back to the VCO. Notice that when the loop is in lock, the difference frequency component is always dc, so the lock range is independent of the band edge of the low pass filter.

LOCK AND CAPTURE

Consider now the case where the loop is not yet in lock. The phase comparator again mixes the input and VCO signals to produce sum and difference frequency components. However, the difference component may fall outside the band edge of the low pass filter and be removed along with the sum frequency component. If this is the case, no information is transmitted around the loop and the VCO remains at its initial free-running frequency. As the input frequency approaches that of the VCO, the frequency of the difference component decreases and approaches the band edge of the low pass filter. Now some of the difference component is passed, which tends to drive the VCO towards the frequency of the input signal. This, in turn, decreases the frequency of the difference component and allows more information to be transmitted through the low pass filter to the VCO. This is essentially a positive feedback mechanism which causes the VCO to snap into lock with the input signal. With this mechanism in mind, the term "capture range" can again be defined as *the frequency range centered about the VCO initial free-running frequency over which the loop can acquire lock with the input signal.* The capture range is a measure of how close the input signal must be in frequency to that of the VCO to acquire lock. The "capture range" can assume any value within the lock range and depends primarily upon the band edge of the low pass filter together with the closed loop gain of the system. It is this signal capturing phenomenon which gives the loop its frequency selective properties.

It is important to distinguish the "capture range" from the "lock range" which can, again, be defined as *the frequency range usually centered about the VCO initial free-running frequency over which the loop can track the input signal once lock has been achieved.*

When the loop is in lock, the difference frequency component at the output of the phase comparator (error voltage) is dc and will always be passed by the low pass filter. Thus, the lock range is limited by the range of error voltage that can be generated and the corresponding VCO frequency deviation produced. The lock range is essentially a dc parameter and is not affected by the band edge of the low pass filter.

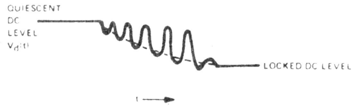
THE CAPTURE TRANSIENT

The capture process is highly complex and does not lend itself to simple mathematical analysis. However, a qualitative description of the capture mechanism may be given as follows. Since frequency is the time derivative of phase, the frequency and the phase errors in the loop can be related as

$$\Delta\omega = \frac{d\Theta_e}{dt} \tag{2}$$

ASYNCHRONOUS ERROR BEAT FREQUENCY DURING THE CAPTURE PROCESS:

(A) VCO CONTROL VOLTAGE VARIATION DURING CAPTURE TRANSIENT



(B) OSCILLOGRAM SHOWING A CAPTURE PROCESS

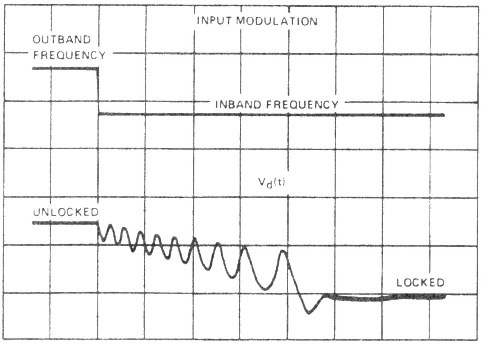


Figure 2

EXHIBITED BY FIRST ORDER LOOP FAST CAPTURE TRANSIENT

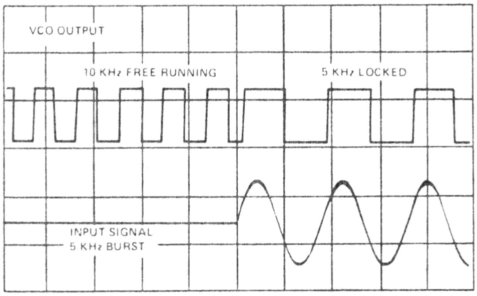


Figure 3

where $\Delta\omega$ is the instantaneous frequency separation between the signal and VCO frequencies and Θ_e is the phase difference between the input signal and VCO signals.

If the feedback loop of the PLL were opened between the low pass filter and the VCO control input, then for a given condition of ω_o and ω_i the phase comparator output would be a sinusoidal beat note at a fixed frequency $\Delta\omega$. If ω_i and ω_o were sufficiently close in frequency, this beat note would appear at the filter output with negligible attenuation.

Now suppose that the feedback loop is closed by connecting the low pass filter output to the VCO control terminal. The VCO frequency will be modulated by the beat note. When this happens, $\Delta\omega$ itself will become a function of time. If during this modulation process, the VCO frequency moves closer to ω_i (i.e., decreasing $\Delta\omega$), then $\frac{d\Theta_e}{dt}$ decreases and the output of the phase comparator becomes a slowly varying function of time. Similarly, if the VCO is modulated away from ω_i, $\frac{d\Theta_e}{dt}$ increases and the error voltage becomes a rapidly varying function of time. Under this condition the beat note waveform no longer looks sinusoidal; it looks like a series of aperiodic cusps, depicted schematically in Figure 2(a). Because of its asymmetry, the beat note waveform contains a finite dc component that pushes the average value of the VCO toward ω_i, and lock is established. When the system is in lock, $\Delta\omega$ is equal to zero and only a steady-state dc error voltage remains.

Figure 2(b) displays an oscillogram of the loop error voltage $V_d(t)$ in an actual PLL system during the capture process. Note that as lock is approached, $\Delta\omega$ is reduced, the low pass filter attenuation becomes less, and the amplitude of the beat note increases.

The total time taken by the PLL to establish lock is called *the pull-in time*. Pull-in time depends on the initial frequency and phase differences between the two signals as well as on the overall loop gain and the low pass filter bandwidth. Under certain conditions, the pull-in time may be shorter than the period of the beat note and the loop can lock without an oscillatory error transient.

A specific case to illustrate this is shown in Figure 3. The 565 PLL is shown acquiring lock within the first cycle of the input signal. The PLL was able to capture in this short time because it was operated as a first order loop (no low pass filter) and the input tone-burst frequency was within its lock and capture range.

EFFECT OF THE LOW PASS FILTER

In the operation of the loop, the low pass filter serves a dual function:

First, by attenuating the high frequency error components at the output of the phase comparator, it enhances the interference-rejection characteristics; second, it provides a short-term memory for the PLL and ensures a rapid recapture of the signal if the system is thrown out of lock due to a noise transient. Decreasing the low pass filter bandwidth has the following effects on system performance: (Long Time Constant).

a The capture process becomes slower, and the pull-in time increases.
b The capture range decreases.
c Interference-rejection properties of the PLL improve since the error voltage caused by an interfering frequency is attenuated further by the low pass filter.
d The transient response of the loop (the response of the PLL to sudden changes of the input frequency within the capture range) becomes underdamped.

MODELING THE PLL

The last effect also produces a practical limitation on the low pass loop filter bandwidth and roll-off characteristics from a stability standpoint. These points will be explained further in the following analysis.

LINEAR MODEL OF PLL SYSTEM

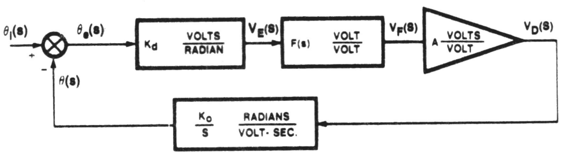

$\theta_i(s)$
$\theta_e(s)$
+
−
$\theta(s)$
K_d $\frac{\text{VOLTS}}{\text{RADIAN}}$
$V_E(S)$
$F(s)$ $\frac{\text{VOLT}}{\text{VOLT}}$
$V_F(S)$
A $\frac{\text{VOLTS}}{\text{VOLT}}$
$V_D(S)$
$\frac{K_o}{S}$ $\frac{\text{RADIANS}}{\text{VOLT-SEC.}}$

Figure 4

MEASUREMENT SCHEME FOR K_d AND K_o DETERMINATIONS

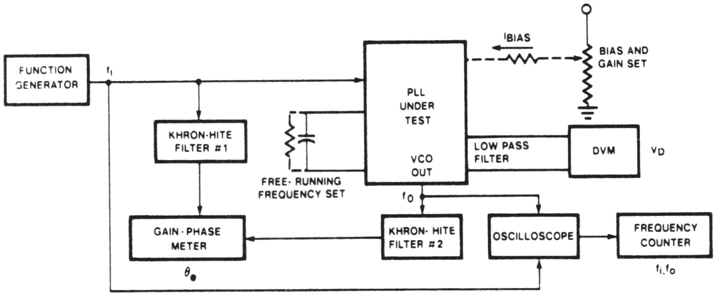


Figure 5

MATHEMATICALLY DEFINING PLL OPERATION

As mentioned previously, the phase comparator is basically an analog multiplier that forms the product of an RF input signal, $v_i(t)$, and the output signal, $v_o(t)$, from the VCO. Refer to Figure 1 and assume that the two signals to be multiplied can be described by

$$v_i(t) = V_i \sin \omega_i t \tag{3}$$

$$v_o(t) = V_o \sin (\omega_o t + \Theta_e) \tag{4}$$

where ω_i, ω_o, and Θ_e are the frequency and phase difference (or phase error) characteristics of interest. The product of these two signals is an output voltage given by

$$v_e(t) = K_1 V_i V_o (\sin \omega_i t) [\sin (\omega_o t + \Theta_e)] \tag{5}$$

where K_1 is an appropriate dimensional constant. Note that the amplitude of $v_e(t)$ is directly proportional to the amplitude of the input signal V_i. The two cases of an unlocked loop ($\omega_i \neq \omega_o$) and of a locked loop ($\omega_i = \omega_o$) are now considered separately.

Unlocked State ($\omega_i \neq \omega_o$)

When the two frequencies to the phase comparator are not synchronized, the loop is not locked. Furthermore the phase angle difference Θ_e in Equations 4 and 5 is meaningless for this case since it can be eliminated by appropriately choosing the time origin.

Using trigonometric identities, Equation 5 can be rewritten as

$$v_e(t) = \frac{K_1 V_i V_o}{2} [\cos(\omega_i - \omega_o)t - \cos(\omega_i + \omega_o)t] \tag{6}$$

When $v_e(t)$ is passed through the low pass filter, F(s), the sum frequency component is removed, leaving

$$v_f(t) = K_2 V_i V_o \cos (\omega_i - \omega_o)t \tag{7}$$

where K_2 is a constant. After amplification, the control voltage for the VCO appears as

$$v_d(t) = AK_2 V_i V_o \cos (\omega_i - \omega_o)t \tag{8}$$

This equation shows that a beat frequency effect is established between ω_i and ω_o, causing the VCOs frequency to deviate by $\pm\Delta\omega$ from ω_o' in proportion to the signal amplitude ($AK_2V_iV_o$) passing through the filter. If the amplitude of V_i is sufficiently large and if signal limiting or saturation does not occur, the VCO output frequency will be shifted from ω_o' by some $\Delta\omega$ until lock is established where

$$\omega_i = \omega_o = \omega_o' \pm \Delta\omega \tag{9}$$

If lock cannot be established, then either V_i is too small to drive the VCO to produce the necessary $\pm\Delta\omega$ deviation or ω_i is beyond the dynamic range of the VCO, i.e., $\omega_i \gtrless \omega_o \pm \Delta\omega$. Remedies for these no lock conditions are:

1 Increase V_i either internally or externally to the loop by providing additional amplification.

2 Increase the internal loop gain by adjusting upward (larger −3dB frequency) the response of the low-pass filter.

3 Shift ω_o' closer to the expected ω_i. Establishing frequency lock leads to the second case where $\omega_i = \omega_o$.

Locked State ($\omega_i = \omega_o$)

When ω_i and ω_o are frequency synchronized, the output signal from the phase comparator for $\omega_i = \omega_o = \omega$ and a phase shift of Θ_e is

$$v_e(t) = K_1 V_i V_o (\sin \omega t)(\sin \omega t + \Theta_e) = \frac{K_1 V_i V_o}{2} [\cos \Theta_e - \cos (2\omega t + \Theta_e)] \tag{10}$$

The low pass filter removes the high frequency, ac component of $v_e(t)$, leaving only the dc component. Thus,

$$v_f(t) = K_2 V_i V_o \cos \Theta_e \tag{11}$$

After amplification the dc voltage driving the VCO and maintaining lock within the loop is

$$v_d(t) = V_D = AK_2 V_i V_o \cos \Theta_e \tag{12}$$

Suppose ω_i and ω_o are perfectly synchronized to the free-running frequency ω_o'. For this case, V_D will be zero, indicating that Θ_e must be ±90°. Thus V_D is proportional to the phase difference or phase error between Θ_i and Θ_o centered about a reference phase angle of ±90°. If ω_i changes slightly from ω_o', the first effect will be a change in Θ_e from ±90°. V_D will adjust and settle out to some nonzero value to correct ω_o; under this condition frequency lock is maintained with $\omega_i = \omega_o$. The phase error will be shifted by some amount $\Delta\Theta$ from the reference phase angle of ±90°. This concept can be simplified by redefining Θ_e as

$$\Theta_e = \Theta_r \pm \Delta\Theta \tag{13}$$

where Θ_r is the inherent, reference phase shift of ±90° and $\Delta\Theta$ is the departure from this reference value. Now the VCO control voltage becomes

$$V_D = AK_2 V_i V_o \cos (\Theta_r \pm \Delta\Theta) = \pm AK_2 V_i V_o \sin\Delta\Theta \tag{14}$$

Since the sine function is odd, a momentary change in $\Delta\Theta$ contains information about which way to adjust the VCO frequency to correct and maintain the locked condition. The maximum range over which $\Delta\Theta$ changes can be tracked is $-90°$ to $+90°$. This corresponds to a Θ_e range from 0 to 180°.

In addition to being an error signal, V_D represents the demodulated output of an FM input applied as $v_{in}(t)$ assuming a linear VCO characteristic. Thus FM demodulation can be accomplished with the PLL without the inductively tuned circuits that are employed with conventional detectors.

DETERMINING PLL MODEL PARAMETERS

Since the PLL is basically an electronic servo loop, many of the analytical techniques developed for control systems are applicable to phase locked systems. Whenever phase lock is established between $v_i(t)$ and $v_o(t)$ the linear model of Figure 4 can be used to predict the performance of the PLL system. Here Θ_i and Θ_o represent the phase angles associated with the input output waveshapes repectively; F(s) represents a generalized voltage transfer function for the low pass filter in the s complex frequency domain; and K_d and K_o are conversion gains of the phase comparator and VCO respectively, each having units as shown. The 1/s term associated with the VCO accounts for the inherent 90° phase shift in the loop since the VCO converts a voltage to a frequency and since phase is the integral of frequency. Thus the VCO functions as an integrator in the feedback loop.

Specific values of K_d and K_o for all of Signetics general purpose PLLs can be found in the sections describing the particular loop of interest. However, sometimes it may be desired to determine these conversion gains exactly for a specific device. The measurement scheme shown in Figure 5 can be used to determine K_d and K_o for a loop under lock. The function of hte Khron-Hite filters is to extract the fundamental sinusoidal frequency component of their square wasve inputs for application to the Gain-Phase Meter. If the input signal from the Function Generator is sinusoidal, then the first Khron-Hite filter may be eliminated. It is recommended to use high impedance oscilloscope probes so as to not distort the input of VCO waveshapes, thereby potentially altering their phase relationships. The frequency counter can be driven from the scope as shown, or connected directly to the input or VCO provided its input impedance is large.

The procedure to follow for obtaining K_d and K_O is as follows:

1. Established the desired external bias and gain conditions for the PLL under test.
2. With the Function Generator turned off, set the free-running frequency of the loop via the timing capacitor and timing resistor if appropriate. Monitor f_O' with the Frequency Counter.
3. Turn on the Function Generator and check to make sure the amplitude of the input signal is appropriate for the particular loop under test.
4. Adjust the input frequency for lock. Lock is discernable on a dual-trace scope when the input and VCO waveforms are synchronized and stationary with respect to each other. One should be especially careful to check that locking has not occurred between the VCO and some harmonic frequency. Carefully inspect both waveshapes, making sure each has the same period. (If a second Frequency Counter is available, an alternate scheme can be used to confirm frequency locking. One frequency counter is used to monitor the input signal frequency, and the second counter is used for the VCO frequency. When the two counters display the same frequency, the PLL is locked).
5. Set the input frequency to the free-running frequency and note the Gain-Phase Meter display. It should be approximately 90°, ± 10° nominally. Record the phase error, Θ_e, the VCO control voltage, V_D, and the input frequency, f_i.
6. Adjust f_i for frequencies above and below f_O' and record Θ_e and V_D for each f_i as appropriate.
7. Making a plot of V_D versus Θ_e is useful for checking the measurement data and the systems linearity. The slope of this plot ($\Delta V_D / \Delta\Theta_e$) is K_d in units of volts/degree. Multiplying this slope by $180/\pi$ gives the desired K_d in volts/radian.
8. A plot of $f_i = f_O$ versus V_D while the loop remains locked will check the VCO linearity. The slope of this plot is K_O at the particular free-running frequency. The units of slope taken directly from the graph are Hz/volt. Multiplying this slope figure by 2π gives the desired K_O in units of radians/volt-sec.

K_d is generally constant over wide frequency ranges, but is linearily related to the input signal amplitude. K_O is constant with input signal level but does vary linearily with f_O'. Often it is convenient to specify a normalized K_O as

$$K_{O(norm)} = \frac{K_O}{f_O'} \quad \frac{\text{radians}}{\text{volt}} \qquad (15)$$

The K_O value at any desired free-running frequency then can be estimated as

$$K_O\ (@\ \text{any}\ f_O') = K_{O(norm)}\, f_O' \qquad (16)$$

The loop gain for the PLL system is

$$K_V = K_d K_O A \qquad (17)$$

(Often when the gain A is due to an amplifier internal to the IC, A will be included in either K_d or K_o. This is further illustrated in the article on the 565 PLL.

MODELING THE PLL SYSTEM WITH VARIOUS LOW PASS FILTERS

The open loop transfer function for the PLL is

$$T(s) = \frac{K_V F(s)}{s} \qquad (18)$$

Using linear feedback analysis techniques, the closed loop transfer characteristics H(s) can be related to the open loop performance as

$$H(s) = \frac{T(s)}{1+T(s)} \qquad (19)$$

and the roots of the characteristic system polynominal can be readily determined by root-locus techniques.

From these equations, it is apparent that the transient performance and frequency response of the loop is heavily dependent upon the choice of filter and its corresponding transfer characteristic, F(s).

Zero Order Filter - F(s) = 1

The simplest case is that of the first order loop where F(s) = 1 (no filter). The closed loop transfer function then becomes

$$T(s) = \frac{K_V}{s + K_V} \qquad (20)$$

This transfer function gives the root locus as a function of the total loop gain K_v and the corresponding frequency response shown in Figure 6(a). The open loop pole at the origin is due to the integrating action of the VCO. Note that the frequency response is actually the amplitude of the difference frequency component versus modulating frequency when the PLL is used to track a frequency modulated input signal. Since there is no low pass filter in this case, sum frequency components are also present at the phase comparator output and must be filtered outside of the loop if the difference frequency component (demodulated FM) is to be measured.

First Order Filter

With the addition of a single pole low pass filter F(s) of the form

$$F(s) = \frac{1}{1+\tau_1 s} \qquad (21)$$

where $\tau_1 = R_1C_1$, the PLL becomes a second order system with the root locus shown in Figure 6(b). Again an open loop pole is located at the origin because of the integrating action of the VCO. Another open loop pole is positioned on the real axis at $-1/\tau_1$ where τ_1 is the time constant of the low pass filter.

One can make the following observations from the root locus characteristics of Figure 6(b):

a As the loop gain K_V increases for a given choice of τ_1, the imaginary part of the closed loop poles increase; thus, the natural frequency of the loop increases and the loop becomes more and more underdamped.

b If the filter time constant is increased, the real part of the closed loop poles becomes smaller and the loop damping is reduced.

As in any practical feedback system, excess shifts or non-dominant poles associated with the blocks within the PLL can cause the root loci to bend toward the right half plane as shown by the dashed line in Figure 6(b). This is likely to happen if either the loop gain or the filter time constant is too large and may cause the loop to break into sustained oscillations.

First Order Lag-Lead Filter

The stability problem can be eliminated by using a lag-lead type of filter, as indicated in Figure 6(c). This type of a filter has the transfer function

$$F(s) = \frac{1 + \tau_2 s}{1 + (\tau_1 + \tau_2)s} \tag{22}$$

where $\tau_2 = R_2C$ and $\tau_1 = R_1C$. By proper choice of R_2, this type of filter confines the root locus to the left-half plane and ensures stability. The lag-lead filter gives a frequency response dependent on the damping, which can now be controlled by the proper adjustment of τ_1 and τ_2. In practice, this type of filter is important because it allows the loop to be used with a response between that of the first and second order loops and it provides an additional control over the loop transient response. If $R_2 = 0$, the loop behaves as a second order loop and as $R_2 \rightarrow \infty$, the loop behaves as a first order loop due to a pole-zero cancellation. However, as first-order operation is approached, the noise bandwidth increases and interference rejection decreases since the high frequency error components in the loop are now attenuated to a lesser degree.

Second and Higher Order Filters

Second and higher order filters as well as active filters occasionally are designed and incorporated within the PLL to achieve a particular response not possible or easily obtained with zero or first order filters. Adding more poles and more gain to the closed loop transfer function reduces the inherent stability of the loop. Thus the designer must exercise extreme care and utilize complex stability analysis if second order (and higher) filters or active filters are to be considered.

CALCULATING LOCK AND CAPTURE RANGES

In terms of the basic gain expression in the system, the lock range of the PLL ω_L can be shown to be numerically equal to the dc loop gain (2 sided lock range).

$$2\omega_L = 4\pi f_L = 2K_V F(0) \tag{23}$$

where F(0) is the value of the low pass filters transfer function at dc.

Since the capture range ω_C denotes a transient condition, it is not as readily derived as the lock range. However, an approximate expression for the capture range can be written as (2 sided capture range).

$$2\omega_C = 4\pi f_C \simeq 2K_V \left|F(j\omega_C)\right| \tag{24}$$

where $F(i\omega_C)$ is the magnitude of the low pass filter transfer function evaluated at ω_C. Solution of Equation 24 frequently involves a "trial and error" process since the capture range is a function of itself. *Note that at all times the capture range is smaller than the lock range.*

For the simple first-order lag filter of Figure 6(b) the capture range can be approximated as

$$2\omega_C \simeq 2\sqrt{\frac{\omega_L}{\tau_1}} = 2\sqrt{\frac{K_V}{\tau_1}} \tag{25}$$

This approximation is valid for

$$\tau_1 >> \frac{1}{2\omega_L} \tag{26}$$

Equations 23 and 24 show that the capture range increases as the low pass filter time constant is decreased, whereas the lock range is unaffected by the filter and is determined solely by the loop gain.

Figure 7 shows the typical frequency-to-voltage transfer characteristics of the PLL. The input is assumed to be a sine wave whose frequency is swept slowly over a broad frequency range. The vertical scale is the corresponding loop error voltage. In Figure 7(a), the input frequency is being gradually increased. The loop does not respond to the signal until it reaches a frequency ω_1, corresponding to the lower edge of the capture range. Then, the loop suddenly locks on the input and causes a negative jump of the loop error voltage. Next, V_d varies with frequency with a slope equal to the reciprocal of VCO conversion gain ($1/K_o$) and goes through zero as $\omega_i = \omega_o'$. The loop tracks the input until the input frequency reaches ω_2, corresponding to the upper edge of the lock range. The PLL then loses lock and the error voltage drops to zero. If the input frequency is swept slowly back, the cycle repeats itself, but is inverted, as shown in Figure 7(b). The loop recaptures the signal at ω_3 and tracks it down to ω_4. The total capture and lock ranges of the system are:

$$2\omega_C = \omega_3 - \omega_1 \tag{27}$$

and

$$2\omega_L = \omega_2 - \omega_4 \tag{28}$$

Note that, as indicated by the transfer characteristics of Figure 7, the PLL system has an inherent selectivity about the free-running frequency, ω_o'. It will respond only to the input signal frequencies that are separated from ω_o' by less than ω_C or ω_L, depending on whether the loop starts with or without an initial lock condition. The linearity of the frequency-to-voltage conversion characteristics for the PLL is determined solely by the VCO conversion gain. Therefore, in most PLL applications, the VCO is required to have a highly linear voltage-to-frequency transfer characteristic.

DETERMINING LOOP RESPONSE

The transient response of a PLL can be calculated using the model of Figure 4 and Equations 18 and 19 as starting points. Combining these equations gives

$$H(s) = \frac{\Theta_o(s)}{\Theta_i(s)} = \frac{K_V F(s)}{s + K_V F(s)} \tag{29}$$

The phase error which keeps the system in lock is

$$\Theta_e(s) = \Theta_i(s) - \Theta_o(s) \tag{30}$$

Define a phase error transfer function

$$E(s) = \frac{\Theta_e(s)}{\Theta_i(s)} = 1 - \frac{\Theta_o(s)}{\Theta_i(s)} = 1 - H(s) \tag{31}$$

As an example of the utilization of these equations, consider the most common case of a loop employing a simple first-order lag filter where

$$F(s) = \frac{1}{1 + s\tau_1} \tag{32}$$

For this filter, Equations 29 and 31 become

$$H(s) = \frac{K_V/\tau_1}{s^2 + s/\tau_1 + K_V/\tau_1} \tag{33}$$

$$E(s) = \frac{s(s + 1/\tau_1)}{s^2 + s/\tau_1 + K_V/\tau_1} \tag{34}$$

Both equations are second order and have the same denominator which can be expressed as

$$D(s) = s^2 + s/\tau_1 + K_V/\tau_1 = s^2 + 2\zeta\omega_n s + \omega_n^2 \tag{35}$$

where ω_n and ζ are respectively the systems undamped natural frequency and damping factor defined as

$$\omega_n = \sqrt{K_V/\tau_1} \tag{36}$$

ROOT LOCUS AND FREQUENCY RESPONSE PLOTS

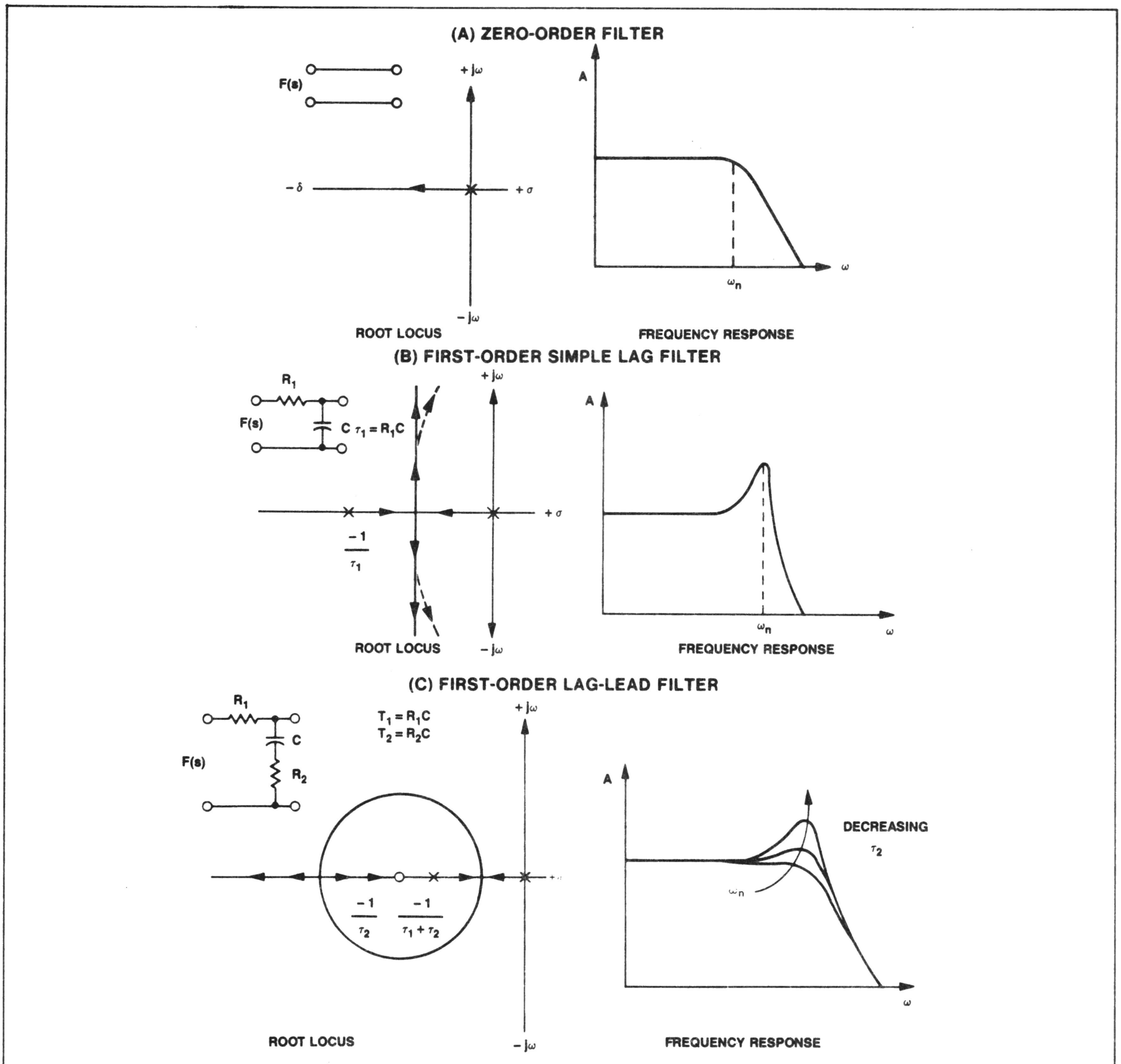

(A) ZERO-ORDER FILTER
F(s)
+jω
−δ
+σ
−jω
A
ω
ωn
ROOT LOCUS
FREQUENCY RESPONSE
(B) FIRST-ORDER SIMPLE LAG FILTER
R1
F(s)
C τ1 = R1C
+jω
+σ
−1/τ1
−jω
A
ωn
ω
ROOT LOCUS
FREQUENCY RESPONSE
(C) FIRST-ORDER LAG-LEAD FILTER
R1
C
R2
F(s)
T1 = R1C
T2 = R2C
+jω
−1/τ2
−1/(τ1 + τ2)
−jω
A
DECREASING τ2
ωn
ω
ROOT LOCUS
FREQUENCY RESPONSE

Figure 6

$$\zeta = \frac{1}{2\sqrt{K_v\tau_1}} = \frac{\omega_n}{2K_v} \qquad (37)$$

The system is considered overdamped for >1.0, and critically damped $\zeta = 1.0$.

Now examine this PLL systems response to various types of inputs.

Step of Phase Input

Consider a unit step of phase as the input signal. This input is shown in Figure 8 and can be thought of as simply shifting the time axis by a unit step (one radian or one degree depending upon the working units) while maintaining the same input frequency. Mathematically this input has the form

$$\Theta_i(s) = \frac{1}{s} \qquad (38)$$

The phase of VCO output and the systems phase error are represented by

$$\Theta_o(s) = \frac{H(s)}{s} = \frac{\omega_n{}^2}{s\,(s^2 + 2\zeta\omega_n s + \omega_n{}^2)} \qquad (39)$$

$$\Theta_e(s) = \frac{E(s)}{s} = \frac{s + 2\zeta\omega_n}{s^2 + 2\zeta\omega_n s + \omega_n{}^2} \qquad (40)$$

depending upon the working units) while maintaining the same input frequency. Mathematically this input has the form

$$\Theta_o(t) = 1 + \frac{e^{-\zeta\omega_n t}}{\sqrt{1-\zeta^2}}\sin\left(\omega_n t\sqrt{1-\zeta^2} + \Psi\right) \qquad (41)$$

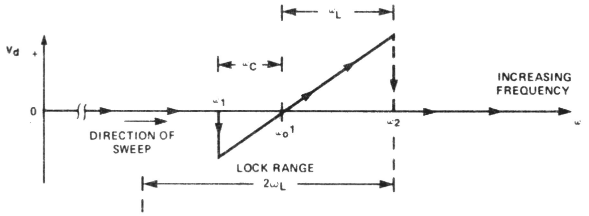
where $\Psi = \arc\tan \dfrac{\sqrt{1-\zeta^2}}{\zeta}$ (42)

and $\zeta \neq 1$.

$$\Theta_e(t) = \frac{e^{-\zeta\omega_n t}}{\sqrt{1-\zeta^2}}\sin\left(\omega_n t\sqrt{1-\zeta^2} + \Psi\right) \qquad (43)$$

TYPICAL PLL FREQUENCY-TO-VOLTAGE TRANSFER CHARACTERISTICS

(A) INPUT FREQUENCY INCREASING



(B) DECREASING INPUT FREQUENCY

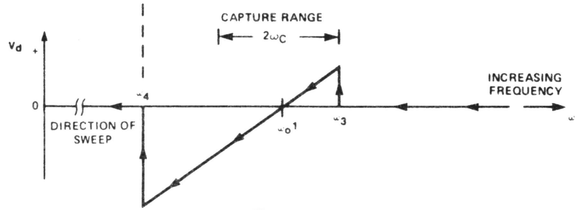


Figure 7

INPUT SIGNAL REPRESENTING A UNIT STEP OF PHASE AT CONSTANT FREQUENCY

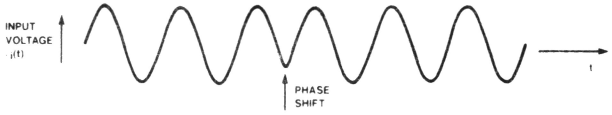


Figure 8

When $\zeta = 1$, these phase responses are

$$\Theta_o(t) = 1 - (1 - \omega_n t)e^{-\omega_n t} \tag{44}$$

and

$$\Theta_e(t) = (1 + \omega_n t)e^{-\omega_n t} \tag{45}$$

Figure 9 is a plot of the VCO phase response and the phase error transient for various damping factors. Note from this figure that an under-damped system has overshoot which can cause the loop to break lock if this overshoot is too large. The critical condition for maintaining lock is to keep the phase error within the dynamic range for the phase comparator of $-\pi/2$ to $\pi/2$ radians. For the under-damped case, the peak phase-error overshoot is

$$\Theta_{e(max)} = e^{-\zeta\pi/\sqrt{1 - \zeta^2}} \tag{46}$$

which must be less than $\pi/2$ to maintain lock. Lock can also be broken for the over-damped and critically-damped loops if the input phase shift is too large where the phase error exceeds $\pm\pi/2$ radians.

The analysis and equations given are based upon the small-signal model of Figure 4. If the signal amplitudes become too large, one or more functional blocks in the system can saturate, causing a slew-rate type limiting action that may break lock.

The *transient change* in the VCO frequency due to the unit step of phase input can be found by taking the time derivative of Equation 41 or alternatively by finding the inverse Laplace transform of

$$\omega_o(s) = s\Theta_o(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{47}$$

which is

$$\omega_o(t) = \frac{\omega_n e^{-\zeta\omega_n t}}{\sqrt{1 - \zeta^2}} \sin \omega_n t \sqrt{1 - \zeta^2} \tag{48}$$

Unit Step of Frequency Input

This type of input occurs when the input frequency is instantaneously changed from one frequency to another as is done in FSK and modem applications. For this input as shown in Figure 10,

$$\Theta_i(s) = \frac{1}{s^2} \tag{49}$$

The VCO output phase is

$$\Theta_o(s) = \frac{\omega_n^2}{s^2(s^2 + 2\zeta\omega_n s + \omega_n^2)} \tag{50}$$

The transient time expression for the *VCO phase change* is

$$\Theta_o(t) = t - \frac{2\zeta}{\omega_n} + \frac{e^{-\zeta\omega_n t}}{\omega_n\sqrt{1 - \zeta^2}}$$

$$\sin (\omega_n t \sqrt{1 - \zeta^2} + 2\Psi) \tag{51}$$

for $\zeta \neq 1$.

The time expression for the VCO *frequency change* for a unit step of frequency input is the same as the time response VCO phase change due to a step of phase input (Equation 41), or

$\omega_O(t)$ for frequency step input $= \Theta_o(t)$ for phase step input

Thus

$$\omega_o(t) = 1 + \frac{e^{-\zeta\omega_n t}}{\sqrt{1 - \zeta^2}} \sin (\omega_n t \sqrt{1 - \zeta^2} + \Psi) \tag{52}$$

for $\zeta \neq 1$.

Unit Ramp of Frequency Input

This form of input signal represents sweeping the input frequency at a constant rate and direction as shown in Figure 11. The amplitude and phase of the input remain constant; the input frequency changes linearly with time. Since the input signal to the PLL model is a phase, a unit ramp of frequency appears as a phase acceleration type input that can be mathematically described as

$$\Theta_i(s) = \frac{1}{s^3} \tag{53}$$

The VCO output phase change is

$$\Theta_o(s) = \frac{\omega_n^2}{s^3 (s^2 + 2\zeta\omega_n s + \omega_n^2)} \tag{54}$$

The time expression for the VCO phase change is

$$\Theta_o(t) = \frac{t^2}{2} - \frac{2\zeta t}{\omega_n} + \frac{2\zeta}{\omega_n^2}\Bigg[2\zeta(1 - \omega_n^2) + \left(\frac{1 - 4\zeta^2\omega_n^2 + 4\zeta^2\omega_n^4}{1 - \zeta^2}\right)^{1/2} \times e^{-\zeta\omega_n t} \sin (\omega_n t \sqrt{1 - \zeta^2} + \Psi')\Bigg] \tag{55}$$

where $\Psi' = \arctan \dfrac{\sqrt{1 - \zeta^2}}{\zeta(1 - 2\omega_n^2)} + \Psi$

and Ψ is given in **Equation** 42.

PLL BUILDING BLOCKS

VCO

Since three different forms of VCO have been used in the Signetics PLL series, the VCO details will not be discussed until the individual loops are described. However, a few general comments about VCOs are in order.

When the PLL is locked to a signal, the VCO voltage is a function of the frequency of the input signal. Since the VCO control voltage is the demodulated output during FM demodulation, it is important that the VCO voltage-to-frequency characteristic be lin-

ear so that the output is not distorted. Over the linear range of the VCO, the conversion gain is given by K_O (in radian/volt-sec)

$$k_o = \frac{\Delta\omega_o}{\Delta V_d} \tag{56}$$

Since the loop output voltage is the VCO voltage, we can get the loop output voltage as

$$\Delta V_d = \frac{\Delta\omega_o}{K_o} \tag{57}$$

The gain K_o can be found from the data sheet. When the VCO voltage is changed, the frequency change is virtually instantaneous.

Phase Comparator

All of Signetics analog phase locked loops use the same form of phase comparator - often called the doubly-balanced multiplier or mixer. Such a circuit is shown in Figure 12.

The input stage formed by transistors Q1 and Q2 may be viewed as a differential amplifier which has an equivalent collector resistance R_c and whose differential gain at balance is the ratio of R_c to the dynamic emitter resistance, r_e, of Q1 and Q2.

$$A_d = \frac{R_C}{r_e} = \frac{R_C}{\frac{0.026}{I_E/2}} = \frac{R_C I_E}{0.052} \tag{58}$$

where I_E is the total dc bias current for the differential amplifier pair.

The switching stage formed by Q3–Q6 is switched on and off by the VCO square wave. Since the collector current swing of Q2 is the negative of the collector current swing of Q1, *the switching action has the effect of multiplying the differential stage output first by +1 and then by −1.* That is, when the base of Q4 is positive, R_{C2} receives I_1 and when the base of Q6 is positive, R_{C2} receives $i_2 = i_1$. *Since the circuit is called a multiplier, performing the multiplication will gain further insight into the action of the phase comparator.*

VCO PHASE AND LOOP PHASE ERROR TRANSIENT RESPONSES FOR VARIOUS DAMPING FACTORS

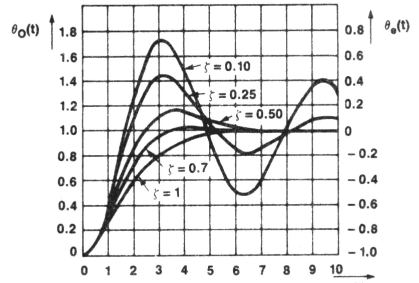


Figure 9

INPUT SIGNAL FOR A UNIT STEP OF FREQUENCY AT CONSTANT PHASE

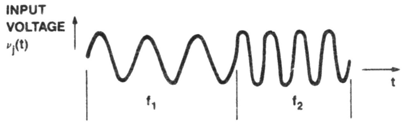


Figure 10

INPUT SIGNAL FOR A UNIT RAMP OF FREQUENCY INPUT

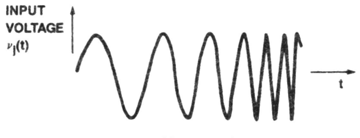


Figure 11

Consider an input signal which consists of two added components: a component at frequency ω_i which is close to the free-running frequency and a component at frequency ω_k which may be at any frequency. The input signal is

$$v_i(t) + v_k(t) = V_i \sin(\omega_i t + \Theta_i) + V_k \sin(\omega_k t + \Theta_k) \tag{59}$$

where Θ_i and Θ_k are the phase in relation to the VCO signal. The unity square wave developed in the multiplier by the VCO signal is

$$v_o(t) = \sum_{n=0}^{\infty} \frac{4}{\pi(2n+1)} \sin\left[(2n+1)\omega_o t\right] \tag{60}$$

where ω_o is the VCO frequency. Multiplying the two terms, using the appropriate trigonometric relationships, and inserting the differential stage gain A_d gives:

$$\begin{aligned} v_e(t) = \frac{2A_d}{\pi} & \left[\sum_{n=0}^{\infty} \frac{V_i}{(2n+1)} \cos\left[(2n+1)\omega_o t - \omega_i t - \Theta_i\right]\right. \\ & - \sum_{n=0}^{\infty} \frac{V_i}{(2n+1)} \cos\left[(2n+1)\omega_o t + \omega_i t + \Theta_i\right] \\ & + \sum_{n=0}^{\infty} \frac{V_k}{(2n+1)} \cos\left[(2n+1)\omega_o t - \omega_k t - \Theta_k\right] \\ & \left. - \sum_{n=0}^{\infty} \frac{V_k}{(2n+1)} \cos\left[(2n+1)\omega_o t + \omega_k t + \Theta_k\right]\right] \end{aligned} \tag{61}$$

Assuming that temporarily V_k is zero, if ω_1 is close to ω_o, the first term (n = 0) has a low frequency difference frequency component. This is the beat frequency component that feeds around the loop and causes lock up by modulating the VCO. As ω_o is driven closer to ω_i, this difference component becomes lower and lower in frequency until $\omega_o = \omega_i$ and lock is achieved. The first term then becomes

$$v_e(t) = V_E = \frac{2A_d V_i}{\pi} \cos\Theta_i \tag{62}$$

which is the usual phase comparator formula showing the dc component of the phase comparator during lock. This component must equal the voltage necessary to keep the VCO at ω_o. It is possible for ω_o to equal ω_i momentarily during the lock up process and, yet, for the phase to be incorrect so that ω_o passes through ω_i without lock being achieved. This explains why lock is usually not achieved instantaneously, even when $\omega_i = \omega_o$ at t = 0.

If $n \neq 0$ in the first term, the loop can lock when $\omega_i = (2n+1)\,\omega_o$, giving the dc phase comparator component

$$V_e(t) = V_E = \frac{2A_d V_i}{\pi(2n+1)} \cos\Theta_i \tag{63}$$

INTEGRATED PHASE COMPARATOR CIRCUIT

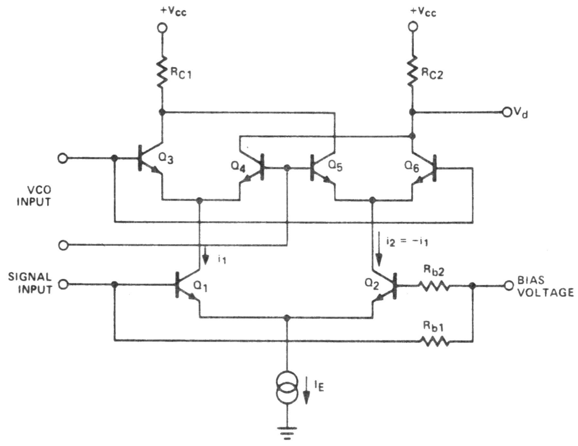


Figure 12

showing that the loop can lock to odd harmonics of the free-running frequency. The (2n + 1) term in the denominator shows that the phase comparators output is lower for harmonic lock, which explains why the lock range decreases as higher and higher odd harmonics are used to achieve lock.

Note also that the phase comparators output during lock is (assuming A_d is constant) also a function of the input amplitude V_i. Thus, for a given dc phase comparator output V_E, an input amplitude decrease must be accompanied by a phase change. Since the loop can remain locked only for Θ_i between 0 and 180°, the lower V_i becomes, the more the lock range is reduced.

Note from the second term that during lock the lowest possible frequency is $\omega_o + \omega_i = 2\omega_i$. A sum frequency component is always present at the phase comparator output. This component is usually greatly attenuated by the low pass filter capacitor connected to the phase comparator output. However, when rapid tracking is required (as with high-speed FM detection or FSK-frequency shift keying), the requirement for a relatively high frequency cutoff in the low pass filter may leave this component unattenuated to the extent that it interferes with detection. At the very least, additional filtering may be required to remove this component. Components caused by $n \neq 0$ in the second term are both attenuated and of much higher frequency, so they may be neglected.

Suppose that other frequencies represented by V_k are present. What is their effect for $V_k \neq 0$?

The third term shows that V_k introduces another difference frequency component. Obviously, if ω_k is close to ω_i, it can interfere with the locking process since it may form a beat frequency of the same magnitude as the desired locking beat frequency. However, suppose lock has been achieved so that $\omega_o = \omega_i$. In order for lock to be maintained, the average phase comparator output must be constant. If $\omega_o = \omega_k$ is relatively low in frequency, the phase Θ_i must change to compensate for this beat frequency. Broadly speaking, any signal in addition to the signal to which the loop is locked causes a phase variation. Usually this is negligible since ω_k is often far removed from ω_i. However, it has been stated that the phase Θ_i can move only between 0 and 180°. Suppose the phase limit has been reached and V_k appears. Since it cannot be compensated for, it will drive the loop out of lock. This explains why extraneous signals can result in a decrease in the lock range. If V_k is assumed to be an instantaneous noise component, the same effect occurs. When the full swing of the loop is being utilized, noise will decrease the lock or tracking range. This effect can be reduced by decreasing the cutoff frequency of the low pass filter so that the $\omega_o - \omega_k$ is attenuated to a greater extent, which illustrates that noise immunity and out-band frequency rejection is improved (at the expense of capture range since $\omega_o - \omega_i$ is likewise attenuated) when the low pass filter capacitor is large.

The third term can have a dc component when ω_k is an odd harmonic of the locked frequency so that $(2n + 1)(\omega_o - \omega_1)$ is zero and Θ_k makes its appearance. This will have an effect on Θ_1 which will change the Θ_1 versus frequency ω_1. This is most noticeable when the waveform of the incoming signal is, for example, a square wave. The Θ_k term will combine with the Θ_i term so that the phase is a linear function of input frequency. Other waveforms will give different phase versus frequency functions. When the input amplitude V_i is large and the loop gain is large, the phase will be close to 90° throughout the range of VCO swing, so this effect is often unnoticed.

The fourth term is of little consequence except that if ω_k approaches zero, the phase comparator output will have a component at the locked frequency ω_o at the output. For example, a dc offset at the input differential stage will appear as a square wave of fundamental ω_o at the phase comparator output. This is usually small and well attenuated by the low pass filter. Since many out-band signals or noise components may be present, many V_k terms may be combining to influence locking and phase during lock. Fortunately, only those close to the locked frequency need be considered.

Quadrature Phase Detector (QPD)

The quadrature phase detector action is exactly the same except that its output is proportional to the sine of the phase angle. When the phase Θ_i is 90°, the quadrature phase detector output is then at its maximum, which explains why it makes a useful lock or amplitude detector. The output of the quadrature phase detector is given by

$$V_q = \frac{2A_qV_i}{\pi} \sin \Theta_i \qquad (64)$$

where V_i is the constant or modulated AM signal and $\Theta_i \approx 90°$ in most cases so that $\sin \Theta_i = 1$ and

$$V_q = \frac{2A_qV_i}{\pi} \qquad (65)$$

This is the demodulation principle of the autodyne receiver and the basis for the 567 tone decoder operation.

INITIAL PLL SETUP CHOICES

In a given application, maximum PLL effectiveness can be achieved if the designer understands the tradeoffs which can be made. Generally speaking, the designer is free to select the frequency, lock range, capture range, and input amplitude.

FREE-RUNNING FREQUENCY SELECTION

Setting the center or free-running frequency is accomplished by selecting one or two external components. The center frequency is usually set in the center of the expected input frequency range. Since the loops ability to capture is a function of the *difference* between the incoming and free-running frequencies, the band edges of the capture range are *always* an equal distance (in Hz) from the center frequency. Typically, the lock range is also centered about the free-running frequency. Occasionally, the center frequency is chosen to be offset from the incoming frequency so that the tracking range is limited on one side. This permits rejection of an adjacent higher or lower frequency signal without paying the penalty for narrow band operation (reduced tracking speed).

All of Signetics loops use a phase comparator in which the input signal is multiplied by a unity square wave at the VCO frequency. The odd harmonics present in the square wave permit the loop to lock to input signals at these odd harmonics. Thus, the center frequency may be set to, say, 1/3 or 1/5 of the input signal. The tracking range however, will be considerably reduced as the higher harmonics are utilized.

The foregoing phase comparator discussion would suggest that the PLL cannot lock to subharmonics because the phase comparator cannot produce a dc component if ω_i is less than ω_o.

The loop can lock to both odd harmonic and subharmonic signals in practice because such signals often contain harmonic components at ω_o. For example, a square wave of fundamental $\omega_o/3$ will have a substantial component at ω_o to which the loop can lock. Even a pure sine wave input signal can be used for harmonic locking if the PLL input stage is overdriven (the resultant internal limiting generates harmonic frequencies). Locking to even harmonics or subharmonics is the least satisfactory since the input or VCO signal must contain second harmonic distortion. If locking to even harmonics is desired, the duty cycle of the input and VCO signals must be shifted away from the symmetrical to generate substantial even harmonic content.

In evaluating the loop for a potential application, it is best to actually compute the magnitude of the expected signal component nearest ω_o. This magnitude can be used to estimate the capture and lock ranges.

All of Signetics loops are stabilized against center frequency drift due to power supply variations. Both the 565 and the 567 are temperature compensated over the entire military temperature range (−55 to +125°C). To benefit from this inherent stability, however, the designer must provide equally stable (or better) external components. For maximum cost effectiveness in some noncritical applications, the designer may wish to trade some stability for lower cost external components.

GUIDELINES FOR LOCK RANGE CONTROL

Two things limit the lock range. First, any VCO can swing only so far; if the input signal frequency goes beyond this limit, lock will be lost. Second, the voltage developed by the phase comparator is proportional to the product of *both* the phase and the amplitude of the in-band component to which the loop is locked. If the signal amplitude decreases, the phase difference between the signal and the VCO must increase in order to maintain the same output voltage and, hence, the same frequency deviation. The 564 contains an internal limiter circuit between the signal input and one input to the phase comparator. This circuit limits the amplitude of large input signals such as those from TTL outputs to approximately 100mV before they are applied to the phase comparator. The limiter significantly improves the AM rejection of the PLL for input signal amplitudes greater than 100mV.

It often happens with low input amplitudes that even the full ±90° phase range of the phase comparator cannot generate enough voltage to allow tracking wide deviations. When this occurs, the effective lock range is reduced. Weak input signals cause a reduction of tracking capability and greater phase errors. Conversely, a strong input signal will allow the use of the entire VCO swing capability and keeps the VCO phase (referred to the input signal) very close to 90° throughout the range. Note that the lock range does not depend on the low pass filter. However, if a low pass filter *is* in the loop, it will have the effect of limiting the maximum *rate* at which tracking can occur. Obviously, the LPF capacitor voltage cannot change instantly, so lock may be lost when large enough step changes occur. Between the constant frequency input and the step-change frequency input is some limiting frequency slew rate at which lock is just barely maintained. When tracking at this rate, the phase difference is at its limit of 0° or 180°. It can be seen that if the LPF cutoff frequency is low, the loop will be unable to track as fast as if the LPF cutoff frequency is higher. *Thus, when maximum tracking rate is needed, the LPF should have a high cutoff frequency.* However, a high cutoff frequency LPF will attenuate the sum frequencies to a lesser extent so that the output contains a significant and often bothersome signal at twice the input frequency. The phase comparators output contains both sum and difference frequencies. During lock, the difference frequency is zero, but the sum frequency of twice the locked frequency is still present. This sum frequency component can then be filtered out with an external low pass filter.

INPUT LEVEL AMPLITUDE SELECTION

Whenever amplitude limiting of the in-band signal occurs, whether in the loop input stages or prior to the input, the lock and capture ranges become independent of signal amplitude.

Better noise and out-band signal immunity is achieved when the input levels are below the limiting threshold since the input stage is in its linear region and the creation of cross-modulation components is reduced. Higher input levels will allow somewhat faster operation due to greater phase comparator gain and will result in a lock range which becomes constant with amplitude as the phase comparator gain becomes constant. Also, high input levels will result in a linear phase versus frequency characteristic.

CAPTURE RANGE CONTROL

There are two main reasons for making the low pass filter time constant large. First, a large time constant provides an increased memory effect in the loop so that it remains at or near the operating frequency during momentary fading or loss of signal. Second, the large time constant integrates the phase comparators output so that increased immunity to noise and out-band signals is obtained.

Besides the lower tracking rates attendant to large loop filters, other penalties must be paid for the benefits gained. The capture range is reduced and the capture transient becomes longer. Reduction of capture range occurs because the loop must utilize the magnitude of the difference frequency component at the phase comparator to drive the VCO towards the input frequency.

If the LPF cutoff frequency is low, the difference component amplitude is reduced and the loop cannot swing as far. Thus, the capture range is reduced.

LOCK-UP TIME AND TRACKING SPEED CONTROL

In tracking applications, lock-up time is normally of little consequence, but occasions do arise when it is desirable to keep lock-up time short to minimize data loss when noise or extraneous signals drive the loop out of lock. Lock-up time is of great importance in tone decoder type applications. Tracking speed is important if the loop is used to demodulate an FM signal. Although the following discussion dwells largely on lock-up time, the same comments apply to tracking speeds.

No simple expression is available which adequately describes the acquisition or lock-up time. This may be appreciated when we review the following factors which influence lock-up time.

a Input phase
b Low pass filter characteristic
c Loop damping
d Deviation of input frequency from center frequency
e In-band input amplitude
f Out-band signals and noise
g Center frequency

Fortunately, it is usually sufficient to know how to improve the lock-up time and what must be sacrificed to get faster lock-up. Consider an operational loop or tone decoder where occasionally the lock-up transient is too long. What can be done to improve the situation-keeping in mind the factors that influence lock?

a Initial phase relationship between incoming signal and VCO - This is the greatest single factor influencing the lock time. If the initial phase is wrong, it first drives the VCO frequency *away* from the input frequency so that the VCO frequency must walk back on the beat notes. Figure 13 gives a typical distribution of lock-up times with the input pulse initiated at random phase. The only way to overcome this variation is to send phase information all the time so that a favorable phase relationship is guaranteed at t = 0. For example, a number of PLLs or tone decoders may be weakly locked to low amplitude harmonics of a pulse train and the transmitted tone phase related to the same pulse train. Usually, however, the incoming phase cannot be controlled.

PROBABILITY OF LOCK VERSUS INPUT CYCLES

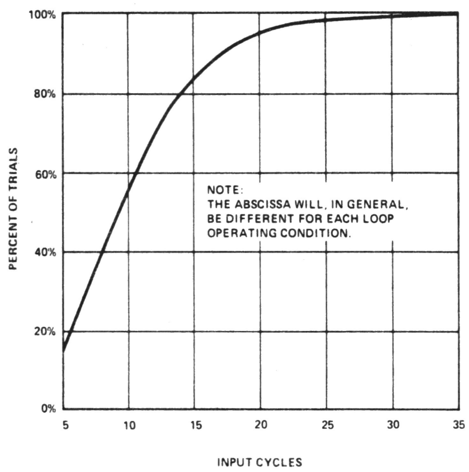


Figure 13

b Low pass filter - The larger the low pass filter time constant, the longer will be the lock-up time. The lock-up time can be reduced by decreasing the filter time constant, but in doing so, some of the noise immunity and out-band signal rejection will be sacrificed. This is unfortunate since this is what necessitated the use of a large filter in the first place. Also present will be a sum frequency (twice the VCO frequency) component at the low pass filter and greater phase jitter resulting from out-band signals and noise. In the case of the tone decoder (where control of the capture range is required since it specifies the device bandwidth) a lower value of low pass capacitor automatically increases the bandwidth. Speed is gained only at the expense of added bandwidth.

c Loop damping - A simple first-order low pass filter of the form

$$F(s) = \frac{1}{1 + s\tau} \qquad (66)$$

produces a loop damping of

$$\zeta = \frac{1}{2}\sqrt{\frac{1}{\tau K_V}} \qquad (67)$$

Damping can be increased not only by reducing τ, as discussed above, but also by reducing the loop gain K_V. Using the loop gain reduction to control bandwidth or capture and lock ranges achieves better damping for narrow bandwidth operation. The penalty for this damping is that more phase comparator output is required for a given deviation so that phase errors are greater and noise immunity is reduced. Also, more input drive may be required for a given deviation.

d Input frequency deviation from free-running frequency - Naturally, the further an applied input signal is from the free-running frequency of the loop, the longer it will take the loop to reach that frequency due to the charging time of the low pass filter capacitor. Usually, however, the effect of this frequency deviation is small compared to the variation resulting from the initial phase uncertainty. Where loop damping is very low, however, it may be predominant.

e In-band input amplitude - Since input amplitude is one factor in the phase comparators gain K_d and since K_d is a factor in the loop gain K_V, damping is also a function of input amplitude. When the input amplitude is low, the lock-up time may be limited by the rate at which the low pass capacitor can charge with the reduced phase comparator output (see d above).

f Out-band signals and noise - Low levels of extraneous signals and noise have little effect on the lock-up time, neither improving or degrading it. However, large levels may overdrive the loop input stage so that limiting occurs, at which point the in-band signal starts to be suppressed. The lower effective input level can cause the lock-up time to increase, as discussed in e above.

g Center frequency-Since lock-up time can be described in terms of the number of cycles to lock, fastest lock-up is achieved at higher frequencies. Thus, whenever a system can be operated at a higher frequency, lock will typically take place faster. Also, in systems where different frequencies are being detected, the higher frequencies *on the average* will be detected before the lower frequencies.

However, because of the wide variation due to initial phase, the reverse may be true for any single trial.

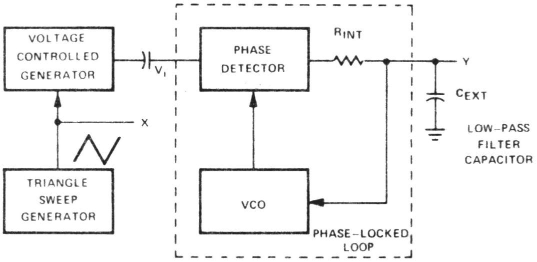
PLL MEASUREMENT TECHNIQUES

This section deals with measurements of PLL operation. The techniques suggested are meant to help the designer in evaluating the performance of the PLL during the initial setup period as well as to point out some pitfalls that may obscure loop evaluation. Recognizing that the test equipment may be limited, techniques are described which require a minimum of standard test items.

The majority of the PLL tests described can be done with a signal generator, a scope and a frequency counter. Most laboratories have these. A low-cost digital voltmeter will facilitate accurate measurement of the VCO conversion gain. Where the need for a FM generator arises, it may be met in most cases by the VCO of a Signetics PLL. Any of the loops may be set up to operate as a VCO by simply applying the modulating voltage to the low pass filter terminal(s). The resulting generator may be checked for linearity by using the counter to check frequency as a function of modulating voltage. Since the VCOs may be modulated right down to dc, the calibration may be done in steps. Moreover, loop measurements may be made by applying a *constant* frequency to the loop input and the modulating signal to the low pass filter terminal to simulate the effect of a FM input so that a FM generator may be omitted for many measurements.

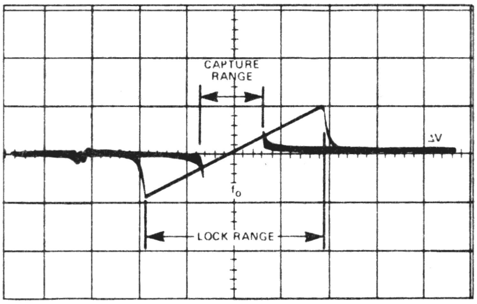
CAPTURE AND LOCK RANGES

MEASUREMENT SETUP



(a)

OSCILLOSCOPE DISPLAY



(b)

Figure 14

FREE-RUNNING FREQUENCY

Free-running frequency measurements are easily made by connecting a frequency counter or oscilloscope to the VCO output of the loop. The loop should be connected in its final configuration with the chosen values of input, bypass, and low pass filter capacitors. No input signal should be present. As the free-running frequency is read out, it can be adjusted to the desired value by the adjustment means selected for the particular loop. It is important not to make the frequency measurement directly at the timing capacitor unless the capacity added by the measurement probe is much less than the timing capacitor value since the probe capacity will then cause a frequency error.

When the frequency measurement is to be converted to a dc voltage for production readout or automated testing, a calibrated phase locked loop can be used as a frequency meter.

CAPTURE AND LOCK RANGES

Figure 14(a) shows a typical measurement setup for capture and lock range measurements. The signal input from a variable frequency oscillator is swept linearly through the frequency range of interest and the loop FM output is displayed on a scope or (at low frequencies) X-Y recorder. The sweep voltage is applied to the X axis.

Figure 14(b) shows the type of trace which results. The lock range is given by the outer lines on the trace, which are formed as the incoming frequency sweeps away from the center frequency. The inner trace, formed as the frequency sweeps toward the center frequency, designates the capture range. Linearity of the VCO is revealed by the straightness of the trace portion within the lock range. The slope $(\Delta f/\Delta V)$ is the conversion gain K_o for the VCO *at the particular free-running frequency.*

By using the sweep technique, the effect on free-running frequency, capture range, and lock range of the input amplitude, supply voltage, low pass filter and temperature can be examined.

Because of the lock-up time duration and variation, the sweep frequency must be very much lower than the free-running frequency, especially when the capture range is below 10% of the free-running frequency. Otherwise, the *apparent* capture and lock range will be function os sweep frequency. It is best to start sweeping as slow as possible and, if desired, increase the rate until the capture range begins to show an apparent reduction - indicating that the sweep is too fast. Typical sweep frequencies are in the range of 1/1000 to 1/100,000 of the free-running frequency. In the case of the 567, the quadrature detector output may be similarly displayed on the Y axis, as shown in Figure 15 showing the output level versus frequency for one value of input amplitude.

Capture and lock range measurements may also be made by sweeping the generator manually through the band of interest. Sweeping must be done very slowly as the edges of the capture range are approached (sweeping toward center frequency) or the

QUADRATURE PHASE DETECTOR AND PHASE COMPARATOR OUTPUTS OF THE 567 PLL

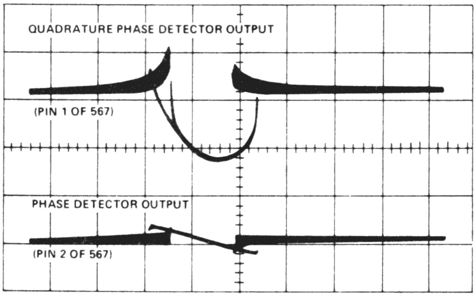


Figure 15

lock-up transient delay will cause an error in reading the band edge. Frequency should be read from the generator rather than the loop VCO because the VCO frequency gyrates wildly around the center frequency just before and after lock. Lock and unlock can be readily detected by simultaneously monitoring the input and VCO signals, the dc voltage at the low pass filter or the ac beat frequency components at the low pass filter. The latter are greatly reduced during lock as opposed to frequencies just outside of lock.

FM AND AM DEMODULATION DISTORTION

These measurements are quite straightforward. The loop is simply setup for FM detection and the test signal is applied to the input. A spectrum analyzer or distortion analyzer (HP333A) can be used to measure distortion at the FM output.

For FM demodulation, the input signal amplitude must be large enough so that lock is not lost at the frequency extremes. The data sheets give the lock (or tracking) range as a function of input signal and the optional range control adjustments. Due to the inherent linearity of the VCOs, it makes little difference whether the FM carrrier is at the free-running frequency or offset slightly as long as the tracking range limits are not exceeded.

The faster the FM modulation in relation to the center frequency, the lower the value of the capacitor in the low pass filter must be for satisfactory tracking. As this value decreases, however, it attenuates the sum frequency component of the phase comparator output less. The demodulated signal will appear to have greater distortion unless this component is filtered out before the distortion is measured.

NATURAL FREQUENCY AND DAMPING

Circuits and mathematical expressions for the natural frequencies and dampings are given in Figure 16 for two, first-order low pass filters. Because of the integrator action of the PLL in converting frequency to phase, the order of the loop always will be one greater than the order of the LPF. Hence both these first order LPFs produce a second order PLL system.

The natural frequency (ω_n) of a loop in its final circuit configuration can be measured by applying a frequency modulated signal of the desired amplitude to the loop. Figure 16 shows that the natural frequency is a function of K_d, which is, in turn, a function of input amplitude. As the modulation frequency (ω_m) is increased, the phase relationship between the modulation and recovered sine wave will go through 90° at $S_m = \omega_n$ and the output amplitude will peak.

Damping is a function of K_d, K_o, and the low pass filter. Since K_o and K_d are functions of the free-running frequency and input amplitude respectively, damping is highly dependent on the particular operating condition of the loop. Damping estimates for the desired operating condition can be made by applying an input signal which is frequency modulated within the lock range by a square wave. The low pass filter voltage is then monitored on an oscilloscope which is synchronized to the modulating waveform, as shown in Figure 17. Figure 18 shows typical waveforms displayed. The loop damping can be estimated by comparing the number and magnitude of the overshoots with the graph of Figure 19 which gives the transient phase error due to a step in input frequency.

An expression for calculating the damping for any underdamped second-order system ($\zeta < 1.0$) when the normalized peak overshoot is known is

$$M_p = 1 + e^{-\zeta\pi/\sqrt{1-\zeta^2}} \qquad (68)$$

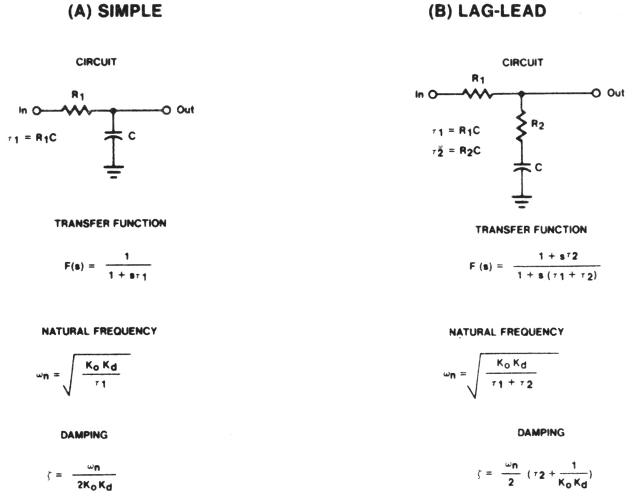
Examination of Figure 18 shows that the normalized peak overshoot of the error voltage is approximately 1.4. Using this value for M_p in Equation 68 gives a damping of $\zeta \cong 0.28$.

Another way of estimating damping is to make use of the frequency response plot measured for the natural frequency (ω_n) measurement. For low damping constants, the frequency response measurement peak will be a strong function of damping. For high damping constants, the 3dB-down point will give the damping. Figure 19 tabulates some approximate relationships.

NOISE

The effect of input noise on loop operation is very difficult to predict. Briefly, the input noise components near the center frequency are converted to phase noise. When the phase noise becomes so great that the ±90° permissible phase variation is exceeded, the loop drops out of lock or fails to acquire lock. The best technique is to actually apply the anticipated noise amplitude and bandwidth to the input and then perform the capture and lock range measurements as well as perform operating tests with the anticipated input level and modulation deviations. By including a small safety factor in the loop design to compensate for small processing variations, satisfactory operation can be assured.

FIRST ORDER LOW PASS FILTERS


(A) SIMPLE
CIRCUIT
R1
In
Out
C
(B) LAG-LEAD
CIRCUIT
R1
In
Out
R2
C

(A) SIMPLE

$\tau_1 = R_1C$

TRANSFER FUNCTION

$$F(s) = \frac{1}{1 + s\tau_1}$$

NATURAL FREQUENCY

$$\omega_n = \sqrt{\frac{K_o K_d}{\tau_1}}$$

DAMPING

$$\zeta = \frac{\omega_n}{2K_o K_d}$$

(B) LAG-LEAD

$\tau_1 = R_1C$

$\tau_2 = R_2C$

TRANSFER FUNCTION

$$F(s) = \frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)}$$

NATURAL FREQUENCY

$$\omega_n = \sqrt{\frac{K_o K_d}{\tau_1 + \tau_2}}$$

DAMPING

$$\zeta = \frac{\omega_n}{2}\left(\tau_2 + \frac{1}{K_o K_d}\right)$$

Figure 16

MEASUREMENT SETUP FOR DISPLAY OF PLL TRANSIENT RESPONSE

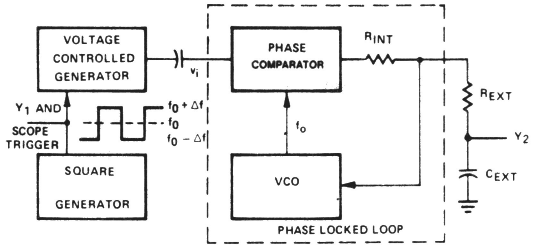
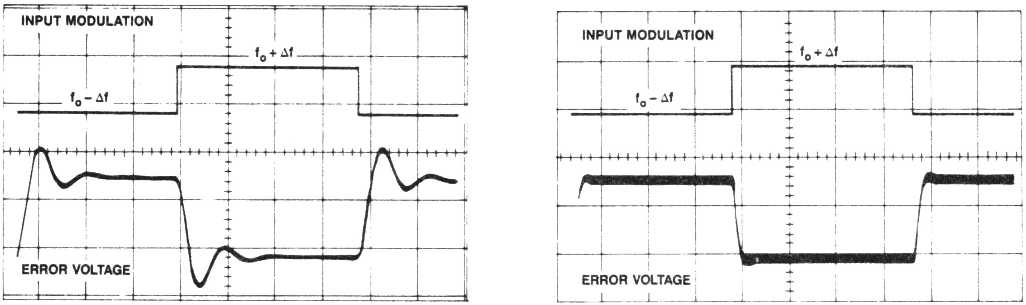

VOLTAGE CONTROLLED GENERATOR
v_i
PHASE COMPARATOR
R_{INT}
R_{EXT}
Y_1 AND SCOPE TRIGGER
$f_0 + \Delta f$
f_0
$f_0 - \Delta f$
f_o
Y_2
SQUARE GENERATOR
VCO
C_{EXT}
PHASE LOCKED LOOP

Figure 17

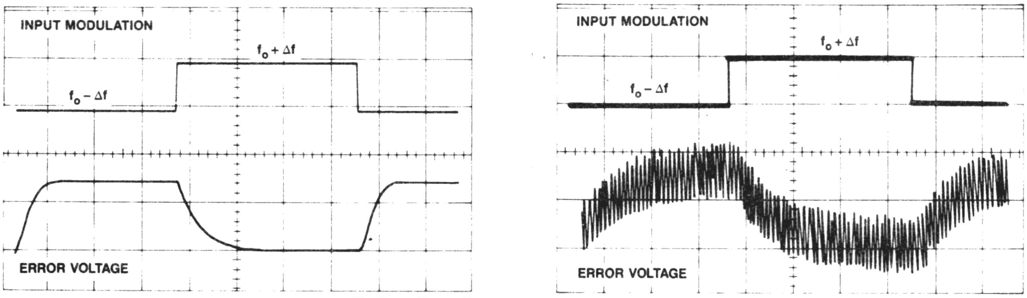
TRANSIENT RESPONSE OF PLL ERROR VOLTAGE TO SQUARE WAVE FREQUENCY MODULATION FOR VARIOUS DAMPING CONDITIONS:

(a) UNDERDAMPED WITH $\zeta \simeq 0.28$ (b) CRITICALLY DAMPED WITH $\zeta \simeq 1.0$



$(C_{EXT} > C_{CRIT}, R_{EXT} = 0)$ $(C_{EXT} = C_{CRIT}, R_{EXT} = 0)$

(c) OVERDAMPED WITH $\zeta \simeq 10$ (d) HIGHLY OVERDAMPED WITH $\zeta > 10$

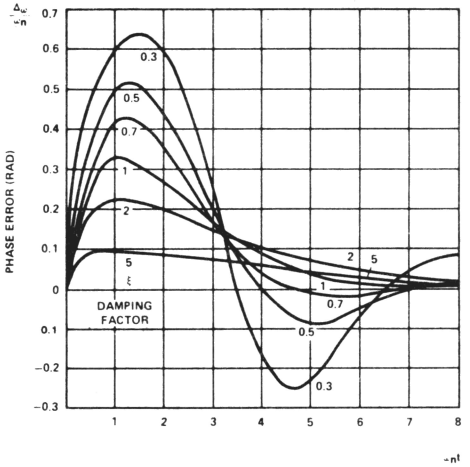


$(C < C_{CRIT}, R_{EXT} > 0)$ $(C << C_{CRIT}, R_{EXT} = 0)$

Figure 18

ESTIMATING THE DAMPING IN A SECOND ORDER PLL

(A) TRANSIENT PHASE ERROR AS AN INDICATION OF DAMPING



(a)

(B) RATIO OF PEAK AMPLITUDE TO LOW FREQUENCY AMPLITUDE OF ERROR VOLTAGE FROM MODULATING FREQUENCY RESPONSE

ζ	$\frac{\text{PEAK AMPLITUDE}}{\text{LOW FREQUENCY AMPLITUDE}}$	$\frac{\omega_{-3db}}{\omega_n}$
.3	6.0dB	1.8
.5	3.2dB	2.1
.7	2.2dB	2.5
1.0	1.3dB	4.3
5.0	0.5dB	10

(b)

Figure 19

CIRCUIT DESCRIPTION OF THE NE564

AN179

CIRCUIT DESCRIPTION OF THE 564

The 564 contains the functional blocks shown in Figure 1. In addition to the normal PLL functions of phase comparator, VCO, amplifier and low-pass filter, the 564 has internal circuitry for an input signal limiter, a dc retriever, and a Schmitt trigger. The complete circuit for the 564 is shown in Figure 1.

Limiter

The input limiter functions to produce a near constant amplitude output that serves as the input for the phase comparator. Eliminating amplitude variations in the FM input signal improves the AM rejection of the PLL. Additional features of the 564s limiter are that it is capable of accepting TTL signals, operates at high-frequencies up to 50MHz, and remains functional with variable supply voltages between 5 and 12* volts.

Signal limiting is accomplished in the 564 with a differential amplifier whose output voltage is clipped by diodes D_1 and D_2 (see Figure 2). Schottky diodes are used because their limiting occurs between 0.3 to 0.4 volts instead of the 0.6 to 0.7 volt for regular IC diodes. This lower limiting level is helpful in biasing, especially for 5 volt operation. When limiting, the dc voltage across R_2 R_3 remains at the Schottky diode voltage. Good high-frequency performance for Q2 and Q3 is achieved with current levels in the low mA range. Current-source biasing is established via the current mirror of D_5 and Q4 (See Figure 1).

Base biasing for Q3 is of concern because of the nature of the input signal which can be either a TTL digital signal of 0 to 5 volts amplitude or a low-level, ac coupled analog signal. Compatibility for either type is achieved by modifying the limiter of Figure 2 with the addition of the vertical Schottky PNP transistors Q1 and Q5 shown in Figure 3. The input signal voltage appears as a collector-base voltage for Q1 which presents no problems for either high TTL level inputs or low-level analog inputs. Q5 is in turn diode biased by D_3 and D_4 (see Figure 1) which places the base voltages of Q1 and Q5 at approximately 1.0 volt. This same biasing network establishes a 1.3 volt bias at the base of Q13 for biasing the phase comparator section. A differential output signal from the input limiter is applied to one input of the phase comparator (Q9 through Q12) after buffering the level shifting though the Q7-Q8 emitter followers.

Phase Comparator

The phase comparator section of the 564 is shown in Figure 4. It is basically the conventional, double-balanced mixer commonly used in PLL circuits with a few exceptions. The transconductance, g_m, for the Q13-Q14 differential amplifier is directly proportional to the mirror current in Q15. Thus by externally sinking or sourcing current at pin 2, g_m can be changed to alter the phase comparators conversion gain, K_d. The nominal current injected into this node by the internal current source is 0.75mA for 5 volt operation. If the current is

SCHEMATIC DIAGRAM OF 564

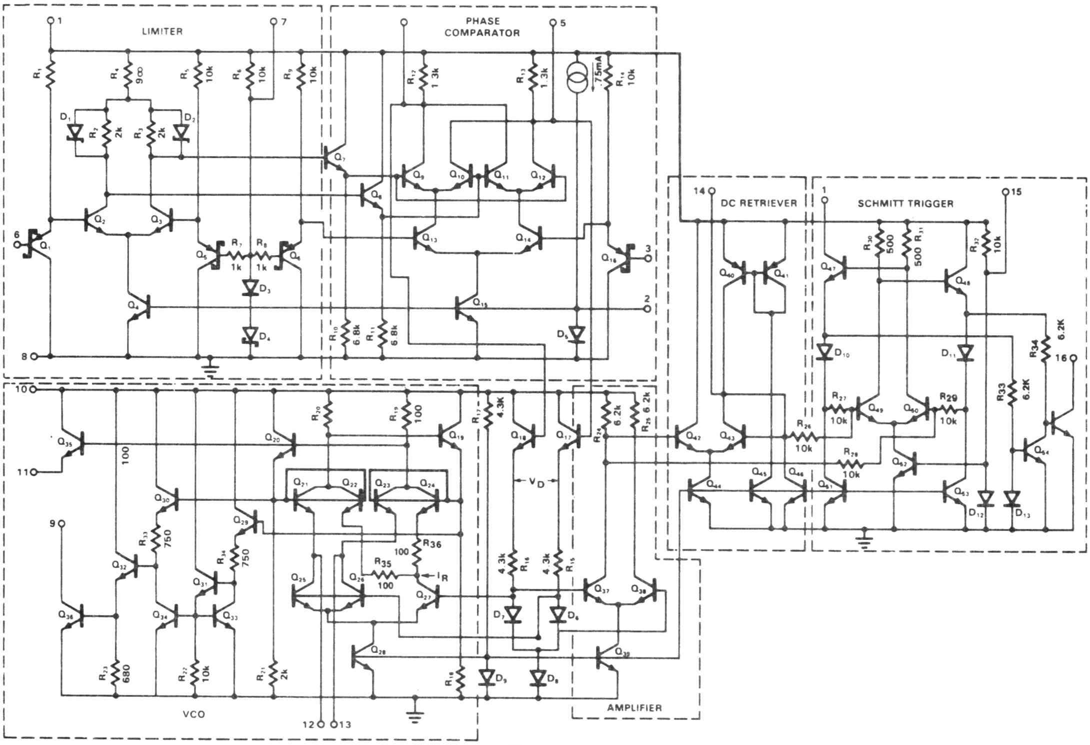


Figure 1

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*When operating above 5Vdc, a limiting resistor must be used from V_{CC} to pin 10 of the 564.

BASIC LIMITER STAGE

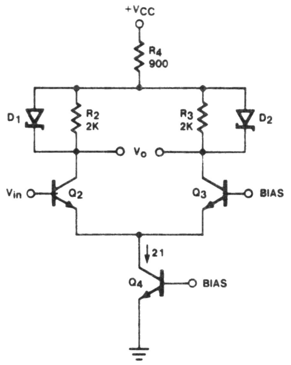

+VCC
R4
900
D1
R2
2K
R3
2K
D2
Vo
Vin
Q2
Q3
BIAS
21
Q4
BIAS

Figure 2

LIMITER STAGE WITH INPUT BUFFERING

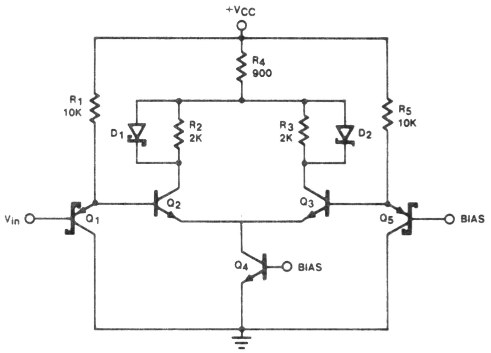

+VCC
R4
900
R1
10K
R5
10K
D1
R2
2K
R3
2K
D2
Vin
Q1
Q2
Q3
Q5
BIAS
Q4
BIAS

Figure 3

PHASE COMPARATOR SECTION

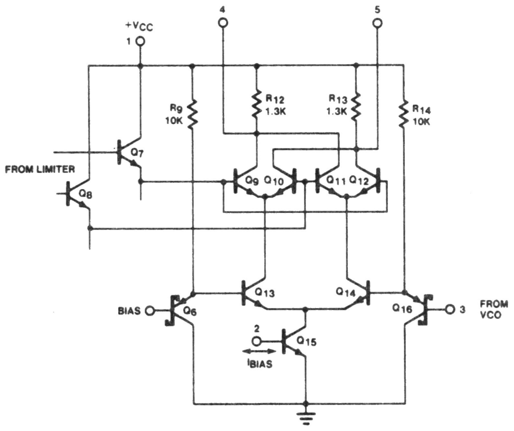

4
5
+VCC
1
R9
10K
R12
1.3K
R13
1.3K
R14
10K
Q7
FROM LIMITER
Q8
Q9
Q10
Q11
Q12
Q13
Q14
BIAS
Q6
Q16
3
FROM
VCO
2
Q15
IBIAS

Figure 4

VARIATION OF THE PHASE COMPARATOR'S OUTPUT VOLTAGE VERSUS PHASE ERROR AND BIAS CURRENT

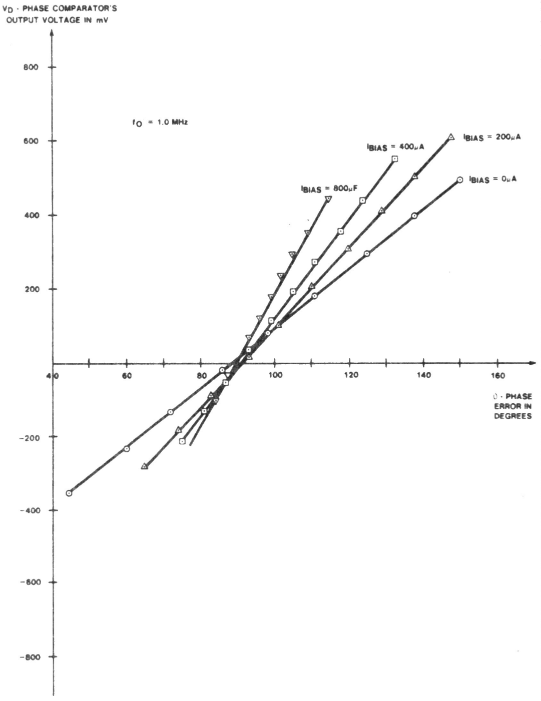


Figure 5

CIRCUIT DESCRIPTION OF THE NE564

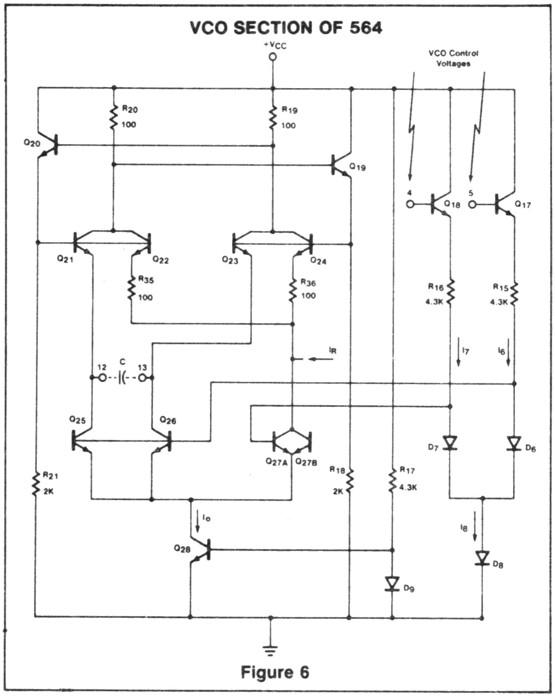


Figure 6

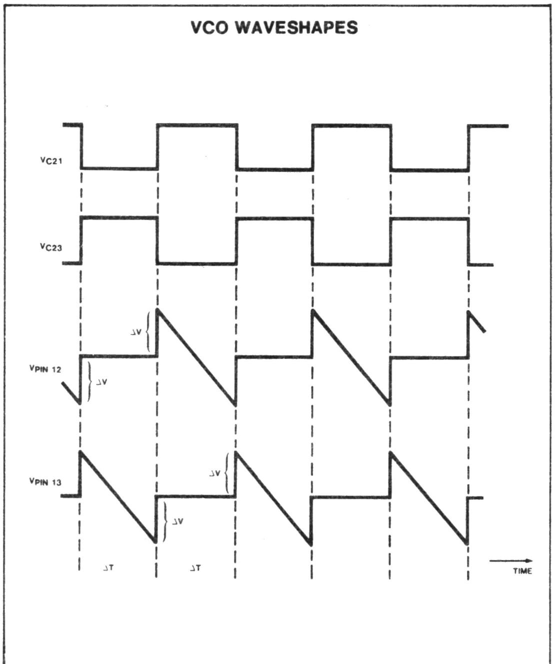


Figure 7

externally removed by gating, the phase comparator can be disabled and the VCO will operate at its free-running frequency.

The variation of K_d with bias current at pin 2 is shown in the experimental results of Figure 5. Note the inherent 90° phase error in the loop produces an approximate zero phase comparator output voltage. For any particular bias current, the slope of the line is the K_d conversion gain for the phase comparator. Numerically the data of Figure 5 can be expressed as

$$K_d \simeq 0.46 \frac{\text{volts}}{\text{rad}} + 7.3 \times 10^{-4} \frac{\text{volts}}{\text{rad} \times \mu A} \times I_{BIAS} \qquad (1)$$

where I_{BIAS} is in μA. Equation 1 is valid for bias current less than $800\mu A$ where saturation occurs within the phase comparator.

The current level established in Q15 of Figure 3 determines all other quiescent currents in the phase comparator (Q9 through Q14). Currents through R_{12} and R_{13} set the common-mode output voltage from the phase comparator (pins 4 and 5). Since this common-mode voltage is applied to the VCO to establish its quiescent currents, the VCO conversion gain (K_o) also depends upon the bias current at pin 2.

VCO

The VCO is of the basic emitter-coupled astable type with several modifications included to achieve the high frequency, TTL compatible operation while maintaining low frequency drift with temperature changes. The basic oscillator in Figure 6 consists of Q19, Q20, Q21, and Q23 with current sinks of Q25 and Q26. The master current sink of Q28 keeps the total current constant by altering the ratio of currents in Q25-Q26 and the dummy current sink of Q27.

The input drive voltage for the VCO is made up of common-mode and difference-mode components from the phase comparator. After buffering the level shifting through Q17-Q18 and R_{15}-R_{16}, the VCO control voltage is applied differentially to the base of Q27 and to the common bases of Q25 and Q26.

The VCO control voltages from the phase comparator are the pin 4 and pin 5 voltages or

$$V_4 = V_{C9} = V_{B18} = V_{CM} + \frac{1}{2} V_{DM} \qquad (2)$$

$$V_5 = V_{C12} = V_{B17} = V_{CM} - \frac{1}{2} V_{DM} \qquad (3)$$

where V_{CM} and V_{DM} are the respective common-mode and the difference-mode voltages.

Emitter followers Q17 and Q18 convert these control voltages into control currents through D_6 and D_7 of the form

$$I_6 = \frac{1}{R_{15}} \left[V_{CM} - \frac{1}{2} V_{DM} - 3\, V_{BE} \right] \qquad (4)$$

$$I_7 = \frac{1}{R_{16}} \left[V_{CM} + \frac{1}{2} V_{DM} - 3\, V_{BE} \right] \qquad (5)$$

These individual currents are summed in D_8 and become with $R_{15} = R_{16} = R$.

$$I_8 = I = I_6 + I_7 = \frac{2}{R} (V_{CM} - 3\, V_{BE}) \qquad (6)$$

Writing I_6 and I_7 as functions of the total I current gives

$$I_6 = \frac{I}{2} \left(1 - \frac{V_{DM}}{RI}\right) \qquad (7)$$

$$I_7 = \frac{I}{2} \left(1 + \frac{V_{DM}}{RI}\right) \qquad (8)$$

Now consider variations in I_6 and I_7 while I remains constant.

Let x indicate the current imbalance such that

$$I_6 = (1 - x)\, I = \frac{I}{2} \left(1 - \frac{V_{DM}}{RI}\right) \qquad (9)$$

$$I_7 = xI = \frac{I}{2} \left(1 + \frac{V_{DM}}{RI}\right) \qquad (10)$$

where $0 \leq x \leq 1$. Thus x is defined to be

$$x = \frac{1}{2} \left(1 + \frac{V_{DM}}{RI}\right) \qquad (11)$$

Currents I_6 and I_7 establish proportional currents in Q25, Q26, and Q27 in a manner

CIRCUIT DESCRIPTION OF THE NE564

similar to the analysis above since the current in Q28 is a constant, or

$$I_o = I_{C28} = I_{E25} + I_{E26} + I_{E27A} + I_{E27B}$$

Gilbert (10) has shown that the D_7-D_8 diode pair will cause identical differential currents to be reflected in both the Q25-Q26 and the Q27A-Q27B differential amplifier pairs. Consequently the constant current of I_o jointly shared by the differential amplifier pairs will divide in each pair with the same x factor imbalance as in Equation 11.

$$I_{E25} + I_{E26} = xI_o \tag{12}$$

$$I_{E25} = I_{E26} = \frac{x}{2} I_o \tag{13}$$

$$I_{E27A} + I_{E27B} = (1 - x)\, I_o \tag{14}$$

$$I_{E27A} = I_{E27B} = (\frac{1-x}{2})\, I_o \tag{15}$$

Now consider placing a capacitor between the collectors of Q25 and Q26 (pins 12 and 13). Oscillation will occur with the capacitor alternately being charged by Q21 and Q23 and constantly discharged by Q25 and Q26. When the Q21 and Q22 pair conducts, Q23 and Q24 will be off causing a negative ramp voltage to appear at pin 13 and a constant voltage at pin 12 as shown in Figure 7. During the next half-cycle, the transistor roles and voltages are reversed. Capacitor discharge is via Q25 and Q26 which act as constant-current sinks with current amplitudes as in Equation 13.

During each half-cycle, the capacitor voltage changes linearily by 2ΔV volts in ΔT seconds where

$$\Delta V = 2R_{20} I_o (\frac{x}{2} + \frac{1-x}{2}) = R_{20} I_o \tag{16}$$

and

$$\Delta T = \frac{C2\Delta V}{I_{E25}}. \tag{17}$$

Combining these two equations with Equation 13 gives a half period of

$$\Delta T = \frac{4C\,R_{20}}{x} \tag{18}$$

Utilizing Equation 11 with the ΔT expression gives the desired VCO frequency expression of

$$f_o = f_o' (1 + \frac{V_{DM}}{RI}) = f_o' \left[\frac{V_{DM}}{2(V_{CM} - 3\,V_{BE})} \right] \tag{19}$$

where f_o' is the VCOs free-running frequency given by

$$f_o' = \frac{1}{16\,R_{20}\,C} \tag{20}$$

Equation 19 shows that the oscillator frequency is a linear function of the differential voltage from the phase comparator. Resistors R_{35} and R_{36} function to insure that an initial current imbalance exists between the Q25 - Q26 transistor pair and the dummy Q27. This imbalance insures that the oscillator is self-starting when power is first applied to the circuit.

The VCO conversion gain is determined as

$$K_o = \frac{\partial f_o}{\partial V_{DM}} = \frac{f_o'}{RI} \quad \text{Hz/volt} \tag{21}$$

which is valid as long as the transistors V_{BE} changes are small with respect to the common-mode voltage. Both f_o and K_o are inversely proportional to R which has a strong positive temperature coefficient. An internal current I_R having an equal and opposite negative temperature coefficient is inserted into the VCO as shown in Figure 6.

Experimental determination of K_o can be found from the data of Figure 8 where K_o is the slope of either line. Numerically these results are for $I_{BIAS} = 0$.

$$K_o = 0.95 \frac{\text{MHz}}{\text{volt}} = 5.9 \times 10^6 \frac{\text{rad}}{\text{volt-sec}} \tag{22}$$

and for $I_{BIAS} = 800\mu A$

$$K_o = 1.7 \frac{\text{MHz}}{\text{volt}} = 10.45 \times 10^6 \frac{\text{rad}}{\text{volt-sec}} \tag{23}$$

It must be noted that the specific values obtained for K_O in the manner above are valid only for the 1.0MHz free-running frequency where the data was taken. However, good estimates for K_O at other free-running frequencies can be obtained by linearly scaling K_O to the desired f_O'. Thus it is sometimes convenient to define a normalized K_O as

$$K_{o(norm)} = \frac{K_o}{f_o'} = 5.9 \frac{\text{rad}}{\text{volt}} (I_{BIAS} = 0)$$

$$= 10.45 \frac{\text{rad}}{\text{volt}} (I_{BIAS} = 800\mu A) \tag{24}$$

The K_O estimate for any bias then can be obtained by multiplying the normalized conversion gain by the desired free-running frequency, or

$$K_o\,(\text{any } f_o') = K_{o(norm)}\, f_o'. \tag{25}$$

The additonal VCO circuitry of Q29 through Q36 functions to produce the TTL and ECL compatible outputs at pins 9 and 11.

VCO OUTPUT FREQUENCY AS A FUNCTION OF INPUT VOLTAGE AND BIAS CURRENT

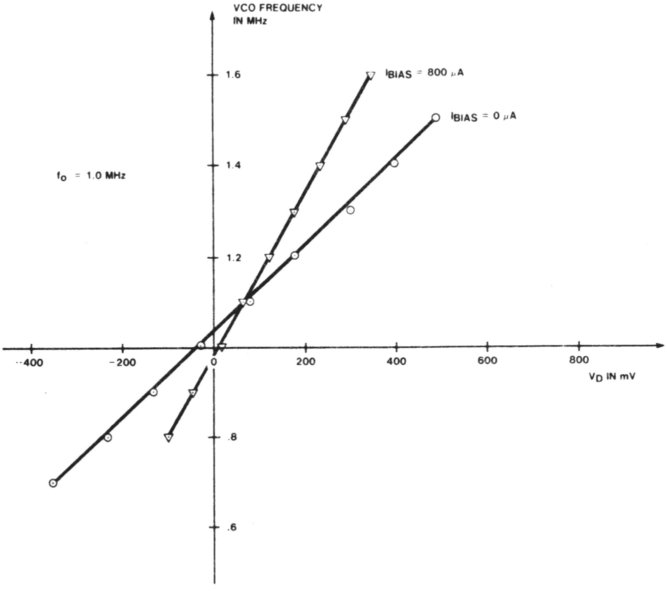


Figure 8

Amplifier

The difference-mode voltage from the phase comparator is extracted and amplified by the amplifier in Figure 1. The single-ended output from this amplifier serves as input signals for both the Schmitt Trigger and a second differential amplifier. Low-pass filtering with a large capacitance at pin 14 produces a stable dc reference level as the second input to the Schmitt Trigger. When the PLL is locked, the voltage at pin 14 is directly proportional to the difference between the input frequency and

POST DETECTION PROCESSOR FOR FSK

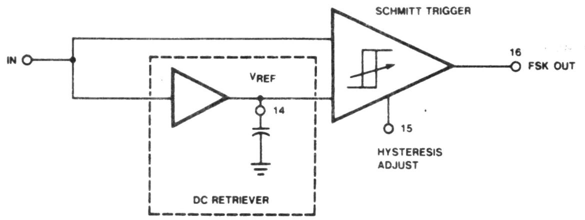
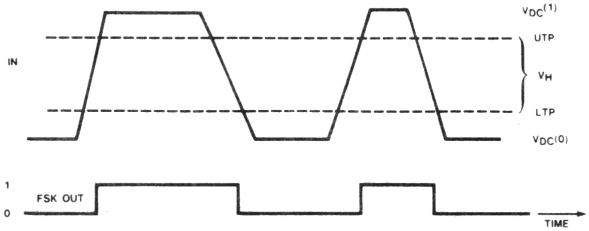


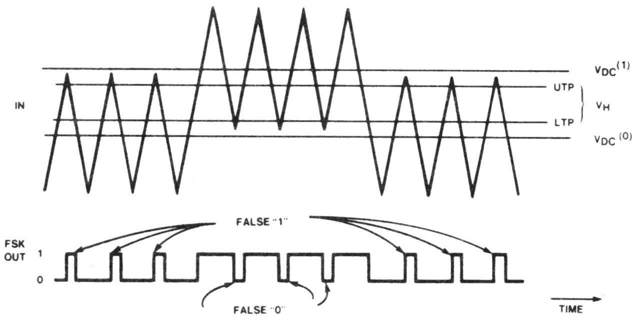
Figure 9

WAVESHAPES FOR FSK DECODING IN THE POST DETECTION PROCESSOR

(A) LOW DATA RATES WITH NEGLIGIBLE CARRIER FEEDTHROUGH



(B) FALSE FSK OUTPUTS DUE TO FEEDTHROUGH AND LOW HYSTERESIS



(C) INCREASED HYSTERESIS RESTORES PROPER FSK OUTPUT IN THE PRESENCE OF FEEDTHROUGH

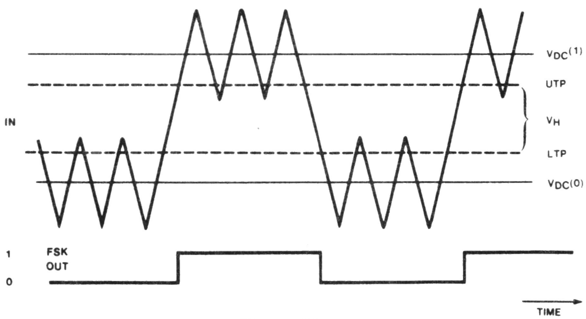


Figure 10

f_o'. Thus pin 14 provides the demodulated output for a FM input signal.

Schmitt Trigger

In FSK applications the pin 14 voltage will assume two different voltage levels corresponding to the mark and space input frequencies. A voltage comparator could be used to sense and convert these two voltage levels to logic compatible levels. However at high data rates, V_{DM} will contain a considerable amount of carrier signal which can be removed by extensive filtering. Normally this complex filtering requires quite a few components, most all of which are external to the monolithic PLL. Also since the control voltage for the comparator depends upon K_O and the deviations of the mark and space frequencies from f_O', the filtering has to be optimized for each different system utilized. However the necessary dc reference level for the comparator is present in the PLL but buried in carrier frequency feedthrough which appears as noise in the system. A Schmitt trigger with variable hysterisis can be used successfully to decode the FSK data without the need for extensive filtering.

Consider the system shown in Figure 9 where the input signal is the single-ended output derived from the amplifier section of the 564. The dc retriever functions to establish a dc reference voltage for the Schmitt trigger. The upper and lower trigger points and adjustable externally around the reference voltage giving the variable hysteresis. For very low data rates, carrier feedthrough will be neglible and the ideal situation depicted in Figure 10 results. Increased data rate produces the carrier feedthrough shown in the (b) figure where false FSK outputs result because the feedthough amplitude exceeds the hysteresis voltage. Having the capability to increase the hysteresis as in (c) produces the desired FSK output in the presence of carrier feedthrough.

Another important factor to be considered is the temperature drift of the f_o' in the VCO. Small changes in f_o' will change the dc level of the input voltage to the Schmitt trigger. This dc voltage shift would produce errors in the FSK output in narrow-band systems where the mark and space deviations in f_{in} are less than the f_o' change with temperature. However this effect can be eliminated if the dc or average value of the amplifier signal is retrieved and used as the reference voltage for the Schmitt trigger. In this manner, variations in the f_o' with temperature do not affect the FSK output.

FREQUENCY SYNTHESIS WITH THE NE564

Frequency multiplication can be achieved with the PLL in two ways:

a Locking to a harmonic of the input signal.
b Insertion of a counter (digital frequency divider) in the loop.

Harmonic locking is simpler and usually can be achieved by setting the VCO free-running frequency to a multiple of the input frequency and allowing the PLL to lock. However, a limitation of this scheme is that the lock range decreases as successively higher and weaker harmonics are used for locking. This limits the practical harmonic locking range to multiples of approximately less than ten. For larger multiples, the second scheme is more desirable.

A block diagram of the second scheme is shown in Figure 1a. Here, the loop is broken between the VCO and the phase comparator and a counter is inserted. In this case, the fundamental of the divided VCO frequency is locked to the input reference frequency so that the VCO is actually running at a multiple of the reference frequency. The amount of multiplication is determined by the counter. An obvious practical application of this multiplication property is the use of the PLL in wide range frequency synthesizers.

In frequency multiplication applications it is important to take into account that the phase comparator is actually a mixer and that its output contains sum and difference frequency components. The difference frequency is dc and is the error voltage which drives the VCO to keep the PLL in lock. The sum frequency components (of which the fundamental is twice the frequency of the input signal) if not well filtered, will induce incidental FM on the VCO output. This occurs because the VCO is running at many times the frequency of the input signal and the sum frequency component which appears on the control voltage to the VCO causes a periodic variation of its frequency about the desired multiple. For frequency multiplication it is generally necessary to filter quite heavily to remove this sum frequency component. The tradeoff, of course, is a reduced capture range and a more underdamped loop transient response.

Producing a large number of frequencies with close spacing requires a counter with a large N for the system of Figure 1(a). Large N values. in turn, require reference frequencies too low to be practical for commercially available crystals. To overcome this difficulty, a second counter (+ M) is inserted as a prescaler as in Figure 1(b) to divide down the reference frequency input. This also gives more programming flexibility since the synthesized output frequencies are functions of both M and N integers, each of which can be changed separately. As an example of fractional frequency synthesis, the two counters can be set to generate an output frequency exactly 16/3 of the input reference frequency. In this case N = 16, M = 3, and the initial f_o' is set to approximately 16/3 times the reference frequency input. The output always will be exactly 16/3 of the input frequency as long as the PLL remains in lock.

PLL frequency synthesizers based upon Figure 1b find wide applications in many types of communications systems that require precisely spaced channels having narrow bandwidths which are centered around relatively high frequencies. For example, Citizens Band (CB) transceiver applications require forty channels corresponding to forty different reference frequencies, each separated by 10kHz bandwidths and centered in the 26 - 27MHz range. Channel 4 uses 27.055MHz; Channel 5 uses 27.015MHz; Channel 6 uses 27.025MHz; and so on. These frequencies could be produced by using forty different crystals - one for each channel. However, this becomes expensive and adds unnecessary complexity to the system. Frequency mixing techniques have been employed to reduce the number of crystals needed to less than one crystal per channel. For example one common mixer design uses 14 crystals for 23 channels. As a general rule, most practical approaches that use numerous crystals and mixers to produce discrete frequencies require more than one crystal for every two channel frequencies produced. As the number of channels grows large, frequency synthesis using PLLs becomes more attractive, especially since usually only one or two crystals are needed. Frequency stability of all channels will be essentially the same as that of the crystal reference frequency. Reduced system complexity, size, weight, and power consumption are key advantages of PLL synthesizers.

FREQUENCY SYNTHESIS USING PLLs

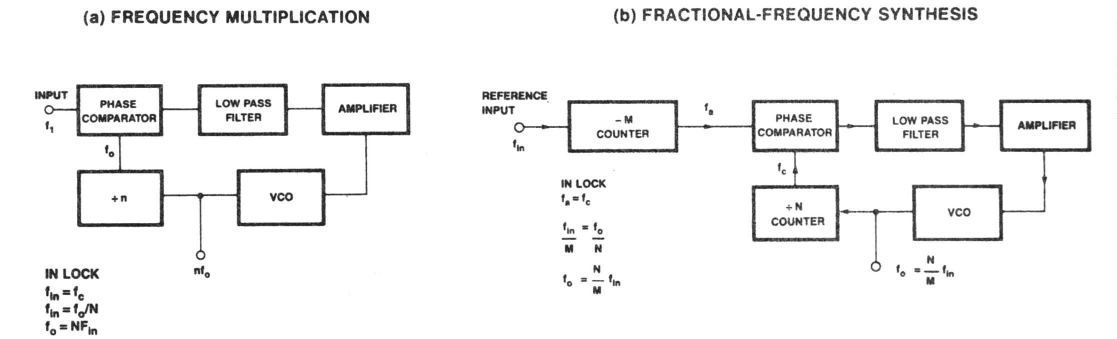
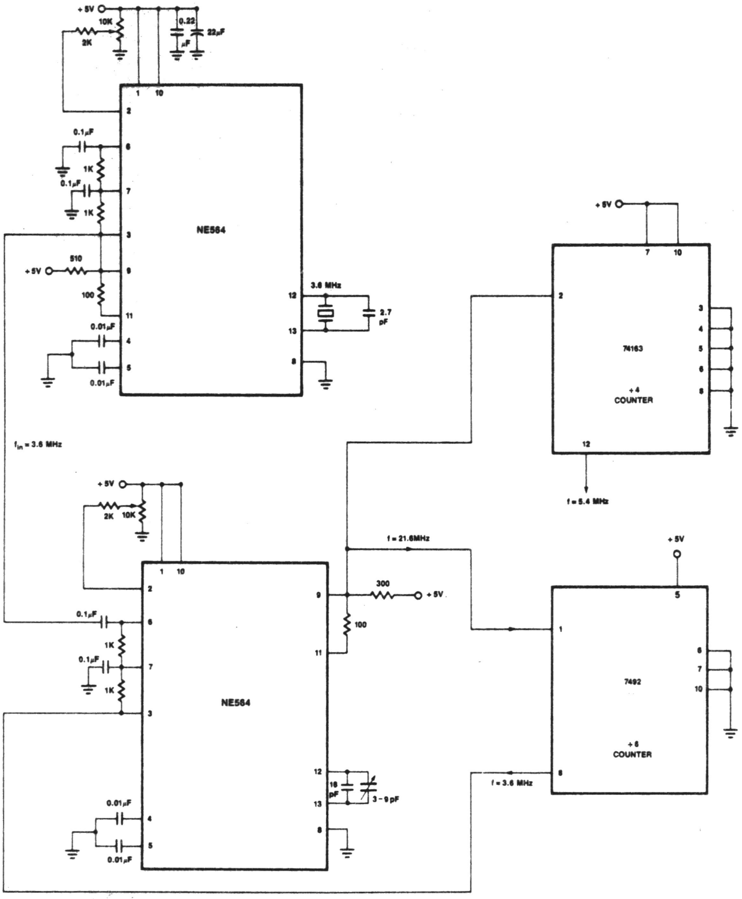


Figure 1

FRACTIONAL FREQUENCY SYSTHESIS WITH THE 564

(b) CIRCUIT IMPLEMENTATION


+5V
10K
2K
0.22 μF
22μF
1
10
2
0.1μF
6
1K
0.1μF
7
1K
3
NE564
510
+5V
9
100
11
0.01μF
4
5
0.01μF
12
3.6 MHz
2.7 pF
13
8
fin = 3.6 MHz
+5V
7
10
2
3
4
5
6
8
74163
÷4 COUNTER
12
f = 5.4 MHz
+5V
2K
10K
f = 21.6MHz
+5V
5
1
10
2
9
300
+5V
100
0.1μF
6
1K
0.1μF
7
1K
11
3
NE564
1
7492
6
7
10
÷6 COUNTER
12
18 pF
3-9pF
13
f = 3.6 MHz
8
0.01μF
4
5
0.01μF
8

(a) BLOCK DIAGRAM ORGANIZATION

(c) WAVESHAPES

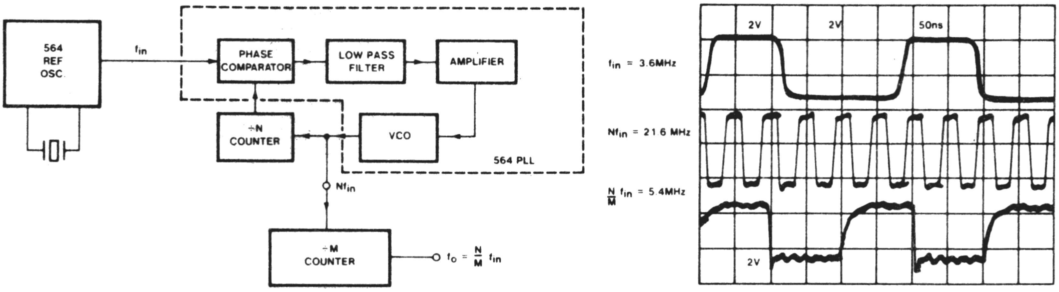

564 REF OSC
fin
PHASE COMPARATOR
LOW PASS FILTER
AMPLIFIER
÷N COUNTER
VCO
564 PLL
Nfin
÷M COUNTER
fo = N/M fin
fin = 3.6MHz
Nfin = 21.6 MHz
N/M fin = 5.4MHz
2V
2V
50ns
2V

Figure 2

Since the function of frequency synthesizers is to generate frequencies and not to linearily decode or demodulate input signals, digital PLLs are more commonly used than analog loops.

Analog PLLs also can be used for frequency synthesis applications. The 564 is particularly well suited for these applications because the loop is open between the VCO output and the phase comparator input. Also the phase comparator input and VCO output are compatible with TTL counters.

NE564 FREQUENCY SYNTHESIS WITH CRYSTAL CONTROL

The system shown in Figure 2 has been used to generate frequencies of 5.4MHz and 21.6MHz from a 3.6MHz crystal-controlled source. This reference signal input is produced by using the crystal as the frequency determining element in the VCO of a second PLL. The thermal stability of all three frequencies will be same as the stability afforded by the crystal. It may be necessary to place a small detuning capacitor in parallel with the crystal to precisely tune the PLL to the crystals resonant frequency and to prevent oscillations at harmonics of the resonant frequency. The value of this tuning capacitance must always be kept considerably less than the value required to produce an f_o' without the crystal present. Otherwise the crystal will lose control and the input reference frequency will be set by the capacitor alone.

A recommendation for improved 564 operation is to utilize a divide-by-N counter in the loop which produces "square" waves for the phase comparator that have as close to a 50% duty cycle as possible. Normally counters with even N values produce square wave outputs perfectly compatible for the phase comparator. Counters for odd N values more commonly produce unsymmetrical outputs that can be less desirable inputs to the phase comparator. An easy modification to "square up" odd divide-by-N counter outputs is to insert a single toggling flip-flop stage between the counter output and the phase comparators input. This produces an effective 2N multiplication of the input frequency within the PLL. The extra factor of two is removed by a second toggle flip-flop whose input is the output from the first flip-flop. This is the same system as was previously shown in Figure 2(a) where the ÷N counter becomes a ÷2N and M=2 for the second counter.

FSK Demodulation with the 564

The 564 PLL is particularly attractive for FSK demodulation since it contains an internal voltage comparator and VCO which have TTL compatible inputs and outputs, and it can operate from a single 5 volt power supply. Demodulated dc voltages associated with the mark and space frequencies are recovered with a single external capacitor in a dc retriever without utilizing extensive filtering networks. An internal comparator, acting as a Schmitt trigger with an adjustable hysteresis, shapes the demodulated voltages into compatible TTL output levels. The high frequency design of the 564 enables it to demodulate FSK at high data rates in excess of 1.0M baud.

Figure 3 shows a high-frequency FSK decoder designed for input frequency deviations of ±1.0MHz centered around a freerunning frequency of 10.8MHz. The value of the timing capacitance required was estimated from Figure 4(a) to be approximately 40pF. A trimmer capacitor was added to fine tune f_o' to 10.8MHz.

Figure 4(b) indicates that the ±1.0MHz frequency deviations will be within the lock range for input signal levels greater than approximately 50mV with zero pin 2 bias current. While strictly this figure is appropriate only for 5MHz, it can be used as a guide for lock range estimates at other f_o' frequencies.

A more thorough analysis confirms these lock range conclusions and serves as a guide for designing other systems. The closed loop gain of the PLL is equal to the systems lock range and is found as the product of K_d and K_o, or

$$2\omega_L = K_v = K_d K_o \tag{1}$$

$$2\omega_L = \left(0.46\,\frac{\text{volt}}{\text{radian}}\right)\left(0.75\,\frac{\text{MHz}}{\text{volt}}\right)\left(2\pi \times 10.8 \times 10^6\,\frac{\text{radian}}{\text{sec}}\right)$$

$$2\omega_L = 3 \times 10^7\,\frac{\text{radian}}{\text{sec}}\ \text{(Lock range total)}$$

Thus pin 2 could be left as an open circuit and the internally set closed-loop gain would be adequate for tracking the mark and space input frequencies. However, to be safe, a bias adjustment as shown in Figure 3 is recommended to allow for K_d and K_o variations from device to device.

Designing for a capture range of approximately 700kHz gives a low-pass filter time constant of

$$\omega_C \simeq \sqrt{\frac{\omega L}{\tau}} \qquad \omega_L = K_V \tag{2}$$

$$(2\pi \times 700 \times 10^3) \simeq \sqrt{\frac{7.38 \times 10^6}{\tau}}$$

$$\tau = 0.775$$

Therefore, choose the low-pass filter capacitor as

$$C = \frac{\tau}{R} = \frac{0.775\mu s}{1.3K} = 596\text{pF} \tag{3}$$

Two 300pF capacitors were selected for the design.

Capacitive coupling was used for the FSK input and is recommended to avoid dc feedthrough. This dc voltage would act as a dc offset to shift f_o' from 10.8MHz. Balanced biasing with the 1.0kΩ resistors from pin 7 to pins 3 and 6 also is recommended to establish symmetrical, quiescent current conditions in the limiter and phase comparator sections of the 564. The 300Ω pull-up resistor for the VCO output was found to give a rise time less than 10ns. This rise time was further reduced by adding the 100Ω resistor between pins 9 and 11. Figure 5 shows an unmodulated 10.8MHz input signal and the VCO output. Note the approximate 90° phase lag of the VCO output.

A 0.1μF dc retriever capacitor (pin 14) has less than 1 ohm impedance at f_o' and represents a good compromise between high baud rates (~100K baud) at f_o' and higher order filtering. If very high baud rates are used, this capacitor could be made smaller with an accompanying increase in the Schmitt trigger hysteresis voltage. The hysteresis was adjusted experimentally via the 10kΩ potentiometer and 2kΩ bias arrangement to give the waveshape shown in Figure 6 for 20K, 500K, 2M baud rates with square wave FSK modulation. Note the magnitude and phase relationships of the phase comparators output voltages with respect to each other and to the FSK output. The high frequency sum components of the input and VCO frequency also are visible as noise on the phase comparators outputs.

The phase comparators outputs exhibit the waveshapes shown in Figure 7 when the FM input is changed from a square wave FSK modulation to a triangular sweep at a 100Hz modulation rate. The amplitude of the triangular sweep was increased from that used with square wave modulation, causing the loop to be driven in and out of lock. The loop is locked during the smooth, linear portions of the phase comparators waveshapes and locked during the remaining portions. Lock and capture frequencies were measured for a pin 2 bias current of 375μA and $f_o' = 1.08$MHz as:

Lock: $f_{L1} = 6.2$MHz $f_{L2} = 16.4$MHz

Capture: $f_{C1} = 9.3$MHz $f_{C2} = 12.2$MHz

When the loop is locked, the phase detectors outputs represent the demodulated FM output. When unlocked, high frequency harmonics are present, increasing in amplitude until lock is achieved.

10.8 MHz FSK DECODER USING THE 564

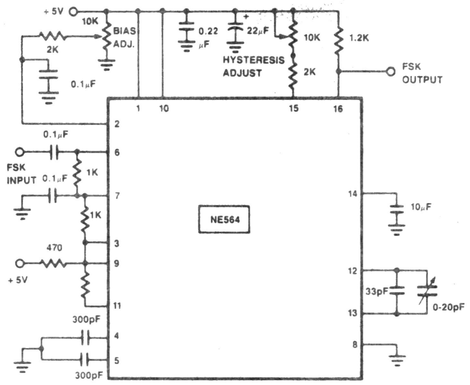
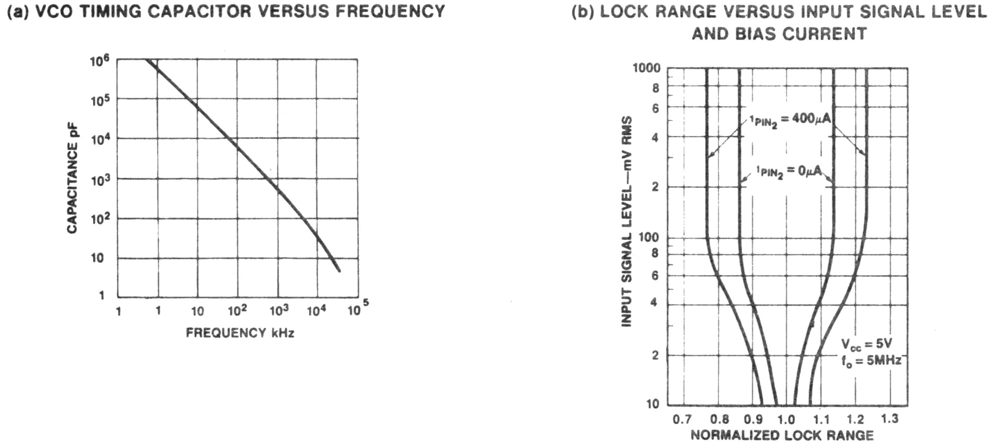

+5V
10K
BIAS ADJ.
2K
0.1μF
0.22 μF
22μF
+
HYSTERESIS ADJUST
10K
2K
1.2K
FSK OUTPUT
1
10
15
16
2
0.1μF
6
FSK INPUT
0.1μF
1K
7
1K
NE564
14
10μF
3
470
9
+5V
12
33pF
0-20pF
13
11
300pF
4
5
300pF
8

Figure 3

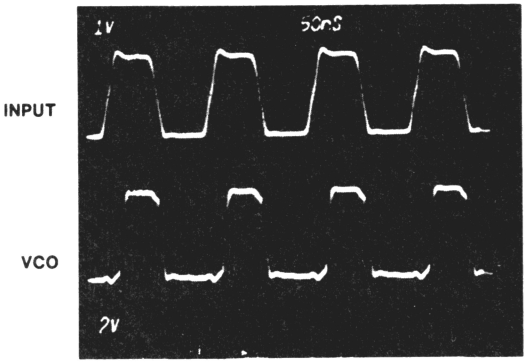
564 CHARACTERISTICS


(a) VCO TIMING CAPACITOR VERSUS FREQUENCY

(b) LOCK RANGE VERSUS INPUT SIGNAL LEVEL AND BIAS CURRENT

Figure 4

PLL INPUT AND VCO OUTPUT FOR PHASE AND FREQUENCY LOCK AT 10.8 MHz



f_L = 1.17 MHz (tracking range about 10.8 MHz)

Figure 5

PHASE COMPARATOR OUTPUTS SHOWING LOCK AND CAPTURE RANGES

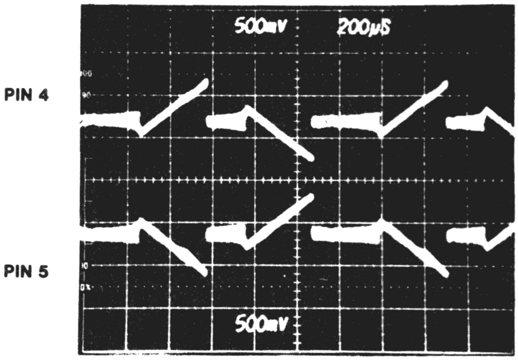
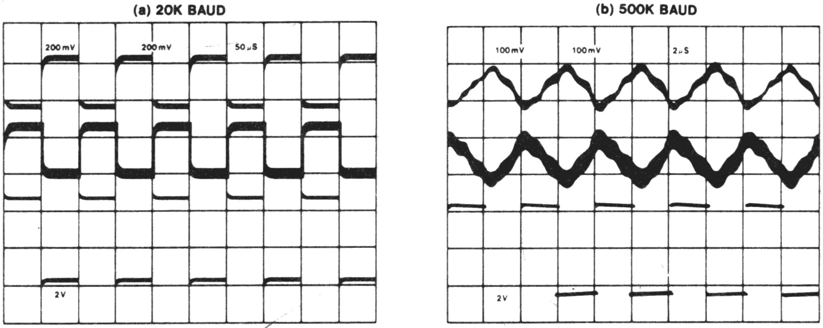


Figure 7

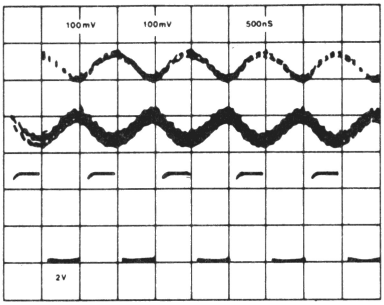
PHASE COMPARATOR (PINS 4 AND 5) AND FSK (PIN 16) OUTPUTS FOR DATA RATES OF



(a) 20K BAUD

(b) 500K BAUD

(c) 2.0M BAUD



NOTE
Top trace-pin 4
Center trace-pin 5
Bottom trace-pin 16

Figure 6

A 6MHZ FSK CONVERTER DESIGN EXAMPLE FOR THE NE564 AN181

Design Example

It is desired to design an FSK converter operating at 6MHz with deviation of ±1%. Supply voltage is 5 volts. Input to the 564 is from a radio receiver with an amplitude of 0.5 $\text{volts}_{\text{rms}}$. Worst case S/N is 10dB. An overall loop damping factor of 0.5 is specified (ζ).

Using the circuit in Figure 1

First the frequency determining capacitor must be established. Using the equation $f_o = \frac{1}{25R_cC_o}$ where R_c is the internal resistance in the VCO oscillator equal to 100 ohms. Given two parameters the third is calculated $f_o = 6\text{MHz}$; therefore

$$C_o = \frac{1}{2\pi \times 100 \times 6 \times 10^6} = 66\text{pF}.$$

A parallel 2–20pF trimmer and a 47pF ±5% fixed mica capacitor is chosen.

Next, signal level versus bias current and lock range is examined.

FSK DECODER USING THE 564

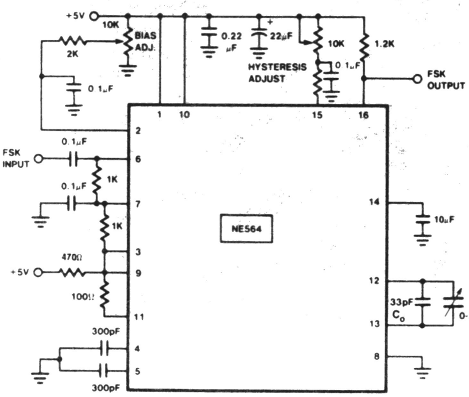


Figure 1

LOCK RANGE vs SIGNAL INPUT

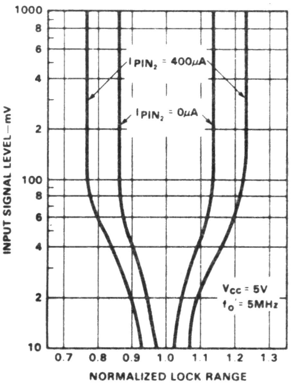


Figure 2

The signal input to the 564 is specified to be 0.5 $\text{volts}_{\text{rms}}$; in the lock range graph, the input level is well within the limiting region of the 564. Thus no external AM limiter circuit is required and a 10dB S/N (3.1:1) min. should provide reliable communication with a narrow deviation of ±1% (±60KHz) and there is no problem with adequate lock range as it pertains to bias current. We are free to use any loop gain necessary. The bias current sinking into pin 2 is set to an initial value of 200μA.

It's now possible to determine the damping factor of the closed loop. First the natural frequency of the loop is calculated from the relationship,

$$\omega_n = \frac{\sqrt{K_OK_D}}{\tau} \qquad (1)$$

where

K_O = VCO conversion gain in $\frac{\text{radians}}{\text{sec} \bullet \text{volt}}$

K_D = Phase detector conversion gain in $\frac{\text{volts}}{\text{radian}}$

τ = Loop filter time constant in seconds

For $f_o = 6\text{MHz}$ and $I_B = 200\mu A$, K_O may be derived from Figure 3a by first constructing an extrapolated transfer line with slope one-quarter of the angle between the existing $I_B = 0$ and $I_B = 800$ plots.

Interpolation gives

$$K_O \cong \frac{(1.48 - 1.25\text{ MHz})}{(0.4 - 0.2\text{ Volt})} = \frac{\Delta f_o}{\Delta V_o};$$

Multiplying ΔF by 2π results in $f \cong 1.45 \times 10^6$ radians/sec at 1MHz and

$$K_O = \frac{1.45 \times 10^6\text{ rad/sec}}{0.2\text{ volts}} = 7.2 \times 10^6 \frac{\text{radians}}{\text{sec} \bullet \text{volt}}$$

Next, using the K_D graph (Figure 3b), ±1 radian (−90° ±57°); i.e., $\Delta\Theta = 1$ radian, results in an output of 0.6 volts/radian.

Therefore, $K_D = \frac{0.6}{1\text{ rad}} = 0.6$ volts/radian at $I_B = 200\mu A$.

The value obtained for K_O is for data taken at 1MHz and must be multiplied by 6 in order to find the correct value.

$$\text{Therefore, } K_O = 6 \times 7.2 \times 10^6 \frac{\text{radians}}{\text{sec} \bullet \text{volt}}$$

$$(6\text{MHz}) = 4.34 \times 10^7 \frac{\text{radians}}{\text{sec} \bullet \text{volt}}$$

$$K_OK_D = K_V = (4.34 \times 10^7)(0.6) = 2.6 \times 10^7$$

(loop gain)

The damping factor specified (0.5) is now used to determine the necessary filter time constant (pins 4, 5).

$$\zeta = \frac{1}{2\tau\frac{\sqrt{K_OK_D}}{\tau}} = \frac{1}{2\sqrt{K_V\tau}} = \frac{\omega_n}{2K_V} \qquad (2)$$

$$\therefore \tau = \frac{1}{(4)(2.6 \times 10^7)(0.5)^2} = 38\text{ns}$$

Note that the filters on pins 4 and 5 operate differentially with the net effect that break frequency is

$$\omega_P = \frac{1}{RC} \text{ (single pole filter } -3\text{dB freq.)}$$

Now solving for ω_n using (1):

$$\omega_n = \left[\frac{(2.6 \times 10^7)}{(3.8 \times 10^{-8})}\right]^{1/2} = 26 \times 10^6 \text{ radians/sec}$$

$f_n = 4.14\text{MHz}$ (natural frequency of the loop and approximate one-sided capture B.W.)

A 6MHZ FSK CONVERTER DESIGN EXAMPLE FOR THE NE564

The value of the loop filter capacitor may be determined by dividing the time constant by the value of the internal resistance 1.3K ohm.

$$C_L = \frac{\tau}{1.3\text{K ohm}} = \frac{3.8 \times 10^{-8}}{1.3 \times 10^{3}}$$

$$= 29\text{pF}$$

This value filter time constant will give a less-than-critically-damped response allowing the fast excursion in VCO frequency necessary to good FSK reception. The tradeoff between response speed and carrier frequency harmonic rejection will have to be considered. A longer time constant gives more carrier rejection but slower response and less damping. (Refer to equation 2.)

The next step is to test the circuit under actual operating conditions with the specified FSK signal. The level on pin 15 (hysteresis adjust) must be set in the vicinity of +1.4 volts in order to attain proper FSK demodulation. Final signal tests may be carried out with noise injected through a resistive summing network at the input (pin 6) to simulate the 10dB S/N.

Note that the loop filter response actually operates on the frequency spectrum above (+) and below (−) the carrier center frequency or center of deviation for a symmetric FM or FSK signal. This may be seen in Figure 4.

VARIATION OF THE PHASE COMPARATOR'S OUTPUT VOLTAGE VERSUS PHASE ERROR AND BIAS CURRENT (K_D)

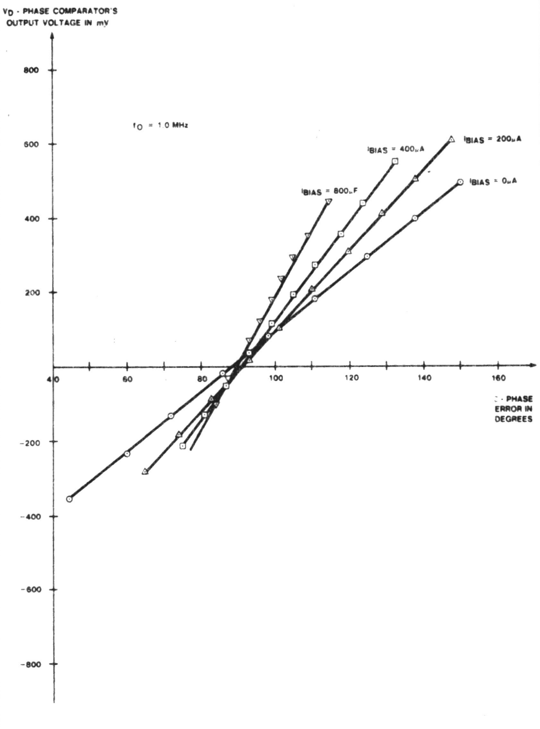


Figure 3b

VCO OUTPUT FREQUENCY AS A FUNCTION OF INPUT VOLTAGE AND BIAS CURRENT (K_O)

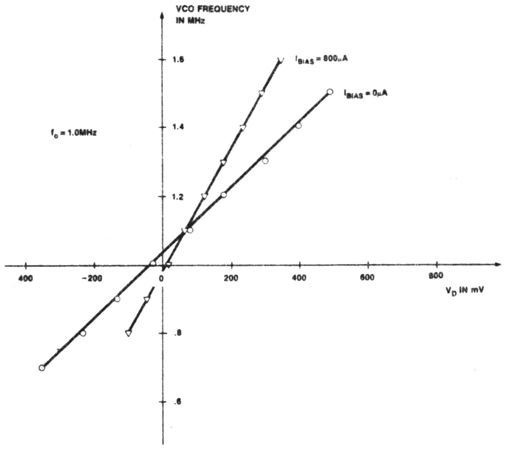


Figure 3a

Bandpass Effect of Loop Filter

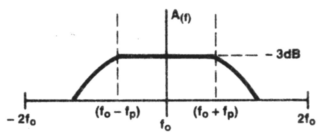


Figure 4

CLOCK REGENERATOR WITH CRYSTAL CONTROLLED PHASE LOCKED VCO

AN182

INTRODUCTION

In order to obtain a local clock signal in Multiplexed Data Transmission systems, a phase and frequency coherent method of signal extraction is required. A Master-Slave system using the quartz crystal as the primary frequency determining element in a phase lock loop VCO is used to reproduce a phase coherent clock from an asynchronous Data Stream.

The NE564, a versatile phase locked loop (PLL) operating at frequencies of 50MHz, has inputs and outputs designed to be TTL compatible. The Signetics NE564 is used to generate the phase locked, crystal-stabilized clock reference signal.

Its particular adaptation, for use with a crystal-controlled VCO instead of the usual R-C control elements, requires a brief review of the principles of the Phase Lock Loop design.

The NE564 Phase Locked Loop is a fully contained system, including limiter, phase detector, VCO, dc amplifiers, dc retriever and output comparator (reference figure 1). For the clock regeneration system to be discussed the portions of the NE564 implemented are the input limiter, phase detector and VCO.

The signal limiter amplifies low level inputs (until saturation is reached, which is typically 60mv p-p for the NE564). The signal limiter output is fed to the phase detector, where the "unknown" input is compared to the "known" VCO frequency of the NE564. The differential error signal that is generated is fed through a dc amplifier and a voltage to current converter. The change in the current generated forces the VCO frequency to vary in its frequency and/or phase relationship, such that a Θ of 90 degrees lagging is obtained (the actual phase relationship may be somewhat less than 90 degrees depending upon the K_dK_o (gain) product of the NE564 at the operating frequency and bias current). The external filtering incorporated at pins 4 and 5 control the dynamic frequency response and loop stability criteria.

The NE564 is a first order system; therefore, the use of single capacitors (at pins 4 and 5) will automatically create a "second order" system. An R-C series filter combination will cause a lead-lag condition that will permit dynamic selectivity, along with closed loop stability.

LOOP GAIN FUNCTIONS

The phase detector conversion gain (K_d) and the VCO conversion gain (K_o) determine, in large part, the lock range, capture range and linearity characteristics of the NE564. These device parameters are both dependent upon bias current and operating frequency. Some typical curves for each of the parameters are shown for the NE564 in figures 2 and 3. The reader should refer to the Signetics Phase Locked Loop Design and Applications Manual for a more in-depth study of these parameters and specific internal circuit configurations.

THE CLOCK REGENERATOR CIRCUIT

The basic building blocks of the clock regenerator circuit are shown in figure 4. The PLL is shown as a frequency multiplier incorporating a divide by "N" in the VCO-phase detector feedback loop (reference to the Signetics PLL Manual will provide greater in-depth explanation of a frequency multiplier). The functions of the ringing circuit and the NE527 high speed comparator will be discussed later.

The wave forms of figure 5 indicate the waveforms transmitted over a T1 line. The bipolar signal transmitted has "no" dc components induced in the transmission line (reference should be made to the effect of normal mode and common effects on signal information). When transmitted over telephone wire pairs, the resultant signal (at the receive end) will have been degraded in both waveshape and signal-to-noise ration. Typical attenuation factors for a T1 line are −30dB per 6000 feet.

In addition, pair-to-pair cross talk can degrade signal-to-noise ratios. The energy transmitted in the bipolar system of signal transfer is centered at 772kHz (generated by the bit format).

At the receiving end the bipolar signal information is converted to a unipolar pulse train after being amplified, filtered and fed through an automatic level control circuit. Some types of PCM systems use the rectified and filtered dc (average) to control the

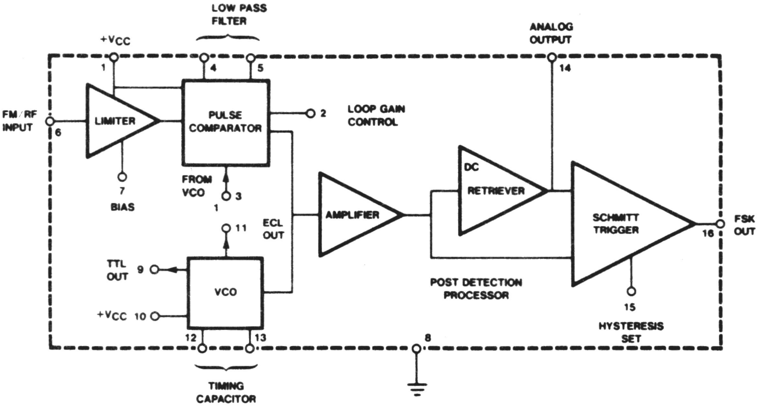


Figure 1

VARIATION OF THE PHASE COMPARATOR'S OUTPUT VOLTAGE VERSUS PHASE ERROR AND BIAS CURRENT

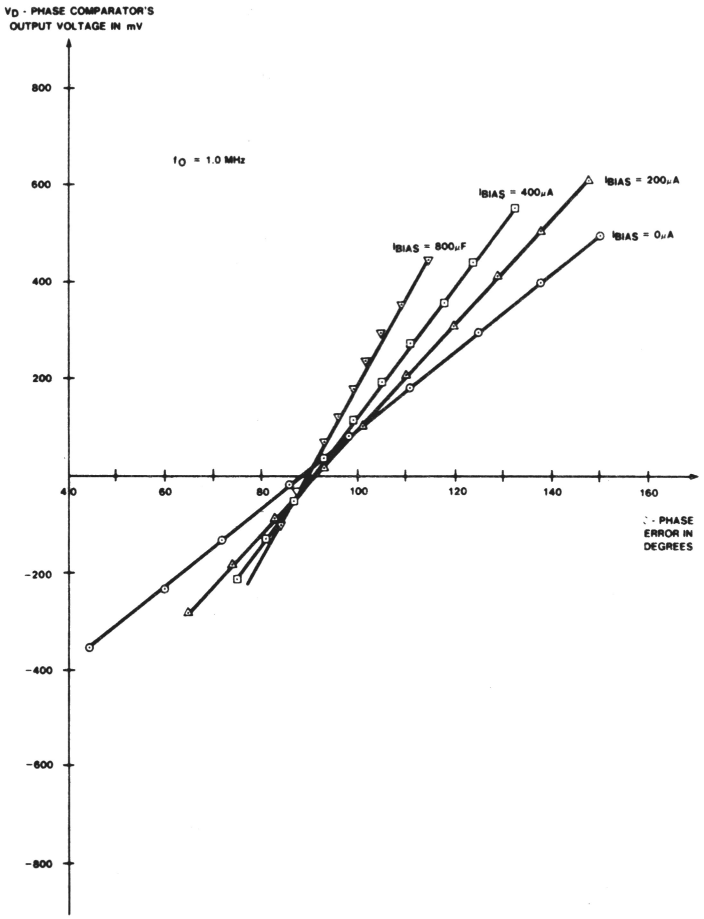


Figure 2

VCO OUTPUT FREQUENCY AS A FUNCTION OF INPUT VOLTAGE AND BIAS CURRENT

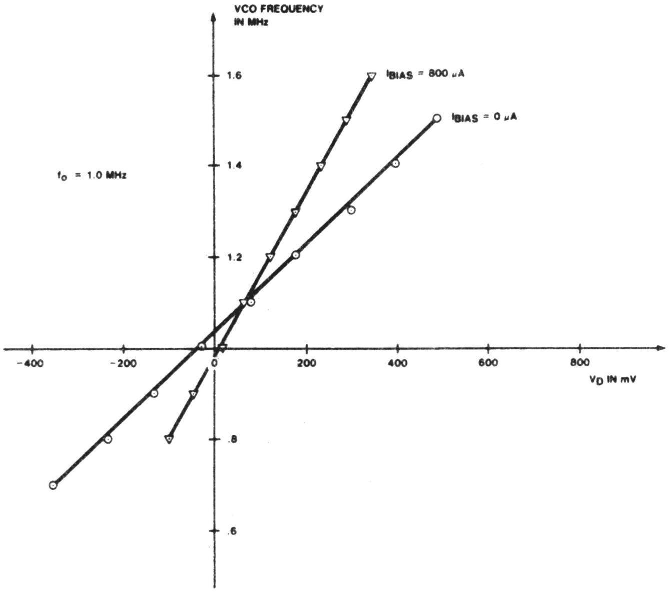


Figure 3

phase of the regenerator clock; however, in newer systems, bipolar signals are preprocessed (or preconditioned) by terminal common equipment resulting in unipolar information.

T1 Data Transmission

The bipolar signal as transmitted on a T1 line appears below with the original binary, converted unipolar and clock waveform (reference figure 5).

The bipolar signal when transmitted over standard wire pairs will be degraded both in wave shape and signal to noise by the time it reaches the signal repeater. This is due to the attenuation factor of the cable which is nearly −30dB for 6000 ft. In addition, pair to pair cross talk degrades signal to noise. The energy in the transmitted bipolar signal is centered at 772kHz due to the particular bit format. Bipolar signals have no dc offset.

At each receiving station the bipolar signal is amplified, filtered and fed through an automatic level control circuit. A full wave rectified signal is then sent to the clock regeneration circuit. This is essentially the format followed by some of the original T1 repeater equipment. The clock regeneration circuit described here could be adapted to this system.

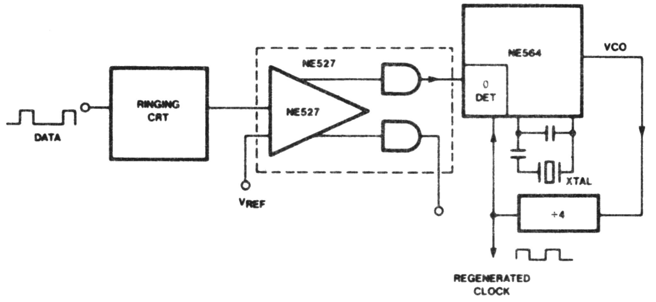


Figure 4

THE T1 SPECTRUM

The bipolar signal is similar to NRZ data in that it does not contain carrier information. In order to give the PLL coherent frequency information sufficient to obtain "capture" and lock, carrier components must be obtained from the data stream. The time duration of the frequency information fed to the PLL is also important in order to obtain ac-

NOTE

*The PLL clock regeneration circuit is fully compatible with NRZ data and needs no signal processing for this format.

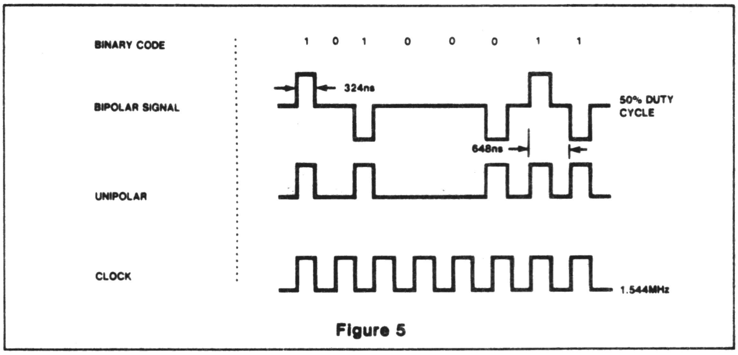


Figure 5

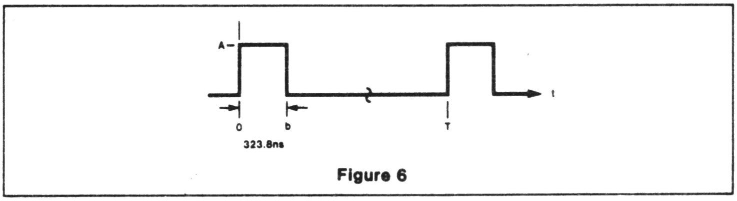


Figure 6

curate and stable information to update the PLL. In order to begin the extraction of frequency information, the positive going portions of the bipolar data signals are used to drive a class "C" transistor tank circuit (reference figure 4) which is sharply tuned to the basic clock frequency (1.544MHz). Each positive half cycle of data then starts a wave train of coherent information which is phase synchronous with each succeeding positive data bit. When the L-C tank is optimally tuned, relatively extended periods without data bits can be tolerated with minimal loss of frequency and phase information. The combination of good short term frequency stability of the high "Q" L-C tank, coupled with the long term stability of the crystal controlled VCO, is the foundation of the NE564 clock regeneration system accuracy.

It must be emphasized that data pulse synchronization of the pre-processing circuit must be frequency coherent with the fundamental period of the time base to be extracted. That is, if the time period of the clock is $\frac{1}{f_c}$ = T, where f_c is the clock frequency, then the spacing between any positive code bit sequence must be n x t (reference figure 6).

Looking at the spectral analysis of the relative energy available to the clock extraction circuitry (with a worst case duty cycle of 1 of 16) will demonstrate the need for enchancing the particular desired frequency component before applying the signal to the Phase Lock Loop. For f_O = 1.544MHz, the period is T = 647.67ns. The pulse or bit width is 323.8ns.

Here the bit duration 323.8ns = b. The Fourier expansion of the discrete spectrum is related by the following equation.

$$F_{(n)} = \frac{(Ab)}{T} \left| \frac{\sin(\frac{n\pi b}{T})}{\frac{n\pi b}{T}} \right| \quad n = 0, 1, 2, \ldots \quad (1)$$

The basic frequency component resulting from various bit spacing factors is defined by the equation

$$f = \frac{1}{T} \quad (2)$$

$$\text{where } f \leq f_O = 1.544\text{MHz}$$

If we consider the special case of a single pulse present out of 16 bipolar or 32NRZ periods, then

$$\begin{aligned} T &= 16 \text{ bipolar bit times} \\ &= 16 \times 647.67\text{ns} = 10.36\mu\text{sec} \\ f &= 96.5\text{kHz} \end{aligned}$$

Accordingly, the spectral lines will be spaced in multiples of 96.5kHz. The spectrum for this particular worst case condition is shown in figure 7 below.

Solving equation 1 for the relative amplitude of the 1.544MHz spectral component with the pulse spacing shown,

$$F_{(16)} \left(\frac{Ab}{T}\right) \left| \frac{\sin(\frac{16\pi b}{T})}{(\frac{16\pi b}{T})} \right|$$

where T = 2nb, n = 16.

$$= \left(\frac{Ab}{(2)(16)b}\right) \frac{\sin(\frac{16\pi b}{32b})}{(\frac{16\pi b}{32b})} = \frac{A}{32}\,\frac{2}{\pi}$$

$$= (.02)A$$

$$= -34\text{dB}$$

It is evident that as the bit spacing increases to the point where f_O is the 16th harmonic of the fundamental, very little f_O energy is available to drive a phase lock regeneration circuit. $F_{(16)}$ is a bad case since it is an even subharmonic of f_O. The PLL will not normally lock to even harmonics; in fact, an error signal is produced which tends to force the VCO out of lock. This fact further stresses the need for preprocessing in the frequency domain. The class "C" pulsed resonant tank significantly multiplies the magnitude of the f_O spectral component and filters out unwanted subharmonics.

The loop error voltage available from the phase detector for phase correction of the VCO is directly related to the product of the incoming coherent spectral energy multiplied in the balanced mixer with the reference signal derived from the VCO. Since the phase error information is integrated in the loop filters, the instantaneous magnitude of the dc error voltage is proportional to the time integral of coherent mixer products. Thus, as the magnitude and time duration of the desired frequency component is in-

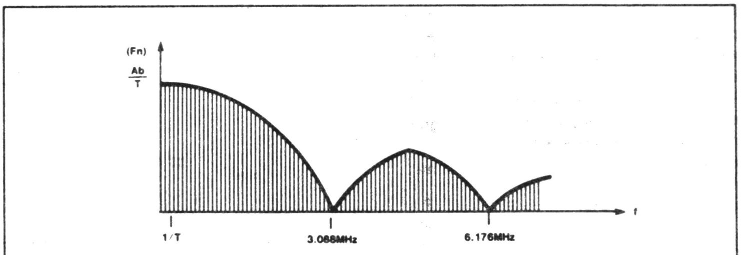


Figure 7

creased in the preprocessing circuitry, the VCO phase accuracy is greatly improved. Capture time is obviously enhanced also.

The signal from the tuned tank is buffered by a FET follower N-channel enhancement mode device (reference figure 12). This provides power gain with virtually no loading on the tank circuit and avoids degrading the "Q". The buffered signal is then fed to a high speed comparator (Signetics NE527) which allows for waveform symmetry adjustment in addition to providing a standard TTL output to drive the NE564 PLL.

In the particular circuit shown in figure 12, the 1.544MHz information is applied to the phase detector input of the NE564 Phase Lock Loop. The VCO, however, is operated at four (4) times this frequency to order to take advantage of economical and readily available crystals. The VCO signal is fed through a divide-by-four counter (74LS73) to provide the Phase Detector reference and final regenerated clock signal. To avoid loading, the clock signal (1.544MHz) is buffered by the 75451 peripheral driver which provides a high speed open collector TTL output. The input signal is AC coupled in order to reduce dc bias errors in the Phase Detector caused by "O" level variations.

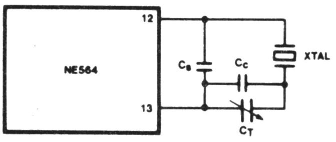


Figure 8

The Crystal

The crystal used was chosen to match the NE564 VCO drive characteristics. It is an "AT" cut oscillator crystal which operates near the anti-resonate or "parallel" mode in this circuit. The crystal may have to be fine tuned, as indicated in figure 8. The pulling characteristic of the crystal is adequate to allow for 0 to 70°C operational drift plus initial and aging accuracy tolerance factors and still retain lock between master and slave station VCXO's. The average lock range at room temperature with one of sixteen data bits present is typically 1000Hz for a 6.176MHz crystal with a capture range greater than 500Hz.

For VCO operation at 6.176MHz, C_s is 22pF, C_C is 18pF, and C_t, a 1-8pF trimmer capacitor (reference figure 8).

NE 564 CRYSTAL CONTROLLED VCO

As shown in figure 8, the crystal is operated with a series capacitor. When properly trimmed, this allows the crystal to operate near the series resonant mode. A crystal manufactured to operate in the series resonant mode will do so only if it sees a pure resistance looking into the oscillator terminals. The circuit below shows an oscillator which looks inductive with the equivalent crystal circuit and trimmer capacitor C_t (reference figure 9).

If L_o is small and the internal gain of the device high over a wide frequency range, L_o may resonate with the C_o of the crystal at a very high frequency. Under certain conditions the circuit may even tend to operate in the 3rd overtone mode unless measures are taken to roll off the circuit gain. This is the purpose of C_s in figure 8. Since the gain of the VCO is a factor in spurious oscillation, the current injected into pin 2 will also have an effect in this respect. (K_o increases with I_2). At higher operating frequencies this parameter may become more critical in attaining stable start ups in the desired frequency mode. Obviously the size of C_s must be smaller than the value needed to cause free running near the desired frequency without the crystal connected.

CRYSTAL SPECIFICATION

Crystals may be manufactured to operate in either the series mode with no external capacitance (purely resistive load) or in the parallel mode with a specified value of load capacitance. The 564 tends to operate at a frequency above the specified value when a series mode crystal is used. For a design frequency of 6.176000MHz and zero load capacitance. Referring to figure 8, for C_s = 10pF and C_T = 10pF the average center frequency for an NE564 sample measured in the lab was 6181.192kHz. For the same C_s but with C_T equal to 60pF, f_o measured 6176.565kHz. A second crystal showed a spread of 6176.600kHz to 6180.855kHz. The effect of the VCO was to pull the xtal to a frequency above its design value. This effect is then nearly tuned out by the external capacitances C_s and C_T. If C_T is sufficiently increased, the crystal will see a purely resistive load and operate at its rated frequency.

A second approach is to specify a crystal which is to operate near the anti-resonate or parallel mode. Normally this is done with a certain value of external load capacitance specified by the customer which matches the existing circuit parameters. The maximum difference between series and parallel resonance for any crystal is 0.5% of f_o (series resonant mode) For f_r = 6.126MHz, 0.5% of f_r = 30kHz. The usual value would be lower than this. ($f_a = f_r\sqrt{1 + \frac{1}{r_o}}$, r_o = electromechanical coupling factor, f_a = parallel resonant frequency). The particular cut of the crystal material determines the drift response over temperature. For oscillator applications the AT cut offers the best overall stability over a wide frequency and temperature range. Final design uses second approach.

For a stability or total tolerance of ± 15ppm over the rated operating range of −20°C to +70°C, a certain manufacturer's crystal actually performed as shown above. (Refer to figure 11.)

Calibration accuracy is the allowable frequency tolerance at the reference temperature, i.e. ± 10ppm @ 25°C.

Third is a **long term drift** spec which determines the customer's maximum allowable drift due to aging effects. An acceptable value in quality crystals is ± 2ppm/year.

Using our reference crystal of 6.176MHz and the above specifications, the crystal limits over a 1 year period would be:

Temperature stability:	± 15ppm x 6.176 = ± 93HZ
Calibration tolerance: @ 25°C	± 10ppm x 6.176 = ± 62Hz
Long term drift:	± 2ppm x 1 x 6.176 = ± 12Hz
Total—	(± 167Hz)

The above figure of ± 167Hz then determines the capture and lock range over which

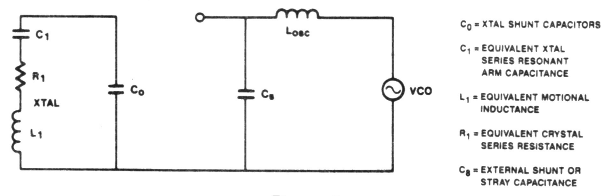

C_1
R_1
XTAL
L_1
C_o
L_{osc}
C_s
VCO
C_0 = XTAL SHUNT CAPACITORS
C_1 = EQUIVALENT XTAL SERIES RESONANT ARM CAPACITANCE
L_1 = EQUIVALENT MOTIONAL INDUCTANCE
R_1 = EQUIVALENT CRYSTAL SERIES RESISTANCE
C_s = EXTERNAL SHUNT OR STRAY CAPACITANCE

Figure 9

BASIC CRYSTAL EQUIVALENT CIRCUIT

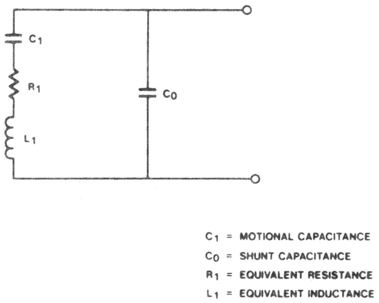

C1
R1
L1
C0
C1 = MOTIONAL CAPACITANCE
C0 = SHUNT CAPACITANCE
R1 = EQUIVALENT RESISTANCE
L1 = EQUIVALENT INDUCTANCE

Figure 10

DESIGN EXAMPLE

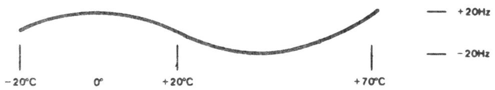


Figure 11

two crystal stabilized VCO's must track under worst case conditions when the exact same crystal specifications are used for master and slave units within an operational system.

CRYSTAL SPECIFICATIONS

'AT' CUT OSCILLATOR TYPE
Fundamental mode operation HC-33 Case (Standard)

Calibration tolerance:
± 10ppm @ 25°C

Temperature stability:
± 15ppm; −15°C to +65°C

Circuit operating condition:
Parallel resonance

Frequency specified: 6.176000MHz

Part designation:
Croven #A330 DEF-32 or equivalent

Set-up Procedure

Referring to figure 12, the following set-up procedure will aid the user in establishing proper circuit operation.

Regulated supply voltage of +5 and −6 volts are required. Current drain on the +5V line is ~ 100mA, and 6mA for the −6V.

With proper voltage applied (1), first check the supply currents to be sure they are in the range indicated above. (2), check the operation of the NE564 VCXO by looking at pin 9 with an oscilloscope (see figure 13). A reasonably symmetric square wave should be present, having a frequency near 6.1MHz. (3), attach a DVM across the 2K resistor which feeds pin 2 of the NE564 and adjust for a reading of 2.00 volts, indicating a 1 milliampere dc current flowing into pin #2.

(The (+) lead of the DVM should be connected to the end of the 2K resistor which ties to the wiper of the 10K pot and the (−) lead to pin 2 of the 564. Reference figure 14).

(4), the exact center frequency is set by adjusting C_t, the crystal trimmer cap, for exactly 6.176000MHz with no signal input (This sets the center frequency of the VCXO to free run in the center of the capture range.).

(5), enable strobe 'A' and 'B' with a +2.7V min. to +5V max. level. Apply a standard 1.544MBS NRZ data signal to the input terminal, terminated in 50 ohms. The amplitude should be +3 to +5V (0 to peak). Set the duty cycle for 1 bit in a 16 bit period. Note the data generator must be driven from a crystal controlled master oscillator also adjusted for a center data rate of 1.544 000MBS. Monitor the buffered output of the ringing circuit with a scope connected to the source of the SD213 (figure 15).

The waveform should appear as in figure 17.

(6), adjust tank trimmer cap C_T for a maximum amplitude and note that the cycle period should be 647 nanoseconds. (7), Now monitor the comparator output signal at pin 7 and adjust R_t for a 50% duty cycle. The same signal will appear at pin 5 of the NE527 except it will be inverted. The signal on pin 7 of the NE527 and pin 6 of the NE564 should appear as shown in figure 19. Now attach one lead of a dual trace scope to pin 7 of the NE527 and the other to pin 3 of the NE564 as shown (figure 16).

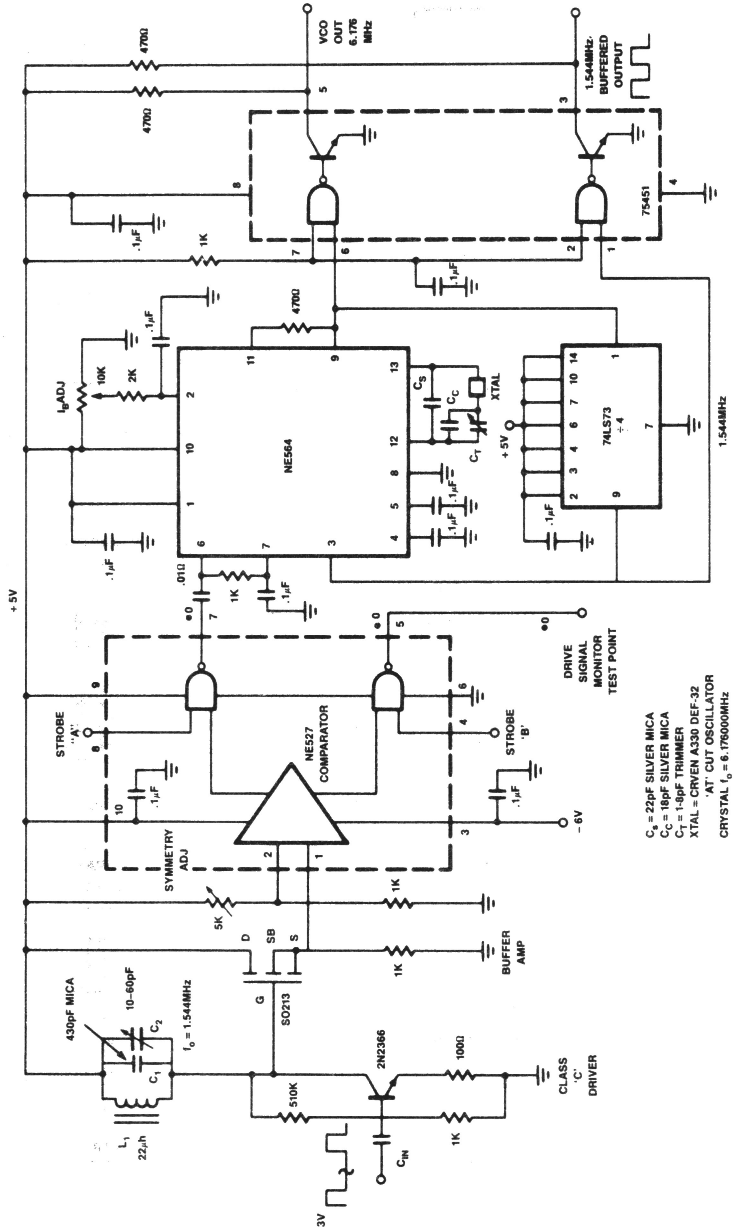
The two signals should be in phase lock with an approximate 90° differential as shown in figure 20 (data signal applied to input @ 1.544MBS). If lock does not occur, a slight trimming of the crystal trimmer C_T should correct for slight differences in master to slave crystal tolerance. It is recommended that master and slave crystals be of the exact same design and specification to insure optimal tracking over time and temperature. A recommended manufacturer and part number appears at the end of this application note for your convenience.

Once lock is attained, move one lead of the dual trace scope to the buffered output of the 75451 pin 3, leaving the other scope probe on pin 6 of the NE564. The phase locked waveform should appear as in figure 25. If a data word generator is being used, you may check overall operation for various bit patterns by synchronizing the scope trigger on the "end of word" pulse, then observe the phase error effect as different combinations are fed in.

PHASE JITTER

When operating with real time A-D data transmission, the PLL loop filters must be optimized to minimize regenerated clock jitter. A good grade of mylar capacitor is recommended as connected to pins 4 and 5 of the NE564. A simple pair of shunt connected loop filter caps of 0.33 µF to 0.76µF was found to be adequate.

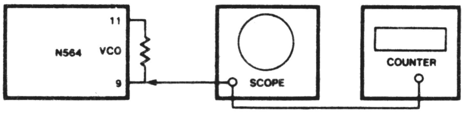
DATA TRANSMISSION SYSTEM CLOCK REGENERATOR


VCO OUT 6.176 MHz
1.544MHz BUFFERED OUTPUT
470Ω
470Ω
75451
.1µF
1K
470Ω
IBADJ
10K
2K
NE564
CS
CC
XTAL
CT
+5V
74LS73 ÷ 4
1.544MHz
+5V
.01Ω
1K
.1µF
STROBE "A"
STROBE 'B'
NE527 COMPARATOR
SYMMETRY ADJ
DRIVE SIGNAL MONITOR TEST POINT
−6V
5K
1K
D
SB
S
G
SO213
BUFFER AMP
430pF MICA
10-60pF
C1
C2
fo = 1.544MHz
L1 22µh
2N2366
510K
100Ω
1K
CIN
CLASS 'C' DRIVER
3V

CS = 22pF SILVER MICA
CC = 18pF SILVER MICA
CT = 1-8pF TRIMMER
XTAL = CRVEN A330 DEF-32
'AT' CUT OSCILLATOR
CRYSTAL fo = 6.176000MHz

Figure 12

CHECK VCO FREE RUNNING FREQUENCY AND OUTPUT WAVESHAPE


11
N564
VCO
9
SCOPE
COUNTER

CHECK VCO FREE RUNNING FREQUENCY AND OUTPUT WAVESHAPE.

Figure 13

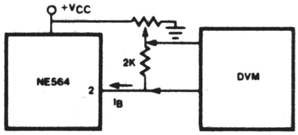

+VCC
NE564
2K
2
IB
DVM

Figure 14

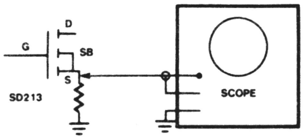

D
G
SB
S
SD213
SCOPE

Figure 15

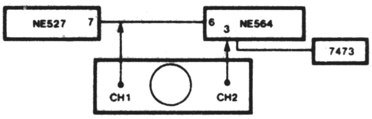

NE527
7
6
3
NE564
7473
CH1
CH2

Figure 16

RINGING CIRCUIT RESPONSE (1 DATA PULSE IN 16)

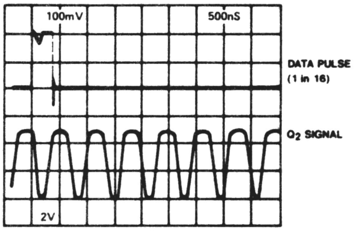


Figure 17

RINGING CIRCUIT RESPONSE (4 DATA PULSES IN 16)

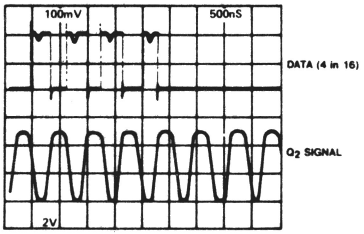


Figure 18

RINGING CIRCUIT TO SQUARE WAVE CONVERSION

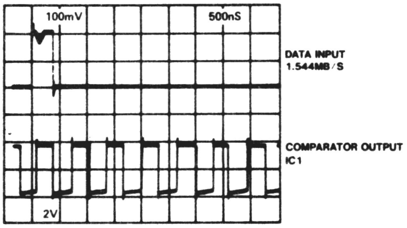


Figure 19

PHASE COMPARATOR SIGNALS (IN LOCK)

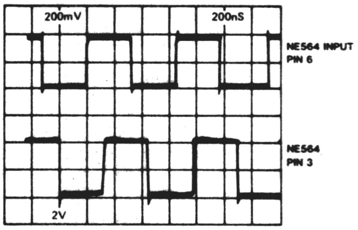


Figure 20

REGENERATED CLOCK SIGNALS

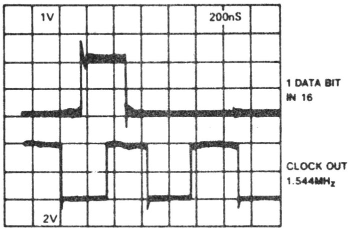


Figure 21

REGENERATED CLOCK SIGNALS

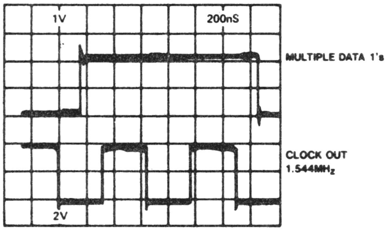


Figure 22

**REGENERATED CLOCK SIGNALS
RELATIVE TO NE564 VCO SIGNAL**

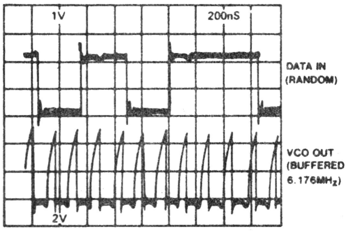


Figure 23

**REGENERATED CLOCK SIGNAL
RELATIVE TO NE564 VCO SIGNAL**

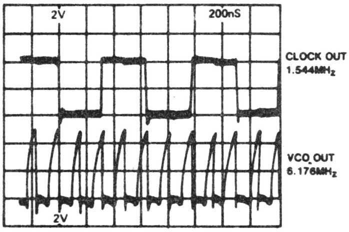


Figure 24

**REGENERATED CLOCK SIGNAL
RELATIVE TO RANDOM NRZ DATA SIGNAL**

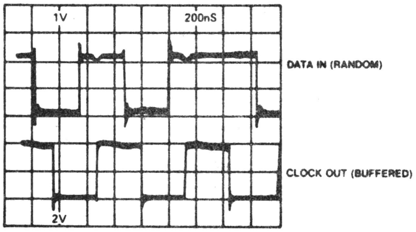


Figure 25

References

1. "Fourier Analysis" by Hwei P. Hsu. Simon & Schuster Tech Outlines
2. "Pulse and Digital Circuits" by Millman and Taub McGraw Hill
3. "Phaselock Techniques" by Floyd M. Gardner Wiley, 1966

CIRCUIT DESCRIPTION OF THE NE565 PLL

The 565 is a general purpose PLL designed to operate at frequencies below 1MHz. The loop is broken between the VCO and phase comparator to allow the insertion of a counter for frequency multiplication applications. With the 565, it is also possible to break the loop between the output of the phase comparator and the control terminal of the VCO to allow additional stages of gain or filtering. This is described later in this section.

The VCO is made up of a precision current source and a non-saturating Schmitt trigger. In operation, the current source alternately charges and discharges an external timing capacitor between two switching levels of the Schmitt trigger, which in turn controls the direction of current generated by the current source.

A simplified diagam of the VCO is shown in Figure 1. I_1 is the charging current created by the application of the control voltage V_C. In the initial state, Q3 is off and the current I_1 charges capacitor C_1 through the diode D_2. When the voltage on C_1 reaches the upper triggering threshold, the Schmitt trigger changes state and activates the transistor Q3. This provides a current sink and essentially grounds the emitters of Q1 and Q2. The charging current I_1 now flows through D_1. Q1 and Q3 to ground. Since the base-emitter voltage of Q2 is the same as that of Q1, an equal current flows through Q2. This discharges the capacitor C_1 until the lower triggering threshold is reached at which point the cycle repeats itself. Because the capacitor C_1 is charged and discharged with the constant current I_1, the VCO produces a triangle wave form as well as the square wave output of the Schmitt trigger.

The complete circuit for the 565 is shown in Figure 2. Transistors Q1-Q7 and diodes D_1-D_3 form the precision current source. The base of Q1 is the control voltage input to the VCO. This voltage is transferred to pin 8 where it is applied across the external resistor R_1. This develops a current through R_1 which enters pin 8 and becomes the charging current for the VCO. With the exception of the negligible Q1 base current, all the current that enters pin 8, appears at the anodes of diodes D_2 and D_3. When Q8 (controlled by the Schmitt trigger) is on, D_3 is reverse biased and all the current flows through D_2 to the duplicating current source Q5-Q7, R_2-R_3 and appears as the capacitor discharge current at the collector of Q5. When Q8 is off, the duplicating current source Q5-Q7, R_2-R_3 floats and the charging current passes through D_3 to charge C_1.

The Schmitt trigger (Q11, Q12) is driven from the capacitor triangle wave form by the emitter follower Q9. Diodes D_6-D_9 prevent saturation of Q11 and Q12, enhancing the switching speed. The Schmitt trigger output is buffered by emitter follower Q13 and is brought out to pin 4, and is also connected back to the current source by the differential amplifier (Q14-Q16).

When operated from dual symmetrical supplies, the square wave on pin 4 will swing between a low level of slightly (0.2V) below ground to a high level of one diode voltage drop (0.7V) below the positive supply. The triangle wave form on pin 9 is approximately centered between the positive and negative supplies and has an amplitude of 2V with supply voltages of ± 5V. The amplitude of the triangle waveform is directly proportional to the supply voltages.

The phase comparator is again of the doubly-balanced modulator type. Transistors Q20 and Q24 form the signal input stage, and must be biased externally. If dual symmetrical supplies are used, it is simplest to bias Q20 and Q24 through external resistors to ground. The switching stage Q18, Q19, Q22 and Q23 is driven from the Schmitt trigger via pin 5 and D_{11}. Diodes D_{12} and D_{13} limit the phase comparator output, and differential amplifier Q26 and Q27 provides increased loop gain.

The loop low pass filter is formed with an external capacitor (connected to pin 7) and the collector resistance R_{24} (typically 3.6KΩ). The voltage on pin 7 becomes the error voltage which is then connected back to the control voltage terminal of the VCO (base of Q1). Pin 6 is connected to a tap on the bias resistor string and provides a reference voltage which is nominally equal to the output voltage on pin 7. This allows differential stages to be both biased and driven by connecting them to pins 6 and 7.

The free-running center frequency of the 565 is adjusted by means of R_1 and C_1 and is given approximately by

$$f_o' \simeq \frac{1.2}{4R_1C_1} \tag{1}$$

When the phase comparator is in the limiting mode ($V_{in} \geq 200mV$ p-p), the lock range can be calculated from the expression:

$$2\omega_L = 2K_oK_dA\Theta_d \tag{2}$$

where K_o is the VCO conversion gain, K_d is the phase comparators conversion gain, A is the amplifier gain, and Θ_d is the maximum phase error over which the loop can remain in lock. Specific values for the terms of Equation 2 for the 565 are

$$K_d = \frac{1.4}{\pi} \text{ volts/radian} \tag{3}$$

$$A = 1.4 \tag{4}$$

$$\Theta_d = \frac{\pi}{2} \text{ radians} \tag{5}$$

$$K_o = \frac{50\, f_o'}{V_{CC}} \frac{\text{radians}}{\text{Volt-sec}} \tag{6}$$

where V_{CC} is the total supply voltage applied to the circuit.

SIMPLIFIED DIAGRAM OF 565 VCO

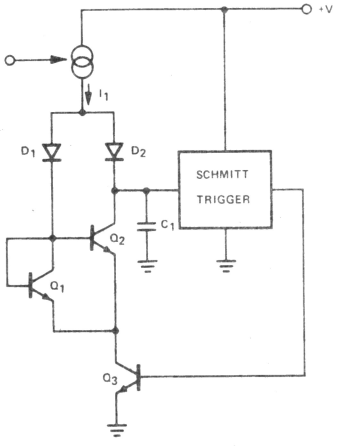


Figure 1

CIRCUIT DESCRIPTION OF THE NE565 PLL

CIRCUIT DIAGRAM OF 565

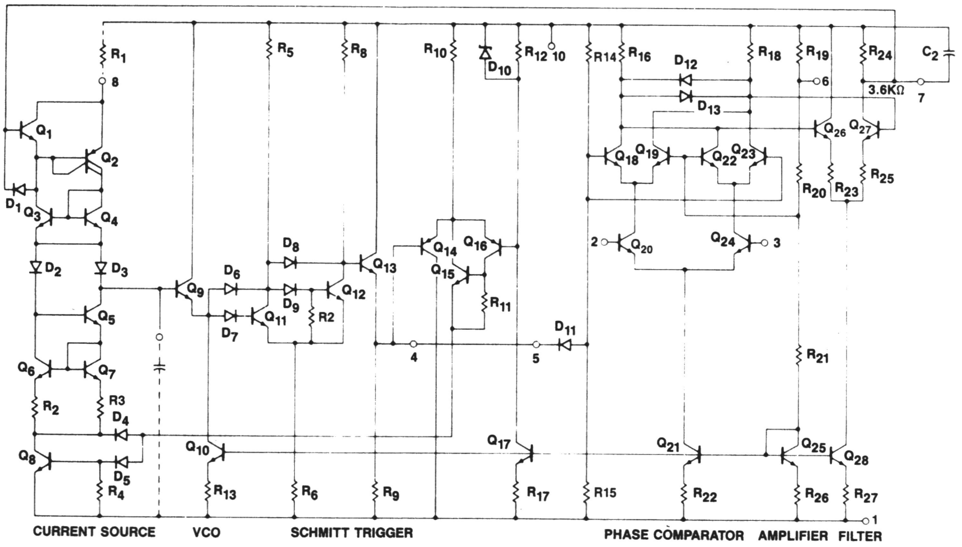


Figure 2

The tracking range for the 565 then becomes:

$$f_L \simeq \pm \frac{\omega_L}{2\pi} \simeq \pm \frac{8f_o}{V_{CC}} \text{ Hz.} \qquad (7)$$

to each side of the free-running frequency, or a total lock range of:

$$2f_L \simeq \frac{16f_o}{V_{CC}} \text{ Hz} \qquad (8)$$

The capture range, over which the loop can acquire lock with the input signal is given approximately by:

$$2\omega_C \simeq 2\sqrt{\frac{\omega_L}{\tau}} \qquad (9)$$

where ω_L is the one-sided tracking range

$$\omega_L = 2\pi f_L \qquad (10)$$

and τ is the time constant of the loop filter

$$\tau = RC_2 \qquad (11)$$

The lock-in range can be written as:

$$f_C \simeq \pm\frac{1}{2\pi}\sqrt{\frac{2\pi f_L}{\tau}} = \pm\frac{1}{2\pi}\sqrt{\frac{32\pi f_o'}{V_{CC}}} \qquad (12)$$

to each side of the free-running frequency or a total capture range of:

$$f_C \simeq \frac{1}{\pi}\sqrt{\frac{32\pi f_o'}{\tau V_{CC}}} \qquad (13)$$

This approximation works well for narrow capture ranges ($f_C = 1/3f_L$ but becomes too large as the limiting case is approached ($f_c = f_L$).

When it is desired to operate the 565 out of its limiting mode ($V_{in} < 200$mV p-p or 32mV rms). K_d can be estimated from the graph in Figure 3 for the specfic input voltage anticipated. The previous calculations for the lock and capture ranges remain valid with the new value of K_d from the graph being used to replace the K_dA product in Equation 2. In Figure 3, the dc amplifier gain A has been included in the K_d value.

For applications where both a narrow lock range and a large output voltage swing are required, it is necessary to inject a constant current into pin 8 and increase the value of R_1. One scheme for this is shown in Figure 4. The basis for this scheme is the fact that the output voltage controls only the current thought R_1 while the current through Q1 remains constant. Thus, if most of the charging current is due to Q1, the total current can be varied only a small amount due to the small change in current through R_1. Consequently, the VCO can track the input signal over a small frequency range yet the output voltage of the loop (control voltage of the VCO) will swing its maximum value.

Diode D_1 is a Zener diode, used to allow a larger voltage drop across R_A than would otherwise be available. D_4 is a diode which should be matched to the emitter-base junction of Q1 for temperature stability. In addition, D_1 and D_2 should have the same breakdown voltages and D_3 and D_4 should be similar so that the voltage seen across R_B and R_C is the same as that seen across pins 10 and 1 of the phase locked loop. This causes the frequency of the loop to be insensitive to power supply variations. The free-running frequency can be found by:

$$f_o' \simeq \frac{2R_B}{(R_B + R_C)\, R_A C_1} + \frac{1}{4R_1C_1} \text{ Hz} \qquad (14)$$

and the total range is given by:

$$2f_L \simeq \frac{22.4V_D(R_B+R_C)R_Af_o'}{(|V_1|+|V_2|-V_Z-V_D)[8R_BR_1+R_A(R_B+R_C)]}\text{Hz} \qquad (15)$$

where V_D is the forward biased diode voltage ($\simeq$0.7V), V_Z is the zener diode breakdown voltage, V_1 is the positive supply voltage, and V_2 is the negative supply voltage.

CIRCUIT DESCRIPTION OF THE NE565 PLL

PHASE COMPARATOR'S CONVERSION GAIN, K_D, FOR THE 565 AS A FUNCTION OF INPUT SIGNAL AMPLITUDE

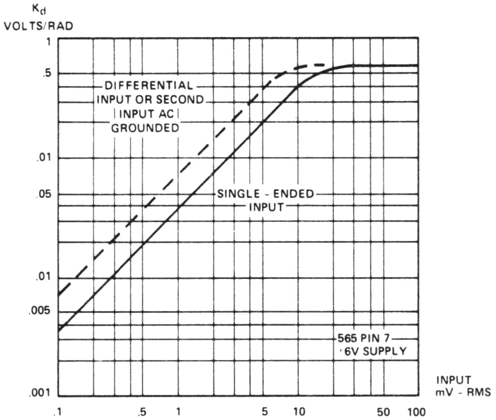


Figure 3

NARROW BANDWIDTH FM DEMODULATOR USING THE 565

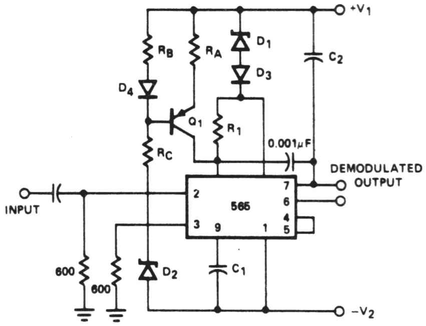


Figure 4

When the output excursion at pin 7 need be only a volt or so, diodes D_1, D_2 and D_3 may be replaced by short circuits.

The value of R_1 can be selected to give a prescribed output voltage for a given frequency deviation.

$$R_1 = \frac{R_A(R_B+R_C)\, f_o'}{R_B(|V_1|+|V_2|-0.7)\,\Delta f} \qquad (16)$$

where Δf is the desired frequency deviation per volt of output.

In most instances, R_B and R_A are chosen to be equal so that the voltage drop across them is about 200mV. For best temperature stability, diode D_1 should be a base-collector shorted transistor of the same type as Q1.

When the 565 is connected normally, feedback to the VCO from the phase comparator is internal. That is, an amplifier makes the pin 8 voltage track the pin 7 (phase comparator output) voltage. Since the capacitor C_1 charge current is determined by the current through resistance R_1, the frequency is a function of the voltage at pin 8. It is possible, however, to bypass and swamp the internal loop amplifier so that the current into pin 8 is no longer a function of the pin 8 voltage but only of the pin 7 voltage. This makes a greater charge-discharge current variation possible, allowing a greater lock range. Figure 5 shows such a circuit in which the µA741 operational amplifier is set for a differential gain of 5, feeding current to pin 8 through the 33KΩ resistor (simulating a current source). Not only is the tracking range greatly expanded, but the output voltage as a function of frequency is five times greater than normal. In setting up such a circuit, the designer should keep in mind that for best frequency stability, the charge-discharge current should be in the range of 50 to 1500µA which also specifies the pin 8 input current range, showing that a ratio of upper to lower lock extremes of about 30 can be achieved.

Many times it would be advantageous to be able to break the feedback connection between the output (pin 7) and the control voltage terminal (Q1) of the VCO. This can be easily done once it is seen that it is the *current* into pin 8 which controls the VCO freqency. Replacing the external resistor R_1 with a current source, such as the Figure 6, effectively breaks the internal voltage feedback connection. The current flowing into pin 8 is now independent of the voltage on pin 8. The output voltage (on pin 7) can now be amplified or filtered and used to drive the current source by a scheme such as that shown in Figure 6. This scheme allows the addition of enough gain for the loop to stay in lock over a 100:1 frequency range, or conversely, to stay in lock with a precise phase difference (between input and VCO signals) which is almost independent of frequency variation. Adjustment of the voltage to the non-inverting input of the op amp, together with a large enough loop gain allows the phase difference to be set at a constant value between 0° and 180°. In addition, it is now possible to do special filtering to improve the performance in certain applications. For instance, in frequency multiplication applications it may be desirable to include a notch filter tuned to the sum frequency component to minimize incidental FM without excessive reduction of capture range.

CIRCUIT DESCRIPTION OF THE NE565 PLL

EXPANDED LOCK RANGE CONFIGURATION FOR THE 565

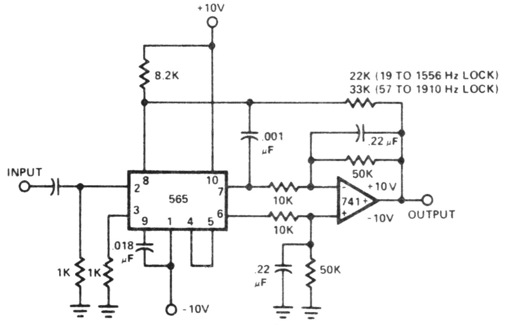

+10V
8.2K
22K (19 TO 1556 Hz LOCK)
33K (57 TO 1910 Hz LOCK)
.001 μF
.22 μF
50K
INPUT
2
8
10
7
565
3
9
1
4
5
6
10K
10K
741
+10V
-10V
OUTPUT
.018 μF
1K
1K
-10V
.22 μF
50K

Figure 5

INCREASED LOOP GAIN AND LOCK RANGE FOR THE 565

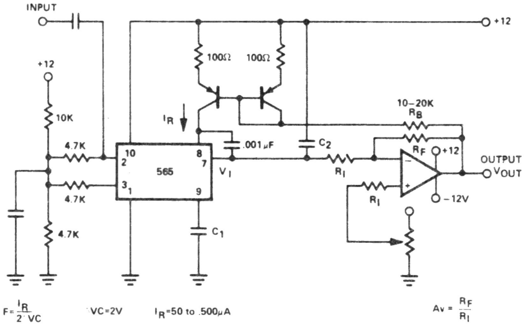

INPUT
+12
+12
100Ω
100Ω
10K
I_R
10–20K
R_B
4.7K
10
2
8
7
565
.001 μF
C_2
R_F
+12
OUTPUT
V_{OUT}
V_I
R_I
3
1
9
4.7K
R_I
-12V
4.7K
C_1
$F = \frac{I_R}{2\ VC}$
VC=2V
I_R=50 to 500μA
$A_V = \frac{R_F}{R_I}$

Figure 6

TYPICAL APPLICATIONS WITH NE565 AN184

FSK DEMODULATION

FSK refers to data transmission by means of a carrier which is shifted between two preset frequencies. This frequency shift is usually accomplished by driving a VCO with the binary data signal so that the two resulting frequencies correspond to the "0" and "1" states (commonly called space and mark) of the binary data signal.

FSK Demodulation with the 565

A simple scheme using the 565 to receive FSK signals of 1070Hz and 1270Hz is shown in Figure 1. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output (pin 7).

The loop filter capacitor C_2 is chosen to set the proper overshoot on the output and a three-stage RC ladder filter is used to remove the sum frequency components. The band edge of the ladder filter is chosen to be approximately half-way between the maximum keying rate (300 baud or bits per second, or 150Hz). The free-running frequency should be adjusted (with R_1) so that the dc voltage level at the output is the same as that at pin 6 of the loop. The output signal can now be made logic compatible by connecting a voltage comparator between the output and pin 6.

The input connection is typical for cases where a dc voltage is present at the source and, therefore, a direct connection is not desirable. Both input terminals are returned to ground with identical resistors (in this case, the values are chosen to achieve a 600Ω input impedance).

A more sophisticated approach primarily useful for narrow frequency deviations is shown in Figure 2. Here, a constant current is injected into pin 8 by means of transistor Q1. This has the effect of decreasing the lock range and increasing the output voltage sensitivity to the input frequency shift. The basis for this scheme is the fact that the output voltage (control voltage for the VCO) controls only the current through R_1, while the current through Q1 remains constant. Thus, if most of the capacitor charging current is due to Q1, the current variation due to R_1 will be a small percentage of the total charging current and, consequently, the total frequency deviation of the VCO will be limited to a small percentage of the center frequency. A 0.25μF loop filter capacitor gives approximately 30% overshoot on the output pulse, as seen in the accompanying photographs. Figure 3 shows the output of the μA710 comparator and the output of the 565 phase locked loop.

FSK DECODER USING THE 565

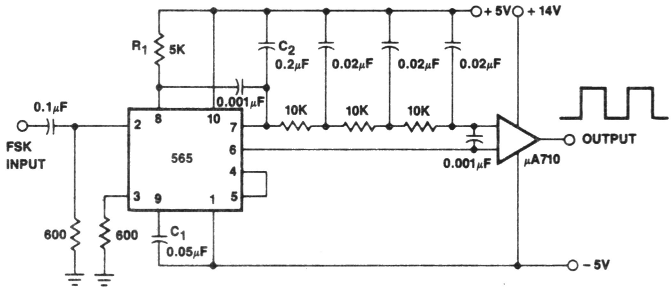


Figure 1

FSK DECODER WITH EXPANDED 565 OUTPUT VOLTAGE RANGE

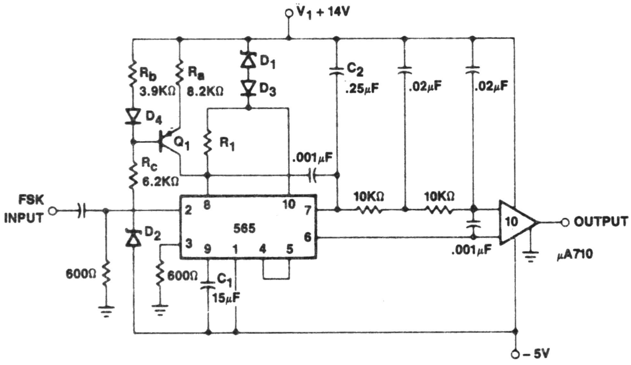
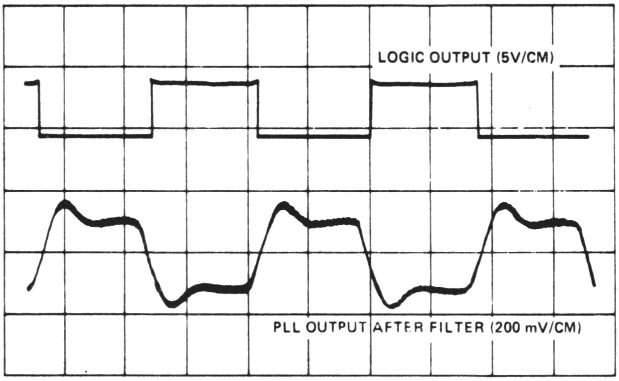
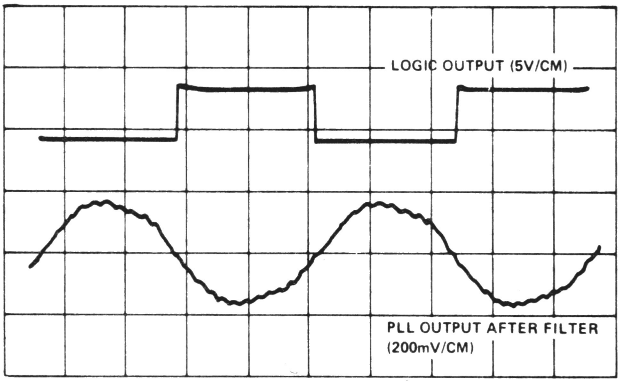


Figure 2

(a) 100 BAUD



(b) 200 BAUD



(c) 300 BAUD

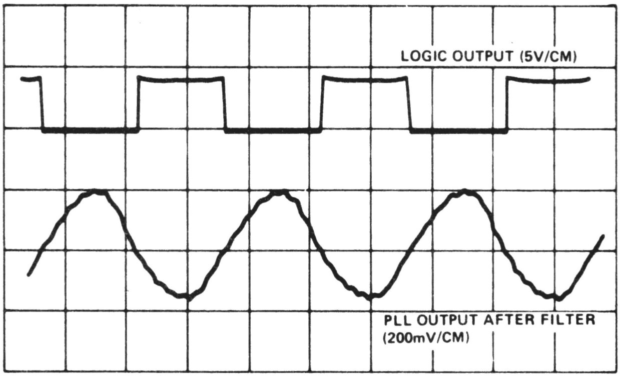


Figure 3

SCA Demodulator Using the 565

This application involves demodulation of a frequency modulated subcarrier of the main channel. A popular example here is the use of the PLL to recover the SCA (Subsidiary Carrier Authorization or storecast music) signal from the combined signal of many commercial FM broadcast stations. The SCA signal is a 67kHz frequency modulated subcarrier which puts it above the frequency spectrum of the normal stereo or monaural FM program material. By connecting the circuit of Figure 5.14 to a point between the FM discriminator and the de-emphasis filter of a commercial band (home) FM receiver and tuning the receiver to a station which broadcasts an SCA signal, one can obtain hours of commercial free background music.

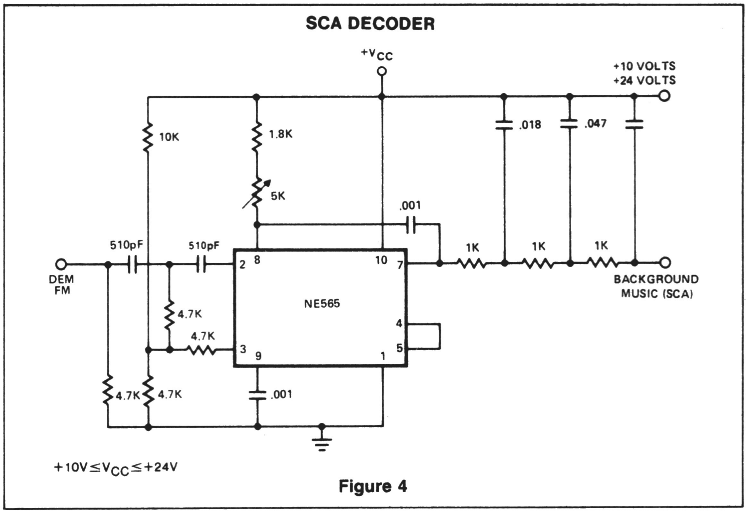

SCA DECODER
+VCC
+10 VOLTS
+24 VOLTS
10K
1.8K
5K
.018
.047
.001
510pF
510pF
DEM
FM
2
8
10
7
1K
1K
1K
NE565
BACKGROUND
MUSIC (SCA)
4.7K
4.7K
4
5
3
9
1
4.7K
4.7K
.001
+10V≤VCC≤+24V

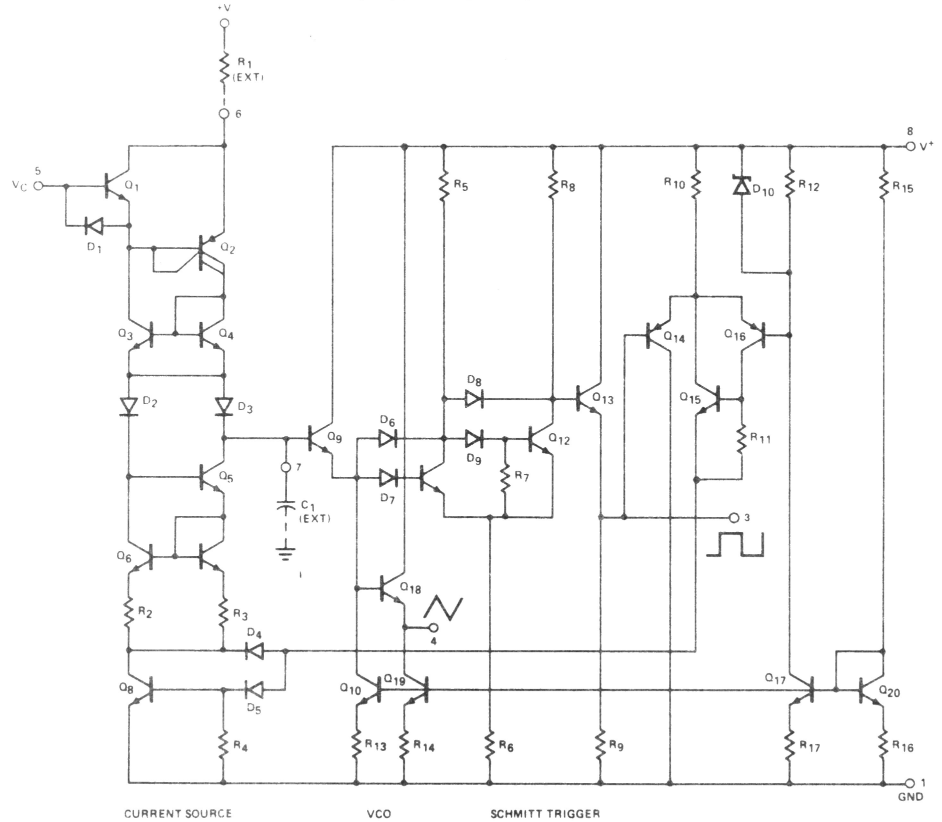
Figure 4

CIRCUIT DESCRIPTION OF THE NE566

CIRCUIT DESCRIPTION OF THE 566 PLL

The 566 is the voltage controlled oscillator portion of the 565. The basic die is the same as that of the 565; modified metalization is used to bring out only the VCO. The 566 circuit diagram is shown in Figure 1. Transistor Q 18 provides a buffered triangle waveform output. (The triangle waveform is available at capacitor C_1 also, but any current drawn from pin 7 will alter the duty cycle and frequency.) The square wave output is available from Q 19 by pin 4. The circuit will opeate at frequencies up to 1MHz and may be programmed by the voltage applied on the control terminal (pin 5), by injecting current into pin 6, or by changing the value of the external resistor and capacitor (R_1 and C_1.)

CIRCUIT DIAGRAM OF 566



+V
R1 (EXT)
6
8
V+
5
VC
Q1
D1
Q2
Q3
Q4
D2
D3
Q5
Q6
R2
R3
D4
Q8
D5
R4
Q9
7
C1 (EXT)
D6
D7
D8
D9
R5
R8
R7
Q12
Q13
Q18
4
Q10
Q19
R13
R14
R6
R9
R10
D10
R12
R15
Q14
Q16
Q15
R11
3
Q17
Q20
R17
R16
1
GND
CURRENT SOURCE
VCO
SCHMITT TRIGGER

Figure 1

WAVEFORM GENERATORS WITH THE NE566 AN186

WAVEFORM GENERATORS

The oscillator portion of many of the PLLs can be used as a precision, voltage-controllable waveform generator. Specifically, the 566 Function Generator contains the oscillator of the 565 PLL. Most of the applications which follow are designs using the 566. Many of these designs can be modified slightly to utilize the oscillator section of the 564 if higher frequency performance is desired.

Ramp Generators

Figure 1 shows how the 566 can be wired as a positive or negative ramp generator. In the positive ramp generator, the external transistor driven by the pin 3 output rapidly discharges C_1 at the end of the charging period so that charging can resume instantaneously. The pnp transistor of the negative ramp generator likewise rapidly charges the timing capacitor C_1 at the end of the discharge period. Because the circuits are reset so quickly, the temperature stability of the ramp generator is excellent. The period τ is $1/2\, f_o$ where f_c is the 566 free-running frequency in normal operation. Therefore,

$$T = \frac{1}{2f_o} = \frac{R_T C_1 V_{CC}}{5(V_{CC} - V_C)} \qquad (1)$$

where V_C is the bias voltage at pin 5 and R_T is the total resistance between pin 6 and V_{CC}. Note that a short pulse is available at pin 3. (Placing collector resistance in series with the external transistor collector will lengthen the pulse.)

Sawtooth and Pulse Generator

Figure 2 shows how the pin 3 output of the 566 can be used to provide different charge and discharge currents for C_1 so that a sawtooth output is available at pin 4 and a pulse at pin 3. The pnp transistor should be well saturated to preserve good temperature stability. The charge and discharge times may be estimated by using the formula

$$T = \frac{R_T C_1 V_{CC}}{5(V_{CC} - V_C)} \qquad (2)$$

where R_T is the combined resistance between pin 6 and V_{CC} for the interval considered.

Triangle to Sine Converters

Conversion of triangle wave shapes to sinusoids is usually accomplished by diode-resistor shaping networks, which accurately reconstruct the sine wave segment by segment. Two simpler and less costly methods may be used to shape the triangle waveform of the 566 into a sinusoid with less than 2% distortion.

In Figure 3, the non-linear $I_{DS} \cdot V_{DS}$ transfer characteristic of a p-channel junction FET is used to shape the triangle waveform.

RAMP GENERATORS

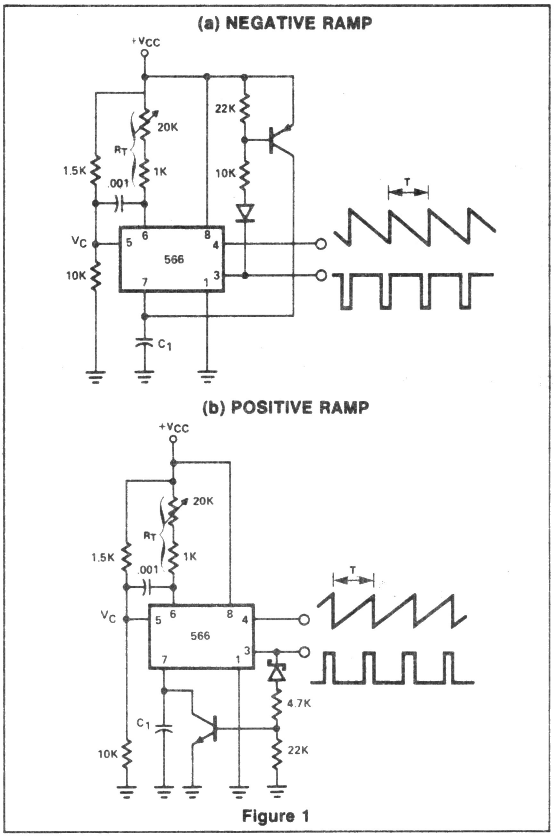

(a) NEGATIVE RAMP
+VCC
20K
RT
1K
.001
1.5K
22K
10K
VC
5
6
8
4
566
7
1
3
10K
C1
T
(b) POSITIVE RAMP
+VCC
20K
RT
1K
.001
1.5K
VC
5
6
8
4
566
7
1
3
C1
10K
4.7K
22K
T

Figure 1

SAWTOOTH AND PULSE GENERATORS

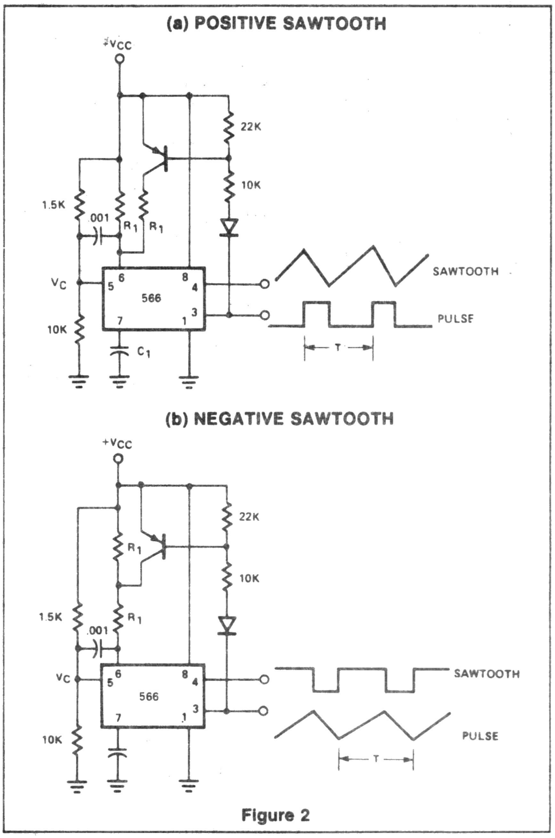

(a) POSITIVE SAWTOOTH
+VCC
22K
10K
1.5K
.001
R1
R1
VC
5
6
8
4
566
7
1
3
10K
C1
SAWTOOTH
PULSE
T
(b) NEGATIVE SAWTOOTH
+VCC
22K
R1
10K
1.5K
R1
.001
VC
5
6
8
4
566
7
1
3
10K
SAWTOOTH
PULSE
T

Figure 2

WAVEFORM GENERATORS WITH THE NE566

The amplitude of the triangle waveform is critical and must be carefully adjusted to achieve a low distortion sinusoidal output. Naturally, where additional waveform accuracy is needed, the diode-resistor shaping scheme can be applied to the 566 with excellent results since it has very good output amplitude stability when operated from a regulated supply.

Single Tone Burst Generator

Figure 4 is a tone burst generator which supplies a tone for one-half second after the power supply is activated; its intended use is a communications network alert signal. Cessation of the tone is accomplished at the SCR, which shunts the timing capacitor C_1 charge current when activated. The SCR is gated on when C_2 charges up to the gate voltage which occurs in 0.5 seconds. Since only 70µA are available for triggering, the SC must be sensitive enough to trigger at this level. The triggering current can be increased, of course, by reducing R_2 (and increasing C_2 to keep the same time constant). If the tone duration must be constant under widely varying supply voltage conditions, the optional Zener diode regulator circuit can be added, along with the new value for R_2, $R_2' = 82k\Omega$.

If the SCR is replaced by a npn transistor, the tone can be switched on and off at will at the transistor base terminal.

Low Frequency FM Generators

Figure 5 shows FM generators for low frequency (less than 0.5MHz center frequency) applications. Each uses a 566 function generator as a modulation generator and a second 566 as the carrier generator.

Capacitor C_1 selects the modulation frequency adjustment range and C_1' selects the center frequency. Capacitor C_2 is a coupling capacitor which only needs to be large enough to avoid distorting the modulating waveform.

If a frequency sweep in only one direction is required, the 566 ramp generators given in this section may be used to drive the carrier generator.

TRIANGLE-TO-SINE CONVERTERS

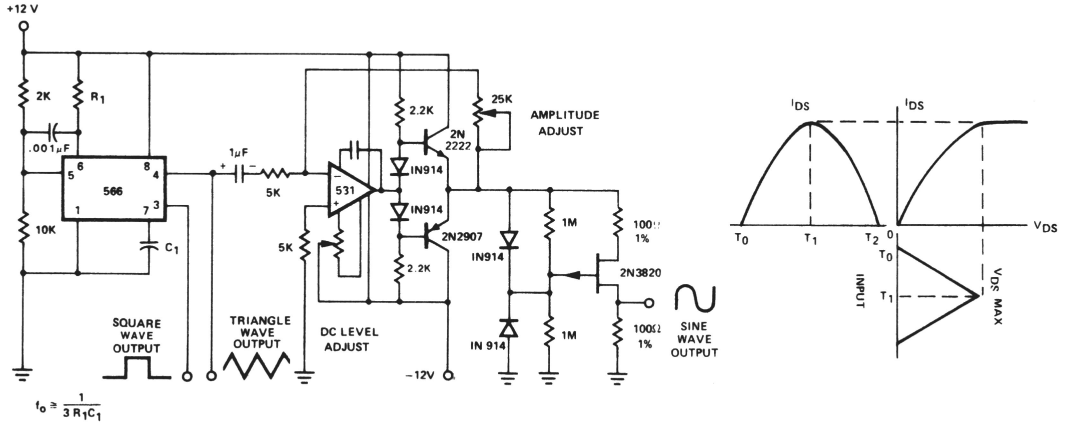

+12 V
2K
R1
.001µF
566
5 6 8 4
1 7 3
10K
C1
1µF
5K
531
5K
2.2K
2N 2222
IN914
IN914
2N2907
2.2K
25K
AMPLITUDE ADJUST
1M
100Ω 1%
IN914
2N3820
1M
100Ω 1%
IN 914
SINE WAVE OUTPUT
SQUARE WAVE OUTPUT
TRIANGLE WAVE OUTPUT
DC LEVEL ADJUST
-12V
$f_0 \approx \frac{1}{3R_1C_1}$
IDS
IDS
T0
T1
T2
0
VDS
T0
T1
INPUT
VDS MAX

Figure 3

SINGLE-BURST TONE GENERATOR

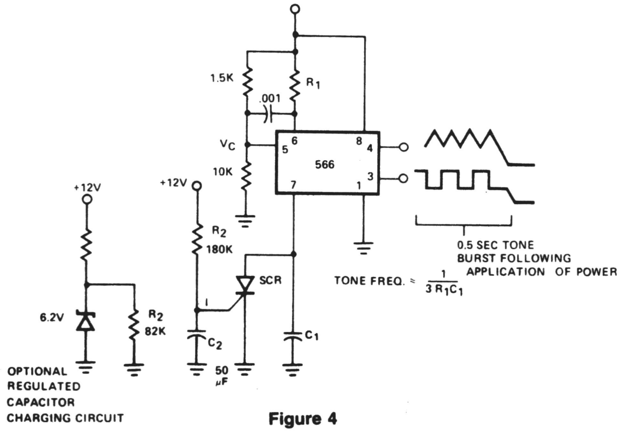
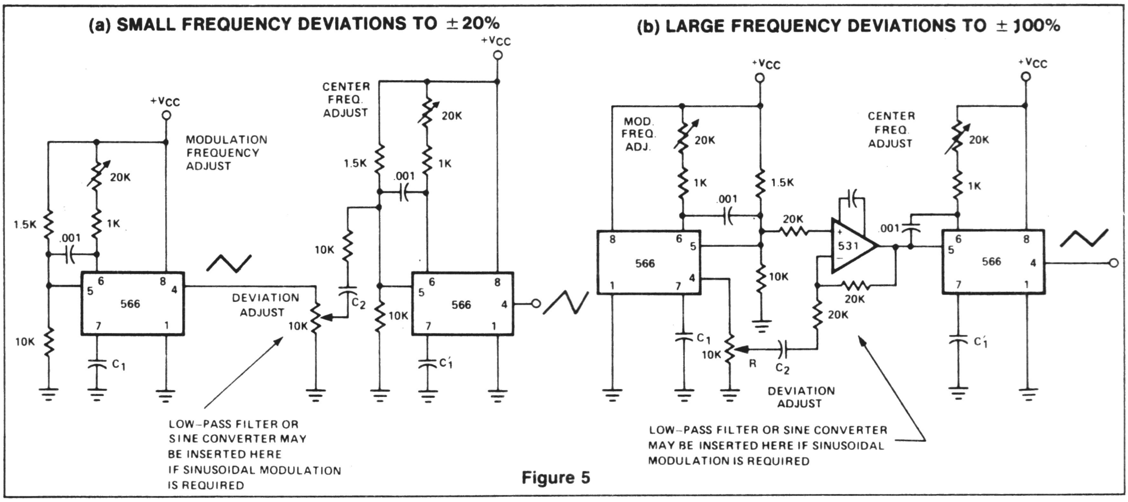

+12V
1.5K
R1
.001
VC
566
5 6 8 4
7 1 3
10K
+12V
R2 180K
SCR
C2
50 µF
C1
+12V
6.2V
R2 82K
OPTIONAL REGULATED CAPACITOR CHARGING CIRCUIT
0.5 SEC TONE BURST FOLLOWING APPLICATION OF POWER
TONE FREQ. $\approx \frac{1}{3R_1C_1}$

Figure 4

FREQUENCY MODULATED GENERATORS


+VCC
MODULATION FREQUENCY ADJUST
20K
1K
1.5K
.001
10K
5
6
8
4
7
1
566
C1
CENTER FREQ. ADJUST
20K
1.5K
1K
.001
10K
C2
DEVIATION ADJUST
10K
566
C'1
MOD. FREQ. ADJ.
20K
1K
1.5K
.001
20K
10K
531
20K
20K
C1
10K
R
C2
DEVIATION ADJUST
CENTER FREQ. ADJUST
20K
1K
.001
566
C'1

(a) SMALL FREQUENCY DEVIATIONS TO ±20%

LOW-PASS FILTER OR SINE CONVERTER MAY BE INSERTED HERE IF SINUSOIDAL MODULATION IS REQUIRED

(b) LARGE FREQUENCY DEVIATIONS TO ±100%

LOW-PASS FILTER OR SINE CONVERTER MAY BE INSERTED HERE IF SINUSOIDAL MODULATION IS REQUIRED

Figure 5

1. Appleton, E.V., "Automatic Synchronization of Triode Oscillators," *Proc. Cambridge Phil. Soc.,* vol. 2, pt. III, p. 231, 1922-1923.
2. Gardner, F.M., *Phaselock Techniques,* New York: Wiley, 1966.
3. Blanchard, A., *Phase-Locked Loops,* New York: Wiley, 1976.
4. Viterbi, A.J., *Principles of Coherent Communication,* New York: McGraw-Hill, 1966.
5. Connelly, J.A., *Analog Integrated Circuits: Devices, Circuits, Systems, and Applications,* New York: Wiley, 1975.
6. Grebene, A.B., *Analog Integrated Circuit Design,* New York: Van Nostrand-Reinhold, 1972.
7. Gupta, S.C., "Phase-Locked Loops," *Proc. IEEE,* vol. 63, no. 2, pp. 291-306, Feb. 1975.
8. D'Azzo, J.J. and C.H. Houpis, *Feedback Control System Analysis* (Second Edition), New York: McGraw-Hill, 1966, p. 81.
9. Gilbert, B., "A New Wideband Amplifier Technique,"*IEEE J. of Solid State Ckts.*, SC-3(4), pp. 353-365, 1968.
10. Gardner, op. cit., pp. 117-119.
11. Milligan, L.V. and E. Cornicelli, "Phase Locked Loops Provide Accurate, Efficient DC Motor Speed Control," *EDN,* August 1, 1972, pp. 32-35.

CIRCUIT DESCRIPTION OF THE 567 TONE DECODER AN187

CIRCUIT DESCRIPTION OF THE 567 TONE DECODER

The 567 is a PLL designed specifically for frequency sensing or tone decoding. The 567 has a controlled oscillator, a phase comparator and a second auxiliary or quadrature phase detector. In addition, however, it contains a power output stage which is driven directly by the quadrature phase detector output. During lock, the quadrature phase detector drives the output stage on, so the device functions as a tone decoder or frequency relay. The tone decoder free-running frequency and bandwidth are specified by the free-running frequency and capture range of the loop portion. Since a tone decoder, by definition, responds to a stable frequency, the lock or tracking range is relatively unimportant except as it limits the maximum attainable capture range. The complete circuit diagram of the 567 is shown in Figure 1.

The current controlled oscillator is shown in simplified form in Figure 2. It provides both a square wave output and a quadrature output. The control current I_c sweeps the oscillator ±7% of the free-running frequency, which is set by external components R_1 and C_1.

Transistors Q1 through Q6 form a flip-flop which can switch pin 5 between V_{BE} and $+V - V_{BE}$. Thus, the R_1C_1 network is driven from a square wave of $+V - 2V_{BE}$ peak-to-peak volts. On the positive portion of the square wave, C_1 is charged through R_1 until V_1 is reached. A comparator circuit driven from C_1 at pin 6 then supplies a pulse which resets the flip-flop so that pin 5 switches to V_{BE} and C_1 is discharged until V_2 is reached. A second comparator then supplies a pulse which sets the flip-flop and C_1 resumes charging.

The total swing of the capacitor voltage, as determined by the comparator sensing voltages, is

$$V_1 - V_2 = (+V - 2V_{BE})\left[\frac{R_{22} + R_{23}}{R_{21} + R_{22} + R_{23} + R_{24}}\right]$$
$$= K\,(+V - 2V_{BE}) \qquad (1)$$

Due to the excellent matching of integrated resistors, the resistor ratio K may be considered constant. Figure 3 shows the pin 5 and pin 6 voltages during operation. It is obvious from the proportion that $t_1 + t_2$ is independent of the magnitude of +V and dependent only on the time constant R_1C_1 of the external components. Moreover, if $(V_1 + V_2)/2 = +V/2$, then $t_1 = t_2$ and the duty cycle is 50%. Note that the triangular waveform is phase shifted from the square wave.

CIRCUIT DIAGRAM OF 567

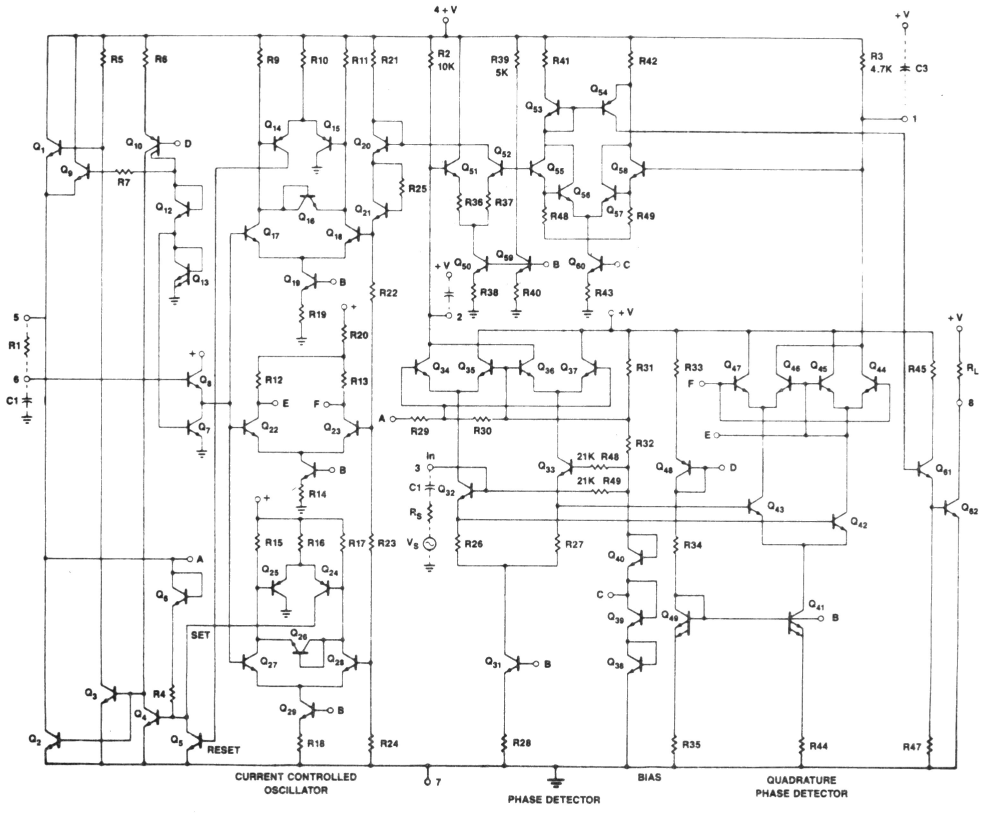

+V
R5
R6
R9
R10
R11
R21
R2 10K
R39 5K
R41
R42
R3 4.7K
C3
1
Q1
Q9
R7
Q10
D
Q12
Q13
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
R25
Q51
Q52
Q53
Q54
Q55
Q56
Q57
Q58
R36
R37
R48
R49
Q50
Q59
Q60
B
C
R38
R40
R43
2
R19
R20
R22
5
R1
6
C1
Q8
Q7
R12
R13
E
F
Q22
Q23
A
R29
R30
Q34
Q35
Q36
Q37
R31
R33
Q47
Q46
Q45
Q44
R45
RL
8
R32
In
3
C1
Q32
Q33
21K R48
21K R49
Q48
Q43
Q42
Q61
Q62
RS
VS
R14
R15
R16
R17
R23
R26
R27
R34
Q40
Q25
Q24
Q6
Q39
Q49
Q41
SET
Q26
Q27
Q28
Q31
Q38
Q3
R4
Q4
Q2
Q5
RESET
Q29
R18
R24
R28
R35
R44
R47
CURRENT CONTROLLED OSCILLATOR
7
PHASE DETECTOR
BIAS
QUADRATURE PHASE DETECTOR

Figure 1

CIRCUIT DESCRIPTION OF THE 567 TONE DECODER

A differential stage (Q22 and Q23) amplifies the triangular wave with respect to $(V_1 + V_2)/2$ to provide the quadrature output. (Due to the exponential distortion of the triangle wave, the quadrature output is actually phase shifted about 80°, but no operating compromises result from this slight deviation from true quadrature.)

One source of error in this oscillator scheme is current drawn by the comparators from the R_1C_1 mode. An emitter follower, therefore, is inserted at X to minimize this drain and Q21 placed in series with Q20 to drop the comparator sensing voltage one V_{BE} to compensate for the V_{BE} drop in the emitter follower.

In order to insure that the square wave drops quickly and accurately to V_{BE}, an active clamp scheme is applied to the collector of Q2. The base of Q9 is held at 2 V_{BE} so that as Q2 is turned on its base current, its collector is held at V_{BE}. Because Q2 and Q3 have the same geometry and their base-emitter voltages are the same, the maximum Q2 current when clamped is essentially the same as the collector current of Q3 (as limited by R_5). The flip-flop was optimized for maximum switching speed to reduce frequency drift due to switching speed variations.

Current control of the frequency is achieved by making R_{21} somewhat less than R_{24} and restoring the proper voltage for 50%

SIMPLIFIED DIAGRAM OF 567 TONE DECODER CURRENT-CONTROLLED OSCILLATOR

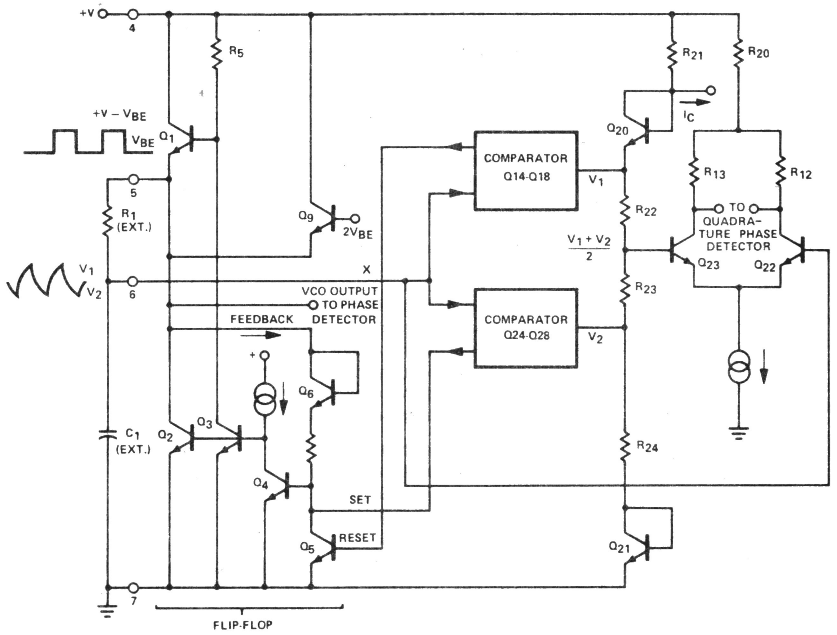

+V
4
R5
+V − VBE
VBE
Q1
5
R1
(EXT.)
Q9
2VBE
X
V1
V2
6
VCO OUTPUT
TO PHASE
FEEDBACK
DETECTOR
+
Q6
C1
(EXT.)
Q2
Q3
Q4
SET
RESET
Q5
7
FLIP-FLOP
COMPARATOR
Q14-Q18
COMPARATOR
Q24-Q28
V1
V2
(V1 + V2)/2
R21
R20
Q20
IC
R13
R12
R22
R23
R24
TO
QUADRATURE PHASE
DETECTOR
Q23
Q22
Q21

Figure 2

CURRENT-CONTROLLED OSCILLATOR WAVESHAPES IN THE 567

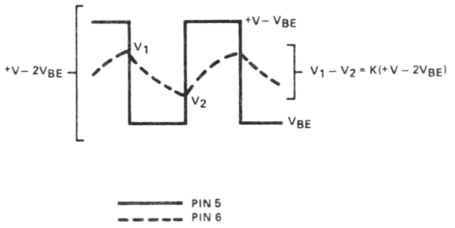

+V − VBE
V1
+V − 2VBE
V1 − V2 = K(+V − 2VBE)
V2
VBE
PIN 5
PIN 6

Figure 3

CIRCUIT DESCRIPTION OF THE 567 TONE DECODER

duty cycle by drawing I_c of 100μA for the R_{21}, Q20 junction. When I_c is then varied between 0 and 200μA, the frequency changes by ±7%. Because of the slight shift in the voltage levels V_1 and V_2 with I_c, the square wave duty cycle changes from about 47% to about 53% over the control range. To avoid drift of free-running frequency with temperature and supply voltage changes when $I_c \neq 0$, I_c is also made a function of $+V - 2\,V_{BE}$.

A doubly balanced multiplier formed by Q32 through Q37 (Figure 1) functions as the phase comparator. The input signal is applied to the base of Q32. Transistors Q34-Q37 are driven by a square wave taken from the CCO at the collector of Q2. Phase comparator input bias is provided by three diodes, Q38 through Q40, connected in series, assuring good bias voltage matching from run to run. Emitter resistors R_{26} and R_{27}, in addition to providing the necessary dynamic range at the input, help stabilize the gain over the wide temperature range.

The loop dc amplifier is formed by Q51 and Q52. Having a current gain of 8, it permits even a small phase detector output to drive the CCO the full ±7%. Therefore, full detection bandwidth can be obtained for any in-band input signal greater than about 70mV rms. However, the main purpose of high loop gain in the tone decoder is to keep the locked phase as close to $\pi/2$ as possible for all but the smallest input levels since this greatly facilitates operation of the quadrature lock detector. Emitter resistors R_{36} and R_{37} help stabilize the gain over the required temperature range. Another function of the dc amplifier is to allow a higher impedance level at the low pass filter terminal (pin 2) so that a smaller capacitor can be used for a given loop cutoff frequency. Once again, emitter resistors help stabilize the loop gain over the temperature range.

The quadrature phase detector (QPD), formed by a second doubly-balanced multiplier Q42-Q47, is driven from the quadrature output (E,F, in Figure 1) of the CCO. The signal input comes from the emitters of the input transistors Q32 and Q33.

The output stage, Q53 through Q62, compares the average QPD current in the low pass output filter R_3C_3 with a temperature compensated current in R_{39} (forming the threshold voltage V_t).

Since R_3 is slightly lower in value than R_{39}, the output stage is normally off. When the lock and the QPD current I_q occurs, pin 1 voltage drops below the threshold voltage V_t and the output stage is energized.

The uncommitted collector (pin 8) of the power npn output transistor can drive both 100 - 200mA loads and logic elements, including TTL.

The K_o conversion gain for the 567 tone decoder is given by

$$K_o = 0.44\,\omega_o' \,\frac{\text{radians}}{\text{volt-sec}} \qquad (2)$$

while the K_d conversion gain depends upon the input signal level as shown in Figure 4. These parameters can be used to calculate the lock and capture range as has been illustrated previously.

The 567 tone decoder is a specialized loop which can be set up to respond to a given tone (constant frequency) within its bandwidth. The free-running frequency is set by a resistor R_1 and capacitor C_1. The bandwidth is controlled by the low pass filter capacitor C_2. A third capacitor C_3 integrates the output of the quadrature phase detector (QPD) so that the dc lock-indicating component can switch the power output stage on when lock is present. The 567 is optimized for stability and predictability of free-running frequency and bandwidth.

Two events must occur before an output is given. First, the loop portion of the 567 must achieve lock. Second, the output capacitor C_3 must charge sufficiently to activate the output stage. For minimum response time, these events must be as brief as possible.

As previously discussed, the lock time of a loop can be minimized by reducing the response time of the low pass filter. Thus, C_2 must be as small as possible. However, C_2 also controls the bandwidth. Therefore, the response time is an inverse function of bandwidth as shown by Figure 5, reprinted from the 567 data sheet. The upper curve denotes the expected worst-case response time when the bandwidth is controlled solely by C_2 and the input amplitude is 200mV rms or greater. The response time is given in cycles of free-running frequency. For example, a 2% bandwidth at a free-running frequency of 1000 cycles can require as long as 280 cycles (280ms) to lock when the initial phase relationship is at its worst. Figure 6 gives a typical distribution of response time versus input phase. Note that, assuming random initial input phase, only 30/180 = 1/6 of the time will the lock-up time be longer than half the worst case lock-up time. Figure 7 shows some actual measurements of lock-up time for a set-up having a worst case lock-up time of 27 cycles and a best-case lock-up time of four input cycles.

The lower curve on the graph of Figure 5 shows the worst-case lock-up time when the loop gain is reduced as a means of reducing the bandwidth (see data sheet, Alternate Method of Bandwidth Reduction). The value of C_2 required for this minimum response time is

$$C_{2(\text{min})} = \frac{130}{f_o'}\left[\frac{10K + R_A}{R_A}\right]\mu F \qquad (3)$$

It is important to note that noise immunity and rejection of out-band tones suffer somewhat when this minimum value of C_2 is used so that response time is gained at their expense. Except at very low input levels, input amplitude has only a minor effect

PHASE COMPARATOR CONVERSION GAIN, K_D, FOR THE 567 TONE DECODER

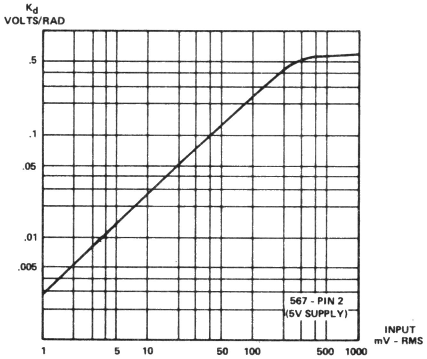


Figure 4

GREATEST NUMBER OF CYCLES BEFORE OUTPUT FOR THE 567 TONE DECODER

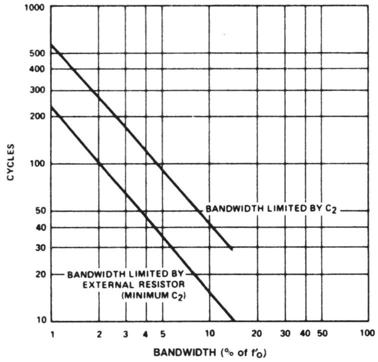


Figure 5

LOCK-UP TIME VERSUS INITIAL PHASE FOR THE 567 TONE DECODER

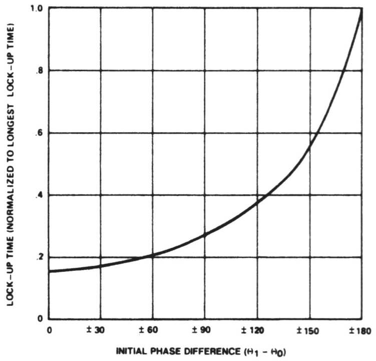


Figure 6

LOCK-UP TIME VARIATION DUE TO RANDOM INITIAL PHASE FOR THE 567 TONE DECODER

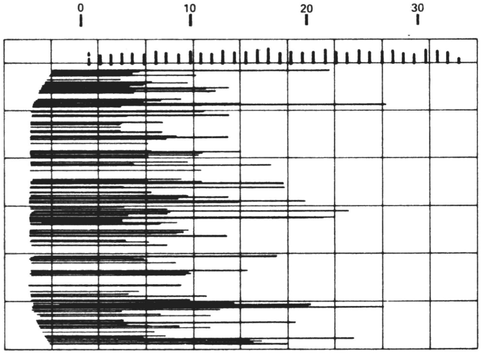


Figure 7

LOCK-UP TRANSIENT RESPONSE FOR 567 TONE DECODER

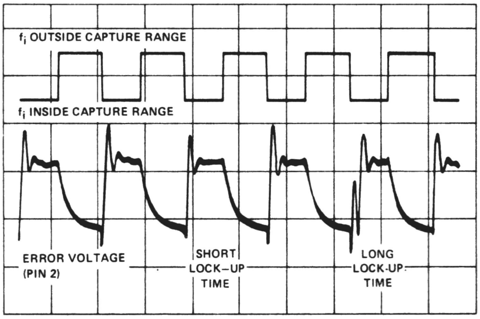


Figure 8

on the lock-up time - usually negligible in comparison to the variation caused by input phase.

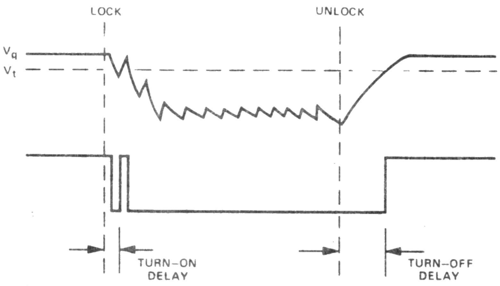
Lock-up transients can be displayed on a two-channel scope with case. Figure 8 shows the display which results. The top trace shows the square wave which either gates the input generator signal off and on (or shifts the frequency in and out of the band if you have a generator which has a frequency control input only). The lower trace shows the voltage at pin 2, the low pass filter voltage. The input frequency is offset slightly from the free-running frequency so that the locked and unlocked voltage are different. It is apparent that, while the c_2 decay during unlock is always the same, the lock transient is different each time.

This is because the turn-on repetition rate is such that a different initial phase relationship occurs with each appearance of the in-band signal. It is tempting to adjust the repetition rate so that a fast, constant lock-up transient is displayed. However, in doing so a favorable initial phase is created that is not present in actual operation. On the contrary, it is most realistic to adjust the repetition rate so that the longest lock-up time is displayed, such as the fifth lock transient shows. Once this display is achieved, the effect of various adjustments in C_2 or input amplitude is seen. However, *the repetition rate must be readjusted for worst-case lock-up after each such change.*

Once lock is achieved, the quadrature phase detector output at pin 1 is integrated by C_3 to extract the dc component. As C_3 charges from its quiescent value V_q (see Figure 9) to its final value ($V_q \bullet \Delta V$), it passes through the output stage threshold, turning it on. The total voltage change is a function of input amplitude. Since the unadjusted V_q is very close (within 50mV) to V_t, the output stage turns on very soon after lock. Only a small fraction of the output stage time constant ($\tau = 4700C_3$) expires before V_t is crossed so that C_3 does not greatly influence the response time. However, as shown in Figure 9(a), the turn-off delay time can be quite long when C_3 is large. Figure 9(b) shows how desensitizing the output stage by connecting a high-value resistor between pin 1 and pin 4 (positive supply voltage) can equalize the turn-on and turn-off time. If turn-off delay is

EFFECT OF THRESHOLD VOLTAGE ADJUSTMENT ON TONE DECODER TURN-ON AND TURN-OFF DELAY

(A) V_Q SLIGHTLY GREATER THAN V_T,



(B) V_Q MUCH GREATER THAN V_T

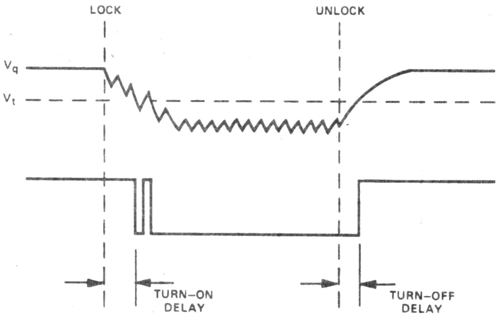


Figure 9

important in the overall response time, then desensitizing can reduce the total delay.

But why not make C_3 very small so that these delays can be totally neglected? The problem here is that the QPD output has a large second harmonic component of the free-running frequency that must be filtered out. Also, noise, outband signals, and difference frequencies formed by close out-band frequencies beating with the VCO frequency appear at the QPD output. All these must be attenuated by C_3 or the output stage will chatter on and off as the threshold is approached. The more noisy the input signal and the larger the near-band signals, the greater C_3 must be to reject them. Thus, there is a complicated relationship between the input spectrum and the size of C_3. What must be done, then, is to make C_3 more than sufficient for proper operation (no false outputs or missed signals) under actual operating conditions and then reduce its value in small steps until either the required response time is obtained or operation becomes unsatisfactory.

In setting up the tone decoder for maximum speed, it is best to proceed as follows:

a After the center frequency has been set, adjust C_2 to give the desired bandwidth or, if the graph of response time in cycles (Figure 7) suggests that worst case lock-up time will be too long, incorporate the loop gain reduction scheme as an alternate means of bandwidth reduction. (See data sheet).

b Check lock-up time by observing the waveform at pin 2 while pulsing the input signal on and off (or in and out of the band when a FM generator is used). Adjust repetition rate to reveal worst lock-up time.

c Starting with a large value of C_3 (say 10 C_2), reduce it as much as possible in steps while monitoring the output to be certain that no false outputs or missed signals occur. The full input spectrum should be used for this test. Ignore brief transients or chatter during turn-on and turn-off as they can be eliminated with the chatter prevention feedback technique described in the data sheet.

d Use the desensitizing technique, also described in the data sheet, to balance turn-on and turn-off delay.

e Apply the chatter prevention technique to clean up the output.

If this procedure results in a worst-case response time that is too slow, the following suggestions may be considered:

a Relax the bandwidth requirement.

b Operate the entire system at higher frequency when this option is available.

c Use two tone decoders operating at slightly different frequencies and OR the outputs. This will reduce the statistical occurrence of the worst-case lock-up time so that excessive lock-up time occurs. For example, if the lock-up time is marginal 10% of the time with one unit, it will drop to 1% with two units.

d Control the in-band input amplitude to stabilize the bandwidth, set up two tone decoders for maximum bandwidth, and overlap the detection bands to make the desired frequency range equal to the overlap. Since both tone decoders are on only when a tone appears within the overlap range, the outputs can be ANDed to provide the desired selectivity.

e If the system design permits, send the tone to be detected continuously at a low level (say 25mV rms) to keep the loop in lock at all times. The output stage, slightly desensitized, can then be gated on as required by increasing the signal amplitude during the on time. Naturally, the signal phase should be maintained as the amplitude is changed. This scheme is extremely fast, allowing repetition rates as fast as 1/3 to 1/2 the free- running frequency when C_3 is small. This is equivalent to ASK (amplitude shift keying).

SELECTED CIRCUITS USING THE NE567

Touch-Tone® Decoder

Touch-Tone® decoding is of great interest since all sorts of remote control applications are possible if you make use of the encoder (the pushbutton dial) that will ultimately be part of every phone. A low cost decoder can be made as shown in Figure 1. Seven 567 tone decoders, their inputs connected in common to a phone line or acoustical coupler, drive three integrated NOR gate packages. Each tone decoder is tuned, by means of R_1 and C_1, to one of the seven tones. The R_2 resistor reduces the bandwidth to about 8% at 100mV and 5% at 50mV rms. Capacitor C_4 decouples the seven units. The seven R_2 resistors and capacitor C_4 can be eliminated at the expense of a somewhat slower response at low input voltages (50 to 100mV rms). The bandwidth can be controlled in the normal manner by selecting C_2 to be 4.7μF for the three lower frequencies and 2.2μF for the four higher frequencies.

The only unusual feature of this circuit is the means of bandwidth reduction using the R_2 resistors. An external resistor R_A can be used to reduce the loop gain and, therefore, the bandwidth. Resistor R_2 serves the same function as R_A except that instead of going to a voltage divider for dc bias, it goes to a common point with the six other R_2 resistors. In effect, the five 567s which are not being activated during the decoding process serve as bias voltage sources for the R_2 resistors of the two 567s which are being activated. Capacitor C_4 decouples the ac currents at the common point.

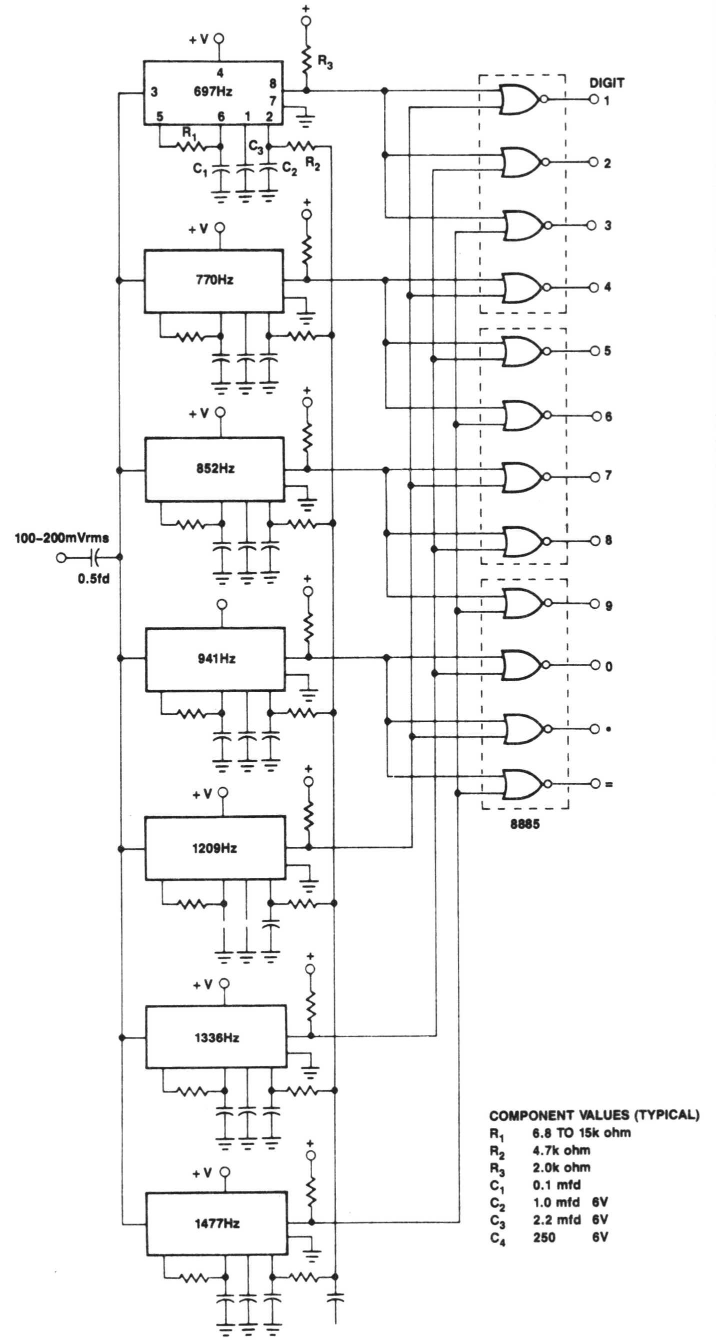
TONE DECODER APPLICATIONS (567)

The 567 is a special purpose PLL intended solely for use as a tone decoder. It contains a complete PLL including VCO, phase comparator, and amplifier as well as a quadrature phase detector or multiplier. If the signal amplitude at the lock frequency is above a minimal value, the driver amplifier turns on, driving a load with as much as 200mA. Thus the 567 gives an output whenever an inband tone is present. The 567 is optimized for both free-running frequency and bandwidth stability.

Dual Tone Decoder

Two 567 tone decoders connected as shown in Figure 2(a) permit decoding of simultaneous or sequential tones. Both units must be on before an output is given. R_1C_1 and $R_1'C_1'$ are chosen respectively for tones 1 and 2. If sequential tones (tone 1 followed by tone 2) are to be decoded, then C_3 is made very large to delay turn off of unit 1 until unit 2 has turned on and the NOR gate is activated.

LOW-COST TOUCH TONE® DECODER



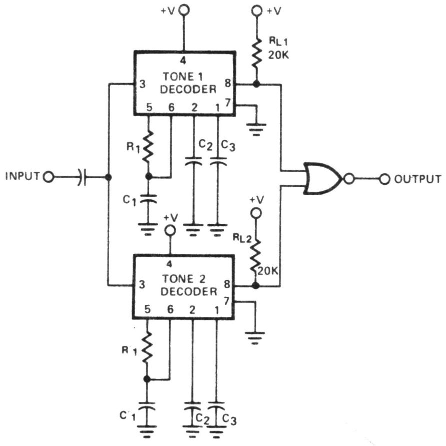
COMPONENT VALUES (TYPICAL)

R_1	6.8 TO 15k ohm	
R_2	4.7k ohm	
R_3	2.0k ohm	
C_1	0.1 mfd	
C_2	1.0 mfd	6V
C_3	2.2 mfd	6V
C_4	250	6V

(Figure 1)

DETECTION OF TWO SIMULTANEOUS OR SEQUENTIAL TONES

(a) NORING OUTPUTS TOGETHER


+V
+V
R_{L1}
20K
4
TONE 1
DECODER
3
8
7
5 6 2 1
R_1
C_2
C_3
INPUT
OUTPUT
C_1
+V
+V
R_{L2}
20K
4
TONE 2
DECODER
3
8
7
5 6 2 1
R_1
C'_1
C_2
C_3

(B) DISABLING THE SECOND DECODER UNTIL ENABLED BY THE FIRST

(C) BLOCKING POWER TO THE SECOND DECODER (PIN 7) UNTIL THE FIRST IS ENABLED.

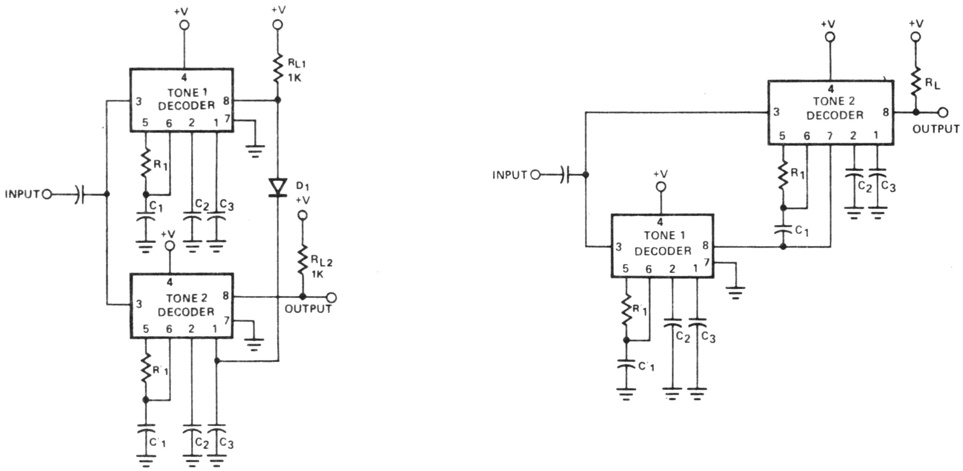

+V
+V
R_{L1}
1K
4
TONE 1
DECODER
3
8
7
5 6 2 1
R_1
C_1
C_2
C_3
INPUT
D_1
+V
R_{L2}
1K
+V
4
TONE 2
DECODER
3
8
7
5 6 2 1
OUTPUT
R'_1
C'_1
C_2
C_3
+V
+V
R_L
4
TONE 2
DECODER
3
8
5 6 7 2 1
OUTPUT
INPUT
R_1
C_2
C_3
C_1
+V
4
TONE 1
DECODER
3
8
7
5 6 2 1
R_1
C'_1
C_2
C_3

Figure 2

Note that the wrong sequence (tone 2 followed by tone 1) will not provide an output since unit 2 will turn off before unit 1 comes on. Figure 2(b) shows a circuit variation which eliminates the NOR gate. The output is taken from unit 2, but the unit 2 output stage is biased off by R_{L1} and D_1 until activated by tone 1. A further variation is given in Figure 2(c). Here, unit 2 is turned on by the unit 1 output when tone 1 appears, reducing the standby power to half. Thus, when unit 2 is on, tone 1 is or was present. If tone 2 is now present, unit 2 comes on also and an output is given. Since a transient output pulse may appear during unit 1 turn on, even if tone 2 is not present, the load must be slow in response to avoid a false output due to tone 1 alone.

High-Speed, Narrow-Band Tone Decoder

The circuit of Figure 2(a) may be used to obtain a fast, narrrow-band tone decoder. The detection bandwidth is achieved by overlapping the detection bands of the two tone decoders. Thus, only a tone within the overlap portion will result in an output. The input amplitude should be greater than 70mV rms at all times to prevent detection band shrinkage and C_2 should be between $130/f_o$ and $1300/f_o\mu F$ where f_o is the nominal detection frequency. The small value of C_2 allows operation at the maximum speed so that worst-case output delay is only about 14 cycles.

Low-Cost Frequency Indicator

Figure 3 shows how two tone decoders set up with overlapping detection bands can be used for a go/no-go frequency meter. Unit 1 is set 6% above the desired sensing frequency and unit 2 is set 6% below the desired frequency. Now, if the the incoming frequency is within 13% of the desired frequency, either unit 1 or unit 2 will give an output. If both units are on, it means that the incoming frequency is within 1% of the desired frequency. Three light bulbs and a transistor allow low cost read-out.

Phase Modulator

If a phase locked loop is locked onto a signal at the free-running frequency, the phase of the VCO will be 90° with respect to the input signal. If a current is injected into the VCO terminal (the low pass filter output), the phase will shift sufficiently to develop an opposing average current out of the phase comparator so that the VCO voltage is constant and lock is maintained. When the input signal amplitude is low enough so that the loop frequency swing is limited by the phase comparator output rather than the VCO swing, the phase can be modulated over the full range of 0 to 180°. If the input signal is a square wave, the phase will be a linear function of the injected current.

A block diagram of the phase modulator is given in Figure 4(a). The conversion factor K is a function of which loop is used, as well as the input square wave amplitude. Figure 4(b) shows an implementation of this circuit using the 567.

FREQUENCY DETECTOR WITH LOW-COST, LAMP READOUT

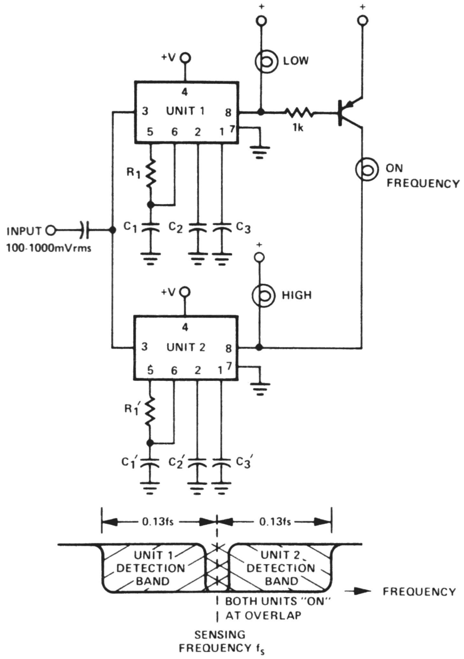
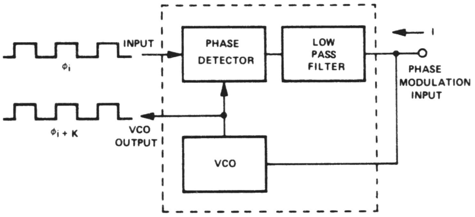

+
+
+V
LOW
4
3 UNIT 1 8
5 6 2 1 7
1k
ON FREQUENCY
R1
INPUT
100-1000mVrms
C1
C2
C3
+
+V
HIGH
4
3 UNIT 2 8
5 6 2 1 7
R1′
C1′
C2′
C3′
0.13fs
0.13fs
UNIT 1 DETECTION BAND
UNIT 2 DETECTION BAND
FREQUENCY
BOTH UNITS "ON" AT OVERLAP
SENSING FREQUENCY fs

Figure 3

PHASE MODULATION USING THE PLL

(a) BLOCK DIAGRAM


INPUT
φi
PHASE DETECTOR
LOW PASS FILTER
I
PHASE MODULATION INPUT
φi + K
VCO OUTPUT
VCO

(b) CIRCUIT IMPLEMENTATION WITH THE 567

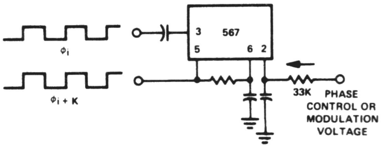

3 567
5 6 2
φi
φi + K
33K
PHASE CONTROL OR MODULATION VOLTAGE

Figure 4

BALANCED MODULATOR/ DEMODULATOR APPLICATIONS USING MC1496/MC1596

The MC1496 is a monolithic transistor array arranged as a balanced modulator-demodulator. The device takes advantage of the excellent matching qualities of monolithic devices to provide superior carrier and signal rejection. Carrier suppressions of 50dB at 10MHz are typical with no external balancing networks required.

Applications include AM and suppressed carrier modulators, AM and FM demodulators, and phase detectors.

THEORY OF OPERATION

As Figure 1 suggests, the topography includes three differential amplifiers. Internal connections are made such that the output becomes a product of the two input signals V_C and V_S.

To accomplish this the differential pairs Q1-Q2 and Q3-Q4, with their cross coupled collectors, are driven into saturation by the zero crossings of the carrier signal V_C. With a low level signal, V_S driving the third differential amplifier Q5-Q6, the output voltage will be a full wave multiplication of V_C and V_S. Thus for sine wave signals. V_{out} becomes:

$$V_{out} = E_x E_y[\cos(\omega x + \omega y)t + \cos(\omega x - \omega y)t] \qquad (1)$$

As seen by font = K (fc – fs) + K (fc + fs) (see Figure 2), the output voltage will contain the sum and difference frequencies of the two original signals. In addition, with the carrier input ports being driven into saturation, the output will contain the odd harmonics of the carrier signals.

BIASING

Since the MC1496 was intended for a multitude of different functions as well as a myriad of supply voltages, the biasing techniques are specified by the individual application. This allows the user complete freedom to choose gain, current levels, and power supplies. The device can be operated with single ended or dual supplies.

Internally provided with the device are two current sources driven by a temperature compensated bias network. Since the transistor geometries are the same and since V_{BE} matching in monolithic devices is excellent, the currents through Q7 and Q8 will be identical to the current set at pin 5. Figures 2 and 3 illustrate typical biasing arrangements from split and single ended supplies respectively.

Of primary interest in beginning the bias circuitry design is relating available power supplies and desired output voltages to device requirements with a minimum of external components.

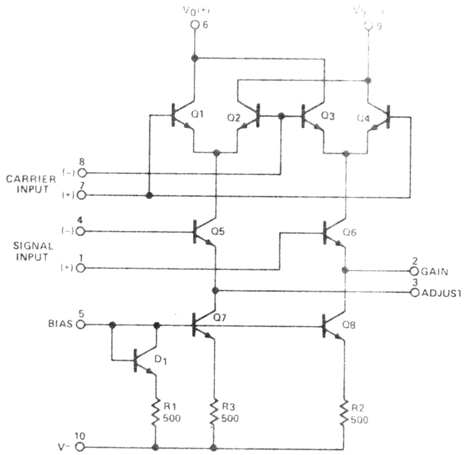
The transistors are connected in a cascode fashion. Therefore sufficient collector voltage must be supplied to avoid saturation if linear operation is to be achieved. Voltages greater than 2 volts are sufficient in most applications.

Biasing is achieved with simple resistor divider networks as shown in Figure 3. This configuration assumes the presence of symmetrical supplies. Explaining the dc biasing technique is probably best accomplished by an example. Thus, the initial assumptions and criteria are set forth:

1. Output swing greater than 4 volts p-p.
2. Positive and negative supplies of 6 volts are available.
3. Collector current is 2mA. It should be noted here that the collector output current is equal to the current set in the current sources.

As a matter of convenience the carrier signal ports are referenced to ground. If desired the modulation signal ports could be ground referenced with slight changes in the bias arrangement. With the carrier inputs at dc ground, the quiescent operating point of the outputs should be at one half the total positive voltage or 3 volts for this case. Thus a collector load resistor is selected which drops 3 volts at 2mA or 1.5k ohm. A quick check at this point reveals that with

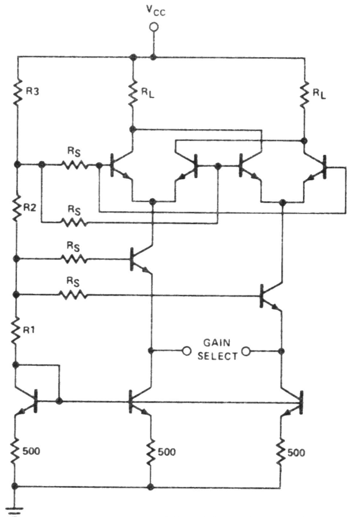
BALANCED MODULATOR SCHEMATIC



All resistor values are in ohms

Figure 1

SINGLE SUPPLY BIASING



All resistor values are in ohms

Figure 2

these loads and current levels the peak to peak output swing will be greater than 4 volts. It remains to set the current source level and proper biasing of the signal ports.

The voltage at pin 5 is expressed by

$V_{bias} = V_{BE} = 500 \times I_S$

where I_s is the current set in the current sources.

For the example V_{BE} is 700mV at room temperature and the bias voltage at pin 5 becomes 1.7 volts. Because of the cascode configuration both the collectors of the current sources and the collectors of the signal transistors must have some voltage to operate properly. Hence the remaining voltage of the negative supply (-6v + 1.7v = -4.3v) is split between these transistors by biasing the signal transistor bases at -2.15 volts.

Countless other bias arrangements can be used with other power supply voltages. The important thing to remember is that sufficient dc voltage is applied to each bias point to avoid collector saturation over the expected signal wings.

BALANCED MODULATOR

In the primary application of balanced modulation, generation of double sideband suppressed carrier modulation is accomplished. Due to the balance of both modulation and carrier inputs, the output, as mentioned, contains the sum and difference frequencies while attenuating the fundamentals. Upper and lower sideband signals are the strongest signals present with harmonic sidebands being of diminishing amplitudes as characterized by Figure 4.

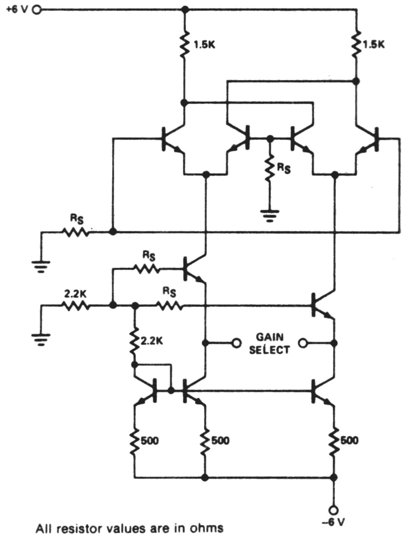
Gain of the 1496 is set by including emitter degeneration resistance located as R_E in Figure 5. Degeneration also allows the maximum signal level of the modulation to be increased. In general, linear response defines the maximum input signal as

$V_S \leq 15 \bullet R_E \text{ (Peak)}$

and the gain is given by

$$A_{vs} = \frac{R_L}{R_E + 2r_e} \qquad (2)$$

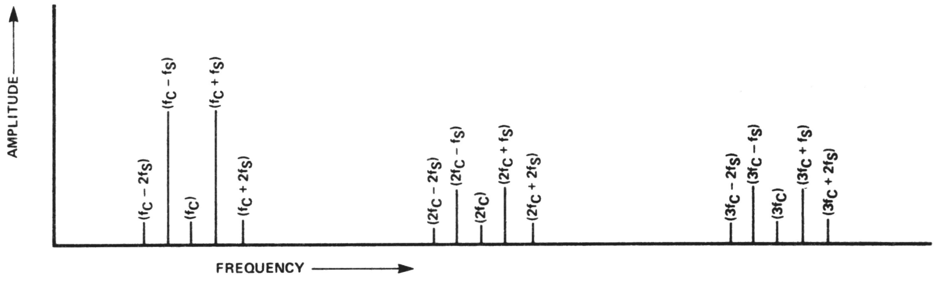
DUAL SUPPLY BIASING



All resistor values are in ohms

Figure 3

MODULATOR FREQUENCY SPECTRUM



f_C	Carrier Fundamental	$f_C \pm nf_S$	Fundamental Carrier Sideband Harmonics
f_S	Modulating Signal	nf_C	Carrier Harmonics
$f_C \pm f_S$	Fundamental Carrier Sidebands	$nf_C \pm nf_S$	Carrier Harmonic Sidebands

Figure 4

This approximation is good for high levels of carrier signals. Table 1 summarizes the gain for different carrier signals.

As seen from Table 1 the output spectrum suffers an amplitude increase of undesired sideband signals when either the modulation or carrier signals are high. Indeed, the modulation level can be increased if R_E is increased without significant consequence. However, large carrier signals cause odd harmonic sidebands (Figure 4) to increase. At the same time, due to imperfections of the carrier waveforms and small imbalances of the device, the second harmonic rejection will be seriously degraded. Output filtering is often used with high carrier levels to remove all but the desired sideband. The filter removes unwanted signals while the high carrier level guards against amplitude variations and maximizes gain. Broadband modulators, without benefit of filters, are implemented using low carrier and modulation signals to maximize linearity and minimize spurious sidebands.

AM MODULATOR

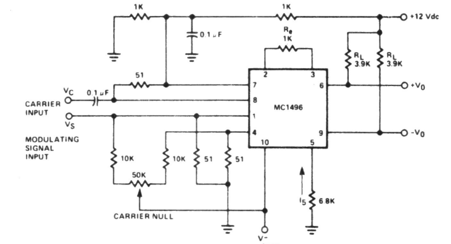
The basic current of Figure 5 allows no carrier to be present in the output. By adding offset to the carrier differential pairs, controlled amounts of carrier appear at the output whose amplitude becomes a function of the modulation signal or AM modulation. As shown, the carrier null circuit is changed from Figure 5 to have a wider range so that wider control is achieved. All connections are shown in Figure 6.

AM DEMODULATION

As pointed out in equation 1 the output of the balanced mixer is a cosine function of the angle between signal and carrier inputs. Further, if the carrier input is driven hard enough to provide a switching action, the output becomes a function of the input amplitude. Thus the output amplitude is maximum when there is 0° phase difference as shown in Figure 7.

Amplifying and limiting of the AM carrier is accomplished by IF gain block providing 55 dB of gain or higher with limiting of 400µV. The limited carrier is then applied to the detector at the carrier ports to provide the desired switching function. The signal is then demodulated by the synchronous AM demodulator (1496) where the carrier frequency is attenuated due to the balanced nature of the device. Care must be taken not to overdrive the signal input so that distortion does not appear in the recovered audio. Maximum conversion gain is reached when the carrier signals are in phase as indicated by the phase-gain relationship drawn in Figure 7. Output filtering will also be necessary to remove high frequency sum components of the carrier from the audio signal.

DOUBLE SIDEBAND SUPPRESSED CARRIER MODULATOR



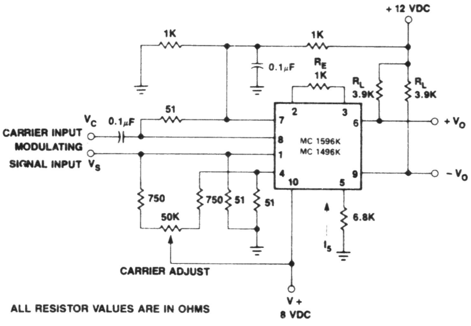
All resistor values are in ohms

Figure 5

CARRIER INPUT SIGNAL (V_C)	APPROXIMATE VOLTAGE GAIN	OUTPUT SIGNAL FREQUENCY(S)
Low-level dc	$\dfrac{R_L V_C}{2(R_E + 2r_E)\left(\frac{KT}{q}\right)}$	f_M
High-level dc	$\dfrac{R_L}{R + 2r_e}$	f_M
Low-level ac	$\dfrac{R_L V_{C(rms)}}{2\sqrt{2}\left(\frac{KT}{q}\right)(R_E + 2r_e)}$	$f_C \pm f_M$
High-level ac	$\dfrac{0.637 R_L}{R_E + 2r_e}$	$f_C \pm f_M$, $3f_C \pm f_M$, $5f_C \pm f_M$....

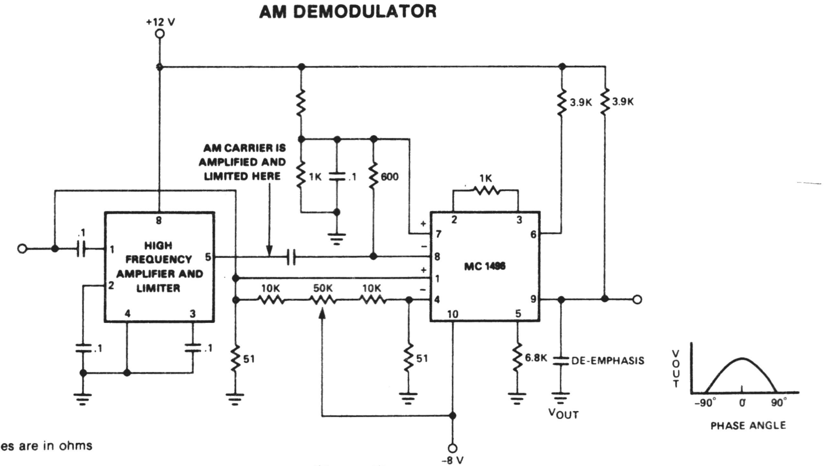
Table 1 VOLTAGE GAIN & OUTPUT SPECTRUM VS INPUT SIGNAL

AM MODULATOR



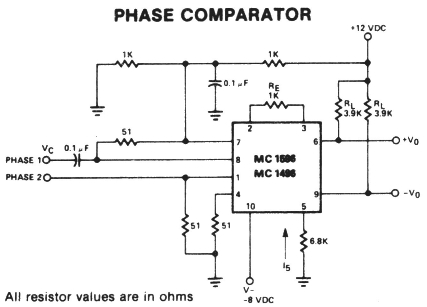
ALL RESISTOR VALUES ARE IN OHMS

Figure 6


AM DEMODULATOR
+12 V
3.9K
3.9K
AM CARRIER IS AMPLIFIED AND LIMITED HERE
1K
.1
600
1K
.1
HIGH FREQUENCY AMPLIFIER AND LIMITER
MC 1496
10K
50K
10K
51
51
6.8K
DE-EMPHASIS
VOUT
-8 V
VOUT
-90°
0
90°
PHASE ANGLE

All resistor values are in ohms

Figure 7


PHASE COMPARATOR
+12 VDC
1K
1K
0.1 μF
R_E 1K
R_L 3.9K
R_L 3.9K
51
V_C
0.1 μF
PHASE 1
PHASE 2
MC 1596
MC 1496
+Vo
-Vo
51
51
6.8K
I_5
V-
-8 VDC

All resistor values are in ohms

Figure 8

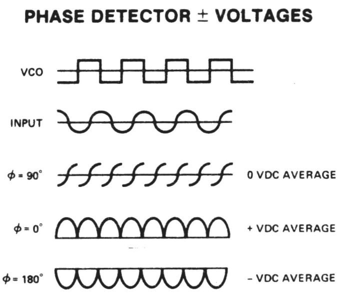
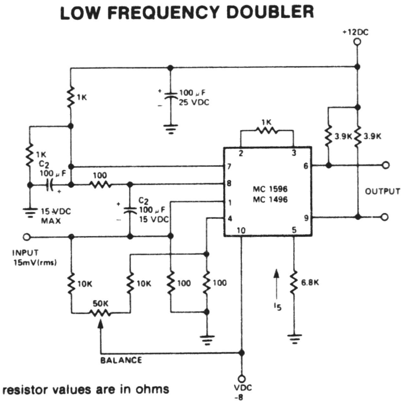

PHASE DETECTOR ± VOLTAGES
VCO
INPUT
φ = 90°
0 VDC AVERAGE
φ = 0°
+ VDC AVERAGE
φ = 180°
- VDC AVERAGE

Figure 9

PHASE DETECTOR

The versatility of the balanced modulator or multiplier also allows the device to be used as a phase detector. As mentioned, the output of the detector contains a term related to the cosine of the phase angle. Two signals of equal frequency are applied to the inputs as per Figure 8. The frequencies are multiplied together producing the sum and difference frequencies. Equal frequencies cause the difference component to become dc while the undesired sum component is filtered out. The dc component is related to the phase angle by the graph of Figure 9. At 90 degrees the cosine becomes zero, while being at maximum positive or maximum negative at 0° and 180° respectively.

The advantage of using the balanced modulator over other types of phase comparators is the excellent linearity of conversion. This configuration also provides a conversion


LOW FREQUENCY DOUBLER
+12DC
1K
100 μF 25 VDC
1K
3.9K
3.9K
1K
C_2 100 μF
100
C_2 100 μF 15 VDC
15 VDC MAX
MC 1596
MC 1496
OUTPUT
INPUT 15mV(rms)
10K
10K
100
100
6.8K
50K
I_5
BALANCE
VDC -8

All resistor values are in ohms

Figure 10

gain rather than a loss for greater resolution. Used in conjunction with a phase locked loop for instance, the balanced modulator provides a very low distortion FM demodulator.

FREQUENCY DOUBLER

Very similar to the phase detector of Figure 8, a frequency doubler schematic is shown in Figure 10. Departure from Figure 8 is primarily the removal of the low pass filter. The output then contains the sum component which is twice the frequency of the input since both input signals are the same frequency.

APPLICATIONS OF LOW NOISE STEREO PREAMPLIFIERS: NE542

Introduction

Stereo preamplifiers have come into greater and greater demand with the increased usage of tape recorders. With stereophonic recording systems, the need increased to have multiple devices in the same package to insure greater thermal tracking and packing density, without sacrificing performance.

The NE542 qualifies as a low noise dual preamplifier. The NE542 is a pin dual-in-line device.

This device has greater than 100dB open loop gain and (15-20) MHz gain bandwidth product. In selecting the proper "low noise" preamplifier several factors must be considered.

I Frequency shaping characteristic required.
II Closed loop response with respect to a system reference level.
III Response of the record/playback head.
IV System distortion requirements.
V Response of the tape used.

The following will deal with items I, II, IV.

When approaching the design criteria of Item 2, the designer should be concerned with the open loop device characteristics. These characteristcs will aid in determining the maximum boost available, knowing that a specific loop gain (open loop gain minus closed loop gain) will be necessary to keep the system distortion low and maintain the output impedance of the "low noise" preamplifier constant over the required operating frequency range.

RIAA standards call for a maximum recording velocity of 21cm/sec for stereo discs. This worst case velocity describes a bound for the preamplifier gain because the input signal at this velocity is maximum.

NAB TAPE EQUALIZATION

Recording and playback characteristics of magnetic tape and record/playback heads are not flat but exhibit a loss at high frequencies and a boost at lower frequencies. To obtain an overall flat frequency response and improved signal to noise ratio, the audio signals are equalized by boosting the higher frequencies in amplitude before recording. Playback amplifiers must exhibit bass boost to remove the effects of pre-emphasis for an overall flat response. Known as the NAB equalization curve, the standard deemphasis employs attenuation from the turnover frequency of 50Hz to the turnover frequency of 3180Hz for 7 1/2 Ips recording. The slower recording speed of 3.75 Ips employs turnover frequencies of 50Hz and 1326Hz. These curves are shown in Figure 1. A reference level of 800μV head sensitivity at 1kHz is also used by the NAB.

STEREO PREAMPLIFICATION

The voltage level appearing at the output of tape playback heads and some phono cartridges are too small to be useful without a large amount of low noise preamplification. In addition to providing low noise amplification, the preamplifier should possess enough open loop gain so that the RIAA and NAB equalization curves can be produced in the feedback networks of the amplifier. The following paragraphs describe the characteristics and applications of the 542. This device provides a matched pair of amplifiers which have been specifically designed to minimize amplifier noise and maximize signal to noise ratio.

542 DEVICE DESCRIPTION

The NE542 is a dual low noise amplifier with 104dB open loop gain produced by two stages of voltage gain followed by one stage of current gain.

In the design of low noise devices special attention must be focused on the input stage. If differential topography is used, the stage should be designed so that one of the differential transistors is turned off. This reduces the noise contribution by a factor of 1.4 since only one transistor is producing noise. Current sources and mirrors cannot be used for biasing loads because active elements will contribute more noise.

Implementing these observations, the first gain stage of the 542 is pictured with the complete schematic by Figure 2.

TAPE EQUALIZATION CURVES

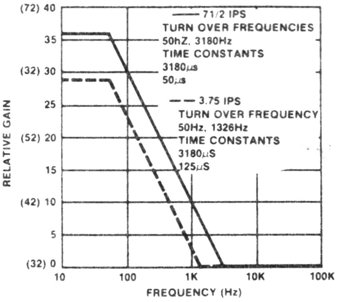
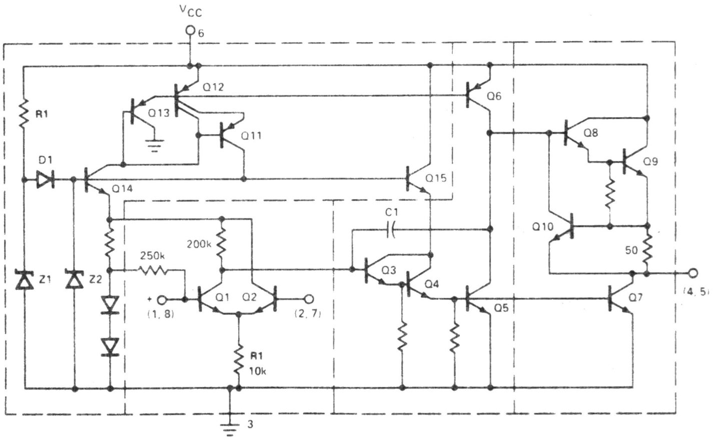


Figure 1

EQUIVALENT SCHEMATIC NE542



All resistor values are in ohms

Figure 2

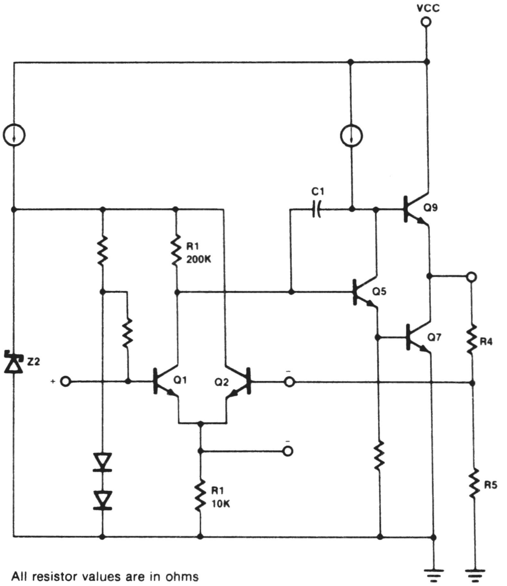
APPLICATIONS OF LOW NOISE STEREO AMPLIFIERS: NE542

Although the differential input configuration degrades the noise performance slightly, using differential inputs has the advantages of higher input impedance, allowing smaller capacitors and larger resistors to be used to achieve the RIAA and NAB curves.

The second stage is a common-emitter amplifier (Q5) with a current source load (Q6). The Darlington emitter-follower Q3-Q4 provides level shifting and current gain to the common-emitter stage (Q5) and the output current sink (Q7). The voltage gain of the second stage is approximately 2000 making the total gain of the amplifier typically 160,000 in the differential input configuration.

The preamplifier is internally compensated with the pole-splitting capacitor, C1. This compensates to unity gain at 15MHz. The compensation is adequate to preserve stability to a closed loop gain of 10.

DIFFERENTIAL INPUT BIASING NE542



All resistor values are in ohms

Figure 3

BIASING

The non-inverting input has been internally biased from a 1.4 Volt internal voltage source. Following the zero differential rule of amplifiers, the output voltage will be set by the resistor feedback network (R4 and R5) of Figure 3.

The base of Q2 requires 0.5µA bias current. Hence R5 should pass 5µA minimum for stability, for an output dc voltage of $\frac{V_{CC}}{2}$ the values of R4 and R5 are:

$$R5 = \frac{2\,V_{BE}}{10\,I_B} = 240K\text{ Max.} \qquad (1)$$

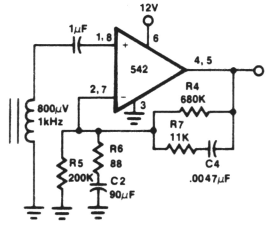
$$R4 = \left(\frac{V_{CC}}{2.8 - 1}\right) R5 \qquad (2)$$

DC amplifier gain is defined by the ratio of R4 and R5. Open loop ac gain can be regained by adding a shunt capacitor across R5. The low frequency 3dB corner is then defined by the capacitor-resistor break point.

NAB Tape Preamplifier

Design of a preamplifier begins by determining the gain and output signal amplitudes in reference to the standard 800µV input signal level. For the following design example, we will use the 542 to achieve a 100mV output level at 1kHz following the 7-1/2 Ips NAB equalization curve. The graph of Figure 1 has been calibrated both in absolute gain for this example and relative gain for general use.

NAB RESPONSE AMPLIFIER



All resistor values are in ohms

Figure 4

From the given parameters, the closed loop gain becomes 32dB at the highest frequency of interest. The NAB response is achieved by adding frequency selective ac feedback as depicted by Figure 4. Resistors R4 and R5 select the dc gain as defined by Equations 1 and 2. Placing a value of 200K upon R5, Equation 2 yields a value of 680K ohms.

The lower corner frequency is determined next by the reactance of C4 and R4 such that:

$$f_1 = \frac{.159}{C4\ R4} \qquad (3)$$

Solving for C4 yields a value of .0047µfd.

The upper corner frequency, f_2, is similarly fixed by the reactance of C4 and R7.

$$f_2 = \frac{.159}{C4\ R7} \qquad (4)$$

Then solving Equation 4 for R7 defines a value of 11k ohms.

Midband gain is now fixed by the relationship.

$$A = \frac{R6 + R7}{R6} \qquad (5)$$

Solving for the 1kHz gain of 42dB using 11k for R7 yields a value of 88 ohms for R6. The final calculation of the low frequency cut off of the preamp determines the size of C2.

$$C2 = \frac{.159}{f_{CUTOFF}\ R6} \qquad (6)$$

Typical Applications

In addition to the previous detailed design examples, the following general amplifier configurations (see Figures 5 through 8) are presented. The choice of design and the device used is a function of the desired complexity and overall performance.

APPLICATIONS OF LOW NOISE STEREO AMPLIFIERS: NE542

AN190

FLAT RESPONSE TAPE AMPLIFIER

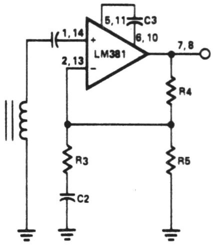

5, 11
C3
1, 14
+
6, 10
LM381
7, 8
2, 13
−
R4
R3
R5
C2

Figure 5

TWO-POLE FAST TURN-ON NAB TYPE PREAMP

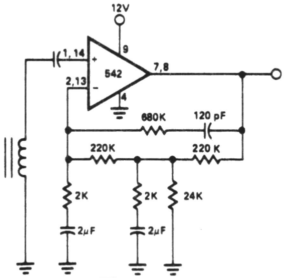
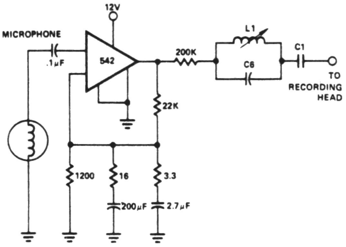

12V
1, 14
+
9
542
7, 8
2, 13
−
4
680K
120 pF
220K
220 K
2K
2K
24K
2μF
2μF

Figure 6

TYPICAL NAB RECORD PREAMPLIFIER


12V
MICROPHONE
.1μF
542
200K
L1
C1
C6
TO
RECORDING
HEAD
22K
1200
16
3.3
200μF
2.7μF

All resistor values are in ohms

Figure 7

TYPICAL TAPE PLAYBACK AMPLIFIER

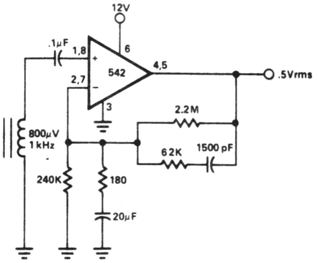

12V
.1μF
1,8
+
6
542
4,5
.5Vrms
2,7
−
3
2.2M
800μV
1 kHz
62K
1500 pF
240K
180
20μF

Figure 8

STEREO DECODER APPLICATIONS USING THE μA758 AN191

STERO DECODER APPLICATIONS: μA758

Introduction

The phase locked loop (PLL) has been used for many years in consumer equipment. Due to the nature of FM STEREO MULTIPLEX SYSTEMS, where prime importance is the channel separation, discrete systems lacked the tracking ability over wide temperature and voltage ranges to be done economically.

The development of the monolithic PLL and improvements in IC processing has made the Phase Locked Loop FM Stereo Multiplexer Decoder a reality.

Major Advantages

The economic advantages in using the PLL multiplex decoding system are not only cost reduction, by eliminating peripheral components, but the man hour cost reduction by eliminating turning coils, thereby eliminating tedious alignment procedures.

The cost advantages are extremely significant and are in addition to the following:

- 45 dB Channel Separation
- Automatic Stereo/Mono Switching
- Stereo Indicator Lamp Driver With Current Limiting
- High Impedance Input—Low Impedance Outputs
- 70dB SCA Rejection (Subsidiary Carrier Authorization)
- One Adjustment for Complete Alignment
- 10V to 16V Supply Voltage Range

FM Stereo Multiplex Subcarrier and Pilot

The two (2) basic signals differentiating an FM stereo multiplex signal from an FM monaural signal are the 19kHz pilot and the 38kHz subcarrier. The frequency and phase relationship of these signals is well defined.

Earlier systems had to reconstruct the 38kHz subcarrier by using the 19kHz pilot. This system required frequency multipliers and selective filters (coils). Since maximum channel separation is directly related to proper phasing, alignment procedures were extremely critical and therefore expensive. In addition, long term stability and performance were degraded due to component aging, and temperature.

Use of the PLL as the multiplex decoder eliminated these short comings since the phase accuracy of the 38kHz signal is limited only by the loop gain of the system and the free running oscillator stability. Both of these parameters are easily controlled, providing easy, rapid adjustment and excellent long term stability.

General Description

The μA758 is a monolithic Phase Locked Loop FM Stereo Multiplex decoder using the 16-Lead DIP N Package. This integrated circuit decodes an FM Stereo Multiplex Signal into Right and Left audio channels while inherently suppressing SCA information when it is contained in the composite input signal. Internal functions include automatic mono-stereo mode switching and drive for an external lamp to indicate stereo mode operation.

The μA758 operates over a wide supply voltage range and uses a low number of external components. It has only one control to adjust a potentiometer to set oscillator frequency. No external coils are required. The μA758 is suitable for all line-operated and automotive FM Stereo Receivers.

Referencing The Block Diagram

The upper row of blocks comprises the PLL which regenerates the 38kHz subcarrier, necessary for multiplex signal demodulation. The basic 76kHz generator is voltage controlled, and is divided by 2 to insure a 50% duty cycle 38kHz internally generated signal. This symmetry is necessary for maximum left/right channel separation and SCA rejection (band centered at 67kHz). Dividing the 38kHz by 2 generates the 19kHz signal necessary to lock on to the incoming pilot signal. A second 19kHz signal is generated which is in quadrature to the first internally generated 19kHz signal and in phase with the pilot. This second 19kHz is mixed in a quadrature (synchronous) phase detector to operate the stereo switch and lamp driver circuitry.

When a stereo signal is present, the stereo switch enables the stereo demodulator and when a stereo signal is not present the demodulator is disabled allowing the system to reach optimum noise performance.

Functional Operation

To aid in understanding the system operation, the μA758 equivalent circuit has been broken down into subsections as follows. Reference Figure 2.

I	Buffer Amplifier and Bias Supplies
II	Demodulator
III	Stereo Switch and Lamp Driver
IV	Voltage Controlled Oscillator
V	Frequency Dividers
VI	Pilot Phase and Amplitude Defectors

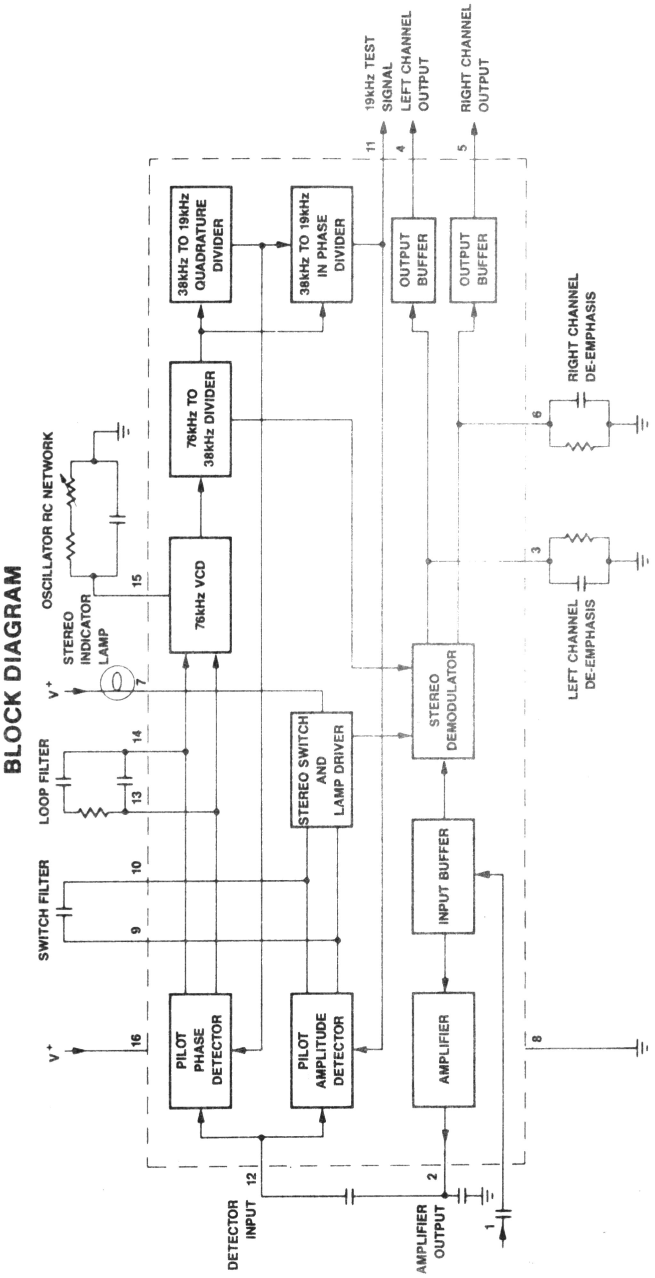

BLOCK DIAGRAM
V+
16
SWITCH FILTER
9
10
LOOP FILTER
13
14
V+
STEREO INDICATOR LAMP
7
OSCILLATOR RC NETWORK
15
PILOT PHASE DETECTOR
PILOT AMPLITUDE DETECTOR
AMPLIFIER
STEREO SWITCH AND LAMP DRIVER
INPUT BUFFER
76kHz VCO
76kHz TO 38kHz DIVIDER
STEREO DEMODULATOR
38kHz TO 19kHz QUADRATURE DIVIDER
38kHz TO 19kHz IN PHASE DIVIDER
OUTPUT BUFFER
OUTPUT BUFFER
11
4
5
19kHz TEST SIGNAL
LEFT CHANNEL OUTPUT
RIGHT CHANNEL OUTPUT
3
6
LEFT CHANNEL DE-EMPHASIS
RIGHT CHANNEL DE-EMPHASIS
8
12
2
1
DETECTOR INPUT
AMPLIFIER OUTPUT

Figure 1

STEREO DECODER APPLICATIONS USING THE μA758

SIGNETICS LINEAR INTEGRATED CIRCUITS • μA758

Equivalent Circuit

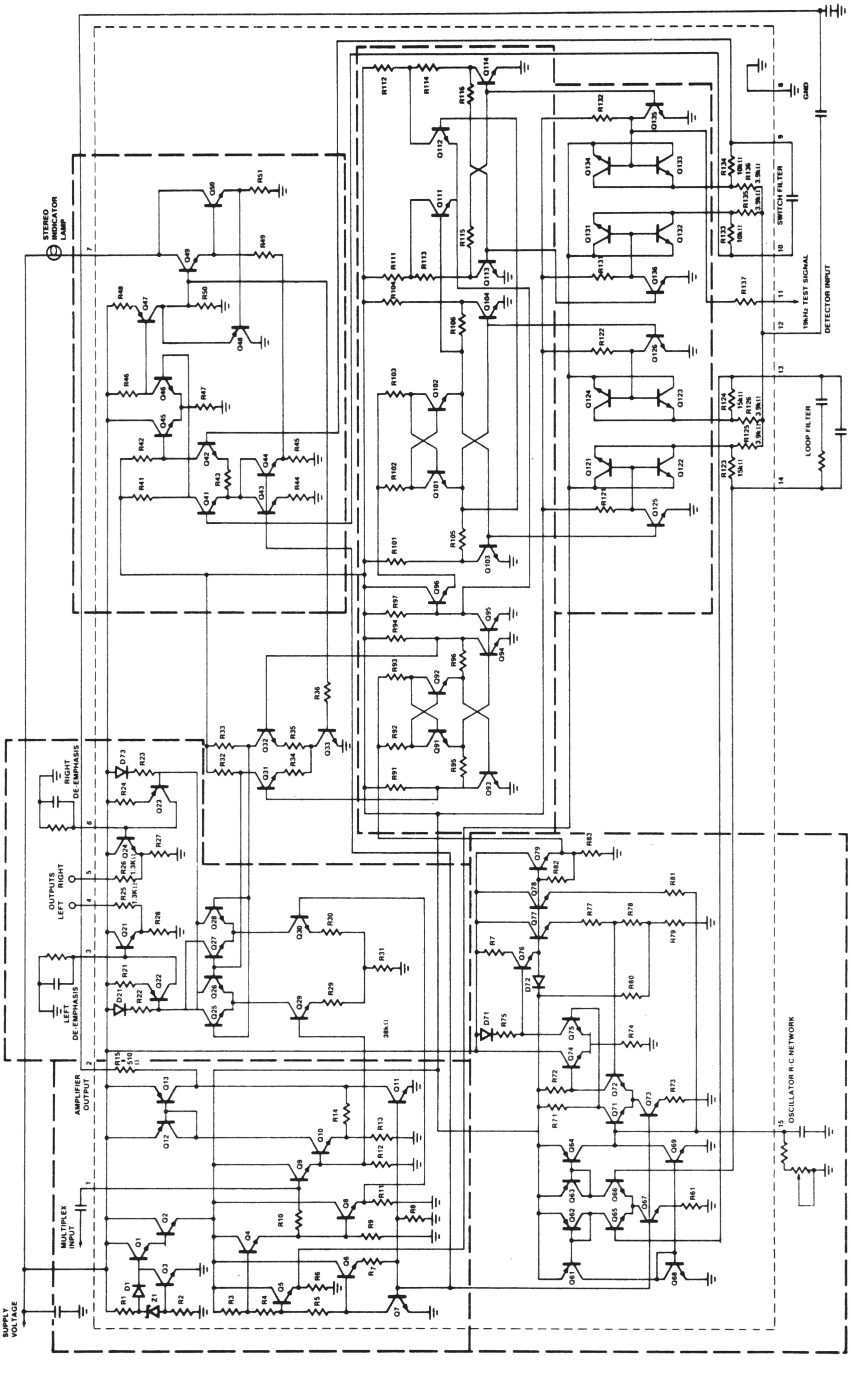

SUPPLY VOLTAGE
MULTIPLEX INPUT
AMPLIFIER OUTPUT
LEFT DE-EMPHASIS
OUTPUTS LEFT RIGHT
RIGHT DE-EMPHASIS
STEREO INDICATOR LAMP
GND
SWITCH FILTER
19kHz TEST SIGNAL
DETECTOR INPUT
LOOP FILTER
OSCILLATOR R-C NETWORK
R15 510Ω
R25 1.3kΩ
R26 1.3kΩ
38kΩ
R133 10kΩ
R134 10kΩ
R135 3.9kΩ
R136 3.9kΩ
R123 15kΩ
R124 15kΩ
R125 3.9kΩ
R126 3.9kΩ
1
2
3
4
5
6
7
9
10
11
12
13
14
15

Figure 2

STEREO DECODER APPLICATIONS USING THE µA758

I Buffer Amplifier and Bias Supplies (Figure 3)

The zener diode Z, and its associated transistors generate a 6V internal voltage reference source. From this 6V reference, additional bias levels are established via resistors R3, R4, and R5. In addition transistor Q7 acts as the control source for several current mirrors; Q11 in the Buffer Amplifier, Q43 and Q44 in the Stereo Switch and Lamp Driver (III) and Q67 and Q73 in the Voltage Controlled Oscillator (IV).

The input Buffer Amplifier (Q8, Q9) level shifts the composite multiplex input signal to 2 levels each in phase with each other.

Transistors Q10 - Q13 amplify this same signal by the ratio of:

$$A = \frac{R_{14}}{R_{13}}$$

This amplified signal, the gain of which is independent of supply voltage variation, is fed to the Pilot Phase and Amplitude Detectors (VI).

II Demodulator (Figure 4)

The basic demodulator, Q25 - Q30, is a fully balanced detector similar to standard phase locked loop types. The addition of resistors R29, R30, and R31 introduces a small offset to allow a small multiplex signal in the collector of Q30. This signal compensates the cross talk components inherent to the synchronous switching demodulation process.

Switching to the left and right channels is accomplished through Q25 and Q26 when the 38kHz drive is present at their bases. This occurs when Q33 is "ON." When Q33 is off, a dc bias is placed at the bases of Q25 and Q26 through resistors R32 and R33, this automatically converts the system to monophonic operation.

Supply voltage rejection is accomplished at the demodulator outputs by converting the audio to current supplies in Q23 and Q24. The voltage developed across pnp transistors is

$$V_e = (V^+ + V_{mod}) - (V_{be} + V_{D1} + \left[R22\ i_{ac}\right] + V_{mod})$$

where V_{be} = base-emitter voltage across Q22 and Q23

V_{mod} = modulation on the power line

V_{D1} = diode drop in D21

$(R22)i_{ac}$ = voltage drop due to current in the demodulator

Simplifying the above reduces to

$$V_e = V^+ - (V_{be} + V_{D1} + R22\ i_{ac}) \qquad (1)$$

The output voltage developed is

INPUT BUFFER/AMPLIFIER AND BIAS SUPPLY

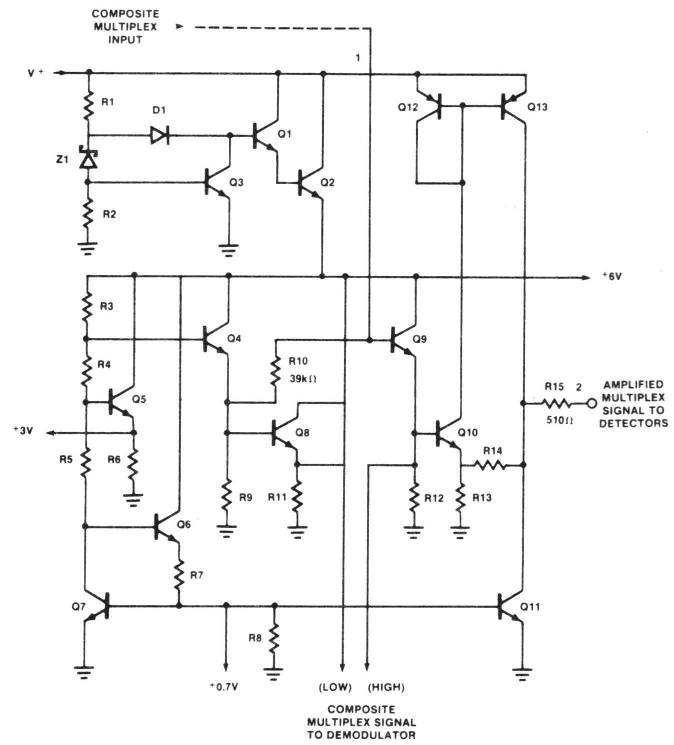

COMPOSITE MULTIPLEX INPUT
1
V+
R1
D1
Z1
R2
Q1
Q2
Q3
Q12
Q13
+6V
R3
Q4
R4
Q5
+3V
R5
R6
R10
39kΩ
Q8
Q9
Q10
R14
R15 2
510Ω
AMPLIFIED MULTIPLEX SIGNAL TO DETECTORS
R9
R11
R12
R13
Q6
R7
Q7
R8
Q11
+0.7V
(LOW)
(HIGH)
COMPOSITE MULTIPLEX SIGNAL TO DEMODULATOR

Figure 3

DEMODULATOR

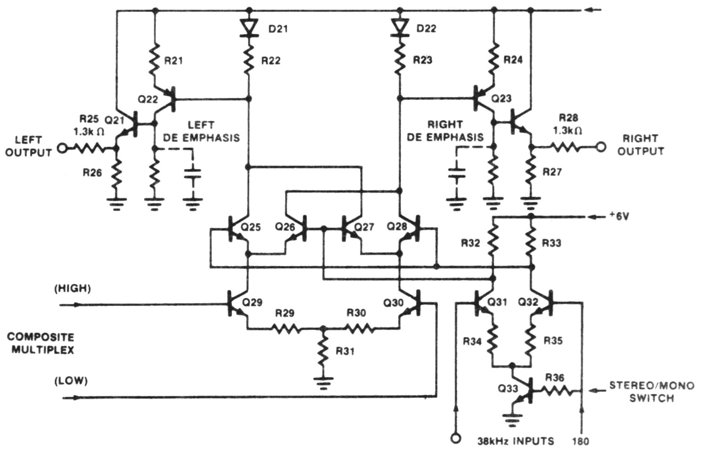

D21
D22
R21
R22
R23
R24
Q22
Q23
R25 1.3k Ω
Q21
LEFT OUTPUT
LEFT DE EMPHASIS
RIGHT DE EMPHASIS
R28 1.3kΩ
RIGHT OUTPUT
R26
R27
+6V
Q25
Q26
Q27
Q28
R32
R33
(HIGH)
Q29
R29
R30
Q30
Q31
Q32
COMPOSITE MULTIPLEX
R31
R34
R35
(LOW)
Q33
R36
STEREO/MONO SWITCH
38kHz INPUTS
180

Figure 4

STEREO DECODER APPLICATIONS USING THE μA758 AN191

$$V_{out} = \left(\frac{V_e}{R21}\right) R_{ext} \quad (2)$$

where R_{ext} = external resistor

The output voltage at pins 4 and 5 are provided through 1.3k resistors driven by Emitter Followers Q21 and Q24.

III Stereo Switch and Lamp Driver (Figure 5)

The pilot amplitude detector differential voltage is sensed by the differential amplifier Q41 and Q42. This pair in conjunction with their load resistors (R41, R42) control amplifiers Q45, Q46. Positive feedback action is achieved through Q47, R50, Q50 and R46 (which turns off Q44).

The turn on threshold is the differential input voltage required to overcome the offset voltage in R43 times the current summation of I_{R44} and I_{R45}. When the lamp is ON, Q44 is off and the differential voltage across R43 is reduced by the amount ($I_{R45} \times R_{43}$), which means a lower turn off voltage is required. This voltage difference is referred to as the switch hysteresis.

Transistors Q48 senses the current across R51 which therefore controls the maximum current in the Stereo Indicator Lamp.

$$I_{max} = \frac{V_{be}\ Q48}{R151} \quad (3)$$

STEREO SWITCH AND LAMP DRIVER

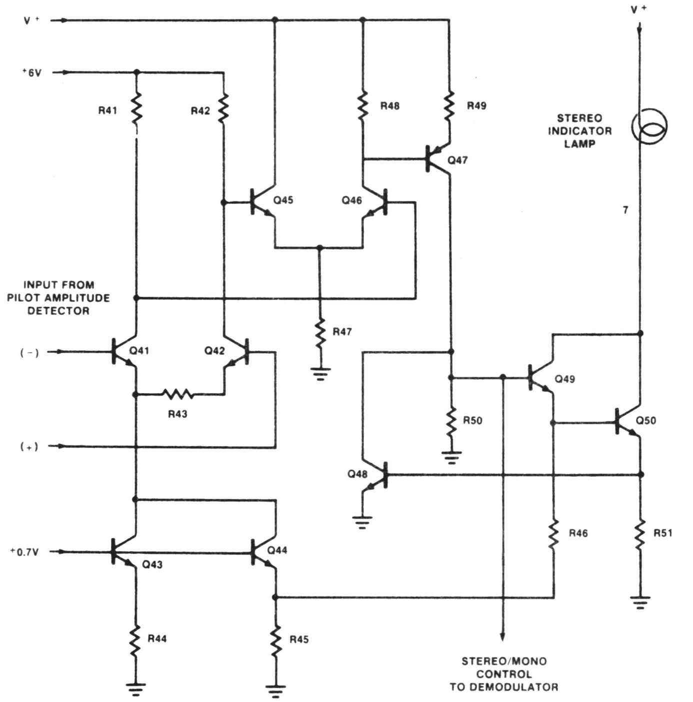

V+
+6V
R41
R42
R48
R49
V+
STEREO INDICATOR LAMP
Q47
Q45
Q46
7
INPUT FROM PILOT AMPLITUDE DETECTOR
R47
(−)
Q41
Q42
Q49
R43
R50
Q50
(+)
Q48
R46
R51
+0.7V
Q44
Q43
R44
R45
STEREO/MONO CONTROL TO DEMODULATOR

Figure 5

IV Voltage Controlled Oscillator (Figure 6)

The basic oscillator Q71-Q79 is an RC relaxation type which generates a positive low duty cycle, 76kHz output. The frequency is established by equations 4 and 5.

The control voltage from the phase detector into the transconductance amplifier Q61 - Q69 converts the differential error to a bidirectional single ended current drive to the oscillator.

Voltage on the capacitor is compared with the set voltages by the differential input stage Q71, Q72. This feeds Q74, Q75. The output of Q75 drives a PNP inverter, Q76, (whose action eliminates power supply modulation as described in the demodulator section of this note), when these set limits are reached the direction of charge reverses.

VOLTAGE CONTROLLED OSCILLATOR (VCO)

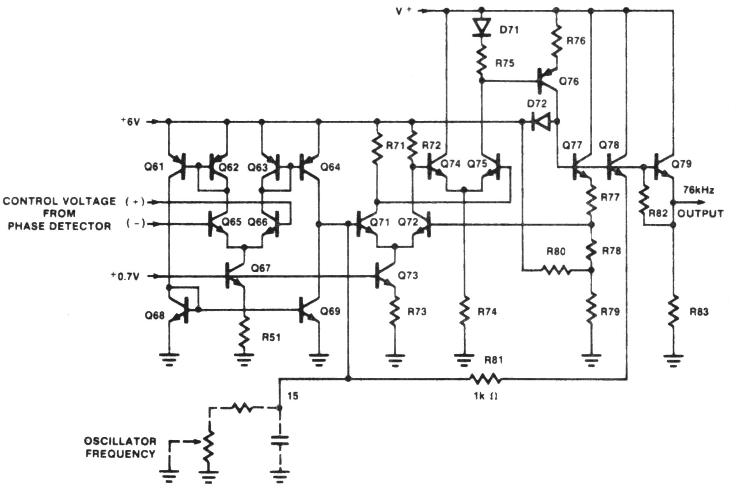

V+
D71
R76
R75
Q76
D72
+6V
R71
R72
Q77
Q78
Q61
Q62
Q63
Q64
Q74
Q75
Q79
76kHz
CONTROL VOLTAGE (+)
FROM PHASE DETECTOR (−)
Q65
Q66
Q71
Q72
R77
R82
OUTPUT
R80
R78
+0.7V
Q67
Q73
Q68
Q69
R73
R74
R79
R83
R51
R81
15
1k Ω
OSCILLATOR FREQUENCY

Figure 6

Lower set voltage is set by R79, R80, and the regulated 6V supply. The upper set voltage (V_H) involves two (2) additional resistors R77 and R78 and is established when Q76 turns on Q77. Both set levels are referenced to the regulated 6V supply and are therefore dependent only on resistor ratios. (Proper design layout should also eliminate temperature variations.)

Capacitor charging is through Q78 and R8 and discharging through the external fixed resistor.

Equations 4 and 5 of Figure 7 are first order expressions for the change and discharge periods.

Q79 supplies a positive output pulse necessary to operate the 38kHz dividers.

V Frequency Dividers (Figure 8)

Transistors Q91 through Q94 form a simple divide-by-two circuit which converts the pulse output from the 76kHz oscillator to a 38kHz square wave.

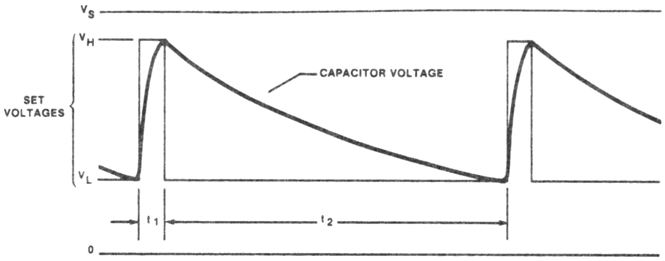
The divider changes state during the positive excursion of the input pulse supplied from the emitter of Q79 in the oscillator. Initially, when the input is low, Q91 and Q92 are OFF and we may arbitrarily assume Q93 is ON and Q94 is OFF.

As the potential on the input rises, Q91 starts conduction before Q92 because the emitter of Q91 is at a lower potential than the emitter of Q92. (The emitter of Q91 is connected through R95 to the collector of Q93 which is in saturation, whereas the emitter of Q92 is at the $V_{BE(ON)}$ potential of Q93). Since Q91 is ON, the current from both R92 and R93 flows through the emitter of Q91 into R95. As this current increases, the rising voltage at the emitter of Q91 turns Q94 ON which removes base drive to Q93 and turns it OFF, thus producing a change of state in the divider. Even though the relative potentials at the emitters of Q91 and Q92 are now reversed, current continues to flow in Q91 for the duration of the positive input because Q92 is held OFF by Q91. When the input returns to a low potential, Q91 turns OFF. The divider remains in its present state until driven by the next positive going input.

Oppositely phased 38kHz outputs to the demodulator are taken from the collectors of Q93 and Q94. Transistors Q95 and Q96 are used to drive the two 38kHz dividers.

The 38kHz Quadrature Divider has an identical configuration to the 76kHz divider. A change of state occurs with each positive excursion of the 38kHz input signal from the emitter of Q96.

OSCILLATOR WAVEFORMS



Basic timing equations:

(Equation 4)

$$t1 = R81\ C\ \ln \frac{V_s - V_L}{V_s - V_H}$$

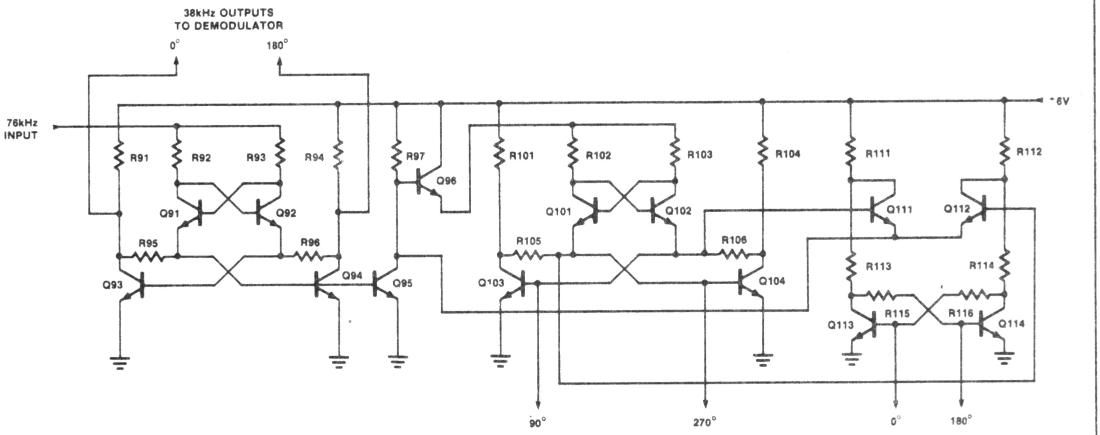
(Equation 5)

$$t2 = RC\ \ln \frac{V_H}{V_L}$$

where R and C are external components on Lead 15, R81 is on the chip, and V_H and V_L are set voltages which are a fixed percentage of V_s, the internally regulated 6 Volt supply.

Figure 7

FREQUENCY DIVIDERS



19kHz outputs to pilot amplitude and phase detectors.

Figure 8

The 38kHz In-Phase divider contains a bistable pair, Q113 and Q114, steered by inputs into Q111 and Q112, (a 38kHz input from the collector of Q95, and 19kHz inputs from the bases of Q103 and Q104). If the 19kHz input to the base of Q111 is high when the 76kHz divider turns Q95 ON, Q111 conducts and removes drive to Q114, changing the state of the bistable pair, Q113 and Q114. The bistable remains in this state until the next 38kHz turn on of Q95 which, this time, turns Q112 ON, removes drive to Q113 and resets the bistable pair. The resulting 19kHz output from Q113 and Q114 is at 90 degrees to the Quadrature Divider output with no ambiguity in phasing.

Pilot Phase and Amplitude Detectors

The pilot phase detector and pilot amplitude detector as shown in Figure 9 are synchronous, balanced chopper types which develop differential output signals across external filters. Back-to-back NPN transistor pairs are used for each switch to insure minimum drop regardless of signal polarity without reliance on inverse NPN beta characteristics.

The chopper transistors (Q121 through Q124), in the phase detector are driven from the 38kHz Quadrature Divider through transistors Q125 and Q126. The input signal is supplied from lead 12 through resistors R125 and R126. A differential output is developed across the loop filter, comprised of resistors R123 and R124 and the external R-C network between leads 13 and 14.

The pilot amplitude detector (Q131 through Q136), has an identical configuration to the phase detector. Since it operates with drive which is in phase with the pilot signal (90 degrees from the drive to the phase detector), its output is proportional to the amplitude of the pilot component of the multiplex signal. The differential output at leads 9 and 10 is filtered by the external capacitor on these two leads.

A reference 19kHz square wave signal is taken from the collector of drive transistor Q136 through resistor R137 to lead 11. It has the same phasing as the pilot contained in the multiplex input signal.

PILOT PHASE AND AMPLITUDE DETECTORS

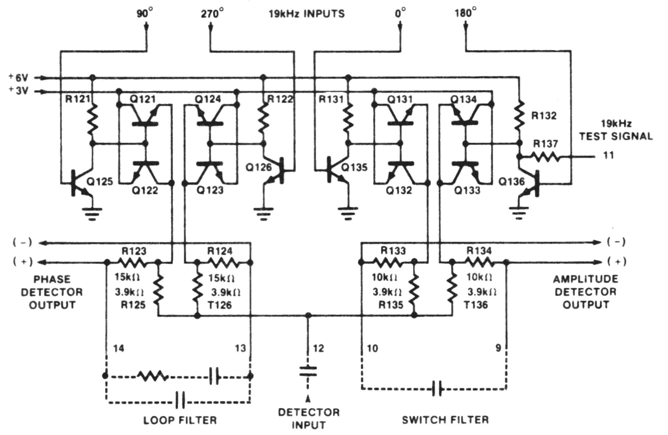
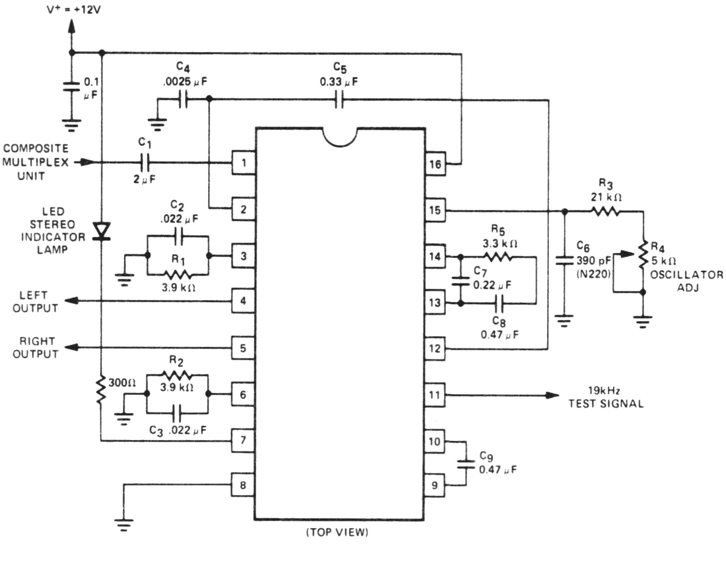

90°
270°
19kHz INPUTS
0°
180°
+6V
+3V
R121
Q121
Q124
R122
R131
Q131
Q134
R132
19kHz TEST SIGNAL
R137
11
Q125
Q122
Q123
Q126
Q135
Q132
Q133
Q136
(−)
(+)
R123
R124
R133
R134
PHASE DETECTOR OUTPUT
15kΩ
3.9kΩ
R125
15kΩ
3.9kΩ
T126
10kΩ
3.9kΩ
R135
10kΩ
3.9kΩ
T136
AMPLITUDE DETECTOR OUTPUT
14
13
12
10
9
LOOP FILTER
DETECTOR INPUT
SWITCH FILTER

Figure 9

TEST CIRCUIT 1 AND TYPICAL APPLICATION


V+ = +12V
0.1 μF
C4 .0025 μF
C5 0.33 μF
COMPOSITE MULTIPLEX UNIT
C1 2 μF
LED STEREO INDICATOR LAMP
C2 .022 μF
R1 3.9 kΩ
LEFT OUTPUT
RIGHT OUTPUT
R2 3.9 kΩ
300Ω
C3 .022 μF
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
R3 21 kΩ
R5 3.3 kΩ
C7 0.22 μF
C8 0.47 μF
C6 390 pF (N220)
R4 5 kΩ OSCILLATOR ADJ
19kHz TEST SIGNAL
C9 0.47 μF
(TOP VIEW)

NOTE

Tolerance on resistors is ±5% and tolerance on capacitors is ±20% unless otherwise specified.
C1 Tolerance = + 100%, −20%
C6 Tolerance = ±1% in test circuit and ±5% in typical application
R3 Tolerance = ±1%
R4 Tolerance = ±10%
R1 and R2 Tolerances = ±1% in test circuit and ±5% in typical application.

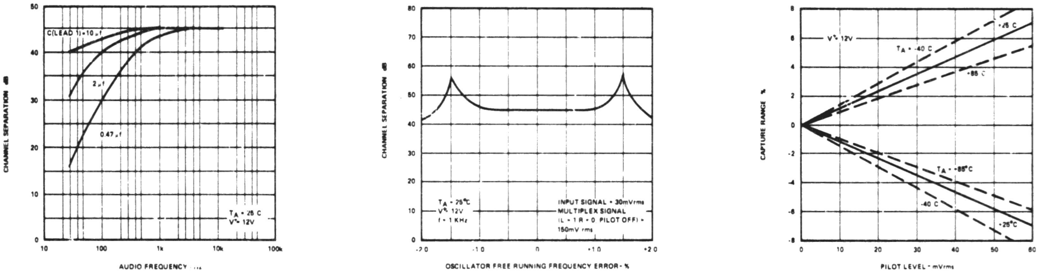
Figure 10

TYPICAL PERFORMANCE CURVES FOR 758
(Test Circuit 1 unless Otherwise Specified)

CHANNEL SEPARATION AS A FUNCTION OF AUDIO FREQUENCY

CHANNEL SEPARATION AS A FUNCTION OF OSCILLATOR FREE RUNNING FREQUENCY ERROR

CAPTURE RANGE AS A FUNCTION OF PILOT LEVEL



TOTAL HARMONIC DISTORTION AS A FUNCTION OF INPUT LEVEL

LAMP TURN ON AND TURN OFF SENSITIVITY AS A FUNCTION OF AMBIENT TEMPERATURE

OSCILLATOR FREE RUNNING FREQUENCY ERROR AS A FUNCTION OF AMBIENT TEMPERATURE

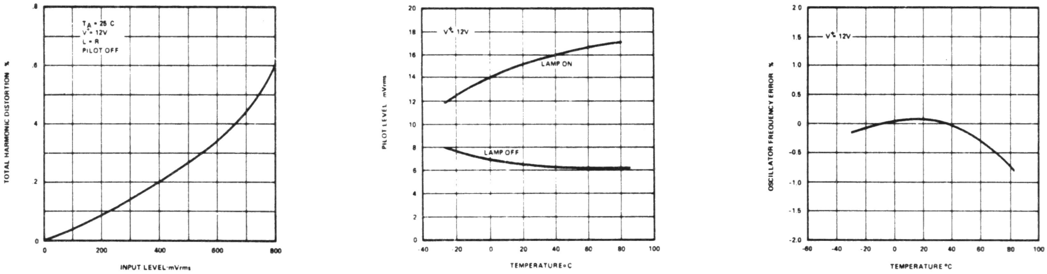


Figure 11

APPLICATIONS FOR COMPANDORS: NE570/571/SA571 AN174

APPLICATIONS

The following circuits will illustrate some of the wide variety of applications for the NE570.

BASIC EXPANDOR

Figure 1 shows how the circuit would be hooked up for use as an expandor. Both the rectifer and ΔG cell inputs are tied to V_{in} so that the gain is proportional to the average value of (V_{in}). Thus, when V_{in} falls 6dB, the gain drops 6dB and the output drops 12dB. The exact expression for the gain is

$$\text{Gain exp.} = \frac{2\,R_3\,V_{in}\,(ave)}{R_1\,R_2\,I_B}\ ;\ I_B = 140\mu A$$

The maximum input that can be handled by the circuit in Figure 1 is a peak of 3V. The rectifier input current can be as large as $I = 3V/R_1 = 3V/10K = 300\mu A$. The ΔG cell input current should be limited to $I = 2.8V/R_2 = 2.8V/20K = 140\mu A$. If it is necessary to handle larger input voltages than $0 \pm 2.8V$ pk, external resistors should be placed in series with R_1 and R_2 to limit the input current to the above values.

Figure 1 shows a pair of input capacitors C_{in1} and C_{in2}. It is not necessary to use both capacitors if low level tracking accuracy is not important. It R_1 and R_2 are tied together and share a common capacitor, a small current will flow between the ΔG cell summing node and the rectifier summing node due to offset voltages. This current will produce an error in the gain control signal at low levels, degrading tracking accuracy.

The output of the expandor is biased up to 3V by the dc gain provided by R_3, R_4. The output will bias up to

$$V_{out}\,dc = (1 + \frac{R_3}{R_4})\quad V_{ref}$$

For supply voltages higher than 6V, R_4 can be shunted with an external resistor to bias the output up to $1/2V_{CC}$.

Note that it is possible to externally increase R_1, R_2, and R_3, and to decrease R_3 and R_4. This allows a great deal of flexibility in setting up system levels. If larger input signals are to be handled, R_1 and R_2 may be increased; if a larger output is required, R_3 may be increased. To obtain the largest dynamic range out of this circuit, the rectifier input should always be as large as possible (subject to the ±300μA peak current restriction).

BASIC COMPRESSOR

Figure 2 shows how to use the NE570/571 as a compressor. It functions as an expandor in the feedback loop of an op amp. If the input rises 6dB, the output can rise only 3dB. The 3dB increase in output level produces a 3dB increase in gain in the ΔG cell, yielding a 6dB increase in feedback current to the summing node. Exact expression for gain is

$$\text{Gain comp} = \left[\frac{R_1\,R_2\,I_B}{2\,R_3\,V_{in}\,(ave)}\right]^{1/2}$$

The same restrictions for the rectifier and ΔG cell maximum input current still hold, which place a limit on the maximum compressor output. As in the expandor, the rectifier and ΔG cell inputs could be made common to save a capacitor, but low level tracking accuracy would suffer. Since there is no dc feedback path around the op amp through the ΔG cell, one must be provided externally. The pair of resistors R_{dc} and the capacitor C_{dc} must be provided. The op amp output will bias up to

$$V_{out}\,dc = (1 + \frac{2\,R_{dc}}{R_4})\ V_{ref}$$

For the largest dynamic range, the compressor output should be as large as possible so that the rectifier input is as large as possible (subject to the ±300μA peak current restriction). If the input signal is small, a large output can be produced by reducing R_3 with the attendant decrease in input impedance, or by increasing R_1 or R_2. It would be best to increase R_2 rather than R_1 so that the rectifier input current is not reduced.

BASIC EXPANDOR

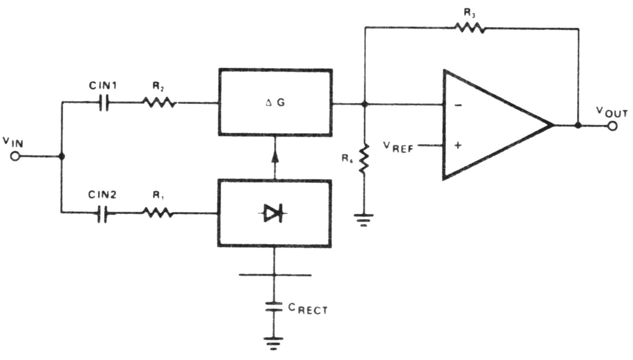


Figure 1

BASIC COMPRESSOR

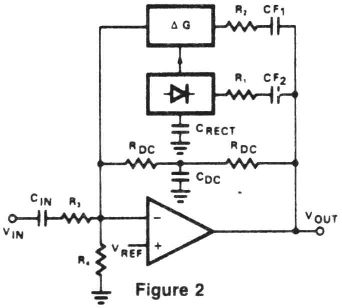


Figure 2

DISTORTION TRIM

Distortion can be produced by voltage offsets in the ΔG cell. The distortion is mainly even harmonics, and drops with decreasing input signal. (Input signal meaning the current into the ΔG cell.) The THD trim terminal provides a means for trimming out the offset voltages and thus trimming out the distortion. The circuit shown in Figure 3 is suitable, as would be any other capable of delivering ±30μA into 100Ω resistor tied to 1.8V.

THD TRIM NETWORK

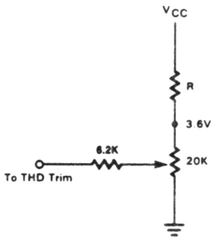


Figure 3

LOW LEVEL MISTRACKING

The compandor will follow a 2 to 1 tracking ratio down to very low levels. The rectifier is responsible for errors in gain, and it is the rectifier input bias current of <100na that produces errors at low levels. The magnitude of the error can be estimated. For a full scale rectifier input signal of ±200μA, the average input current will be 127μA. When the input signal level drops to a 1μA average, the bias current will produce a 10% or 1dB error in gain. This will occur at 42dB below the maximum input level.

It is possible to deviate from the 2 to 1 transfer characteristic at low levels as shown in the circuit of Figure 4. Either R_a or R_b, (but not both), is required. The voltage on C_{rect} is $2 \times V_{be}$ plus V_{in} ave. For low level inputs V_{in} ave is negligible, so we can assume 1.3V as the bias on C_{rect}. If R_a is placed from C_{rect} to gnd we will bleed off a current $I = 1.3V/R_a$. If the rectifer average input current is less than this value, there will be no gain control input to the ΔG cell so that its gain will be zero and the expandor output will be zero. As the input level is raised, the input current will exceed $1.3V/R_a$ and the expandor output will become active. For large input signals, R_a will have little effect. The result of this is that we will deviate from the 2 to 1 expansion, present at high levels, to an infinite expansion, at low levels where the output shuts off completely. Figure 5 shows some examples of tracking curves which can be obtained. Complementary curves would be obtained for a compressor, where at low level signals the result would be infinite compression. The bleed current through R_a will be a function of temperature because of the two V_{be} drops, so the low level tracking will drift with temperature. If a negative supply is available, it would be desirable to tie R_a to that, rather than ground, and to increase its value accordingly. The bleed current will then be less sensitive to the V_{be} temperature drift.

R_b will supply an extra current to the rectifier equal to $(V_{CC} - 1.3V)R_b$. In this case, the expandor transfer characteristic will deviate towards 1 to 1 at low levels. At low levels the expandor gain will stop dropping and the expansion will cease. In a compressor this would lead to a lack of compression at low levels. Figure 6 shows some typical transfer curves. An R_b value of approximately 2.5Meg would trim the low level tracking so as to match the Bell system N2 trunk compandor characteristic.

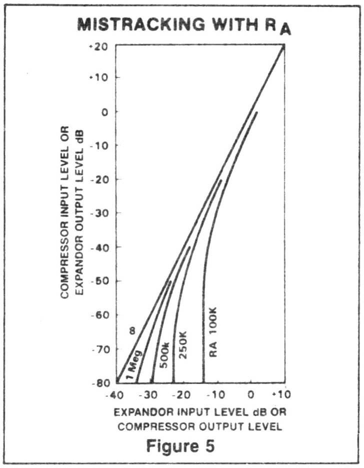


Figure 5

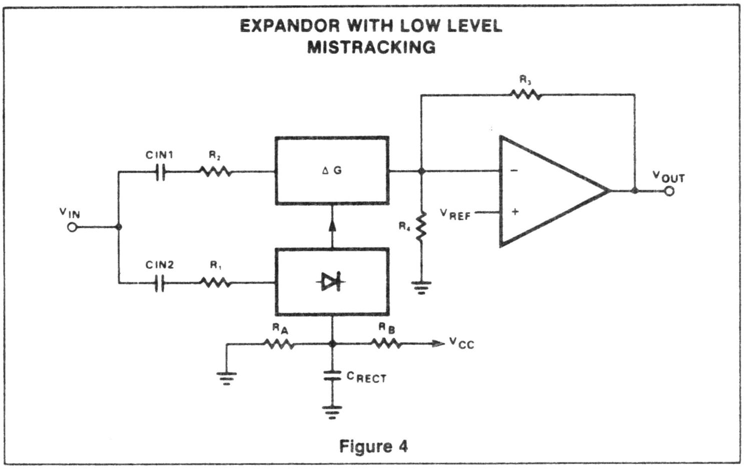


Figure 4

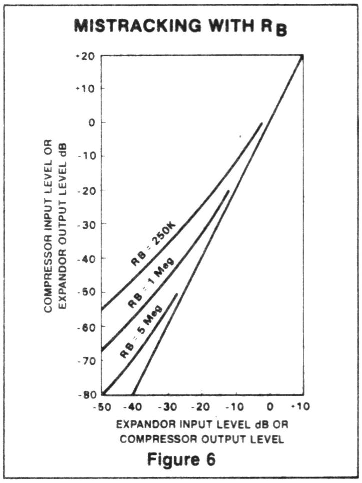


Figure 6

RECTIFIER BIAS CURRENT CANCELLATION

The rectifier has an input bias current of between 50 and 100na. This limits the dynamic range of the rectifier to about 60dB. It also limits the amount of attenuation of the ΔG cell. The rectifier dynamic range may be increased by about 20dB by the bias current trim network shown in Figure 7. Figure 8 shows the rectifier performance with and without bias current cancellation.

ATTACK AND DECAY TIME

The attack and decay times of the compandor are determined by the rectifier filter time constant $10K \times C_{rect}$. Figure 9 shows how the gain will change when the input signal undergoes a 10, 20, or 30dB change in level.

The attack time is much faster than the decay, which is desirable in most applications. Figure 10 shows the compressor attack envelope for a + 12dB step in input level. The initial output level of 1 unit instantaneously rises to 4 units, and then starts to fall towards its final value of 2 units. The CCITT recommendation on attack and decay times for telephone system compandors defines the attack time as when the envelope has fallen to a level of 3 units, corresponding to t = .15 in the figure. The CCITT recommends an attack time of 3 ± 2ms, which suggests an RC product of 20ms. Figure 11 shows the compressor output envelope when the input level is suddenly reduced 12dB. The output, initially at a level of 4 units, drops 12dB to 1 unit and then rises to its final value of 2 units. The CCITT defines release time as when the output has risen to 1.5 units, and suggests a value of 13.5

RECTIFIER BIAS CURRENT COMPENSATION

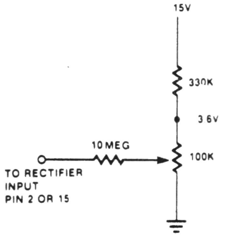


Figure 7

RECTIFIER PERFORMANCE WITH Ib COMPENSATION

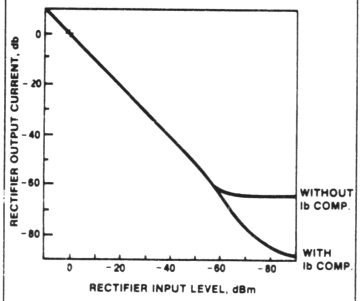


Figure 8

GAIN vs TIME FOR INPUT STEPS OF ± 10, ± 20, ± 30dB

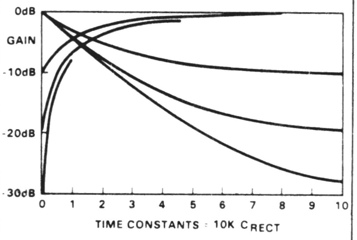


Figure 9

COMPRESSOR ATTACK ENVELOPE +12dB STEP

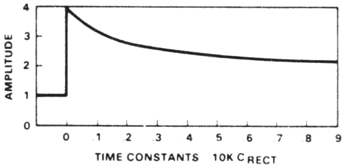


Figure 10

COMPRESSOR RELEASE ENVELOPE -12dB STEP

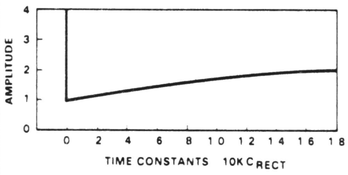


Figure 11

± 9ms. This corresponds to t = .675 in the figure, which again suggests a 20ms RC product. Since $R_1 = 10K$, the CCITT recommendations will be met if $C_{rect} = 2\mu F$.

There is a trade-off between fast response and low distortion. If a small C_{rect} is used to get very fast attack and decay, some ripple will appear on the gain control line and produce distortion. As a rule, a $1\mu F$ C_{rect} will produce .2% distortion at 1kHz. The distortion is inversely proportional to both frequency and capacitance. Thus, for telephone applications where $C_{rect} = 2\mu F$, the ripple would cause .1% distortion at 1kHz and .33% at 300Hz. The low frequency distortion generated by a compressor would be cancelled (or undistorted) by an expandor, providing that they have the same value of C_{rect}.

FAST ATTACK, SLOW RELEASE HARD LIMITER

The NE570/571 can be easily used to make an excellent limiter. Figure 12 shows a typical circuit which requires ½ of an NE570/571, ½ of an LM339 quad comparator, and a pnp transistor. For small signals, the ΔG cell is nearly off, and the circuit runs at unity gain as set by R_8, R_7. When the output signal tries to exceed a + or − 1V peak, a comparator threshold is exceeded. The pnp is turned on and rapidly charges C_4 which activates the ΔG cell. Negative feedback through the ΔG cell reduces the gain and the output signal level. The attack time is set by the RC product of R_{18} and C_4, and the release time is determined by C_4 and the internal rectifier resistor, which is 10K. The circuit shown attacks in less than 1ms and has a release time constant of 100ms. R_9 trickles about $.7\mu A$ through the rectifier to prevent C_4 from becoming completely discharged. The gain cell is activated when the voltage on pin 1 or 16 exceeds two diode drops. If C_4 were allowed to become completely discharged, there would be a slight delay before it recharged to > 1.2V and activated limiting action.

A stereo limiter can be built out of 1 NE570/571, 1 LM339 and two pnp transistors. The resistor networks R_{12}, R_{13} and R_{14}, R_{15}, which set the limiting thresholds, could be common between channels. To gang the stereo channels together (limiting in one channel will produce a corresponding gain change in the second channel to maintain the balance of the stereo image), then pins 1 and 16 should be jumpered together. The outputs of all 4 comparators may then be tied together, and only one pnp transistor and one capacitor C_4 need be used. The release time will then be the product $5K \times C_4$ since two channels are being supplied current from C_4.

USE OF EXTERNAL OP AMP

The operational amplifiers in the NE570/571 is not adequate for some applications. The slew rate, bandwidth, noise, and output drive capability can limit performance in many systems. For best performance, an external op amp can be used. The external op amp may be powered by bipolar supplies for a larger output swing.

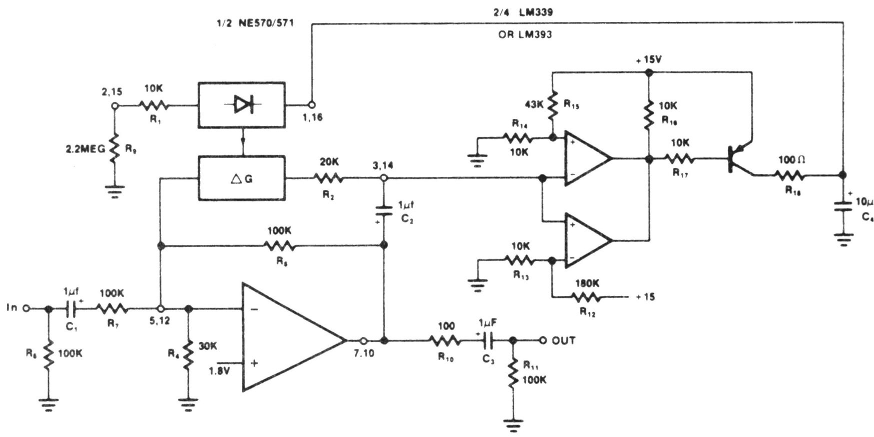
Figure 13 shows how an external op amp may be connected. The non-inverting input must be biased at about 1.8V. This is easily accomplished by tying it to either pin 8 or 9, the THD trim pins, since these pins sit at 1.8V. An optional RC decoupling network is shown which will filter out the noise from the NE570/571 reference (typically about $10\mu V$ in 20kHz BW). The inverting input of the external op amp is tied to the inverting input of the internal op amp. The output of the external op amp is then used, with the internal op amp output left to float. If the external op amp is used single supply ($+V_{CC}$ and ground), it must have an input common mode range down to less than 1.8V.

N2 COMPANDOR

There are four primary considerations involved in the application of the NE570/571 in an N2 compandor. These are matching of input and output levels, accurate 600Ω input and output impedances, conformance to the Bell system low level tracking curve, and proper attack and release times.

Figure 14 shows the implementation of an N2 compressor. The input level of .245V rms is stepped up to 1.41V rms by the 600Ω: 20KΩ matching transformer. The 20K input resistor properly terminates the transformer. An internal 20KΩ resistor (R_3) is provided, but for accurate impedance termination an external resistor should be used. The output impedance is provided by the 4K output resistor and the 4KΩ: 600Ω output transformer. The .275V rms output level requires a 1.4V op amp out-

FAST ATTACK, SLOW RELEASE HARD LIMITER


1/2 NE570/571
2/4 LM339
OR LM393
+15V
2,15
10K
R1
2.2MEG R9
1,16
ΔG
20K
R2
3,14
1μf
C2
100K
R8
43K R15
R14
10K
10K R16
10K R17
100Ω R18
10μf C4
10K R13
180K R12
+15
1μf
C1
100K R7
In
5,12
R6 100K
R4 30K
1.8V
7,10
100 R10
1μF C3
OUT
R11 100K

+15V Pin 13
GND Pin 4
R1, R2, R4 are internal to the NE570/571.

Figure 12

USE OF EXTERNAL OP AMP

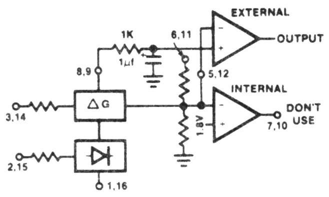

EXTERNAL
OUTPUT
1K
6,11
1μf
8,9
5,12
INTERNAL
3,14
ΔG
DON'T USE
7,10
1.8V
2,15
1,16

Figure 13

N2 COMPRESSOR

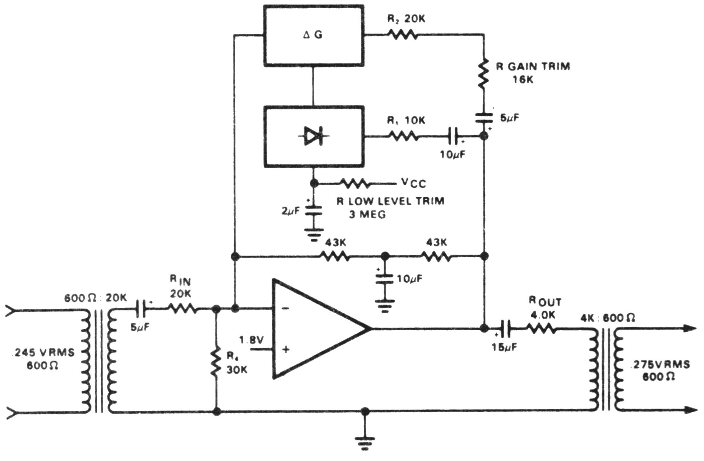

ΔG
R2 20K
R GAIN TRIM 16K
R1 10K
5μF
10μF
VCC
R LOW LEVEL TRIM 3 MEG
2μF
43K
43K
10μF
RIN 20K
600Ω : 20K
5μF
245 VRMS 600Ω
1.8V
R4 30K
ROUT 4.0K
4K : 600Ω
15μF
275VRMS 600Ω

Figure 14

put level. This can be provided by increasing the value of R_2 with an external resistor, which can be selected to fine trim the gain. A rearrangement of the compressor gain equation (6) allows us to determine the value for R_2.

$$R_2 = \frac{Gain^2 \times 2 R_3 V_{in}\,ave}{R_1 I_B} = \frac{12 \times 2 \times 20K \times 1.27}{10K \times 140\mu A} = 36.3K$$

The external resistance required will thus be 36.3K - 20K = 16.3K

The Bell compatible low level tracking characteristic is provided by the low level trim resistor from C_{rect} to V_{CC}. As shown in Figure 6, this will skew the sytem to a 1:1 transfer characteristic at low levels. The 2μF rectifier capacitor provides attack and release times of 3ms and 13.5ms respectively, as shown in Figures 10 and 11. The R-C-R network around the op amp provides dc feedback to bias the output at dc.

An N2 expandor is shown in Figure 15. The input level of 3.27V RMS is stepped down to 1.33V by the 600Ω: 100Ω transformer, which is terminated with a 100Ω resistor for accurate impedance matching. The output impedance is accurately set by the 150Ω output resistor and the 150Ω: 600Ω output transformer. With this configuration the 3.46V transformer output requires a 3.46V op amp output. To obtain

N2 EXPANDOR

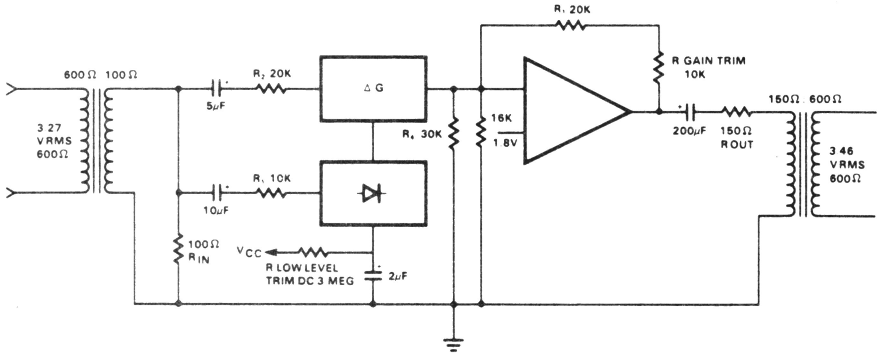


Figure 15

this output level, it is necessary to increase the value of R_3 with an external trim resistor. The new value of R_3 can be found with the expandor gain equation

$$R_3 = \frac{R_1\ R_2\ I_B\ \text{Gain}}{2\ V_{IN}\ \text{avg}} = \frac{10K \times 20K \times 140\mu A \times 2.6}{2 \times 1.20} = 30.3K$$

An external addition to R_3 of 10K is required, and this value can be selected to accurately set the high level gain.

A low level trim resistor from C_{rect} to V_{CC} of about 3Meg provides matching of the Bell low level tracking curve, and the 2μF value of C_{rect} provides the proper attack and release times. A 16K resistor from the summing node to ground biases the output to 7V dc.

VOLTAGE CONTROLLED ATTENUATOR

The variable gain cell in the NE570/571 may be used as the heart of a high quality voltage controlled amplifier (VCA). Figure 16 shows a typical circuit which uses an external op amp for better performance, and an exponential converter to get a control characteristic of – 6dB/V. Trim networks are shown to null out distortion and dc shift, and to fine trim gain to 0dB with zero volts of control voltage.

Op amp A_2 and transistors Q_1 and Q_2 form the exponential converter generating an exponential gain control current, which is fed into the rectifier. A reference current of 150μA, (15V and R_{20} = 100K), is attenuated a factor of two (6dB) for every volt increase in the control voltage. Capacitor C_6 slows down gain changes to a 20ms time constant (C_6 x R_1) so that an abrupt change in the control voltage will produce a smooth sounding gain change. R_{18} assures that for large control voltages the circuit will go to full attenuation. The rectifier bias current would normally limit the gain reduction to about 70dB. R_{18} draws excess current out of the rectifier. After approximately 50dB of attenuation at a -6dB/V slope, the slope steepens and attenuation becomes much more rapid until the circuit totally shuts off at about 9 volts of control voltage. A_1 should be a low noise high slew rate op amp. R_{13} and R_{14} establish approximately a zero volt bias at A_1's output.

With a zero volt control voltage, R_{19} should be adjusted for 0dB gain. At 1V (-6dB gain) R_9 should be adjusted for minimum distortion with a large (+10dBm) input signal. The output dc bias (A_1 output) should be measured at full attenuation (+10V control voltage) and then R_8 is adjusted to give the same value at 0dB gain. Properly adjusted, the circuit will give typically less than .1% distortion at any gain with a dc output voltage variation of only a few millivolts. The clipping level (140μA into pin 3, 14) is ±10V peak. A signal to noise ratio of 90dB can be obtained.

If several VCA's must track each other, a common exponential converter can be used. Transistors can simply be added in parallel with Q_2 to control the other channels. The transistors should be maintained at the same temperature for best tracking.

AUTOMATIC LEVEL CONTROL

The NE570 can be used to make a very high performance ALC as shown in Figure 17. This circuit hookup is very similar to the basic compressor shown in Figure 2 except that the rectifier input is tied to the input rather than the output. This makes gain inversely proportional to input level so that a 20dB drop in input level will produce a 20dB increase in gain. The output will remain fixed at a constant level. As shown, the circuit will maintain an output level of ± 1dbm for an input range of + 14 to – 43dbm at 1kHz. Additional external components will allow the output level to be adjusted. Some relevant design equations are:

$$\text{Output level} = \frac{R_1\ R_2\ I_B}{2\ R_3}\left(\frac{V_{IN}}{V_{IN}(\text{avg})}\right);\ I_B = 140\mu A$$

$$\text{Gain} = \frac{R_1\ R_2\ I_B}{2\ R_3\ V_{IN}\ (\text{avg})} \quad \text{where}$$

$$\frac{V_{IN}}{V_{IN}(\text{avg})} = 2\ \frac{\pi}{\sqrt{2}} = 1.11\ (\text{for sine wave})$$

If ALC action at very low input levels is not desired, the addition of resistor R_X will limit the maximum gain of the circuit.

$$\text{Gain max.} = \frac{\frac{R_1 + R_X}{1.8V} \times R_2 \times I_B}{2\ R_3}$$

The time constant of the circuit is determined by the rectifier capacitor, C_{rect}, and an internal 10K resistor.

$$\tau = 10K\ C_{rect}$$

Response time can be made faster at the expense of distortion. Distortion can be approximated by the equation.

$$\text{THD} = \left(\frac{1\mu F}{C_{rect}}\right)\left(\frac{1KHz}{\text{freq.}}\right) \times .2\%$$

VOLTAGE CONTROLLED ATTENUATOR

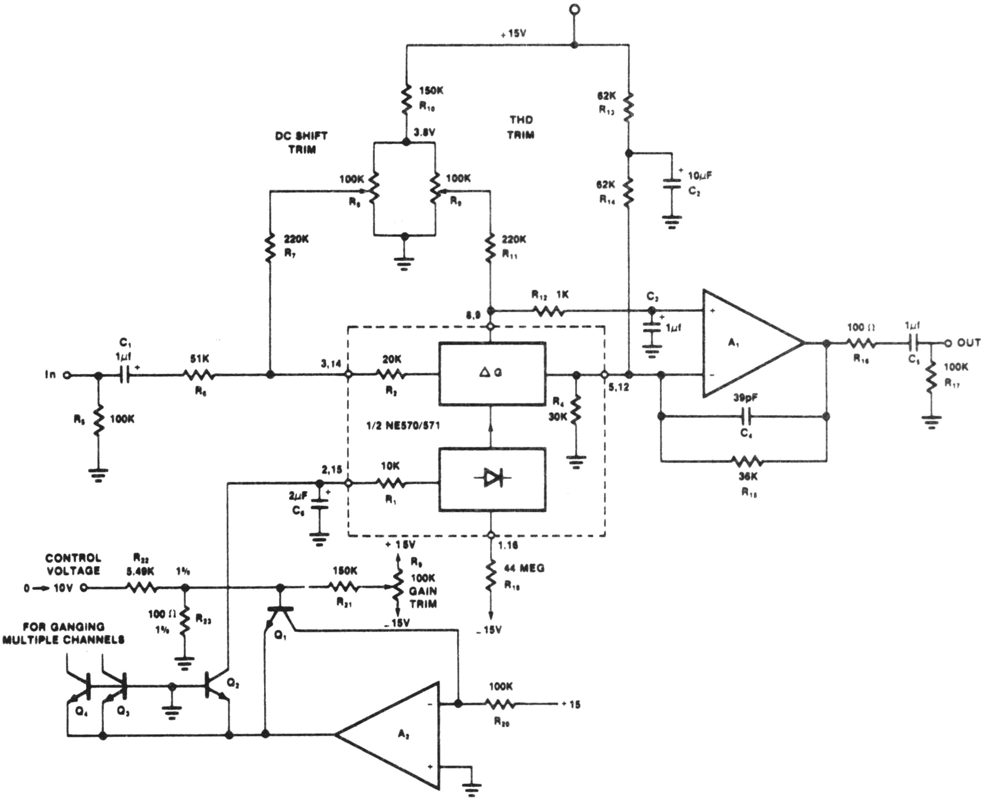

+15V
150K
R10
3.8V
DC SHIFT
TRIM
THD
TRIM
62K
R13
100K
R8
100K
R9
62K
R14
10µF
C2
220K
R7
220K
R11
R12 1K
C3
1µf
8,9
A1
100Ω
1µf
OUT
R16
C5
100K
R17
C1
1µf
In
51K
R6
3,14
20K
R2
ΔG
R4
30K
5,12
39pF
C4
36K
R15
R5
100K
1/2 NE570/571
2,15
10K
R1
2µF
C6
+15V
R9
100K
GAIN
TRIM
1.16
44 MEG
R18
CONTROL
VOLTAGE
0→10V
R22
5.49K
1%
150K
R21
-15V
-15V
100Ω
1%
R23
FOR GANGING
MULTIPLE CHANNELS
Q1
Q2
Q3
Q4
100K
R20
+15
A2

Figure 16

VARIABLE SLOPE COMPRESSOR-EXPANDOR

Compression and expansion ratios other than 2:1 can be achieved by the circuit shown in Figure 18. Rotation of the dual potentiometer causes the circuit hookup to change from a basic compressor to a basic expandor. In the center of rotation, the circuit is 1:1, has neither compression nor expansion. The (input) output transfer characteristic is thus continuously variable from 2:1 compression, through 1:1 up to 1:2 expansion. If a fixed compression or expansion ratio is desired, proper selection of fixed resistors can be used instead of the potentiometer. The optional threshold resistor will make the compression or expansion ratio deviate towards 1:1 at low levels. A wide variety of (input) output characteristics can be created with this circuit, some of which are shown in Figure 18.

HI FI COMPANDOR

The NE570 can be used to construct a high performance compandor suitable for use with music. This type of system can be used for noise reduction in tape recorders, transmission systems, bucket brigade delay lines, and digital audio systems. The circuits to be described contain features which improve performance, but are not required for all applications.

A major problem with the simple NE570 compressor (Figure 2) is the limited op amp gain at high frequencies. For weak input signals, the compressor circuit operates at high gain and the 570 op amp simply runs out of loop gain. Another problem with the 570 op amp is its limited slew rate of about .6V/µs. This is a limitation of the expandor, since the expandor is more likely to produce large output signals than a compressor.

Figure 20 is a circuit for a high fidelity compressor which uses an external op amp and has a high gain and wide bandwidth. An input compensation network is required for stability.

Another feature of the circuit in Figure 20 is that the rectifier capacitor (C_9) is not grounded, but is tied to the output of an op amp circuit. This circuit, built around an LM324, speeds up the compressor attack time at low signal levels. The response times of the simple expandor and compressor (Figures 1 and 2) become longer at low signal levels. The time constant is not simply 10K x C_{rect}, but is really

$$\left(10K + 2\left(\frac{.026V}{I_{rect}}\right)\right) x C_{rect}.$$

When the rectifier input level drops from 0dBm to -30dBm, the time constant increases from 10.7KxC$_{rect}$ to 32.6KxC$_{rect}$. In

AUTOMATIC LEVEL CONTROL

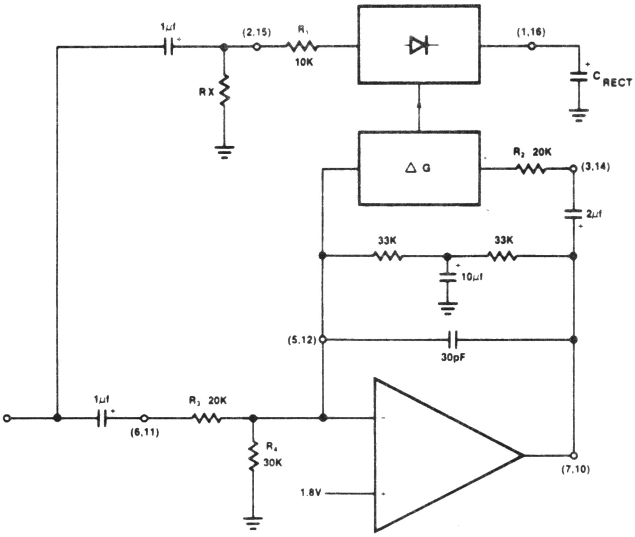

1µf
(2,15)
R1
10K
(1,16)
C RECT
RX
R2 20K
(3,14)
Δ G
2µf
33K
33K
10µf
(5,12)
30pF
1µf
R3 20K
(6,11)
R4
30K
1.8V
(7,10)

Figure 17

VARIABLE SLOPE COMPRESSOR-EXPANDOR

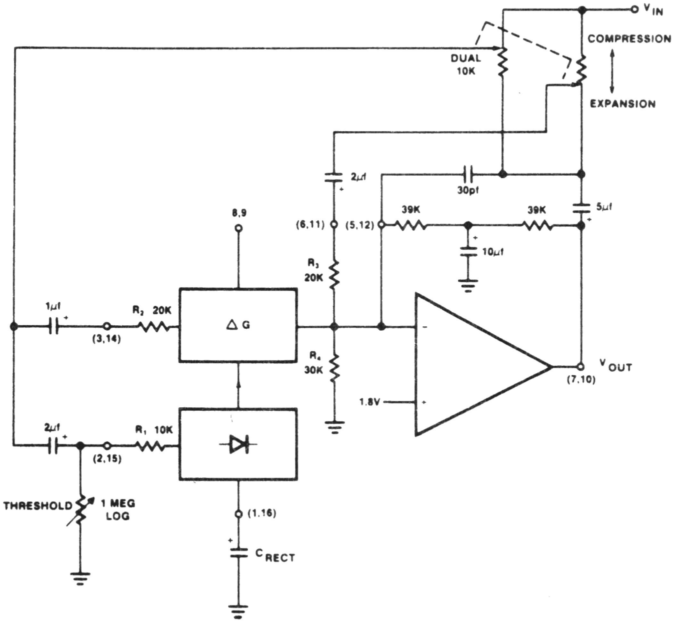

V IN
COMPRESSION
DUAL
10K
EXPANSION
2µf
30pf
5µf
8,9
39K
39K
(6,11)
(5,12)
10µf
R3
20K
1µf
R2 20K
(3,14)
Δ G
R4
30K
V OUT
(7,10)
1.8V
2µf
R1 10K
(2,15)
THRESHOLD
1 MEG
LOG
(1,16)
C RECT

Figure 18

systems where there is unity gain between the compressor and expandor, this will cause no overall error. Gain or loss between the compressor and expandor will be a mistracking of low signal dynamics. The circuit with the LM324 will greatly reduce this problem for systems which cannot guarantee the unity gain.

When a compressor is operating at high gain, (small input signal), and is suddenly hit with a signal, it will overload until it can reduce its gain. Overloaded the output will attempt to swing rail to rail. This compressor is limited to approximately a 7V peak to peak output swing by the brute force clamp diodes D_3 and D_4. The diodes cannot be placed in the feedback loop because their capacitance would limit high frequency gain. The purpose of limiting the output swing is to avoid overloading any succeeding circuit such as a tape recorder input.

The time it takes for the compressor to recover from overload is determined by the rectifier capacitor C_9. A smaller capacitor will allow faster response to transients, but will produce more low frequency third harmonic distortion due to gain modulation. A value of 1µF seems to be a good compromise value and yields good subjective results. Of course, the expandor should have exactly the same value rectifier capacitor for proper transient response. Systems which have good low frequency amplitude and phase response can use compandors with smaller rectifier capacitors, since the third harmonic distortion which is generated by the compressor will be undistorted by the expandor.

Simple compandor systems are subject to a problem known as breathing. As the system is changing gain, the change in the background noise level can sometimes be heard.

TYPICAL INPUT-OUTPUT TRACKING CURVES OF VARIABLE RATIO COMPRESSOR-EXPANDOR

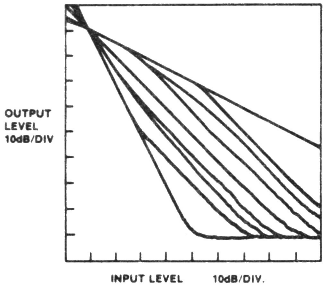


Figure 19

APPLICATIONS FOR COMPANDORS: NE570/571/SA571

The compressor in Figure 20 contains a high frequency pre-emphasis circuit (C_2, R_5 and C_8, R_{14}), which helps solve this problem. Matching de-emphasis on the expandor is required. More complex designs could make the pre-emphasis variable and further reduce breathing.

The expandor to complement the compressor is shown in Figure 21. Here an external op amp is used for high slew rate. Both the compressor and expandor have unity gain levels of 0dBm. Trim networks are shown for distortion (THD) and dc shift. The distortion trim should be done first, with an input of 0dBm at 10kHz. The dc shift should be adjusted for minimum envelope bounce with tone bursts. When applied to consumer tape recorders, the subjective performance of this system is excellent.

HI-FI COMPRESSOR WITH PRE-EMPHASIS

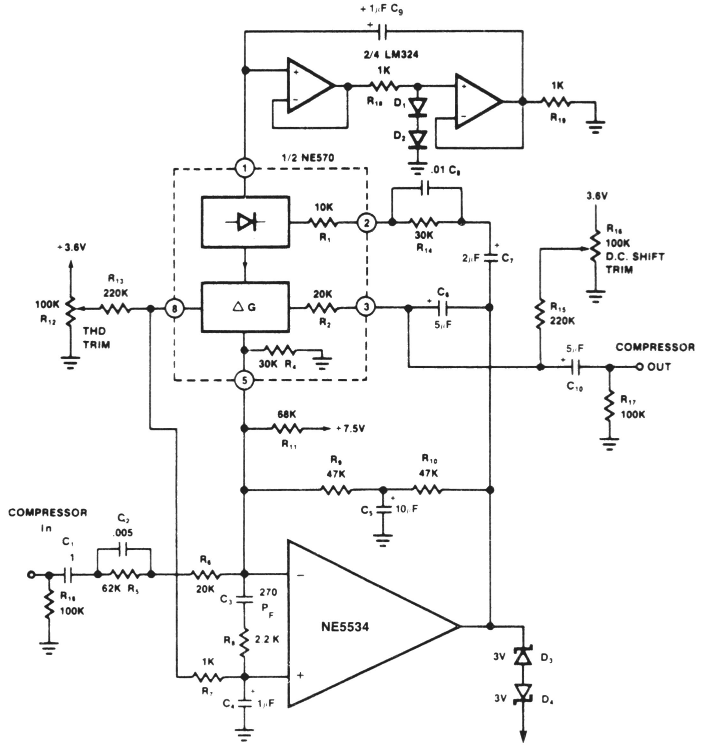
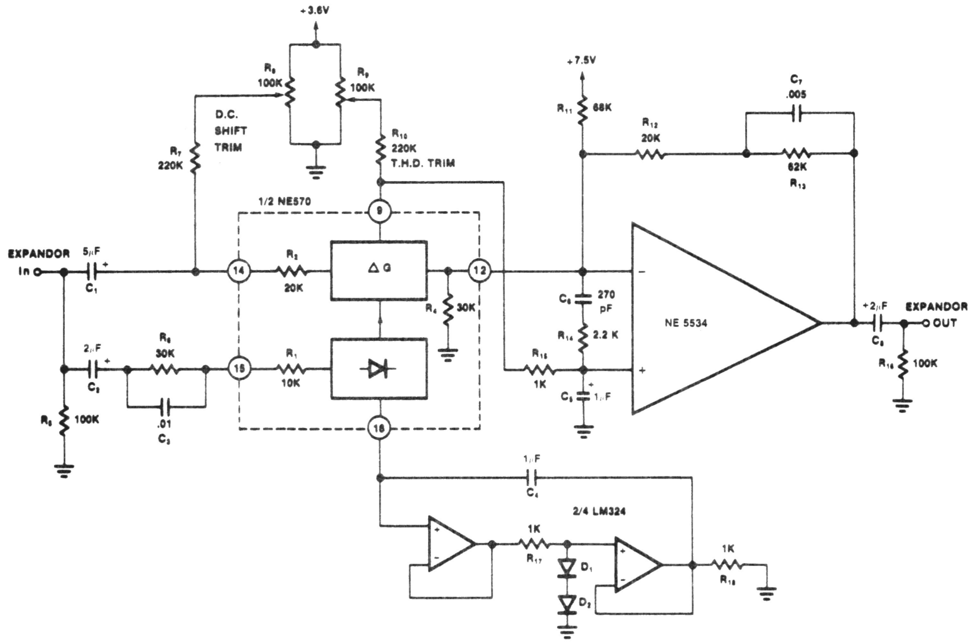

+ 1μF C9
2/4 LM324
1K
R18 D1
D2
1K
R19
1/2 NE570
.01 C8
10K
R1
30K
R14
3.6V
R16
100K
D.C. SHIFT
TRIM
+3.6V
R13
220K
100K
R12
THD
TRIM
ΔG
20K
R2
C6
5μF
2μF C7
R15
220K
30K R4
5μF
COMPRESSOR
OUT
C10
R17
100K
68K
+7.5V
R11
R9
47K
R10
47K
C5
10μF
COMPRESSOR
In
C2
.005
C1
1
62K R5
R6
20K
R18
100K
C3
270
PF
R8
2.2K
NE5534
1K
R7
C4
1μF
3V
D3
3V
D4
1
2
3
5
8

Figure 20

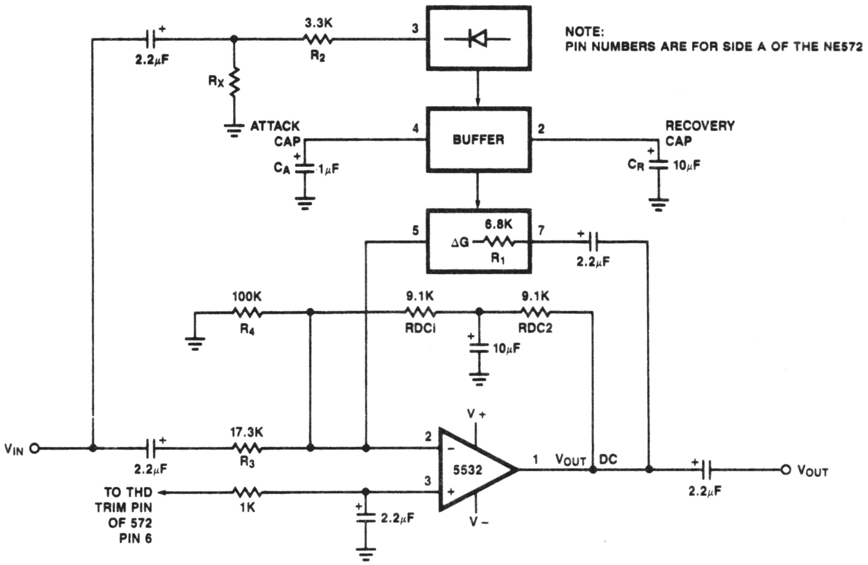

+3.6V
R8
100K
R9
100K
D.C.
SHIFT
TRIM
R7
220K
R10
220K
T.H.D. TRIM
+7.5V
R11
68K
R12
20K
C7
.005
62K
R13
1/2 NE570
9
EXPANDOR
In
5μF
C1
14
R2
20K
ΔG
12
R4
30K
C6
270
pF
R14
2.2 K
NE 5534
+2μF
EXPANDOR
OUT
C8
R16
100K
2μF
C2
R6
30K
15
R1
10K
R15
1K
C5
1μF
R5
100K
.01
C3
16
1μF
C4
2/4 LM324
1K
R17
D1
D2
1K
R18

HI-FI EXPANDOR WITH DE-EMPHASIS

Figure 21

AUTOMATIC LEVEL CONTROL: NE572 AN175

NE572 AUTOMATIC LEVEL CONTROL


2.2μF
3.3K
R2
3
Rx
ATTACK CAP
4
BUFFER
2
RECOVERY CAP
CA 1μF
CR 10μF
5
ΔG
6.8K
R1
7
2.2μF
100K
R4
9.1K
RDCi
9.1K
RDC2
10μF
V+
VIN
2.2μF
17.3K
R3
2
5532
3
1
VOUT
DC
VOUT
2.2μF
TO THD TRIM PIN OF 572 PIN 6
1K
2.2μF
V−

NOTE:
PIN NUMBERS ARE FOR SIDE A OF THE NE572

$$V_{ODC} = V_{REF}\left(1 + \frac{R_{DC1} + R_{DC2}}{R_4}\right)$$

$$\text{OUTPUT LEVEL} = \left(\frac{R_1 R_2 I_B}{2R_3}\right)\left(\frac{V_{IN}}{V_{IN(avg)}}\right)$$

WHERE: $R_4 = 100K$
$R_{DC1} = R_{DC2} = 9.1K$
$V_{REF} = 2.5V$

$$\text{GAIN} = \frac{R_1 R_2 I_B}{2R_3\ V_{IN}\ (avg)}$$

WHERE: $R_1 = 6.8K$ (Internal)
$R_2 = 3.3K$
$R_3 = 17.3K$
$I_B = 140\mu A$

ATTACK TIME = (10K) C_A

RECOVERY TIME = (10K) C_R

$$\frac{V_{IN}}{V_{IN(avg)}} = \frac{\pi}{2\sqrt{2}} = 1.11$$

(FOR SINE WAVES)

TO LIMIT THE GAIN AT VERY LOW INPUT LEVELS, ADD R_X:

$$\text{GAIN MAX.} = \frac{\frac{R_1 + R_X}{1.8V} \cdot R_2 \cdot I_B}{2R_3}$$

COMPANDOR COOKBOOK

Compandors are versatile, low cost, dual channel gain control devices for audio frequencies. They are used in tape decks, cordless telephones, and wireless microphones performing noise reduction. Electronic organs, modems and mobile telephone equipment use compandors for signal level control.

So what is companding? Why do it at all? What happens when we do it? *Compandor* is the contraction of the two words *compressor* and *expandor*. There is one basic reason to compress a signal before sending it through a telephone line or recording it on a cassette tape. It is to process that signal (music, speech, data) so that all parts of it are above the inherent noise floor of the transmission medium and yet not running into the max dynamic range limits, causing clipping and distortion. The diagrams below demonstrate the idea; they are not totally correct because in the real world of electronics the 3kHz tone is riding on the 1kHz tone. They are shown separated for better explanation.

Figure 1 is the signal from the source. Figure 2 shows the noise always in the transmission medium. Figure 3 shows the max limits of the transmission medium and what happens when a signal larger than those limits is sent through it. Figure 4 is the result of compressing the signal. (Note that the larger signal would *not* be clipped when transmitted.)

The received/playback signal is processed (expanded) in exactly the same-only inverted-ratio as the input signal was compressed. The end result is clean, undistorted signal with a high signal-to-noise ratio.

This document has been designed to give the reader a basic working knowledge of the Signetics Compandor family. The analyses of three primary applications will be accompanied by "recipes" describing how to select external components (for both proper operation and function modification). Schematic and artwork for an application board are also provided. For more comprehensive technical information consult the Compandor Product Guide or the Linear LSI Data Manual.

The basic blocks in a compandor are the current controlled variable gain cell (delta-G), voltage to current converter (rectifier), and operational amplifier. Each Signetics compandor package has two identical, independent channels with the following block diagrams (notice that the 570/71 is different from the 572):

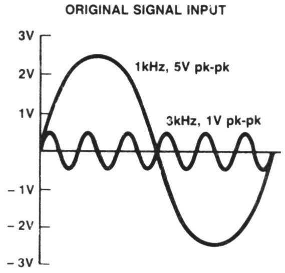


Figure 1

Figure 2

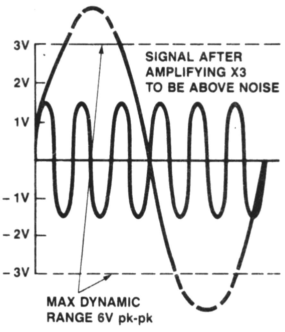


Figure 3

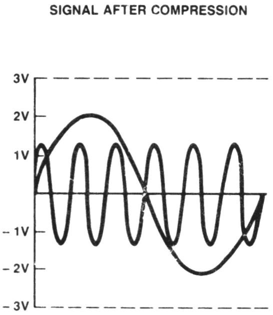
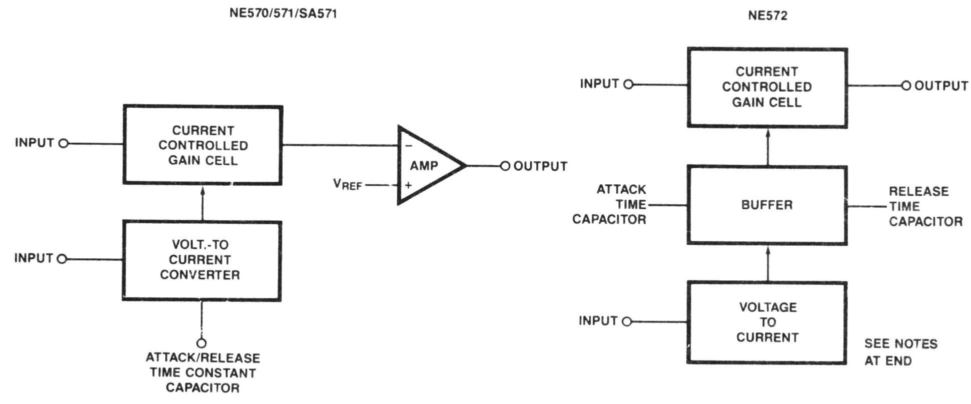


Figure 4

BLOCK DIAGRAMS


NE570/571/SA571
INPUT
CURRENT CONTROLLED GAIN CELL
AMP
VREF
OUTPUT
INPUT
VOLT.-TO CURRENT CONVERTER
ATTACK/RELEASE TIME CONSTANT CAPACITOR
NE572
INPUT
CURRENT CONTROLLED GAIN CELL
OUTPUT
ATTACK TIME CAPACITOR
BUFFER
RELEASE TIME CAPACITOR
INPUT
VOLTAGE TO CURRENT
SEE NOTES AT END

BASIC COMPRESSOR

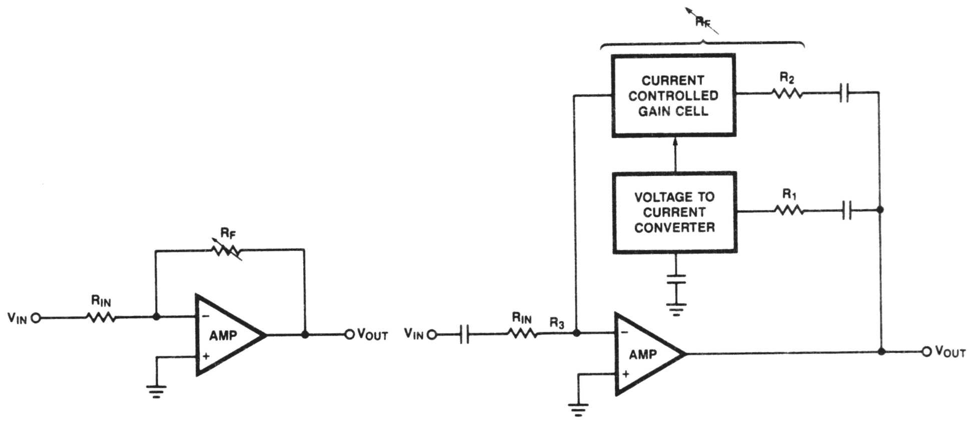


Figure 5

The operational amplifier is the main signal path and output drive.

The full wave averaging rectifier measures the AC amplitude of a signal and develops a control current for the variable gain cell.

The variable gain cell uses the rectifier control current to provide variable gain control for the operational amplifier gain block.

The compandor can function as a COMPRESSOR, EXPANDOR, and AUTOMATIC LEVEL CONTROLLER or as a complete compressor/expandor system as described in the following:

1) The COMPRESSOR function processes uncontrolled input signals into controlled output signals. The purpose of this is to avoid distortion caused by a narrow dynamic range medium such as: telephone lines, RF and satellite transmissions, and magnetic tape. The COMPRESSOR can also limit the level of a signal.
2) The EXPANDOR function allows a user to increase the dynamic range of an incoming compressed signal such as radio broadcasts.
3) The compressor/expandor system allows a user to retain dynamic range and reduce the effects of noise introduced by the transmission medium.
4) The AUTOMATIC LEVEL CONTROL (ALC) function (like the familiar automatic gain control) adjusts its gain proportionally with the input amplitude. This ALC circuit therefore transforms a widely varying input signal into a fixed amplitude output signal without clipping and distortion.

HOW TO DESIGN COMPANDOR CIRCUITS

The rest of the cookbook will provide you with basic compressor, expandor, and automatic level control application information. In all of the circuits a NE570/571 has been used. If high fidelity audio or separately programmable attack and decay time are needed, the NE572 with a low noise op-amp should be used.

The COMPRESSOR (see Figure 5) utilizes all basic building blocks of the compandor. In this configuration, the variable gain cell is placed in the feedback loop of the standard inverting amplifier circuit. The gain equation is $Av = -R_F/R_{IN}$. As shown above, the variable gain cell acts as a variable feedback resistor (R_F). (See Figure 5.)

As the input signal increases (above the crossover level of 0dBm), this variable resistor decreases in value, causing the gain to decrease, thus limiting the output amplitude.

Below the crossover level of 0dBm, an increase in input signal causes the variable resistor to increase in value thereby causing the output signal's amplitude to increase.

In the compressor configuration the rectifier is connected to the output.

The complete equation for the compressor gain is:

$$\text{Gain comp.} = \left[\frac{R_1\ R_2\ I_B}{2\ R_3\ V_{IN}(avg)}\right]^{1/2}$$

where: $R_1 = 10K$
$R_2 = 20K$
$R_3 = 20K$
$I_B = 140\mu A$
$V_{IN}(avg) = 0.9\ (V_{IN}(rms))$

COMPRESSOR RECIPE

1) DC bias the output half way between the supply and ground to get maximum headroom. The circuit in Figure 6 is designed around a system supply of 6 volts so we want the output DC level to be 3 volts.

$$V_{OUT\ DC} = (1 + (2R_{DC}/R_4))\ V_{REF}$$

where: $R_4 = 30K$
$V_{REF} = 1.8V$
R_{DC} is external

manipulating the equation we arrive at . . .

$$R_{DC} = \left(\left(\frac{V_{OUT}}{V_{REF}}\right) - 1\right)\frac{R_4}{2}$$

Note that the $C_{(DC)}$ should be large enough to totally short out any AC in this feedback loop.

2) Analyze the OUTPUT signal's anticipated amplitude.
   a) if larger than 2.8V peak, R_2 needs to be increased. (see INGREDIENTS section, below)
   b) if larger than 3.0V peak, R_1 will *also* need to be increased.

By limiting the peak input currents we avoid signal distortion.

3) The input and output coupling caps need to be large enough not to attenuate any desired frequencies. ($X_c = 1/(6.28xf)$

4) The C(rect) should be 1μF to 2μF for initial setup. This directly affects Attack and Release times.
5) An input buffer may be necessary if the sources' output impedance needs matching.
6) Pre-emphasis may be used to reduce noise-pumping, breathing, etc., if present. See the NE570/571 data sheet for specific details.
7) Distortion (THD) trim pins are available if the already low distortion needs to be further reduced. Refer to data sheet for trimming network. Note that if not used, the THD trim pins should have 200pF caps to ground.
8) At very low input signal levels, the rectifier's errors become significant and can be reduced with the Low Level Mistracking network. (This technique prevents infinite compression at low input levels.)

The EXPANDOR utilizes all the basic building blocks of the compandor (see Figure 7). In this configuration the variable gain cell is placed in the inverting input lead of the operational amplifier and acts as a variable input resistance, R_{IN}. The basic gain equation for operational amplifiers in the standard inverting feedback loop is $Av = -R_F/R_{IN}$.

As the input amplitude increases above the crossover level of 0dBM, this variable resistor decreases in value, causing the gain to increase, thus forcing the output amplitude to increase. (Refer to Figure 10.)

Below the crossover level an increase in input amplitude causes the variable resistor to increase in value, thus forcing the output amplitude to decrease.

In the expandor configuration the rectifier is connected to the input.

The complete equation for the expandor gain is:

Gain expandor = $(2R_3V_{IN}(avg))/R_1R_2I_B$

where: $R_1 = 10K$
$R_2 = 20K$
$R_3 = 20K$
$I_B = 140\mu A$

$V_{IN}(avg) = 0.9\ (V_{IN}(rms))$

EXPANDOR RECIPE

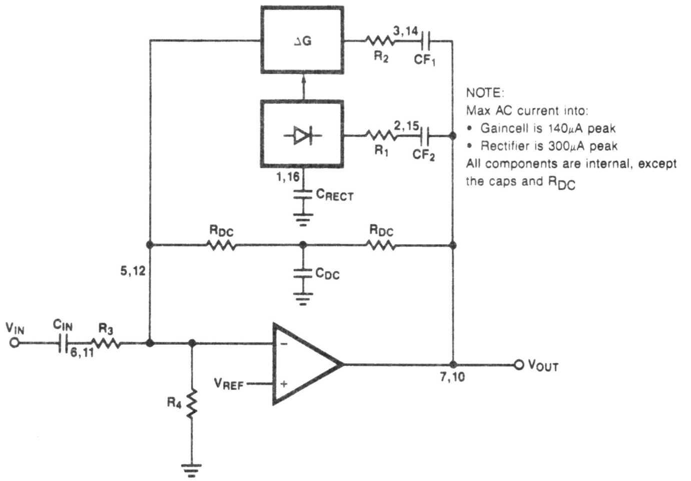
1) DC bias the output half way between the supply and ground to get maximum headroom. The circuit in Figure 8 is designed around a system supply of 6 volts so we want the output DC level to be 3 volts.

$V_{OUT}\ DC = (1 + R_3/R_4)\ V_{REF}$

where: $R_3 = 20K$
$R_4 = 30K$
$V_{REF} = 1.8V$

Note that when using a supply voltage higher than 6 volts the DC output level should be adjusted. To increase the DC output level, it is recommended that R_4 be decreased by adding parallel resistance to it. (Changing R_3 would affect the expandor's AC gain also and thus cause a mismatch in a companding system.)

BASIC COMPRESSOR



NOTE:
Max AC current into:
- Gaincell is 140μA peak
- Rectifier is 300μA peak

All components are internal, except the caps and R_{DC}

Figure 6

BASIC EXPANDOR

BASIC EXPANDOR

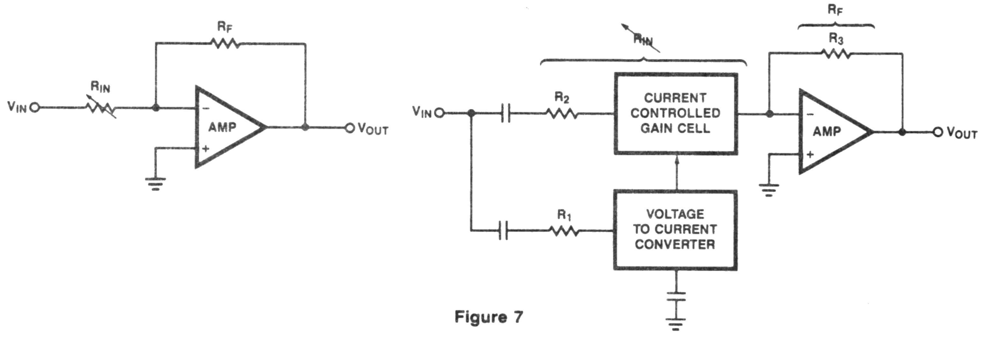


Figure 7

2) Analyze the input signal's anticipated amplitude:
   a) if larger than 2.8 peak, R_2 needs to be increased. (see INGREDIENTS section, below)
   b) if larger than 3.0V peak, R_1 will *also* need to be increased. (see INGREDIENTS, below)

By limiting the peak input currents we avoid signal distortion.

3) The input and output decoupling caps need to be large enough not to attenuate any desired frequencies.
4) The C(rect) should be 1μF to 2μF for initial setup.
5) An input buffer may be necessary if the sources' output impedance needs matching.
6) De-emphasis would be necessary if the complementary compressor circuit had been pre-emphasized (as in a tape deck application). See the HI-FI Expandor application in the Linear LSI Data Manual.
7) Distortion (THD) trim pins are available if the already low distortion needs to be further reduced. See Linear LSI Data Manual for trimming network. Note that if not used, the THD trim pins should have 200pF caps to ground.
8) At very low input signal levels, the rectifier's errors become significant and can be reduced with the Low Level Mistracking network (see Linear LSI Data Manual). (This technique prevents infinite expansion at low input levels.)

In the ALC configuration, (Figure 9), the variable gain cell is placed in the feedback loop of the operational amplifier (as in the COMPRESSOR) and the rectifier is connected to the input.

As the input amplitude increases above the crossover point, the overall system gain decreases proportionally, holding the output amplitude constant.

As the input amplitude decreases below the crossover point, the overall system gain increases proportionally, holding the output amplitude at the same constant level.

The complete gain equation for the ALC is:

$$\text{Gain} = \frac{R_1 R_2 I_B}{2\ R_3\ V_{IN}(\text{avg})}$$

$$\text{Output level} = \frac{R_1 R_2 I_B}{2\ R_3}\left(\frac{V_{IN}}{V_{IN}(\text{avg})}\right)$$

$$\text{where } \frac{V_{IN}}{V_{IN}(\text{avg})} = \frac{\pi}{2\sqrt{2}} = 1.11 \text{ (for sine wave)}$$

Note that for very low input levels, ALC may not be desired and to limit the maximum gain, resistor Rx has been added. The modified gain equation is:

$$\text{Gain max.} = \frac{\dfrac{R_1 + R_X}{1.8V \times R_2 \times I_B}}{2\ R_3}$$

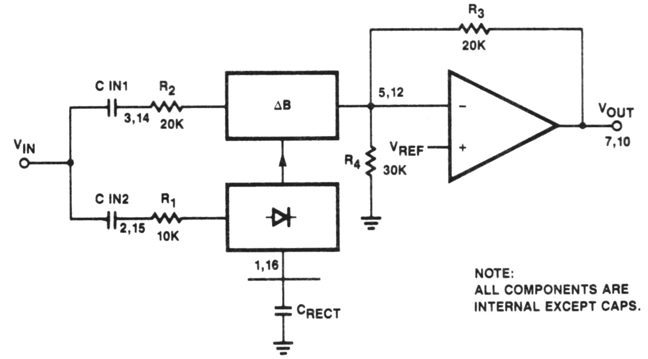
$$R_X \cong ((\text{desired max gain}) \times 26K) - 10K$$

INGREDIENTS

[Application guidelines for internal and external components (and input/output constraints) needed to tailor (cook) each of the three entrees (applications) to your taste.]

R_1 (10Kohms) limits input current to the rectifier. This current should not exceed an AC peak value of ± 300 microamps. An external resistor may be placed in series with R_1 if the input voltage to the rectifier will exceed ± 3.0V peak (i.e., 10K × 300μA = 3.0V).

BASIC EXPANDOR



NOTE:
ALL COMPONENTS ARE INTERNAL EXCEPT CAPS.

Figure 8

AUTOMATIC LEVEL CONTROL

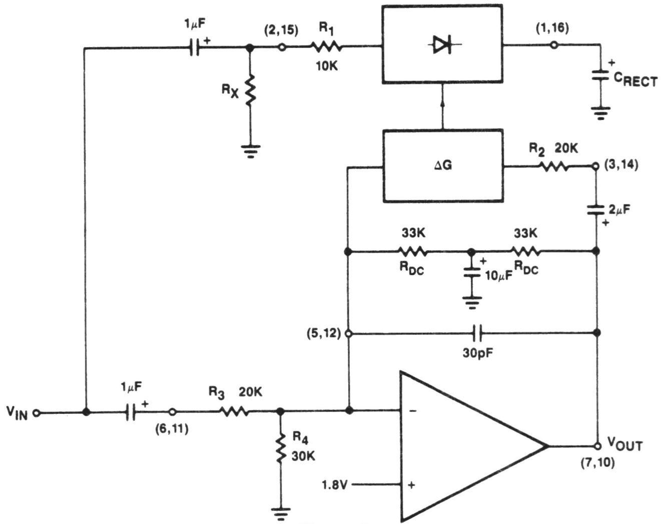


Figure 9

R_2 (20Kohms) limits input current to the variable gain cell. This current should not exceed an AC peak value of ± 140 microamps. Again, an external resistor has to be placed in series with R_2 if the input voltage to the variable gain cell exceeds ± 2.8V (i.e., 20K × 140μA).

R_3 (20Kohms) acts in conjunction with R_4 as the feedback resistor (Rf) (expandor configuration) in the equation. (R_3's value can be either reduced or increased externally.) However, it is recommended that R_4 be the one to change when adjusting the output DC level.

R_4 (30Kohms) acts as the input resistor (R_{IN}) in the standard non-inverting op amp circuit. (Its value can only be reduced.)

$V_{out\,DC} = (1 + (R_3/R_4))V_{ref}$ (for the EXPANDOR)

$V_{out\,DC} = (1 + (2R_{DC}/R_4))V_{ref}$ (for the COMPANDOR,ALC)

[The purpose of these DC biasing equations is to allow the designer to set the output half way between the supply rails for largest headroom (usually some positive voltage and ground).]

C_{DC} acts as an AC shunt to ground to totally remove the DC biasing resistors from the AC gain equation.

C_F caps are AC signal coupling caps.

C_{RECT} acts as the rectifier's filter cap and directly affects the response time of the circuit. There is a trade-off, though, between fast attack and decay times and distortion.

The time constant is: $10K \times C_{RECT}$

The total harmonic distortion (THD) is approximated by:

$$THD \cong (1\mu F/C_{RECT})(1kHz/freq.) \times 0.2\%$$

NOTES:

The NE572 differs from the 570/571 in that:

1. There is no internal op amp.
2. The attack and release times are programmed separately.

SYSTEM LEVELS OF A COMPLETE COMPANDING SYSTEM

Figure 10 demonstrates the compressing and expanding functions:

Point A represents a wide dynamic range signal with a maximum amplitude of + 16dB and minimum amplitude of − 80dB.

Point B represents the compressor output showing a 2:1 reduction in dynamic range (− 40dB is increased to − 20dB, for example). Point B can also be seen as the dynamic range of a transmission medium. Transmission noise is present at the − 60dB level from Point B to Point C.

Point C represents the input signal to the expandor.

Point D represents the output of the expandor. The signal transformation from Point C to D represents a 1:2 expansion.

SYSTEM LEVELS OF A COMPLETE COMPANDING SYSTEM

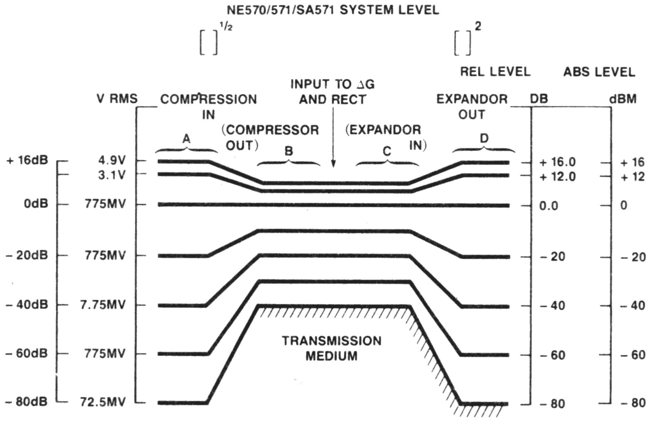
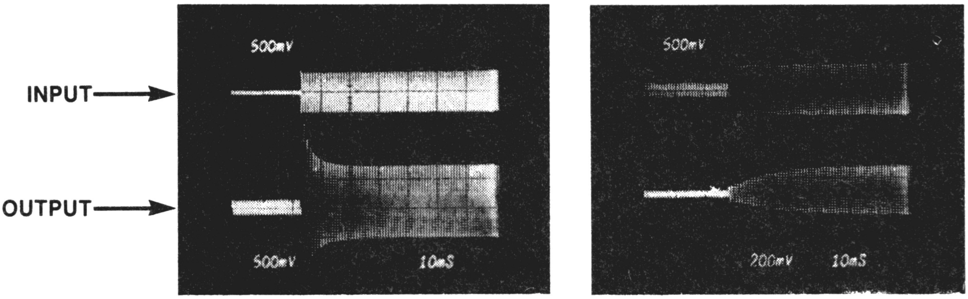

NE570/571/SA571 SYSTEM LEVEL
[ ]^1/2
[ ]^2
REL LEVEL
ABS LEVEL
V RMS
COMPRESSION IN
INPUT TO ΔG AND RECT
EXPANDOR OUT
DB
dBM
A
(COMPRESSOR OUT)
B
(EXPANDOR IN)
C
D
+ 16dB
4.9V
3.1V
0dB
775MV
− 20dB
775MV
− 40dB
7.75MV
− 60dB
775MV
− 80dB
72.5MV
TRANSMISSION MEDIUM
+ 16.0
+ 12.0
0.0
− 20
− 40
− 60
− 80
+ 16
+ 12
0
− 20
− 40
− 60
− 80

Figure 10

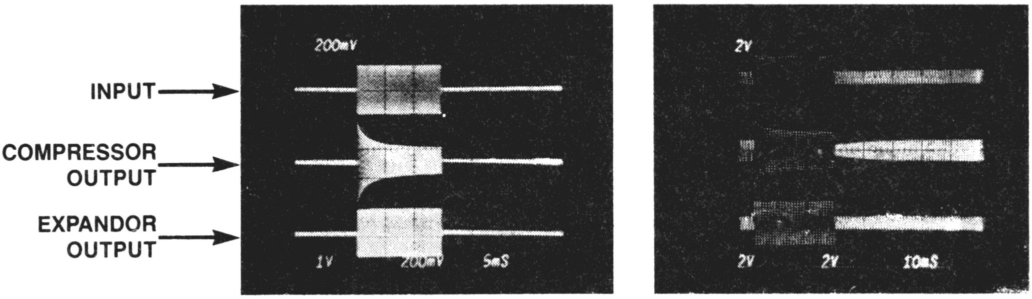
WHAT IS COMPANDING??

Shown here are some scope pictures of what three functions of the compandor look like in the kitchen, responding to tone bursts of varying amplitudes.



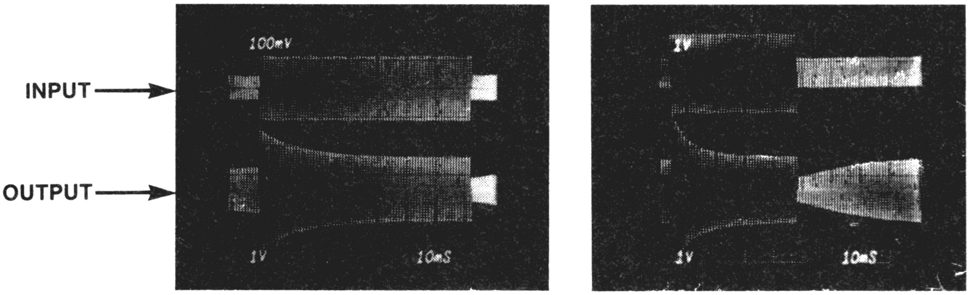
COMPRESSION 1kHz

EXPANSION 1kHz



COMPANDOR SYSTEM 15kHz

COMPANDOR SYSTEM 1kHz



AUTOMATIC LEVEL CONTROL (SMALL SIGNAL INPUT)

AUTOMATIC LEVEL CONTROL (LARGE SIGNAL INPUT)

Figure 11

APPLICATION BOARD

Shown below is the schematic (Figure 12) for Signetics' NE570/571 evaluation/demo board. This board provides one channel of EXPANSION and one channel of COMPRESSION (which can be switched to AUTOMATIC LEVEL CONTROL).

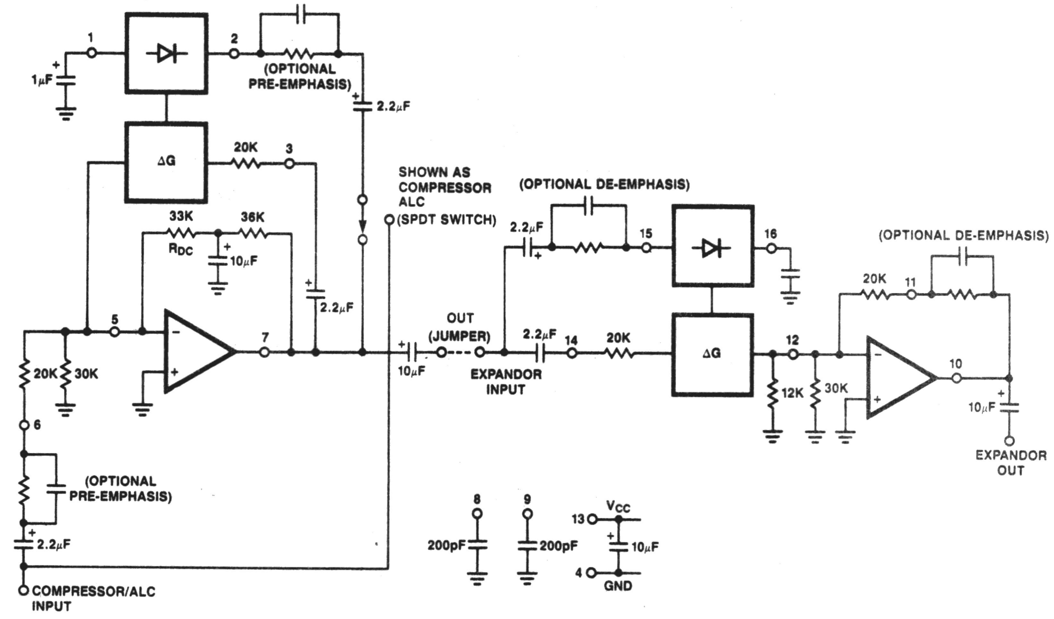

1
2
1μF
(OPTIONAL PRE-EMPHASIS)
2.2μF
ΔG
20K
3
SHOWN AS COMPRESSOR
ALC
(SPDT SWITCH)
(OPTIONAL DE-EMPHASIS)
33K
36K
RDC
10μF
2.2μF
15
16
(OPTIONAL DE-EMPHASIS)
20K
11
2.2μF
5
7
OUT (JUMPER)
2.2μF
14
20K
ΔG
12
10
10μF
EXPANDOR INPUT
20K
30K
12K
30K
10μF
6
EXPANDOR OUT
(OPTIONAL PRE-EMPHASIS)
2.2μF
COMPRESSOR/ALC INPUT
8
9
200pF
200pF
13
VCC
10μF
4
GND

Figure 12

APPLICATIONS USING THE NE5080, NE5081 AN195

APPLICATIONS

Figure 1 shows a block diagram of the NE5080 and NE5081 in a simple point-to-point communications scheme. Pin 5 of the NE5080 is grounded to permanently enable transmission; grounding pin 3 disables the jabber function.

An example of a communications system block diagram using the NE5080 and the NE5081 (as in a modem) is shown in Figure 2.

The jabber function is active in this system. The NE5080 Jabber Flag (pin 2) goes high when the capacitor at pin 3 of the NE5080 charges to about 1.4 volts. This fault condition will interrupt the Transmission Controller, which will cease transmitting and write to the proper address for the decoder to put out a signal to discharge the capacitor. The Controller will then pass the token to the next node.

The transmission medium can be anything from a twisted pair to a fiber optic link. The NE5081 receives the FSK signal and converts it to a digital data stream corresponding to the data sent by the NE5080. Pin 10 of the NE5081 goes high when the signal at its input is above the threshold set by the potentiometer between pins 13 and 14 of the NE5081.

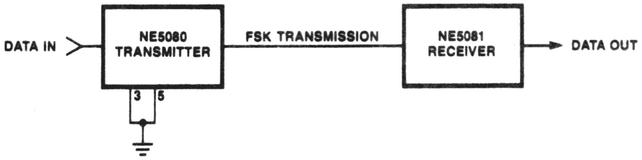


Figure 1. Point-to-Point Communications

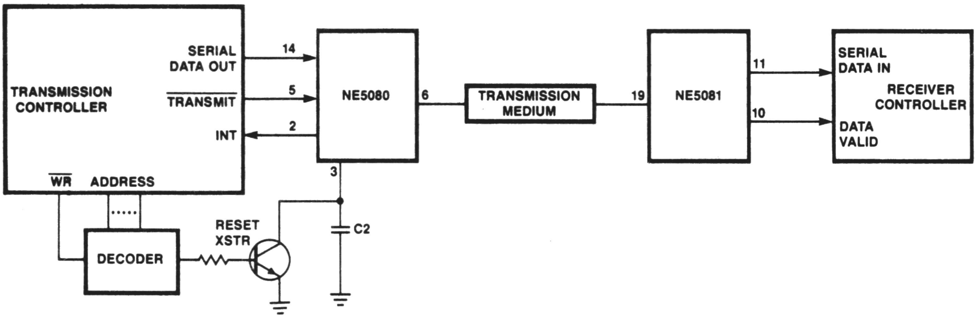

TRANSMISSION CONTROLLER
SERIAL DATA OUT
TRANSMIT
INT
WR
ADDRESS
14
5
2
NE5080
6
3
C2
DECODER
RESET XSTR
TRANSMISSION MEDIUM
19
NE5081
11
10
SERIAL DATA IN
RECEIVER CONTROLLER
DATA VALID

Figure 2. Communications System Block Diagram.

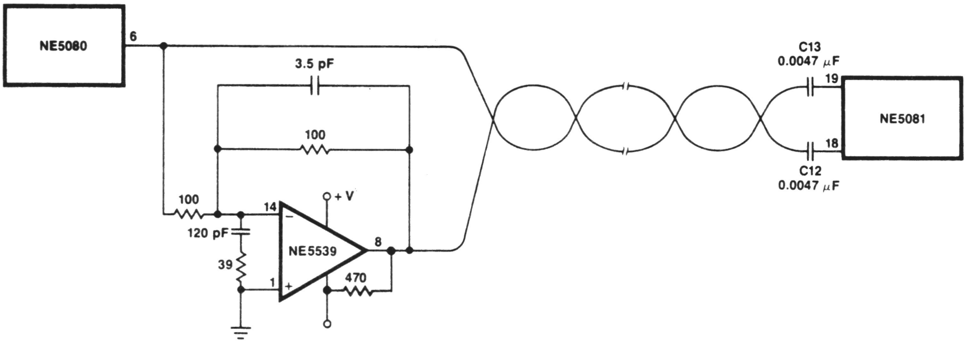

NE5080
6
3.5 pF
100
100
120 pF
39
14
1
+V
NE5539
8
470
C13
0.0047 μF
19
NE5081
18
C12
0.0047 μF

Figure 3. Modem Using a Twisted Pair Transmission Line.

Note: In applications using twisted pair lines where noise pick-up may be excessive, it is recommended that the twisted pair be driven differentially. Figure 8 shows how this may be implemented.

DC to 2 Megabaud Modem Using the NE5080 and NE5081

The NE5080 and NE5081 are designed to be used together as an asynchronous modem. They employ FSK modulation at high carrier frequencies, plus filtering to reject EMI and RFI noise that is frequently encountered in industrial and commercial environments. Figures 4 and 5 show Full and Half Duplex modems.

The carrier frequency is externally adjustable and can range from 50kHz to over 20MHz.

The modem can be used in a number of ways:

1. Multidrop party line of data transmitting and receiving devices (local area networks).
2. Point-to-point operation connecting just two transmitting/receiving devices.
3. Either of the above operated on one cable in the half duplex mode.
4. Either 1 or 2 above operated on two cables in the full duplex mode.

The 30dB dynamic range of modems built using the NE5080 and NE5081 makes it possible to attach them at any point on the cable without any gain adjustment. There is no problem with proximity to other similar modems.

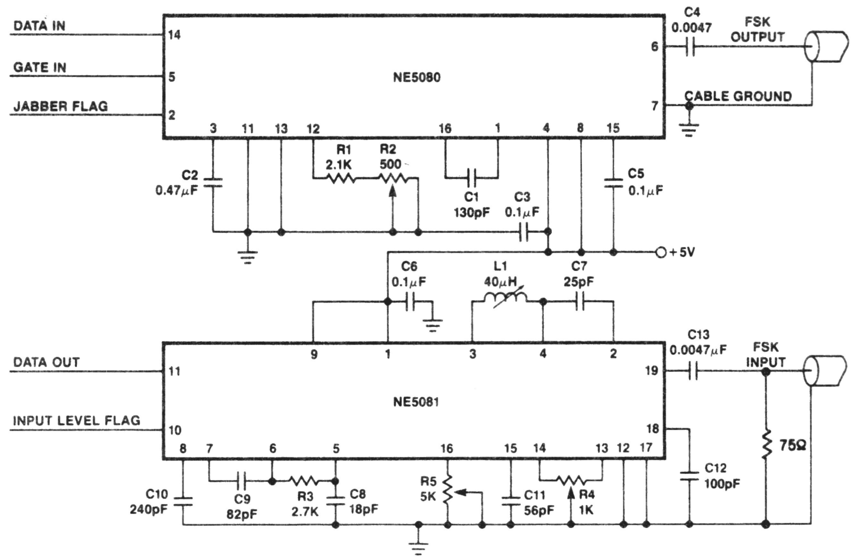
The distance that can be driven varies with the type of cable used, the number of modems attached to the cable, and the carrier frequency.

Typical operation can be 100 modems randomly spaced on up to 2000 meters of RG-11 (foam) cable with a center frequency of 5MHz.

In point-to-point operation, one can drive further. Table 1 gives obtainable distances when different carrier frequencies and cables are used.

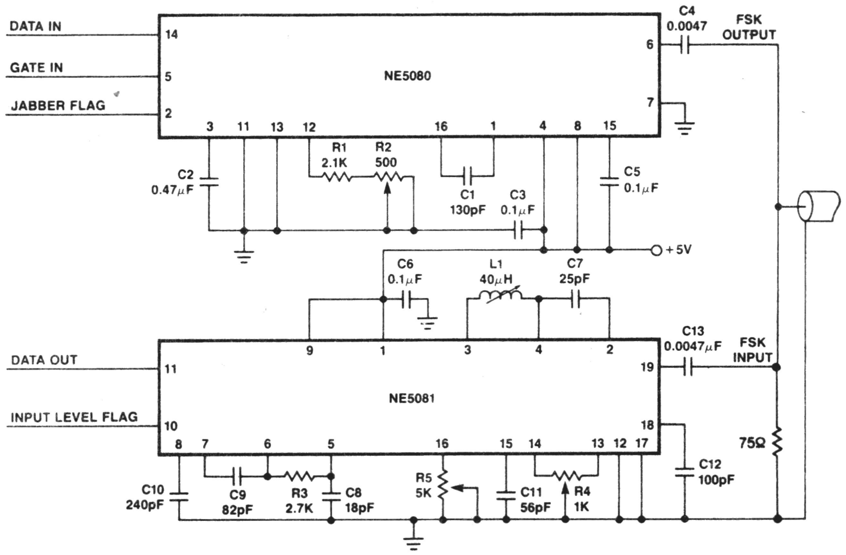
Table 1. TRANSMISSION DISTANCE FOR A SINGLE RECEIVER AS A FUNCTION OF CENTER FREQUENCY AND CABLE TYPE

Carrier Frequency	Maximum Data Rate	Cable			
		RG-59	RG-11 (Foam)	JT34125	JT3750J
1MHz	0.5 Megabaud	6000 Ft	21000 Ft	33000 Ft	50000 Ft
3MHz	1.0 Megabaud	5000 Ft	12000 Ft	20000 Ft	32000 Ft
5MHz	2.0 Megabaud	4200 Ft	9500 Ft	15000 Ft	25000 Ft


DATA IN
GATE IN
JABBER FLAG
NE5080
14
5
2
3 11 13 12 16 1 4 8 15
6
7
C4
0.0047
FSK
OUTPUT
CABLE GROUND
R1
2.1K
R2
500
C2
0.47μF
C1
130pF
C3
0.1μF
C5
0.1μF
+5V
C6
0.1μF
L1
40μH
C7
25pF
9 1 3 4 2
C13
0.0047μF
FSK
INPUT
DATA OUT
INPUT LEVEL FLAG
NE5081
11
10
19
18
8 7 6 5 16 15 14 13 12 17
75Ω
C12
100pF
C10
240pF
C9
82pF
R3
2.7K
C8
18pF
R5
5K
C11
56pF
R4
1K

EXTERNAL COMPONENTS SHOWN ARE FOR 5MHz CARRIER

Figure 4. NE5080 and NE5081 Connected as a Full Duplex Modem.


DATA IN
GATE IN
JABBER FLAG
NE5080
14
5
2
3 11 13 12 16 1 4 8 15
6
7
C4
0.0047
FSK
OUTPUT
R1
2.1K
R2
500
C2
0.47μF
C1
130pF
C3
0.1μF
C5
0.1μF
+5V
C6
0.1μF
L1
40μH
C7
25pF
9 1 3 4 2
C13
0.0047μF
FSK
INPUT
DATA OUT
INPUT LEVEL FLAG
NE5081
11
10
19
18
8 7 6 5 16 15 14 13 12 17
75Ω
C12
100pF
C10
240pF
C9
82pF
R3
2.7K
C8
18pF
R5
5K
C11
56pF
R4
1K

EXTERNAL COMPONENTS SHOWN ARE FOR 5MHz CARRIER

Figure 5. NE5080 and NE5081 Connected as a Half Duplex Modem.

FSK MODEM SET-UP PROCEDURES

To set up the modem per IEEE 802.4 specifications, the following sequence should be followed at 25 ± 2°C ambient.

TRANSMITTER SET-UP:

1. Ground Jabber Control (pin 3) and the transmit gate (pin 5) of the NE5080.
2. Turn on the power and allow the circuit to warm up for 3 minutes.
3. Hold the Data Input (pin 14) of the NE5080 at a logic high.
4. Measure the frequency at the FSK output of the transmitter (cable should be properly terminated) and adjust R2 for a frequency reading of 6.250MHz ±5kHz.
5. Apply a logic low to the Data Input and check the output frequency. If the reading is not 3.750MHZ ±40kHz, readjust R1 until the high frequency is 6.250MHz ±25kHz and the low frequency is 3.750MHZ ±40kHz.

Transmitter set-up is now complete.

RECEIVER SET-UP:

6. Set Detection Timing pot R5 and Input Level Detect pot R4 at the NE5081 to mid range.
7. Apply a 5.000 MHz $1V_{p-p}$ sine wave to the receiver FSK Input.
8. Attach an oscilloscope probe to the Data Output pin of the NE5081 and adjust L1 or C7 (whichever is adjustable) until the output state alternates between high and low levels. Figures 7 and 8 indicate examples of improper tuning.
9. Set the generator to 3.750MHz, $35mV_{p-p}$.
10. Adjust Input Level Detect pot R4 until the Data Output pin is alternating between high and low levels.
11. Increase the generator output to $45mV_{p-p}$ and verify that the data output is low.
12. Decrease the generator output to $25mV_{p-p}$ and verify that the data output is high.
13. Apply a 100kHz $1V_{p-p}$ signal to the FSK Input and connect a scope probe to the Input Level Flag and another probe to the FSK Input. Adjust Detection Timing pot R5 so that the delay from the time the FSK Input signal goes through 0 volts on the Positive to negative transition, to the time when the Input Level Flag goes from high to low, is between 0.5 and 2.5μSec. See Figure 9.
14. Final adjustment to the tuning of L1/C7 should be done by using an adjusted transmitter to transmit pseudo random data and tuning the receiver L1/C7 tank circuit for minimum jitter and symmetrical eye pattern observed on the receiver pin 8 (see Figure 10).

This concludes the receiver set-up procedure.

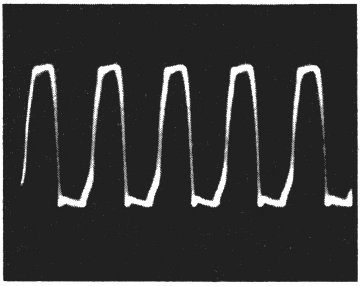


Figure 6. NE5081 Data Output When Correctly Tuned to Incoming 5MHz Carrier.

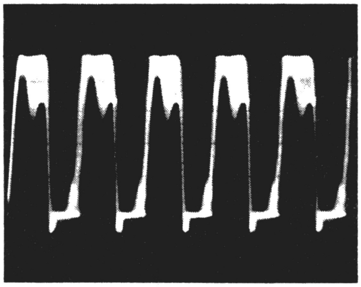


Figure 7. NE5081 Data Output When Tuned Just Below 5MHz Carrier.

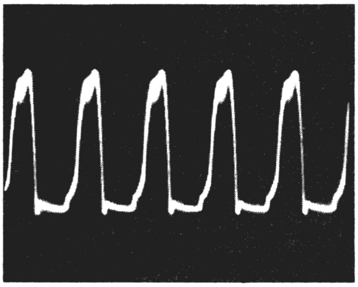


Figure 8. NE5081 Data Output Output Tuned Just Above 5MHz Carrier.

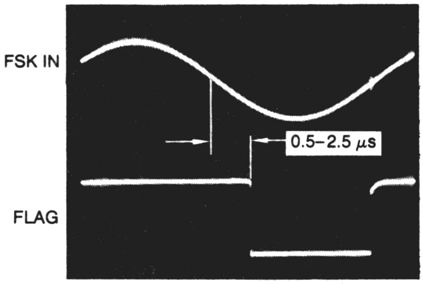


Figure 9. Correct Adjustment of Input Level Detection Timing.

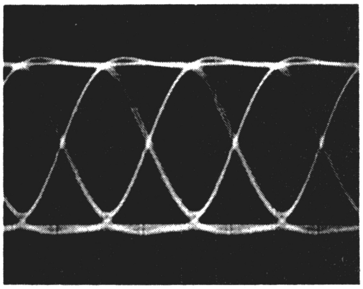


Figure 10. "Eye" Pattern at NE5081 Pin 8.

DETERMINING COMPONENT VALUES

Power supply pins of both devices should be bypassed with high quality 0.1 μF capacitors close to the devices. Additionally, the NE5081 V_{CC2} (pin 9) should be well-decoupled from the power supply by a small inductor (about 10 μH) and another 0.1 μF capacitor as the NE5081 exhibits large changes in power supply current during switching.

The coupling capacitors C4 and C13 are needed to maintain input bias when a low DC impedance line is connected to the FSK Input. Too small a value for these capacitors could result in excessive signal attenuation. If these capacitrs are too large, the receiver Input Level Flag may remain high for an excessive amount of time after the input signal is removed. Each transmitter and each receiver should have its own coupling capacitor. This is necessary to prevent any DC terminations from altering biases.

The external resistance at the NE5080 pin 12 should always be about 2.4 kilohms, with some adjustment allowable to compensate for the tolerance of C1 and slight differences between individual ICs.

C11 and R5 are the Carrier Detect timing components and determine how long after the FSK input signal is discontinued before the Input Level Flag goes low. R5 should not exceed 5 kilohms. With C11 set at 56 pF, a 5 kilohm R5 will allow Carrier Detect Timing adjustment to 2 μSec. R5 can be a fixed resistor if this timing is not critical (perhaps because of the use of an "end of data" signal). This delay is required to allow the signal to propagate through the receiver. Carrier Detect Timing should be adjusted for different center frequencies by choosing C11 according to the relationship:

$$C11 = \frac{1}{3572\ f_c}$$

The Input Level Detect function can be disabled and the receiver be made to hold the Carrier Detect Flag high by removing R5 and C11 and tying pins 15 and 16 together and pulling them up to V_{CC} with a 10 kilohm resistor.

If the Jabber function is not to be used, Jabber control pin 3 of NE5080 should be grounded. If the Jabber function is to be used, a capacitor, C2, should be connected between pin 3 and ground. The value of this capacitor is determined as indicated below:

$$C2 = (0.95 \times 10^{-6})\ t$$

where t is the maximum allowable transmit time in seconds.

The resistance R1, together with capacitor C1, set the transmit frequencies. The logic high frequency is fixed at about 1.67 times the logic low frequency, meaning that the logic low frequency is 0.75 times the center frequency f_c, and the logic high frequency is 1.25 times the center frequency. Note that this center frequency is never transmitted in normal operation and is sometimes referred to as the "carrier frequency."

C1 is chosen by the relationship for f_c at or below 7MHz:

$$C1 = \frac{6.5 \times 10^{-4}}{f_c}$$

Above 7MHz center frequency, this capacitor is found by modifying this equation to:

$$C1 = \frac{5.5 \times 10^{-4}}{f_c}$$

To get the characteristics that are needed for proper operation of the NE5081, it is important to keep the proper relationship between L1 and C7:

$$C7 = \frac{1}{7885\ f_c}$$

$$L1 = \frac{200}{f_c}$$

Capacitor values of the filter are dependent upon operating frequencies to maintain proper characteristics:

$$C8 = \frac{9.0 \times 10^{-5}}{f_c}$$

$$C9 = \frac{4.1 \times 10^{-4}}{f_c}$$

$$C10 = \frac{1.2 \times 10^{-3}}{f_c}$$

$$C12 = \frac{5 \times 10^{-4}}{f_c}$$

Coupling capacitor values also depend upon center frequency:

$$C4 = C13 = \frac{2.5 \times 10^{-2}}{f_c}$$

In all of the above equations, capacitances are in Farads, inductances in Henrys, and frequencies in Hertz.

SOME COMMON BAUD RATES

Although intended to be used with a center frequency of 5MHz, the NE5080 and NE5081 can be used at other center frequencies. Table 2 gives minimum center frequency (f_c) for some common baud rates, together with external component values for those center frequencies. Note that it is not recommended that these devices be operated at center frequencies below 50kHz.

USING THE NE5080/NE5081 WITH A FIBER OPTIC LINK

The NE5080/NE5081 chip set is highly suitable for use in low cost fiber-optic links. There are many advantages to fiber links over open wire or coaxial cable links. These advantages include:

1. Cost savings in conductor weight and size.
2. Immunity to EMI/RFI.
3. Low crosstalk.
4. High communications security; cannot be tapped by electromagnetic induction or surface conduction.
5. Fiber-optic cable does not radiate electromagnetic energy nor disturb other communications media.
6. Extremely wide bandwidth (high channel per conductor density).
7. Low attenuation.
8. No ground loops or shifts caused by common grounds.
9. Complete electrical isolation between transmitter and receiver.
10. Cable breaks cause no shorts, making this technology useful in hazardous environments, e.g., explosive chemical facilities.
11. No damage to equipment is expected due to current surges on adjacent lines.
12. Fiber cable does not act as an antenna to pick up high electromagnetic pulses such as those caused by electrical storms.
13. Low BER (Bit Error Rate).

The circuit of Figure 11 shows a simplex fiber link between the NE5080 transmitter and the NE5081 receiver. The components shown are for a center frequency of 5MHz, although this frequency can be increased to 20MHz with proper selection of external component values. The NE5539 has a 350MHz unity gain bandwidth which may limit maximum operating frequencies in some systems.

Since the NE5081 can adequately accept signals below 10 mV at 5MHz carrier, the gain stage (within the dashed lines of Figure 11) may be eliminated if the attenuation in the link is low. If the gain stage is used, be mindful of the bandwidth trade-off at higher gains. Refer to the NE5539 data sheet for details.

The transmitter and receiver are set up as described under FSK MODEM SET-UP PROCEDURE above.

LAYOUT PRECAUTIONS

As is the case with any components using high frequencies, good layout practice is essential; poor layout can adversely affect performance. All lead lengths should be as short as is practical for all lines which carry R-F, including the tuning capacitor and resistors (C1, R1, R2) of the NE5080. Lead length is especially critical with C1, which should be mounted as close to the NE5080 as is possible. A printed circuit board with a good ground plane, both top and bottom, is also recommended (wire-wrap is NOT recommended). The ground plane should extend below tuning capacitor C1 on both top and bottom of the board, with no other trace coming between the leads of this capacitor.

Because of the high speed switching, pin 9 (V_{CC2}) of the NE5081 can exhibit a large current swing, causing vertical output jitter which may be eliminated by decoupling pin 9 with a small (10μH) R-F choke and a 0.05μF capacitor.

See Figure 12 for an example of a working layout.

Table 2. RECOMMENDED MINIMUM CENTER FREQUENCY AND COMPONENT VALUES FOR VARIOUS BAUD RATES.

BAUD RATE (KBaud)	f_c (kHz)	C1	L1	C4 C13	C7	C8	C9	C10	C11	C12
9.6	50	13nF	4mH	0.50μF	2.4nF	1.8nF	8.2nF	24nF	5.6nF	10nF
19.2	50	13nF	4mH	0.50μF	2.4nF	1.8nF	8.2nF	24nF	5.6nF	10nF
38.4	100	6.8nF	2mH	0.27μF	1.3nF	0.9nF	3.9nF	12nF	2.7nF	5nF
50.1	125	5.1nF	1.6mH	0.20μF	1.0nF	750pF	3.3nF	10nF	2.2nF	3.9nF
64.0	160	3.9nF	1.3mH	0.15μF	800pF	560pF	2.5nF	7.5nF	1.8nF	3nF
128	320	2nF	625μH	0.075μF	390pF	270pF	1.3nF	3.9nF	860pF	1.6nF
256	640	1nF	312μH	0.039μF	200pF	150pF	640pF	1.8nF	430pF	750pF
512	1250	510pF	160μH	0.02μF	100pF	75pF	330pF	1.0nF	220pF	390pF
1500	3750	180pF	53μH	6.8nF	33pF	25pF	110pF	330pF	75pF	130pF
1544	4000	160pF	50μH	6.8nF	33pF	22pF	100pF	300pF	68pF	125pF
2000	5K	130pF	40μH	5.0nF	25pF	18pF	82pF	240pF	56pF	100pF
8000	20K	33pF	10μH	1.2nF	6pF	5pF	20pF	62pF	15pF	25pF

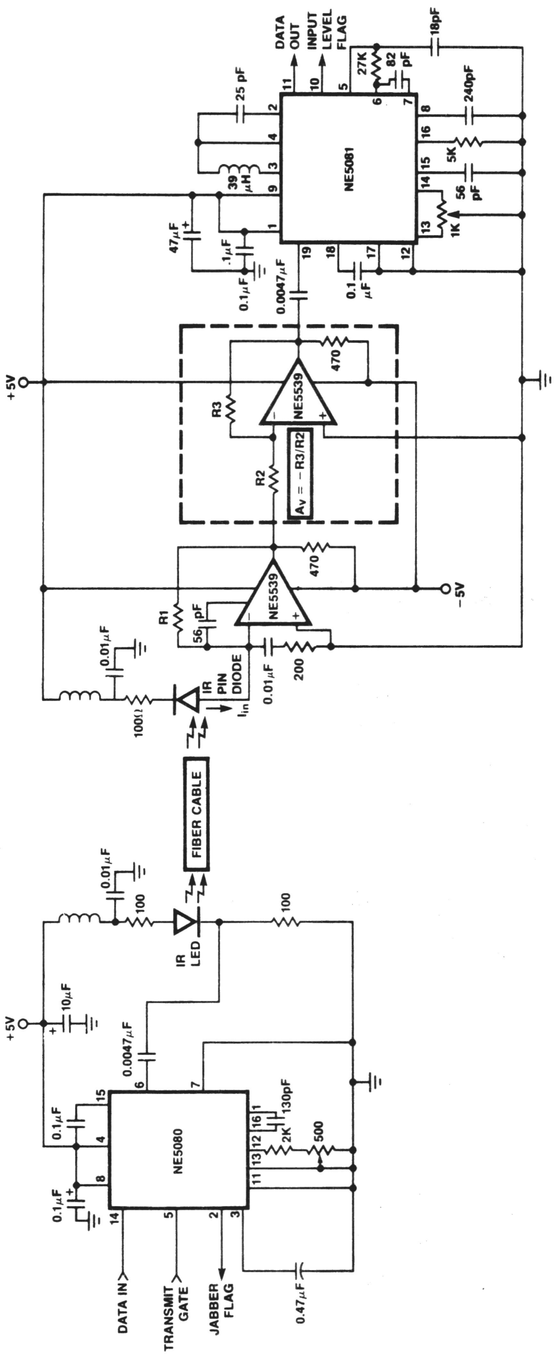
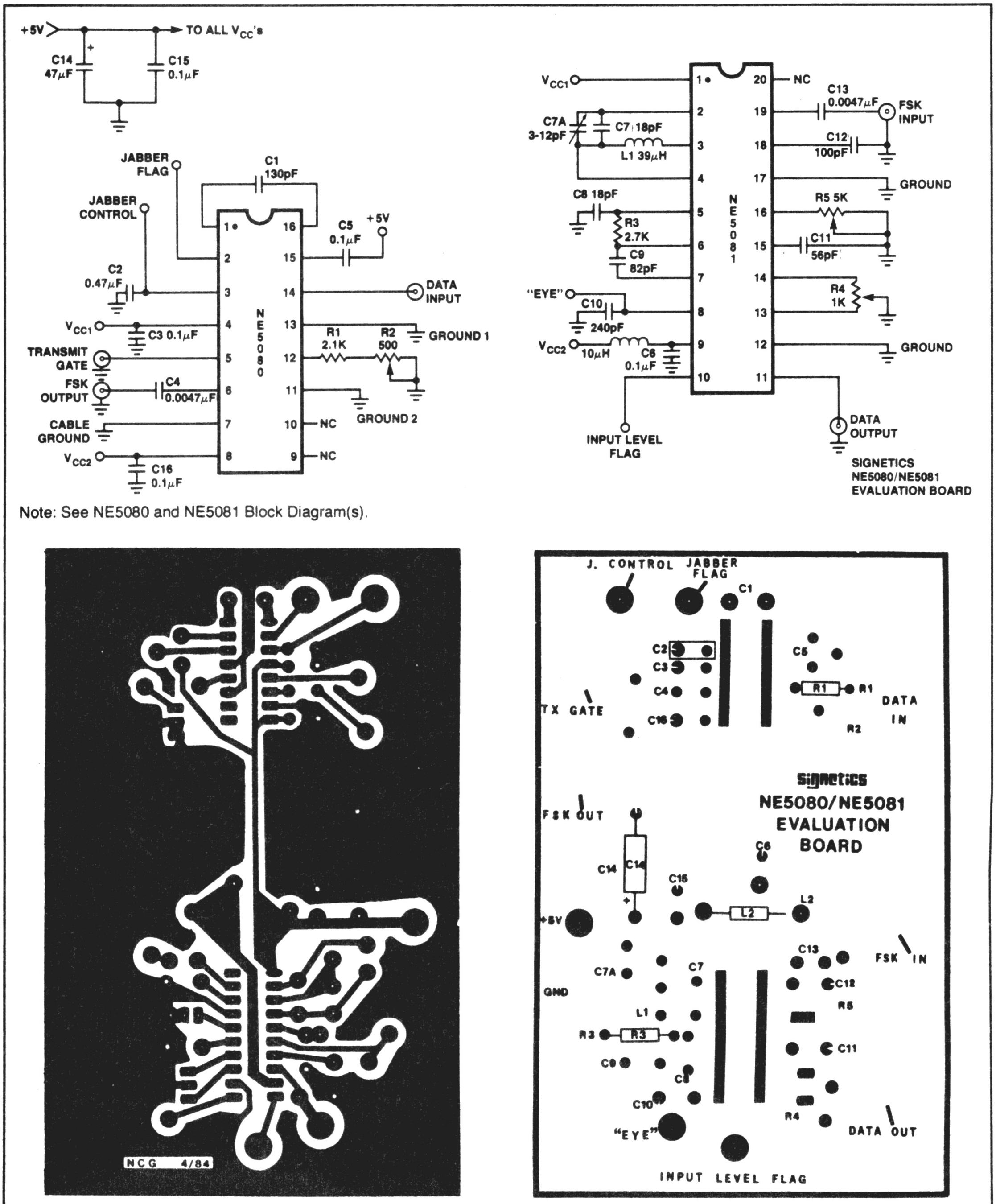

NE5080
DATA IN
TRANSMIT GATE
JABBER FLAG
0.47µF
0.1µF
+5V
10µF
0.0047µF
130pF
2K
500
IR LED
100
0.01µF
FIBER CABLE
IR PIN DIODE
Iin
100Ω
R1
56 pF
NE5539
470
0.01µF
200
-5V
R2
R3
Av = - R3/R2
0.0047µF
0.1µF
47µF
.1µF
39 µH
25 pF
NE5081
DATA OUT
INPUT LEVEL FLAG
27K
82 pF
18pF
240pF
5K
56 pF
1K

Figure 11. Simplex Fiber Optic System


+5V
TO ALL V_{CC}'s
C14 47µF
C15 0.1µF
JABBER FLAG
JABBER CONTROL
C1 130pF
C5 0.1µF
+5V
C2 0.47µF
DATA INPUT
V_{CC1}
C3 0.1µF
NE5080
R1 2.1K
R2 500
GROUND 1
TRANSMIT GATE
FSK OUTPUT
C4 0.0047µF
GROUND 2
CABLE GROUND
NC
NC
V_{CC2}
C16 0.1µF
V_{CC1}
C7A 3-12pF
C7 18pF
L1 39µH
NC
C13 0.0047µF
FSK INPUT
C12 100pF
GROUND
C8 18pF
R3 2.7K
C9 82pF
NE5081
R5 5K
C11 56pF
"EYE"
C10 240pF
R4 1K
GROUND
V_{CC2}
10µH
C6 0.1µF
INPUT LEVEL FLAG
DATA OUTPUT
SIGNETICS NE5080/NE5081 EVALUATION BOARD
NCG 4/84
J. CONTROL
JABBER FLAG
C1
C2
C3
C4
C16
C5
R1
R2
DATA IN
TX GATE
signetics
NE5080/NE5081 EVALUATION BOARD
FSK OUT
C14
C6
C15
+5V
L2
C13
FSK IN
C7A
C7
C12
GND
L1
R5
R3
C11
C9
C8
C10
R4
"EYE"
DATA OUT
INPUT LEVEL FLAG

Note: See NE5080 and NE5081 Block Diagram(s).

Figure 12. Components and Layout Used for Evaluation Board

INTEGRATED OPERATIONAL AMPLIFIER THEORY

AN165

INTRODUCTION

The operational amplifier was first introduced in the early 1940's. Primary usage of these vacuum tube forerunners of the ideal gain block was in computational circuits. They were fed back in such a way as to accomplish addition, subtraction, and other mathematical functions.

Expensive and extremely bulky, the operational amplifier found limited use until new technology brought about the integrated version, solving both size and cost drawbacks.

Volumes upon volumes have been and could be written on the subject of op amps. In the interest of brevity this chapter will cover the basic op amp as it is defined along with test methods and suggestive applications. Also, included is a basic coverage of the feedback theory from which all configurations can be analyzed.

THE PERFECT AMPLIFIER

The ideal operational amplifier possesses several unique characteristics. Since the device will be used as a gain block, the ideal amplifier should have infinite gain. By definition also, the gain block should have an infinite input impedance in order not to draw any power from the driving source. Additionally, the output impedance would be zero in order to supply infinite current to the load being driven. These ideal definitions are illustrated by the ideal amplifier model of Figure 1.

IDEAL OPERATIONAL AMPLIFIER

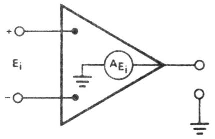


Figure 1

Further desirable attributes would include infinite bandwidth, zero offset voltage, and complete insensitivity to temperature, power supply variations, and common mode input signals.

Keeping these parameters in mind, further contemplation produces two very powerful analysis tools. Since the input impedance is infinite, there will be no current flowing at the amplifier input nodes. In addition, when feedback is employed the differential input voltage reduces to zero. These two statements are used universally as beginning points for any network analysis and will be explored in detail later on.

THE PRACTICAL AMPLIFIER

Tremendous strides have been made by modern technology with respect to the ideal amplifier. Integrated circuits are coming closer and closer to the ideal gain block. Input bias currents for instance are in the pA range for FET input amplifiers while offset voltages have been reduced to less than 1mV in many cases, in Bipolar devices.

Any device has limitations however, and the integrated circuit is no exception. Modern op amps have both voltage and current limitations. Peak to peak output voltage, for instance, is generally limited to one or two base-emitter voltage drops below the supply voltage while output current is internally limited to approximately 25mA. Other limitations such as bandwidth and slew rates are also present, although each generation of devices improves over the previous one.

DEFINITION OF TERMS

Earlier the ideal operational amplifier was defined. No circuit is ideal of course so practical realizations contain some sources of error. Most sources of error are very small and therefore can usually be ignored. It should be noted that some applications require special attention to specific sources of error.

Before the internal circuitry of the op amp is further explored it would be beneficial to define those parameters commonly referenced.

INPUT OFFSET VOLTAGE

Ideal amplifiers produce 0 volts out for 0 volts input. But, since the practical case is not perfect, there will appear a small dc voltage at the output even though no differential voltage is applied. This dc voltage is called the input offset voltage, with the majority of its magnitude being generated by the differential input stage pictured in Figure 2.

DIFFERENTIAL INPUT STAGE

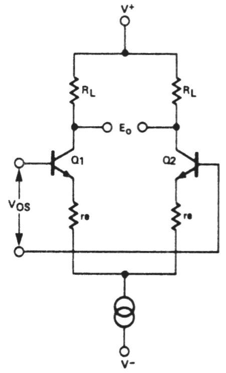


Figure 2

An operational amplifier's performance is in large part dependent upon the first stage. It is the very high gain of the first stage that amplifies small signal levels to drive remaining circuitry. Coincidentally, the input current, a function of beta, must be as small as possible. Collector current levels are thus made very low in the input stage in order to gain low bias currents. It is this input stage also which determines dc parameters such as offset voltage since the amplified output of this stage is of sufficient voltage levels to eclipse most subsequent error terms added by the remaining circuitry. Under balanced conditions the collector currents of Q1 and Q2 are perfectly matched, hence we may say:

$$E_{OS} = I_{C2}R_L - I_{C1}R_L = 0 \tag{1}$$

In practice small differences in geometries of the base emitter regions of Q1 and Q2 will cause E_{OS} not to equal 0. Thus, for balance to be restored a small dc voltage must be added to one V_{BE} or

$$V_{OS} = V_{BE}1 - V_{BE}2 \tag{2}$$

where the V_{BE} of the transistor is found by

$$V_{BE} = \frac{kT}{q} \ln \left(\frac{I_E}{I_S}\right) \tag{3}$$

Reference is made to the input when talking of offset voltage. Thus, the classic definition of input offset voltage is 'that differential dc voltage required between inputs of an amplifier to force its output to zero volts.'

Offset voltage becomes a very useful quantity for the designer because many other sources of error can be expressed in terms of V_{OS}. For instance, the error contribution of input bias current can be expressed as offset voltages appearing across the input resistors.

INPUT OFFSET VOLTAGE DRIFT

Another related parameter to offset voltage is V_{OS} drift with temperature. Present day amplifiers usually possess V_{OS} drift levels in the range of 5μV to 40μV per degree C. The magnitude of V_{OS} drift is directly related to the initial offset voltage at room temperature. Amplifiers exhibiting larger initial offset voltages will also possess higher drift rates with temperature. A rule of thumb often applied is that the drift per degree C will be 3.3μV for each millivolt of initial offset. Thus, for tighter control of thermal drift, a low offset amplifier would be selected.

INPUT BIAS CURRENT

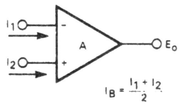


Figure 3

INPUT BIAS CURRENT

Again referring to Figure 3-2, it is apparent that the input pins of this op amp are base inputs. They must, therefore, possess a dc current path to ground in order for the input to function. Input bias current, then is 'the dc current required by the inputs of the amplifier to properly drive the first stage.'

The magnitude of I_{bias} is calculated as the average of both currents flowing into the inputs and is calculated from

$$I_B = \frac{I_1 + I_2}{2} \qquad (4)$$

Bias current requirements are made as small as possible by using high beta input transistors and very low collector currents in the first stage. The trade-off for bias current is lower stage gain due to low collector current levels and lower slew rates. The effect upon slew rate is covered in detail under the compensation section.

INPUT OFFSET CURRENT

The ideal case of the differential amplifier and its associated bias current does not possess an input offset current. Circuit realizations always have a small difference in bias currents from one input to the other, however. This difference is called the input offset current. Actual magnitudes of offset current are usually at least an order of magnitude below the bias current. For many applications this offset may be ignored but very high gain, high input impedance amplifiers should possess as little I_{os} as possible because the difference in currents flowing across large impedances develops substantial offset voltages. Output voltage offset due to I_{os} can be calculated by

$$V_{out} = A_{cl}(I_{os}R_s) \qquad (5)$$

Hence, high gain and high input impedances magnify directly to the output, the error created by offset current. Circuits capable of nulling the input voltage and current errors are available and will be covered later in this chapter.

INPUT OFFSET CURRENT DRIFT

Of considerable importance is the temperature coefficient of input offset current. Even though the effects of offset are nulled at room temperature, the output will drift due to changes in offset current over temperature. Many popular models now include a typical specification for I_{os} drift with values ranging in the .5nA per degree C area. Obviously those applications requiring low input offset currents also require low drift with temperature.

INPUT IMPEDANCE

Differential and common mode impedances looking into the input are often specified for integrated op amps. The differential impedance is the total resistance looking from one input to the other while common mode is the common impedance as measured to ground. Differential impedances are calculated by measuring the change of bias current caused by a change in the input voltage.

COMMON MODE RANGE

All input structures have limitations as to the range of voltages over which they will operate properly. This range of voltages impressed upon *both inputs* which will not cause the output to misbehave is called the common mode range. Most amplifiers possess common mode ranges of ±12 volts with supplies of ±15 volts.

COMMON MODE REJECTION RATIO

The ideal operational amplifier should have no gain for an input signal common to both inputs. Practical amplifiers do have some gain to common mode signals. The classic definition for common mode rejection ratio of an amplifier is the ratio the differential signal gain to the common mode signal gain expressed in dB as shown in equation 6a.

$$\text{CMRR(dB)} = 20 \log \frac{e_o/e_i}{e_o/e_{cm}} \qquad (6a)$$

The measurement CMRR as in 3-6a requires 2 sets of measurements. However, note that if e_o in equation 3-6a is held constant, CMRR becomes:

$$\text{CMRR(dB)} = 20 \log \frac{e_{cm}}{e_i} \qquad (6b)$$

A new alternate definition of CMRR based on 3-6b is the ratio of the change of input offset voltage to the input common mode voltage change producing it.

EFFECTS OF CMRR ON VOLTAGE FOLLOWER

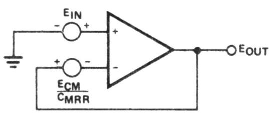


Figure 4

Figure 4 illustrates the application of the equivalent common mode error generator to the voltage follower circuit. The gain of the voltage follower with error contributions caused by both finite gain and finite common mode rejection ratio is shown in equation 7.

$$\frac{e_o}{e_{in}} = \frac{1 \pm 1/\text{CMRR}}{1 + 1/A} \qquad (7)$$

where A equals open loop gain and is frequency dependent.

AC PARAMETERS

Parameter definition has up to this point, been dealing primarily with dc quantities of voltages, currents, etc. Several important ac or frequency dependent parameters will now be discussed.

An ideal gain block was defined earlier as one which would provide infinite gain and bandwidth. Real circuits approximate infinite open loop gain with low frequency gains in excess of 100dB. The very high gains achieved with present designs are possible only by cascading stages. Although providing very high open loop gain the cascading of stages results in the need for frequency compensation in closed loop configurations and reduces the open loop.

LARGE SIGNAL BANDWIDTH

The large signal or power bandwidth of an amplifier refers to its ability to provide its maximum output voltage swing with increasing frequency. At some frequency the output will become slew rate limited and the output will begin to degrade. This point is defined by

$$F_{PL} = \frac{\text{Slew Rate}}{2\pi \bullet E_{out}} \qquad (8)$$

where F_{PL} is the upper power bandwidth frequency and E_{out} is the peak output swing of the amplifier.

SLEW RATE

The maximum rate of change of the output in response to a step input signal is termed slew rate. Deviation from the ideal is caused by the limitation in frequency response of the amplifier stages and the phase compensation technique used. Summing node and amplifier output capacitances must be kept to a minimum to guarantee getting the maximum slew rate of the operational amplifier. Circuit board layout must also be of high frequency quality. Power supplies should be adequately bypassed at the pins, with both low and high frequency components to avoid possible ringing. A selection of a proper capacitor in parallel with the feedback resistor may be necessary. Too small a value could result in excessive ringing and too large a value will decrease frequency response. In general, the worst case slew rate is in the unity gain non-inverting mode (see Figure 5a). Specifications of slew rate should always reflect this worst case condition with the maximum required compensation network.

AMPLIFIER SLEW RATE LIMITATIONS

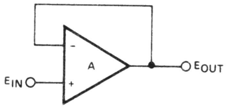


Figure 5a

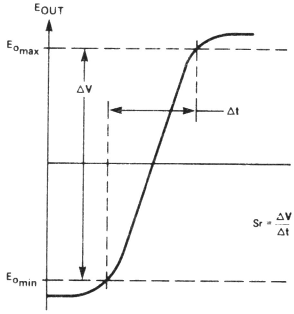


Figure 5b

FREQUENCY RESPONSE

Distributed capacitances and transit times in semiconductors cause an upper frequency limit or pole for each and every gain stage. Monolithic pnp transistors used for level shifting possess poor upper frequency characteristics and cascaded gain stages, used to approach the highest gain, subtract from the maximum frequency response. As shown in Figure 6 the open loop frequency response of the op amps shown crosses unity gain at approximately 10MHz. Closed loop response is unstable without compensation, however, so typical unity gain frequencies are readjusted by the effects of phase compensation, in this case 1MHz.

From Figure 6 it is also apparent that an amplifier has a trade off between gain and bandwidth. Higher gains are achieved at the expense of bandwidth. This trade off is a constant figure called the gain bandwidth product.

TEST METHODS

Product testing of integrated circuits uses automatic test equipment. Large computer controlled test decks test all data sheet limits in a matter of milliseconds. Each parameter is tested in a specific circuit configuration defined by the test hardware.

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

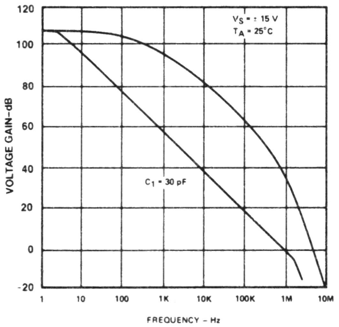


Figure 6

A typical simplified op amp test configuration is depicted by Figure 9. Units may be classed in several categories according to selected parameters. Even failures may be classified categorically depending upon their mode of failure.

Figures 7, 8, 10 and 11 illustrate the general test set-ups commonly used to measure CMRR, average bias current, offset voltage and current, and open loop gain, respectively. In general, the following parameters are tested under the following conditions.

COMMON MODE REJECTION

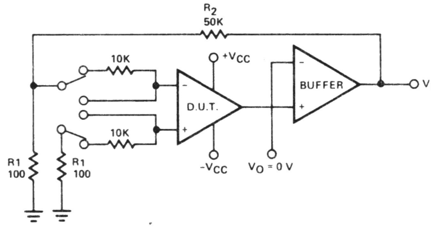
The test set-up for CMRR is given in Figure 7. Resistor values are chosen to provide sufficient sensitivity and accuracy for the device type being tested and the voltage measuring equipment being used.

The positive common mode input voltage within the range V_{CM1} is algebraically subtracted from all supply voltages and from V_O. Then V_1 is measured (V_{11}). The most negative common mode voltage within the range, V_{CM2}, is then subtracted from all the supply voltages and V_O, and V_1 is again measured (V_{12}).

Then

$$\mathrm{CMRR} = (R1 + R2)/R1\,|(V_{CM1} - V_{CM2})/V_{11} - V_{12} \qquad (9)$$

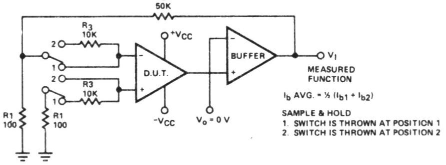
CIRCUIT DIAGRAM USED FOR CMRR MEASUREMENT



All resistor values are in ohms.

Figure 7

CIRCUIT DIAGRAM USED FOR AVERAGE BIAS CURRENT MEASUREMENT



I_b AVG. = ½ (I_{b1} + I_{b2})

SAMPLE & HOLD
1. SWITCH IS THROWN AT POSITION 1
2. SWITCH IS THROWN AT POSITION 2

All resistor values are in ohms.

Figure 8

INTEGRATED OPERATIONAL AMPLIFIER THEORY

A TYPICAL OP AMP TEST CIRCUIT (SIMPLIFIED)

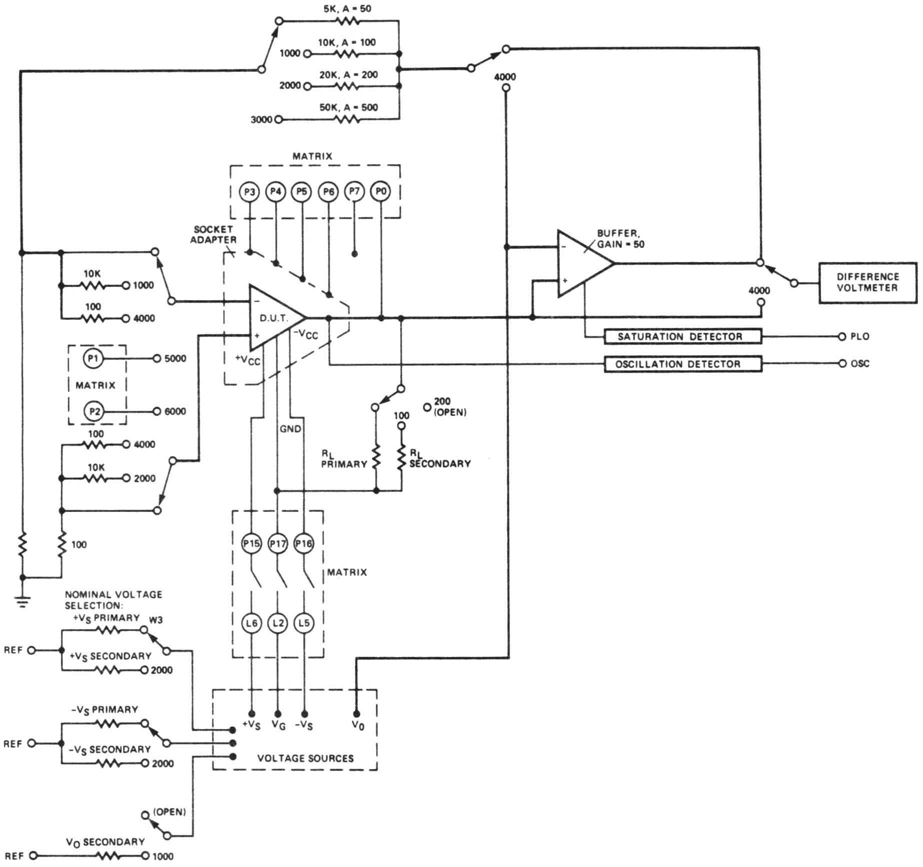
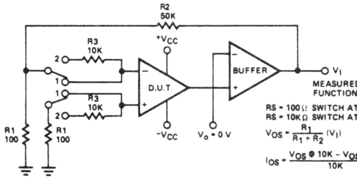

5K, A = 50
10K, A = 100
1000
20K, A = 200
2000
50K, A = 500
3000
4000
MATRIX
P3
P4
P5
P6
P7
P0
SOCKET ADAPTER
BUFFER, GAIN = 50
10K
1000
100
4000
D.U.T.
-VCC
+VCC
DIFFERENCE VOLTMETER
4000
SATURATION DETECTOR
PLO
OSCILLATION DETECTOR
OSC
P1
5000
MATRIX
P2
6000
100
4000
10K
2000
200 (OPEN)
100
RL PRIMARY
RL SECONDARY
GND
100
P15
P17
P16
MATRIX
L6
L2
L5
NOMINAL VOLTAGE SELECTION:
+VS PRIMARY
W3
REF
+VS SECONDARY
2000
-VS PRIMARY
REF
-VS SECONDARY
2000
+VS
VG
-VS
VO
VOLTAGE SOURCES
(OPEN)
VO SECONDARY
REF
1000

Figure 9

CIRCUIT DIAGRAM USED FOR OFFSET VOLTAGE AND OFFSET CURRENT


R2
50K
R3
10K
+VCC
2
1
1
R3
10K
2
D.U.T
BUFFER
VI
MEASURED FUNCTION
R1
100
R1
100
-VCC
Vo = 0 V

RS = 100Ω SWITCH AT POSITION 1
RS = 10KΩ SWITCH AT POSITION 2

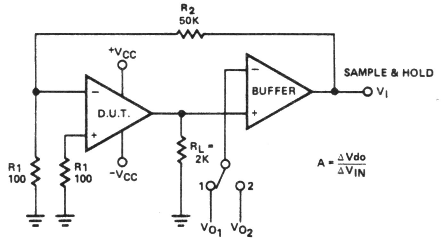
$$V_{OS} = \frac{R_1}{R_1 + R_2}(V_I)$$

$$I_{OS} = \frac{V_{OS} @ 10K - V_{OS} @ 100\Omega}{10K}$$

All resistor values are in ohms.

Figure 10

CIRCUIT DIAGRAM USED FOR LARGE-SIGNAL OPEN LOOP GAIN MEASUREMENT


R2
50K
+VCC
SAMPLE & HOLD
VI
BUFFER
D.U.T.
RL = 2K
R1
100
R1
100
-VCC
1
2
VO1
VO2

$$A = \frac{\Delta V_{do}}{\Delta V_{IN}}$$

All resistor values are in ohms.

Figure 11

This operation is equivalent to swinging both inputs over the full common mode range, and holding the output voltage constant, but it makes the V_I measurement much simpler.

BIAS CURRENT

Bias current is measured in the configuration of Figure 8.

With switches at position 1 and $V_O = 0$ volts, measure V_I1. Move switches to position 2 and again measure V_{I2}. Calculate I_{BIAS} (average), by

$$I_{B1} = \frac{R1}{R1 + R2}\left(\frac{V_1}{R3}\right) \qquad (10a)$$

$$I_{B2} = \frac{R1}{R1 + R2}\left(\frac{V_1}{R3}\right) \qquad (10b)$$

$$I_{BIAS}\ (avg) = \frac{I_{B1} + I_{B2}}{2} = \frac{R1}{R1 + R2}\ \frac{V_I1 - V_I2}{2R3} \qquad (10c)$$

OFFSET VOLTAGE

Figure 10 is used for both offset voltage and current. With V_o at 0 volts and the switches selecting the source impedance of 100 ohms, the offset voltage is measured at V_I and is equal to

$$V_{os} = \frac{R1V_1}{R1 + R2} \qquad (11)$$

OFFSET CURRENT

Offset current is measured by calculation of offset voltage change with a change in source impedance. With switches in position 1, measure V_{I2}. Calculate the contribution of I_{os} by

$$I_{os} = \frac{V_{I2} - V_I}{R3} \qquad (12)$$

SIGNAL GAIN

The signal gain of operational amplifiers is most commonly specified for the full output swing.

This is referred to as large signal voltage gain and can be measured by the circuit of Figure 11. Usually specified under a specific load determined by R_L, a signal equal to the maximum swing of the output voltage is applied to V_o in both positive and negative directions. V_{I1} and V_{I2} are measured values of V_I and and V_o = maximum positive and maximum negative signals respectively. The gain of the device under test then becomes

$$A_{vo} = \left(\frac{R1 + R2}{R1}\right)\left(\frac{V_{o1} - V_{o2}}{V_{I1} - V_{I2}}\right) \qquad (13)$$

SLEW RATE

Many other parameters are checked automatically by similar means. Only the most important ones have been covered here. Of great interest to the designer are other parameters which do not necessarily carry minimum or maximum limits. One such parameter is slew rate. The configuration used to measure slew rate depends upon the intended application. Worst case conditions arise in the unity gain non-inverting mode.

MEASURING SLEW RATE

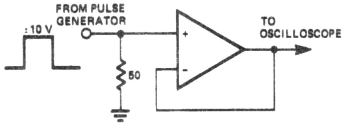


Figure 12a

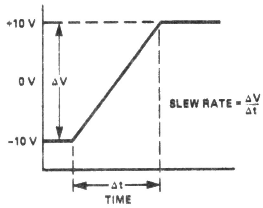


Figure 12b

Figure 12 shows a typical bench set up for measuring the response of the output to a step input. The input step frequency should be of a frequency low enough for the output of the op amp to have sufficient time to slew from limit to limit. In addition, V_{in} must be less than absolute maximum input voltage and the wave form should have good rise and fall times. The slew rate is then calculated from the slope of the output voltage versus time or

$$SR = \frac{\Delta V_{out}}{\Delta T} \text{ in volts}/\mu s \qquad (14)$$

OP AMP CURVE TRACER

Two of the most important parameters of linear integrated circuits having differential inputs are voltage gain and input offset voltage. These parameters may be read directly from a plot of the transfer characteristic of the device. This memo will describe a very simple curve tracer which, when used with an oscilloscope, will display the transfer characteristic of most Signetics linear devices.

Figure 13 shows the transfer characteristics of a typical linear device, the Signetics NE531. Note that the unit saturates at approximately +12 and −12 volts and exhibits a linear transfer characteristic between −10 and +10 volts.

TRANSFER CURVE OF 531

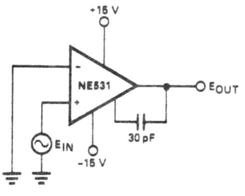


Figure 13a

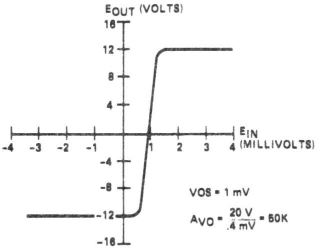


Figure 13b

From the slope of this linear portion of the transfer characteristic, and from the point and +10 volts where it crosses the E_{in} axis, the voltage gain and offset voltage may be determined. It can be seen that the voltage gain of the device under test, (D.U.T.), is 50,000 and its input offset voltage is 1.0mV.

A simple circuit to display the curves of Figure 13 on an oscilloscope is shown in Figure 14. A 60Hz, 44Vp-p sinewave is applied to the horizontal input of oscilloscope and an attenuated version of the sinewave is applied to the input of the D.U.T.

The output of the D.U.T. drives the vertical input of the scope. For providing V+and V− to the D.U.T., the tester uses two simple adjustable regulators, both current limited at 25mA. Input drive to the D.U.T. may be selected by means of S-2 as shown.

To use the curve tracer, first preset the V+ and V− supplies with an accurate meter. The supply voltages are somewhat dependent on ac line regulation and should be checked periodically. The horizontal gain of the scope may be set to give a convenient readout of the peak-to-peak D.U.T. input signal corresponding to the setting of S-2. As some devices have two outputs, a second output line (vertical 2) has been provided for these devices. The transfer function of such devices will be inverted to that of Figure 13 of course.

CURVE TRACER SCHEMATIC

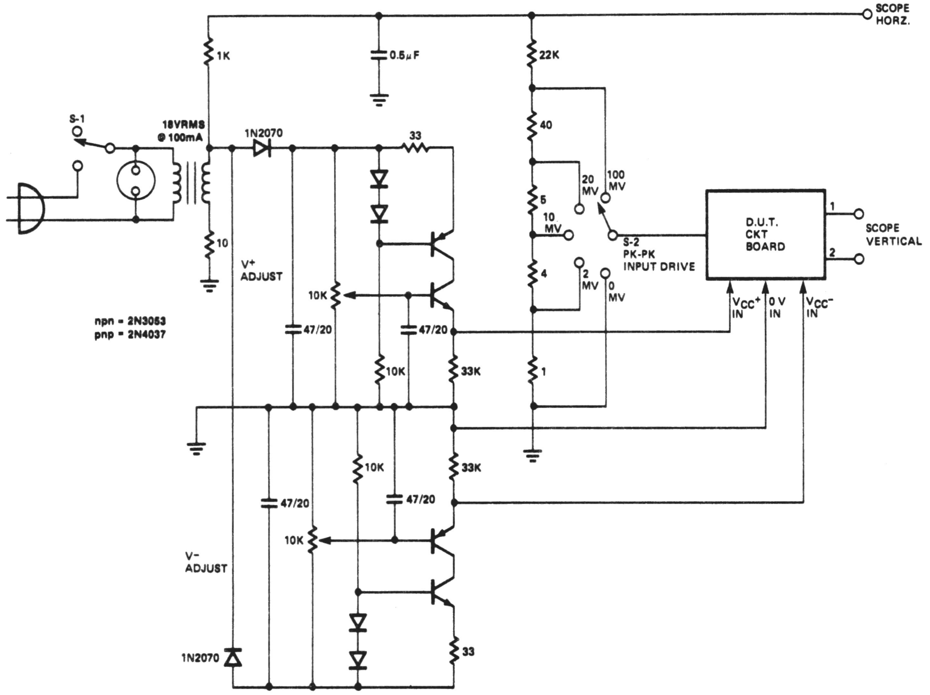


Figure 14

Simplicity and low cost are the two major attributes of this tester. It is not intended to perform highly rigorous tests for all devices. It is, however, a reasonably accurate means of determining the gains and offset voltages of most amplifiers. It will in addition, indicate the transfer curves of comparators and sense amplifiers with equivalent accuracies.

AMPLIFIER DESIGN

Linear operational amplifier IC's were introduced soon after the appearance of the first digital integrated circuits. The performance of these early devices, however, left much to be desired until the introduction of the 709 device. Even with its lack of short circuit protection and its complicated compensation requirements, the 709 gained real acceptance for the IC op amp. The 709 was designed using a three stage approach requiring both input and output stage compensation. In addition the output stage was not short circuit proof and the input stage latched up under certain conditions, requiring external protection.

Much better designs soon were introduced. Among the contenders were the 741, 748, 101, and 107 devices. All were general purpose devices with single capacitor compensation, (some were internally compensated), and all heralded input and output overstress protection. The basic design has two gain stages. By rolling off the frequency response of one of these (the second stage), so that the overall gain is unity at a frequency below the point where excess phase becomes significant, the device can be stabilized for all feedback configurations. Further, by making the first stage a voltage to current converter, with a small g_m and the second stage a current to voltage converter with a high r_m, the second stage can be rolled off at 6dB octave with a small value capacitor in the order of 30pF, which can then be built into the device itself. This concept is shown in Figure 15.

BASIC TWO STAGE OP AMP DESIGN

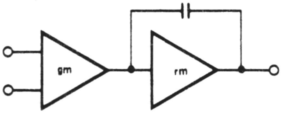


Figure 15

The frequency and phase response of the pnp devices in the first stage dictate a roll off in the second stage to give a loop gain of unity at about 1.0MHz. For the unity gain feedback configuration, this implies an open loop gain of unity at this frequency. The capacitor C_c controls this parameter by looking much smaller than r_m at frequencies above a few cycles, giving a clean 6dB/octave roll off over 5 decades.

The overall gain at frequencies where the impedance of C_c dominates r_m is given by

$$A_V(\omega) = \frac{qI_{s1}}{4KT} \bullet \frac{1}{\omega C_c} \qquad (15)$$

Substituting the value given, we find that a capacitance of $C_c = 30pF$ gives a unity gain frequency of about 1.0MHz.

First stage large signal current also defines the slew rate for a specific compensation technique. It is this current which must charge and discharge the C_C by the expression

$$SR = \frac{dV}{dT} = \frac{I_{LS}}{C_C} \qquad (16)$$

where I_{LS} is the largest signal current of the input stage. Obviously, the slew rate can be improved by increasing the first stage collector current. This would, however, reflect directly upon the bias current by increasing it.

Two serious limitations, then, of these devices for diverse applications are input bias current and slew rate. Both may be overcome with small changes of the input structure to yield higher performance devices.

Reducing the input bias current becomes a matter of raising the transistor beta of the first stage. Several current designs boasting very low input currents use what is termed super beta input devices. These transistors have betas of 1,500 to 7,000. Bias currents under 2nA can be achieved in this way. Even though the B_{VCEO} of such transistors can be as low as 1 volt, the lower breakdowns are accounted for in the input stage by rearranging the bias technique. Bandwidths and slew rates suffer only slightly as a result of the lower current levels.

The second limitation of 741 devices is slew rate. As previously mentioned, the rate of change is dictated by the compensation capacitance as charged by the large signal current of the first stage. By altering the large signal gm of the first stage as depicted by Figure 18, the slew rate can be dramatically increased.

The additional current supplied during large signal swings by current source I_4 causes the first stage transfer function to change as shown in Figure 19. The compensation capacitor is returned to the output of the NE531 structure because the output driving source must be capable of supplying the increased current to charge the capacitor.

Large signal bandwidths with this input structure will be essentially the same as the small signal response. Full bandwidth possibilities of this configuration are still limited by the beta and f_t of the lateral pnp devices used for collector loads in the first stage. Even so, the slew rate of the NE531 and NE538 is a factor of 40 better than general purpose devices.

INPUT STRUCTURE OF 531

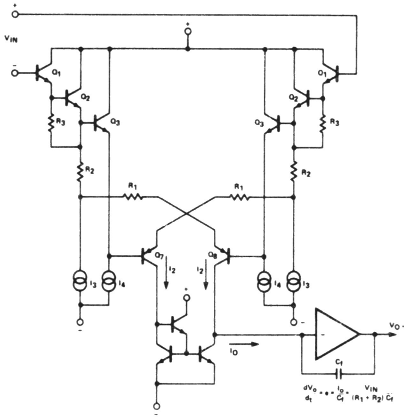


Figure 18

VOLTAGE/CURRENT CURVES OF FIRST STAGE

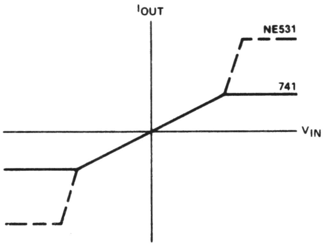


Figure 19

BASIC FEEDBACK THEORY

Earlier, the ideal op amp was defined. The ideal parameters are never fully realized but they present a very convenient method for the preliminary analysis of circuitry. So important are these ideal definitions that they are repeated here. The ideal amplifier possesses.

1. Infinite gain
2. Infinite input impedance
3. Infinite bandwidth
4. Zero output impedance

From these definitions two important theorems are developed:

1. No current flows into or out of the input terminals.
2. When negative feedback is applied the differential input voltage is reduced to zero.

Keeping these rules in mind, the basic concept of feedback can be explored.

VOLTAGE FOLLOWER

Perhaps the most often used and simplest circuit is that of a voltage follower. The circuit of Figure 1 illustrates the simplicity.

VOLTAGE FOLLOWER

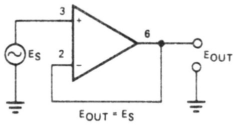


Figure 1

Applying the zero differential input theorem the voltages of pins 2 and 3 are equal and since pins 2 and 6 are tied together, their voltage is equal; hence, $E_{out} = E_{in}$. Trivial to analyze, the circuit nevertheless does illustrate the power of the zero differential voltage theorem. Because the input impedance is multiplied and the output impedance divided by the loop gain the voltage follower is extremely useful for buffering voltage sources and for impedance transformation.

The basic configuration in Figure 1 has a gain of 1 with extremely high input impedance. Setting the feedback resistor equal to the source impedance will cancel the effects of bias current if desired. However, for most applications a direct connection from output to input will suffice. Errors arise from offset voltage, common mode rejection ratio and gain. The circuit can be used with any op amp with the required unity gain compensation, if it is required.

NON-INVERTING AMPLIFIER

Only slightly more complicated is the non-inverting amplifier of Figure 2.

NON-INVERTING AMPLIFIER

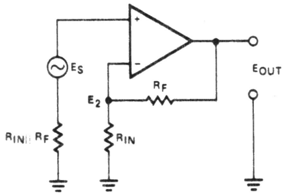


Figure 2

The voltage appearing at the inverting input is defined by

$$E_2 = \frac{E_{out} \cdot R_{in}}{R_F + R_{in}} \qquad (1a)$$

Since the differential voltage is zero, $E_2 = E_s$, and the output voltage becomes

$$E_{out} = E_s \left(1 + \frac{R_F}{R_{in}}\right) \qquad (1b)$$

It should be noted that as long as the gain of the closed loop is small compared to open loop gain, the output will be accurate, but as the closed loop gain approaches the open loop value more error will be introduced.

The signal source is shown in Figure 2 in series with a resistor equal in size to the parallel combination of R_{in} and R_F. This is desirable because the voltage drops due to bias currents to the inputs are equal and cancel out even over temperature. Thus overall performance is much improved.

The amplifier does not phase invert and possesses high input impedance. Again the impedances of the two inputs should be equal to reduce offsets due to bias currents.

INVERTING AMPLIFIER

By slightly rearranging the circuit of Figure 2, the non-inverting amplifier is changed to an inverting amplifier. The circuit gain is found by applying both theorems; hence, the voltage at the inverting input is 0 and no current flows into the input. Thus the following relationships hold.

$$\frac{E_s}{R_{in}} + \frac{E_o}{R_F} = 0 \qquad (2a)$$

Solving for the output E_o

$$E_o = -E_s \frac{R_F}{R_{in}} \qquad (2b)$$

INVERTING AMPLIFIER

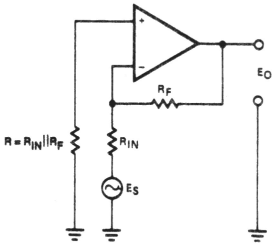


Figure 3

As opposed to the non-inverting circuits the input impedance of the inverting amplifier is not infinite but becomes essentially equal to R_{in}. This circuit has found widespread acceptance because of the ease with which input impedance and gain can be controlled to advantage, as in the case of the summing amplifier.

With the inverting amplifier of Figure 3 the gain can be set to any desired value defined by R divided by R_{IN}. Input impedance is defined by the value or R_{IN} and R should equal the parallel combination or R_{IN} and R to cancel the effect of bias current. Offset voltage, offset current, and gain contribute most of the errors. The ground may be set anywhere within the common mode range and any op amp will provide satisfactory response.

CURRENT TO VOLTAGE CONVERTER

The transfer function of the current to voltage converter is

$$V_{out} = I_n R1 \qquad (3)$$

Evaluation of the circuit depends upon the virtual ground theorem developed earlier. The current flowing into the input must be the same as that flowing across R1, hence, the output voltage is the IR drop of R1.

Limitations, of course, are output saturation voltage and output current capability. The inputs may be biased anywhere within the common mode range.

BASIC FEEDBACK THEORY

DIFFERENTIAL AMPLIFIER

This circuit of Figure 5 has a gain with respect to differential signals of R2/R1.

The common mode rejection is dominated by the accuracy of the resistors. Other errors arise from the offset voltage, input offset current, gain and common mode rejection. The circuit can be used with any op amp discussed in this chapter with the proper compensation.

SUMMING AMPLIFIER

The summing amplifier is a variation of the inverting amplifier. The output is the sum of the input voltages, each being weighed by—R_F/R_{IN}.

The value of R4 may be chosen to cancel the effects of bias current and is selected equal to the parallel combination of R_F and all the input resistors.

INTEGRATOR

Integration can be performed with a variation of the inverting amplifier by replacing the feedback resistor with a capacitance. The transfer function is defined by

$$V_{OUT} = -\frac{1}{RC}\int_0^t V_{IN} \bullet dt \tag{4}$$

The gain of the circuit falls at 6dB per octave over the range in which strays and leakages are small.

Since the gain at dc is very high a method for resetting initial conditions is necessary. Switch S1 removes the charge on the capacitor. A relay or FET may be used in the practical circuit. Bias and offset currents and offset voltage of the switch should be low in such an application.

CURRENT TO VOLTAGE CONVERTER

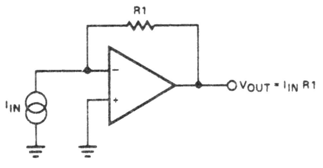


Figure 4

INTEGRATOR

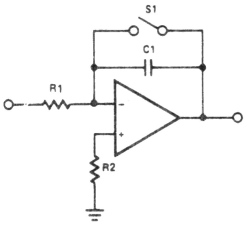


Figure 7

DIFFERENTIAL AMPLIFIER

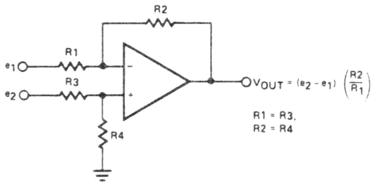


Figure 5

SUMMING AMPLIFIER

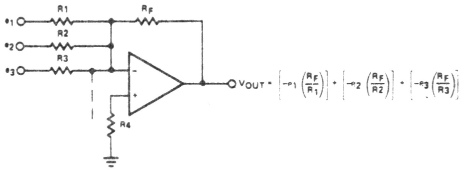


Figure 6

DIFFERENTIATOR

The differentiator of Figure 8 is another variation of the inverting amplifier. The gain increase at 6dB per octave until it intersects the amplifier open loop gain, then decreases because of the amplifier bandwidth. This characteristic can lead to instability and high frequency noise sensitivity.

DIFFERENTIATOR

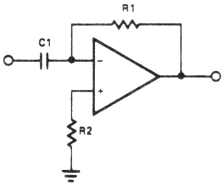


Figure 8

A more practical circuit is shown in Figure 9. The gain has been reduced by R3 and the high frequency gain reduced by C2 allowing better phase control and less high frequency noise. Compensation should be for unity gain.

PRACTICAL DIFFERENTIATOR

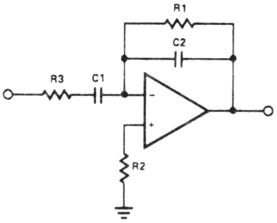


Figure 9

COMPENSATION

Present day operational amplifiers are comprised of multiple stages, each of which has a 3dB point or pole associated with it. Referring to Figure 10, the 3dB break points of a two stage amplifier are approximated by the Bode plot.

As with any feedback loop, the op amp must be protected from phase shifts in excess of 360°. A steady 180° phase shift is developed by the amplifier from output to inverting input. In addition the sum of all additional shifts due to amplifier poles or feedback component poles will cause the necessary additional 180° to sustain oscillation if the

FREQUENCY COMPENSATION

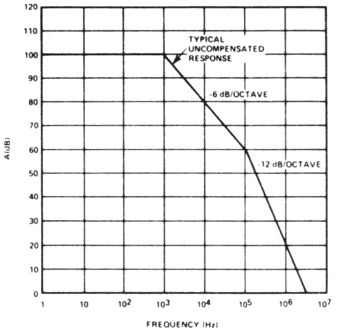


Figure 10

gain of the amplifier is greater than one for the frequency at which the 180° phase shift is reached. By adding poles and zeros to the amplifier response externally, the phase shift can be controlled to insure stability.

Many op amps now include internal compensation. These are single capacitors of 30pF typically and the amplifier will remain stable for all gains. However, since they are unconditionally stable, the compensation is larger than required for most applications. The resultant loss of bandwidth and slew rate may be acceptable in the general case but selection of an externally compensated device can add a great deal to the amplifier response if the compensation is handled properly.

In order to fully develop the point at which instability occurs a fuller understanding of phase response is necessary.

The diagram of Figure 11 depicts the phase shift of a single pole. Note that at the pole position the phase shift is 45° and that phase shift becomes 0° for a decade below the pole adn −90° for a decade above the pole location. This is a Bode approximation which possesses a 5.7° error at 0° and 90° but this error is usually considered small enough to be ignored. The single pole produces a maximum of 90° phase shift and also produces a frequency roll off of 20dB per decade. The addition of the second pole of Figure 12 produces an additional 90° phase shift and increases the role off slope to −40dB per decade.

SINGLE POLE AMPLITUDE AND PHASE RESPONSE

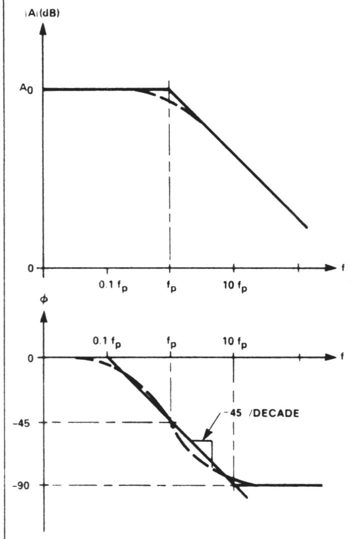


Figure 11

TWO POLE CLOSED LOOP RESPONSE

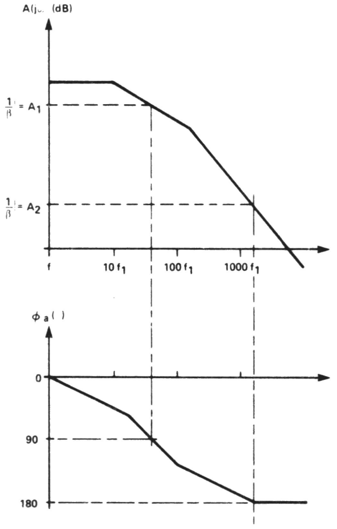


Figure 12

At this point phase shift could exceed 180° because unity gain is reached causing stability. For gain levels equal to A1 or $1/\beta$, the phase shift is only 90° and the amplifier is stable. However, the gain of A2 the phase shift is 180° and the loop is unstable. Gains in between A1 and A2 are marginally stable. However, as shown in Figure 13 the phase shift as it approaches 180° causes increasing frequency peaking and overshoot until sustained oscillations occur.

FREQUENCY PEAKING DUE TO INSUFFICIENT PHASE MARGIN

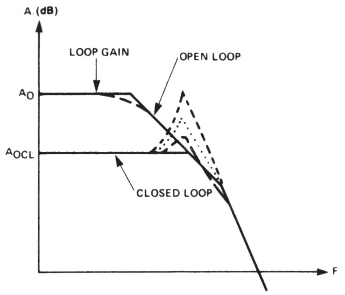


Figure 13

It is generally accepted in the interest of minimized frequency peaking to limit the phase shift of the amplifier to 135° or a phase margin of 45°. At this margin the second order response of the system is critically damped and oscillation is prevented.

Referring to Figure 14, the required compensation can be determined. Given the open loop response of the amplifier, the desired gain is plotted until it intercepts the open loop curve as shown.

FREQUENCY COMPENSATION

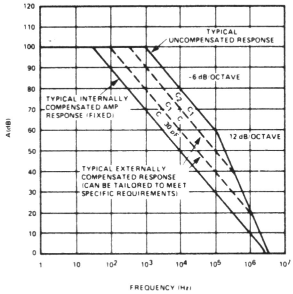


Figure 14

The phase shift for minimum peaking is 135°. Remembering that phase shift is 45° at the frequency pole the example of Figure 14 will be unstable at gains less than 20dB where phase shift exceeds 180°, and will possess excessive overshoot and ringing at gains less than 60dB where phase shift exceeds 135°. Thus, the desired compensation will move the second pole of the amplifier out in frequency until the closed loop gain intersects the open loop response before the second break of the amplifier occurs. Selecting only enough compensation to do the job assures the maximum bandwidths and slew rates of the amplifier. Additional in-depth information on compensation can be found in the reference material.

FEED FORWARD COMPENSATION

External compensation has been shown to improve amplifier bandwidth over internal compensation in the preceding section. Additional bandwidth can be realized if feed forward compensation is used. Bandwidth is limited in monolithic design by the poor frequency response of the pnp level shifters of the first stage.

TECHNIQUE OF FEED FORWARD AROUND 1st STAGE

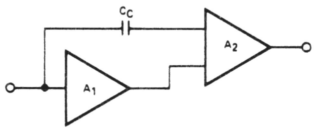


Figure 15

FREQUENCY RESPONSE WITH FEED FORWARD COMPENSATION

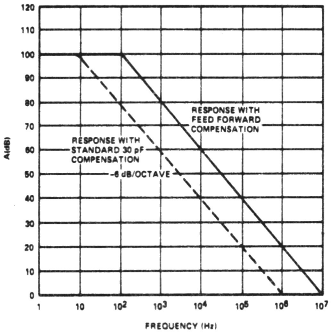


Figure 16

The concept of feed forward compensation bypasses the input stage at high frequencies driving the higher frequency second stage directly as pictured by Figure 15. The Bode plot of Figure 16 shows the additional response added by the feed forward technique. The response of the original amplifier requires less compensation at lower frequencies allowing an order of magnitude improvment in bandwidth. Standard compensation and feed forward are both plotted to illustrate the bandwidth improvement. Unfortunately, the use of feed forward compensation is restricted to the inverting amplifier mode.

REFERENCES

1. *OPERATIONAL AMPLIFIERS-Design & Applications*, Jerald Graeme and Gene Tobey, McGraw Hill Book Company.

AUDIO CIRCUITS USING THE NE5532/33/34 AN142

AUDIO CIRCUITS USING THE NE5532/33/34

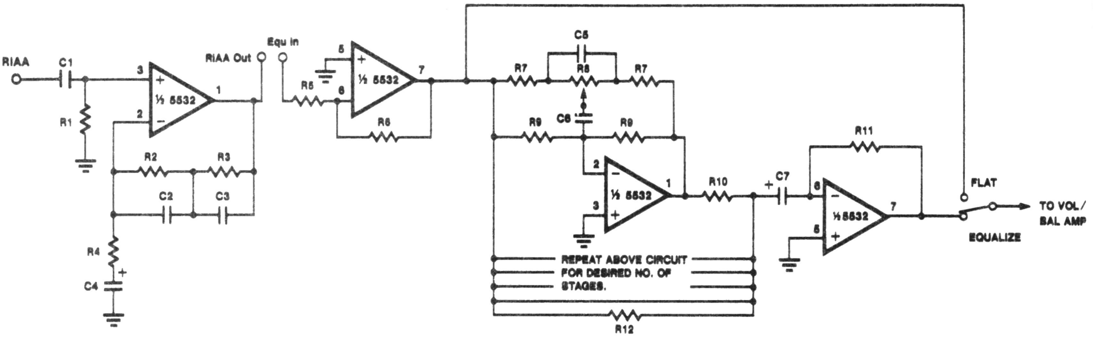
More detailed information is available in the communications section of this manual, regarding other audio circuits. The following will explain the Signetics line of low noise op amps and show their use in some audio application.

DESCRIPTION

The 5532 is a dual high-performance low noise operational amplifier. Compared to most of the standard operational amplifiers, such as the 1458, it shows better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

This makes the device especially suitable for application in high quality and professional audio equipment, instrumentation and control circuits, and telephone channel amplifiers. The op amp is internally compensated for gains equal to one. If very low noise is of prime importance, it is

RIAA—EQUALIZER SCHEMATIC



COMPONENT VALUE TABLES

R8 = 25k R7 = 2.4k R9 = 240k			R8 = 50k R7 = 5.1k R9 = 510k			R8 = 100k R7 = 10k R9 = 1meg		
fo	C5	C6	fo	C5	C6	fo	C5	C6
23 Hz	1µF	.1µF	25 Hz	.47µF	.047µF	12 Hz	.47µF	.047µF
50 Hz	.47µF	.047µF	36 Hz	.33µF	.033µF	18 Hz	.33µF	.033µF
72 Hz	.33µF	.033µF	54 Hz	.22µF	.022µF	27 Hz	.22µF	.022µF
108 Hz	.22µF	.022µF	79 Hz	.15µF	.015µF	39 Hz	.15µF	.015µF
158 Hz	.15µF	.015µF	119 Hz	.1µF	.01µF	59 Hz	.1µF	.01µF
238 Hz	.1µF	.01µF	145 Hz	.082µF	.0082µF	72 Hz	.082µF	.0082µF
290 Hz	.082µF	.0082µF	175 Hz	.068µF	.0068µF	87 Hz	.068µF	.0068µF
350 Hz	.068µF	.0068µF	212 Hz	.056µF	.0056µF	106 Hz	.056µF	.0056µF
425 Hz	.056µF	.0056µF	253 Hz	.047µF	.0047µF	126 Hz	.047µF	.0047µF
506 Hz	.047µF	.0047µF	360 Hz	.033µF	.0033µF	180 Hz	.033µF	.0033µF
721 Hz	.033µF	.0033µF	541 Hz	.022µF	.0022µF	270 Hz	.022µF	.0022µF
1082 Hz	.022µF	.0022µF	794 Hz	.015µF	.0015µF	397 Hz	.015µF	.0015µF
1588 Hz	.015µF	.0015µF	1191 Hz	.01µF	.001µF	595 Hz	.01µF	.001µF
2382 Hz	.01µF	.001µF	1452 Hz	.0082µF	820pF	726 Hz	.0082µF	820pF
2904 Hz	.0082µF	820pF	1751 Hz	.0068µF	680pF	875 Hz	.0068µF	680pF
3502 Hz	.0068µF	680pF	2126 Hz	.0056µF	560pF	1063 Hz	.0056µF	560pF
4253 Hz	.0056µF	560pF	2534 Hz	.0047µF	470pF	1267 Hz	.0047µF	470pF
5068 Hz	.0047µF	470pF	3609 Hz	.0033µF	330pF	1804 Hz	.0033µF	330pF
7218 Hz	.0033µF	330pF	5413 Hz	.0022µF	220pF	2706 Hz	.0022µF	220pF
10827 Hz	.0022µF	220pF	7940 Hz	.0015µF	150pF	3970 Hz	.0015µF	150pF
15880 Hz	.0015µF	150pF	11910 Hz	.001µF	100pF	5955 Hz	.001µF	100pF
23820 Hz	.001µF	100pF	14524 Hz	820pF	82pF	7262 Hz	820pF	82pF
			17514 Hz	680pF	68pF	8757 Hz	680pF	68pF
			21267 Hz	560pF	56pF	10633 Hz	560pF	56pF
						12670 Hz	470pF	47pF
						18045 Hz	330pF	33pF

COMPONENT VALUES

R1	1meg	C1	.22µF
R2	100k	C2	750pF
R3	1meg	C3	.0033µF
R4	1.1k	C4	33µF
R5	100k	C5	SEE TABLE
R6	100k	C6	SEE TABLE
R7	SEE TABLE	C7	2.2µF
R8	(pot) SEE TABLE		
R9	SEE TABLE		
R10	100k		
R11	100k		
R12	20k (5 STAGES)		

Figure 1

recommended that the 5532A version be used which has guaranteed noise voltage specifications.

APPLICATIONS

The Signetics 5532 High Performance Op Amp is an ideal amplifier for use in high quality and professional audio equipment which requires low noise and low distortion.

The circuit included in this application note has been assembled on a P.C. board, and tested with actual audio input devices (Tuner and Turntable). It consists of an RIAA pre-amp, input buffer, 5-band equalizer, and mixer. Although the circuit design is not new, its performance using the 5532 has been improved.

The RIAA pre-amp section is a standard compensation configuration with low frequency boost provided by the Magnetic cartridge and the RC network in the op amp feedback loop. Cartridge loading is accomplished via R1. 47k was chosen as a typical value, and may differ from cartridge to cartridge.

The Equalizer section consists of an input buffer, 5 active variable band pass/notch (depending on R9's setting) filters, and an output summing amplifier. The input buffer is a standard unity gain design providing impedance matching between the pre amplifiers and the equalizer section. Because the 5532 is internally compensated, no external compensations required. The 5-band active filter section is actually 5 individual active filters with the same feedback design for all 5. The main difference in all five stages is the values of C5 and C6 which are responsible for setting the center frequency of each stage. Linear pots are recommended for R9. To simplify use of this circuit, a component value table is provided, which lists center frequencies and their associated capacitor values. Notice that C5 equals (10) C6, and that the Value of R8 and R10 are related to R9 by a factor of 10 as well. The values listed in the table are common and easily found standard values.

RIAA EQUALIZATION AUDIO PREAMPLIFIER USING NE5532A

With the onset of new recording techniques along with sophisticated playback equipment, a new breed of low noise operational amplifiers was developed to complement the state-of-the-art in audio reproduction. The first ultra low noise op amp introduced by Signetics was called the NE5534A. This is a single operational amplifier with less than 4nV/$\sqrt{\text{Hz}}$ input noise voltage. The NE5534A is internally compensated at a gain of three. This device has been used in many audio preamp and equalizer (active filter) applications since its introduction early last year.

Many of the amplifiers that are being designed today are dc coupled. This means that very low frequencies (2-15Hz) are being amplified. These low frequencies are common to turntables because of rumble and tone arm resonancies. Since the amplifiers can reproduce these sub-audible tones, they become quite objectionable because the speakers try to reproduce these tones. This causes non-linearities when the actual recorded material is amplified and converted to sound waves.

The RIAA has proposed a change in its standard playback response curve in order to alleviate some of the problems that were previously discussed. The changes occur primarily at the low frequency range with a slight modification to the high frequency range. (See Figure 2). Note that the response peak for the bass section of the playback curve now occurs at 31.5Hz and begins to roll off below that frequency. The rolloff occurs by introducing a fourth R/C network with a 7950μs time constant to the three existing networks that make up the equalization circuit. The high end of the equalization curve is extended to 20kHz, because recordings at these frequencies are achievable on many current discs.

NE5533/34 DESCRIPTION

The 5533/5534 are dual and single high-performance low noise operational amplifiers. Compared to other operational amplifiers such as TL083, they show better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

This makes the devices especially suitable for application in high quality and professional audio equipment, in instrumentation and control circuits and telephone channel amplifiers. The op amps are internally compensated for gain equal to, or higher than, three. The frequency response can be optimized with an external compensation capacitor for various applications (unity gain amplifier, capacitive load, slew-rate, low overshoot, etc.) If very low noise is of prime importance, it is recommended that the 5533A/5534A version be used which has guaranteed noise specifications.

PROPOSED RIAA PLAYBACK EQUALIZATION

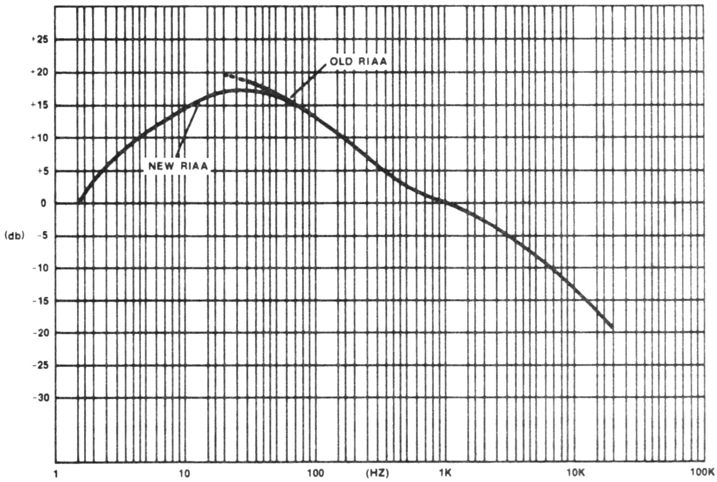
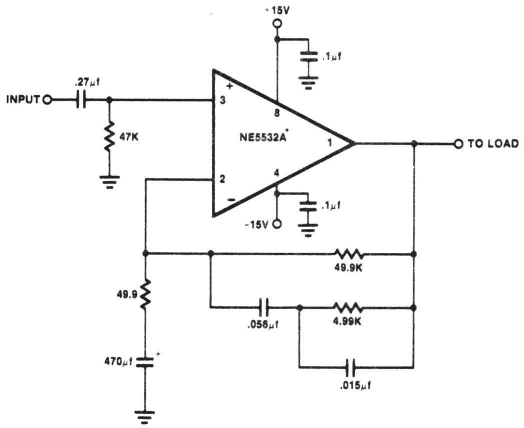


Figure 2

RIAA PHONOGRAPH PREAMPLIFIER USING THE NE5532A


+15V
.1μf
.27μf
INPUT
47K
NE5532A*
3
8
1
2
4
+
-
-15V
.1μf
TO LOAD
49.9K
49.9
.056μf
4.99K
470μf
.015μf

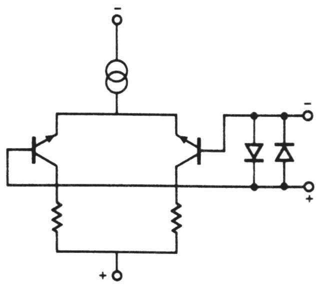
* 1/2 OF DUAL OPERATIONAL AMPLIFIER

NOTE
All resistors are 1% metal film and are valued in

Figure 3

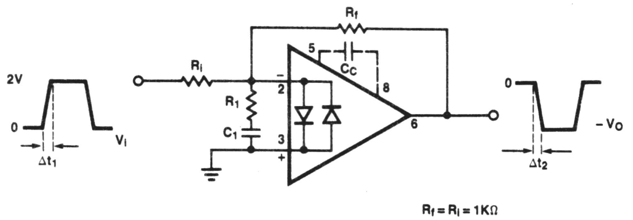
APPLICATIONS

Diode Protection of Input



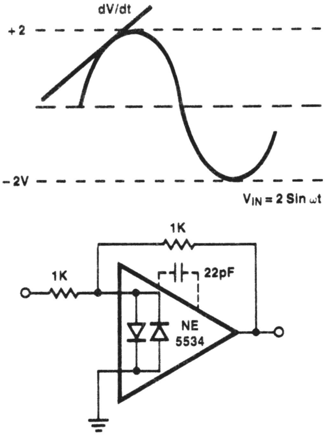
The input leads of the device are protected from differential transients above ±0.6V by internal back-to-back diodes. Their presence imposes certain limitations on the amplifier dynamic characteristics related to closed-loop gain and slew rate.

Consider the unity gain follower as an example:


2V
0
Δt₁
Vᵢ
Rf
Rᵢ
R₁
C₁
Cc
5
8
2
3
6
-
+
0
-Vo
Δt₂
Rf = Rᵢ = 1KΩ

Assume a signal input square wave with dV/dt of 250V per μs and 2V peak amplitude as shown. If a 22 pF compensation capacitor is inserted and the R_1 C_1 circuit deleted, the device slew rate falls to approximately 7V/μs. The input waveform will reach 2V/250V/μs or 8 ns, while the output will have changed (8×10^{-3}) (7) only 56 mV. The differential input signal is then $(V_{IN} - V_O)\ R_i/R_i + R_f$ or approximately 1V.

The diode limiter will definitely be active and output distortion will occur; therefore, $V_{in} < 1V$ as indicated.


dV/dt
+2
-2V
$V_{IN} = 2 \sin \omega t$
1K
1K
22pF
NE
5534

Next, a sine wave input is used with a similar circuit.

The slew rate of the input waveform now depends on frequency and the exact expression is

$$\frac{dv}{dt} = 2\omega \cos \omega t$$

The upper limit before slew rate distortion occurs for *small signal* ($V_{IN} < 100$ mV) conditions is found by setting the slew rate to 7V/μs. That is:

$$7 \times 10^6\ V/\mu s = 2\omega \cos \omega t$$

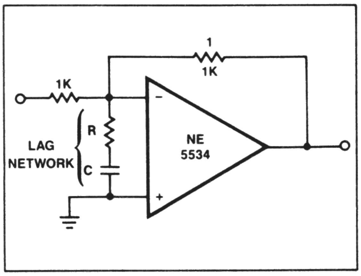
at $\omega t = 0$

$$\omega_{LIMIT} = \frac{7 \times 10^6}{2} = 3.5 \times 10^6 \text{ rad/s}$$

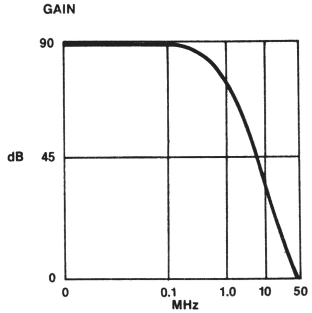
$$f_{LIMIT} \frac{3.5 \times 10^6}{2\pi} \cong 560 \text{ kHz}$$

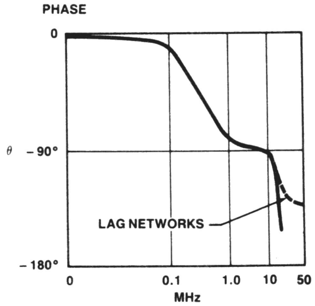
External Compensation Network Improves Bandwidth

By using an external lead-lag network, the follower circuit slew rate and small signal bandwidth can be increased. This may be useful in situations where a closed-loop gain less than 3 to 5 is indicated. A number of examples are shown in subsequent figures. The principle benefit of using the network approach is that the full slew rate and bandwidth of the device is retained, while impulse-related parameters such as damping and phase margin are controlled by choosing the appropriate circuit constants. For example, consider the following configuration:


1
1K
1K
R
LAG
NETWORK
C
NE
5534
−
+

The major problem to be overcome is poor phase margin leading to instability.





By choosing the lag network break frequency one decade below the unity gain crossover frequency (30-50 MHz), the phase and gain margin are improved. An appropriate value for R is 270Ω. Setting the lag network break frequency at 5 MHz, C may be calculated

$$C = \frac{1}{2\pi \cdot 270 \cdot 5 \times 10^6}$$

$$118 = \text{pF}$$

RULES AND EXAMPLES

Compensation Using Pins 5 and 8

(Limited Bandwidth and Slew Rate)

A single pole and zero inserted in the transfer function will give an added 45° of phase margin depending on the network values.

Calculating the Lead-Lag Network

$$C_1 = \frac{1}{2\pi F_1 R_1} \qquad \text{Let } R_1 = \frac{R_{IN}}{10}$$

$$\text{where} \quad F_1 = \frac{1}{10}(\text{UGBW})$$

$$\text{UGBW} = 30 \text{ MHz}$$

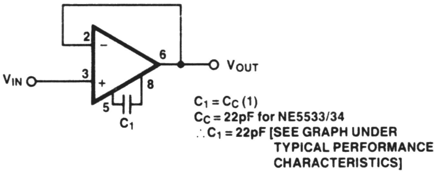

2
−
3
+
6
8
5
VIN
VOUT
C1
C1 = CC (1)
CC = 22pF for NE5533/34
∴ C1 = 22pF [SEE GRAPH UNDER TYPICAL PERFORMANCE CHARACTERISTICS]

Figure 4. Unity Gain Non-Inverting Configuration

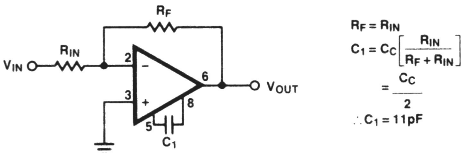
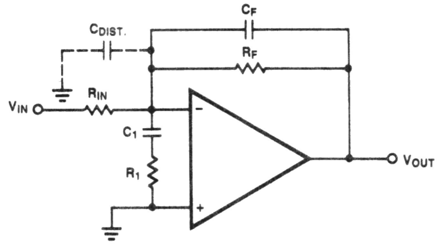

RF
RIN
VIN
2
−
3
+
6
8
5
C1
VOUT
RF = RIN
C1 = CC[RIN / (RF + RIN)]
= CC / 2
∴ C1 = 11pF

Figure 5. Unity Gain Inverting Configuration

External Compensation for Wideband Voltage Follower



NOTE: Input diodes limit differential to < 0.5V

Figure 6 . External Compensation for Wideband Voltage Follower

Shunt Capacitance Compensation

$$C_F = \frac{1}{2\pi F_F R_F}, \; F_F \cong 30\,\text{MHz}$$

or

$$C_F \cong \frac{C_{DIST}}{A_{CL}}$$

$C_{DIST} \cong$ Distributed Capacitance $\cong$ 2-3pF

Many audio circuits involve carefully tailored frequency responses. Pre-emphasis is used in all recording mediums to reduce noise and produce flat frequency response. The most often used de-emphasis curves for broadcast and home entertainment systems are shown in Figure 7. Operational amplifiers are well suited to these applications because of their high gain and easily tailored frequency response.

RIAA PREAMP USING THE NE5534

The preamplifier for phono equalization is shown in Figure 8 along with the theoretical and actual circuit response.

Low frequency boost is provided by the inductance of the magnetic cartridge with the RC network providing the necessary break points to approximate the theoretical RIAA curve.

RUMBLE FILTER

Following the amplifier stage, rumble and scratch filters are often used to improve overall quality. Such a filter designed with op amps uses the 2 pole Butterworth approach and features switchable break points. With the circuit of Figure 9 any degree of filtering from fairly sharp to none at all is switch selectable.

3.75 IPS TAPE EQUALIZATION

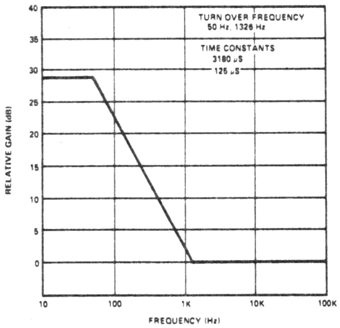


Figure 7c

RIAA EQUALIZATION

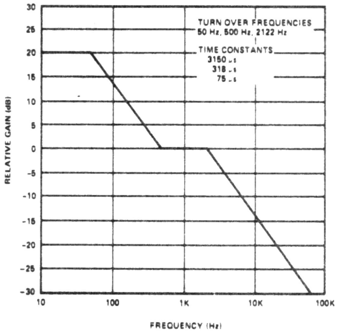


Figure 7a

BASE TREBLE CONTROL CURVE

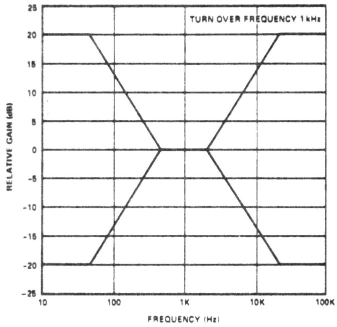


Figure 7d

NAB STANDARD PLAYBACK 7 1/2 IPS

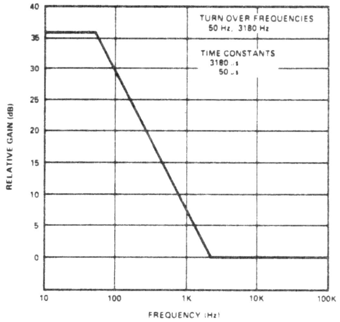


Figure 7b

STANDARD FM BROADCAST EQUALIZATION

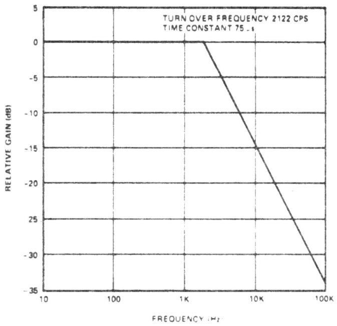
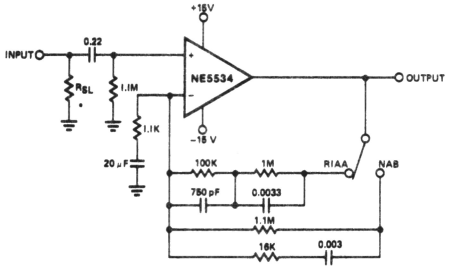


Figure 7e

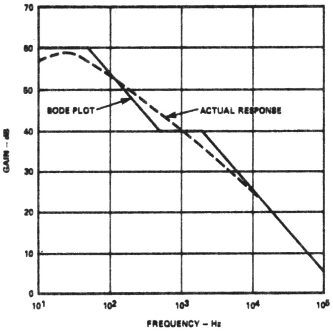
PREAMPLIFIER—RIAA/NAB COMPENSATION


+15V
INPUT
0.22
R_{SL}
*
1.1M
1.1K
20 µF
NE5534
−15 V
OUTPUT
100K
1M
RIAA
NAB
750 pF
0.0033
1.1M
16K
0.003

*Select to provide specified transducer loading.
Output Noise ≅ 0.8mV rms (with input shorted)

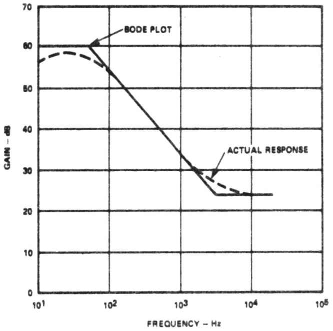
All resistor values are in ohms.

Figure 8a



Bode Plot of RIAA Equalization and the response realized in an actual circuit using the 531.

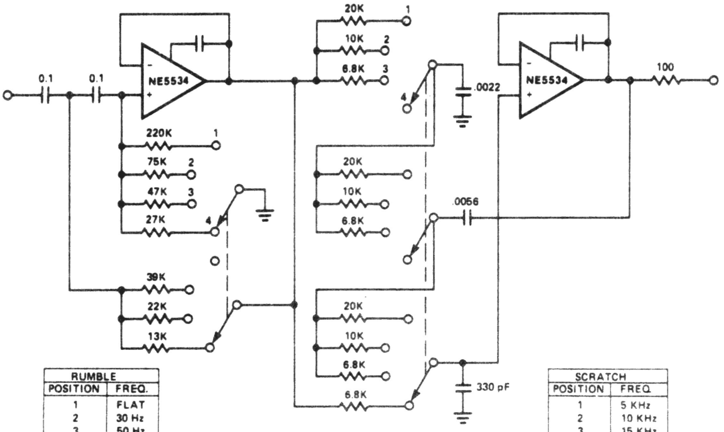
Figure 8b



Bode Plot of NAB Equalization and the response realized in the actual circuit using the 531.

Figure 8c

RUMBLE/SCRATCH FILTER


0.1
0.1
NE5534
220K
1
75K
2
47K
3
27K
4
39K
22K
13K
20K
1
10K
2
6.8K
3
4
20K
10K
6.8K
20K
10K
6.8K
6.8K
.0022
.0056
330 pF
NE5534
100

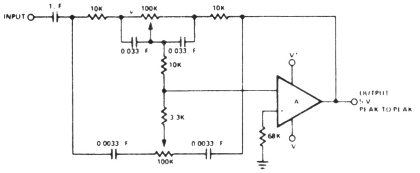
RUMBLE	
POSITION	FREQ.
1	FLAT
2	30 Hz
3	50 Hz
4	80 Hz

SCRATCH	
POSITION	FREQ.
1	5 KHz
2	10 KHz
3	15 KHz
4	FLAT

All resistor values are in ohms.

Figure 9

TONE CONTROL CIRCUIT FOR OPERATIONAL AMPLIFIERS


INPUT
1. F
10K
100K
10K
0.033. F
0.033. F
10K
3.3K
0.0033. F
100K
0.0033. F
68K
A
V+
V-
OUTPUT
5 V
PEAK TO PEAK

All resistor values are in ohms.

NOTES
1. Amplifier A may be a NE531 or 301. Frequency compensation, as for unity gain non-inverting amplifiers, must be used.
2. Turn-over frequency—1kHz.
3. Bass boost +20dB at 20Hz, bass cut -20dB at 20Hz, treble boost +19dB at 20kHz, treble cut -19dB at 20kHz.

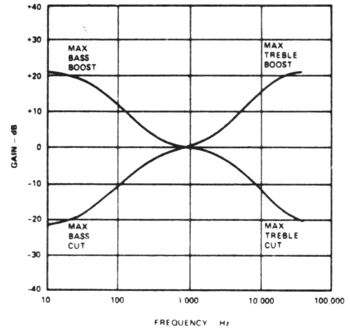


Figure 10

TONE CONTROL

Tone control of audio systems involves altering the flat response in order to attain more low frequencies or more high ones dependent upon listener preference. The circuit of Figure 10 provides 20dB of bass or treble boost or cut as set by the variable resistance. The actual response of the circuit is shown also.

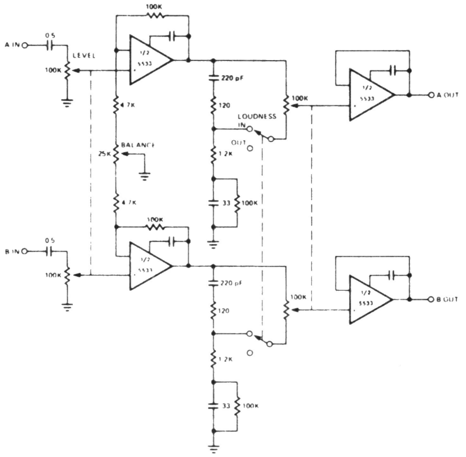
BALANCE AND LOUDNESS AMPLIFIER

Figure 11 shows a combination of balance and loudness controls. Due to the nonlinearity of the human hearing system the low frequencies must be boosted at low listening levels. Balance, level, and loudness controls provide all the listening controls to produce the desired music response.

VOLTAGE AND CURRENT OFFSET ADJUSTMENTS

Many IC amplifiers include the necessary pin connections to provide external offset adjustments. Many times, however, it becomes necessary to select a device not possessing external adjustments. Figure 12, 13, and 14 suggest some possible arrangements for offset voltage adjust and bias current nulling circuitry. The circuitry of Figure 14 provides sufficient current into the input to cancel the bias current requirement. Although more simplified arrangements are possible the addition of Q2 and Q3 provide a fixed current level to Q1, thus, bias cancellation can be provided without regard to input voltage level.

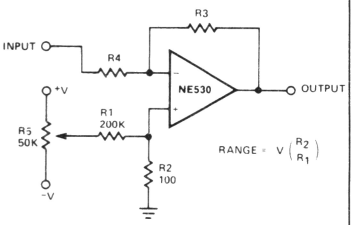
BALANCE AMPLIFIER WITH LOUDNESS CONTROL


A IN
0.5
LEVEL
100K
100K
1/2 5533
4.7K
BALANCE
25K
4.7K
220 pF
120
LOUDNESS
IN
OUT
1.2K
33
100K
100K
1/2 5533
A OUT
B IN
0.5
100K
100K
1/2 5533
220 pF
120
1.2K
33
100K
100K
1/2 5533
B OUT

All resistor values are in ohms.

Figure 11

UNIVERSAL OFFSET NULL FOR INVERTING AMPLIFIERS

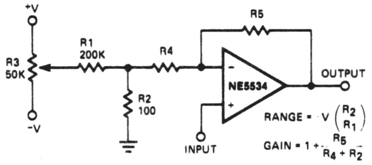

INPUT
R3
R4
NE530
OUTPUT
+V
R1
200K
R5
50K
-V
R2
100
RANGE = V (R2/R1)

All resistor values are in ohms.

Figure 12

AUDIO CIRCUITS USING THE NE5532/33/34 AN142

UNIVERSAL OFFSET NULL FOR NONINVERTING AMPLIFIERS


+V
R3
50K
-V
R1
200K
R4
R2
100
R5
NE5534
OUTPUT
INPUT

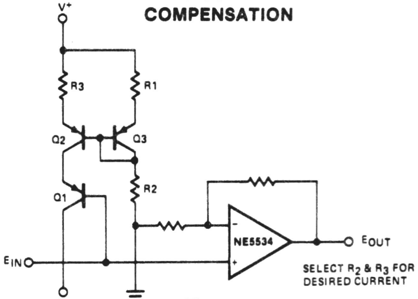
$$\text{RANGE} = V\left(\frac{R_2}{R_1}\right)$$

$$\text{GAIN} = 1 + \frac{R_5}{R_4 + R_2}$$

All resistor values are in ohms.

Figure 13

BIAS CURRENT COMPENSATION


V+
R3
R1
Q2
Q3
R2
Q1
NE5534
E_{IN}
E_{OUT}
V-

SELECT R_2 & R_3 FOR DESIRED CURRENT

Figure 14

APPLICATIONS USING THE SE/NE5535 AN143

APPLICATIONS

Introduction

The NE5535 is a new generation monolithic op amp which features improved input characterisics. The device is compensated to unity gain and has a minimum guaranteed unity gain slew rate of $10V/\mu s$. This is achieved by employing a clamped super beta input stage which has lower input bias current.

Applications

These improved parameters can be put to good use in applications such as sample and hold circuits which require low input current and in voltage follower circuits which require high slew rates. The circuit that follows will yield slew rates. The circuit that follows will yield maximum small signal transient response and slew rate for the NE5535 at unity gain.

It is always good practice in designing a system to use dual tracking regulators to power the dual supply op amps. This will guarantee the positive and negative supply voltage will be equal during power up. With the NE5535, it is possible to degrade the input circuit characteristics by not applying the power supplies simultaneously. The NE5535 is capable of directly replacing the μA741 with higher input resistance which will improve such designed as active filters, sample and hold, as well as voltage followers.

The NE5535 can be used either with single or split power supplies.

APPLICATIONS

CAPACITANCE MULTIPLIER

The circuit in Figure 1 can be used to simulate large capacitances using small value components. With the values shown and $C = 10\mu F$, an effective capacitance of $10{,}000\mu F$ was obtained. The Q available is limited by the effective series resistance. So R1 should be as large as practical.

SIMULATED INDUCTOR

With a constant current excitation, the voltage dropped across an inductance increases with frequency. Thus, an active device whose output increases with frequency can be characterized as an inductance. The circuit of Figure 2 yields such a response with the effective inductance being equal to:

$$L = R1R2C$$

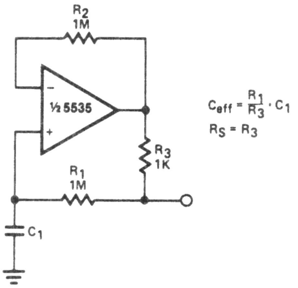
The Q of this inductance depends upon R1 being equal to R2. At the same time, however, the positive and negative feedback paths of the amplifier are equal leading to the distinct possibility of instability at high frequencies. R1 should therefore always be slightly smaller than R2 to assure stable operation.

POWER AMPLIFIER

For most applications, the available power from op amps is sufficient. There are times when more power handling capability is necessary. A simple power booster capable of driving moderate loads is offered in Figure 3.

The circuit as shown uses a NE5535 device. Other amplifiers may be substituted only if R1 values are changed because of the ICC current required by the amplifier. R1 should be calculated from the expression

$$R1 = \frac{600mV}{ICC}$$



All resistor values are in ohms.

Figure 1. Capacitance Multiplier

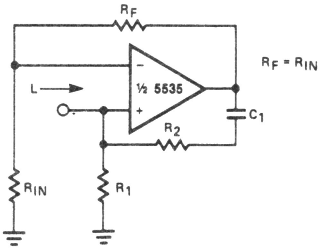
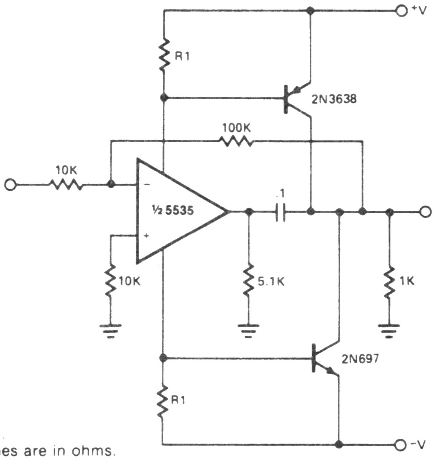


Figure 2. Virtual Inductor



All resistor values are in ohms.

Figure 3. Power Booster

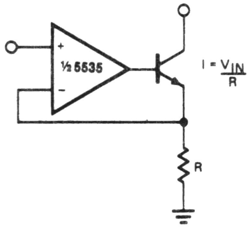


Figure 4. Voltage to Current Converters

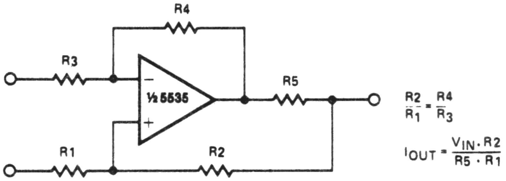

R4
R3
−
½ 5535
+
R5
R1
R2
$\frac{R2}{R1} = \frac{R4}{R3}$
$I_{OUT} = \frac{V_{IN} \cdot R2}{R5 \cdot R1}$

Figure 5. Voltage to Current Converter

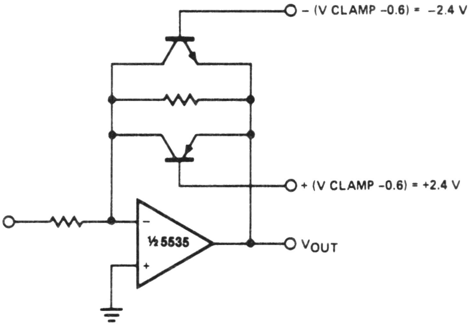
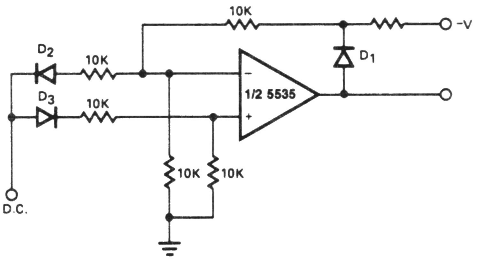


Figure 6. Active Clamp Limiting Amplifier



All resistor values are in ohms.

Figure 7. Absolute Value Amplifier

VOLTAGE-TO-CURRENT CONVERTERS

A simple voltage-to-current converter is shown in Figure 4. The current out is $I_{OUT} \cong V_{IN}/R$. For negative currents, a pnp can be used and, for better accuracy, a Darlington pair can be substituted for the transistor. With careful design, this circuit can be used to control currents of many amps. Unity gain compensation is necessary.

The circuit in Figure 5 has a different input and will produce either polarity of output current. The main disadvantages are the error current flowing in R2 and the limited current available.

ACTIVE CLAMP LIMITING AMPLIFIER

The modified inverting amplifier in Figure 6 uses an active clamp to limit the output swing with precision. Allowance must be made for the Vbe of the transistors. The swing is limited by the base-emitter breakdown of the transistors. A simple circuit uses two back-to-back zener diodes across the feedback resistor, but tends to give less precise limiting and cannot be easily controlled.

ABSOLUTE VALUE AMPLIFIER

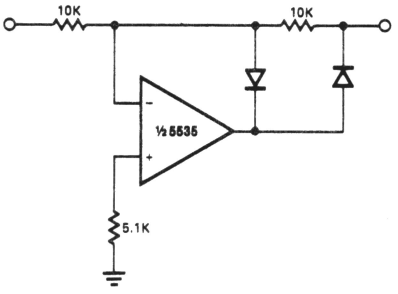
The circuit in Figure 7 generates a positive output voltage for either polarity of input. For positive signals, it acts as a non-inverting amplifier and for negative signals, as an inverting amplifier. The accuracy is poor for input voltages under 1V, but for less stringent applications, it can be effective.

HALF WAVE RECTIFIER

Figure 8 provides a circuit for accurate half wave rectification of the incoming signal. For positive signals, the gain is 0; for negative signals, the gain is −1. By reversing both diodes, the polarity can be inverted. This circuit provides an accurate output, but the output impedance differs for the two input polarities and buffering may be needed. The output must slew through two diode drops when the input polarity reverses. The NE5535 device will work up to 10kHz with less than 5% distortion.

PRECISION FULL WAVE RECTIFIER

The circuit in Figure 9 provides accurate full wave rectification. The output impedance is low for both input polarities, and the errors are small at all signal levels. Note that the output will not sink heavy currents, except a small amount through the 10kΩ resistors. Therefore, the load applied should be referenced to ground or a negative voltage. Reversal of all diode polarities will reverse the polarity of the output. Since the outputs of the amplifiers must slew through two diode drops when the input polarity changes, 741 type devices give 5% distortion at about 300Hz.


10K
10K
-
½5535
+
5.1K

All resistor values are in ohms.

Figure 8. Half Wave Rectifier

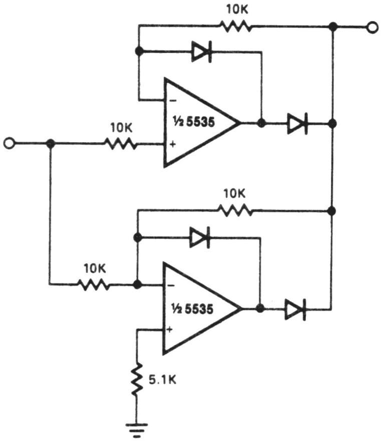
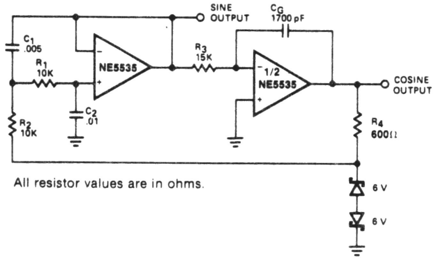

10K
-
½5535
+
10K
10K
10K
-
½5535
+
5.1K

Figure 9. Precision Full Wave Rectifier

TWO-PHASE SINE WAVE OSCILLATOR

The circuit (referring to Figure 10, uses a 2-pole pass Butterworth, followed by a phase shifting single pole stage, fed back through a voltge limiter to achieve sine and cosine outputs. The values shown using 741 amplifiers give about 1.5% distortion at the sine output and about 3% distortion at the cosine output. By careful trimming of C_G and/or the limiting network, better distortion figures are possible. The component values shown give a frequency of oscillation of about 2kHz. The values can be readily selected for other frequencies. The NE5535 should be used at higher frequencies to reduce distortion due to slew limiting.

TWO-PHASE SINE WAVE OSCILLATOR


SINE OUTPUT
CG 1700pF
C1 .005
R1 10K
NE5535
R3 15K
-1/2 NE5535
+
COSINE OUTPUT
R2 10K
C2 .01
R4 600Ω
6V
6V

All resistor values are in ohms.

Figure 10. Two-Phase Sine Wave Oscillator

APPLICATIONS FOR THE NE538 AN150

Introduction

The Signetics NE538 is the under-compensated version of the NE535. The NE538 has a typical slew rate of 50V/μs and a gain bandwidth product of 6MHz.

The internal frequency compensation is designed for a minimum inverting gain of 4 and a minimum non-inverting gain of 5. Below these gains the NE538 will be unstable and the NE535 should be used.

The higher slew rate of the NE538 has made this device quite appealing for high speed designs and the fact that it has a standard pinout will allow it to be used to upgrade existing systems that now use the μA741 or μA748.

OFFSET ADJUST CIRCUIT

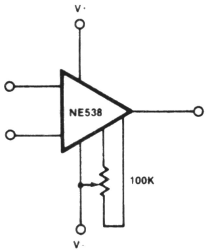
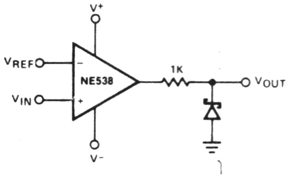


Figure 1

VOLTAGE COMPARATOR



All resistor values are in ohms.

Figure 2

VOLTAGE COMPARATOR

Inexpensive voltage comparators with only modest parameters are often needed. The op amp is often used in the configuration because the high gain provides good selectivity. Figure 2 shows a circuit usable with most any op amp. The zener is selected for the output voltage required (5.1 volt for TTL), and the resistor provides some current protection to the op amp output structure. V_{ref} can be any voltage within the wide common mode range of the amplifier—another advantage of using op amps for comparators.

CYCLIC A TO D CONVERTER

One interesting, but, much ignored A/D converter is the cyclic converter. This consists of a chain of identical stages, each of which senses the polarity of the input. The stage then subtracts V_{ref} from the input and doubles the remainder if the polarity was correct. In Figure 1 the signal is full wave rectified and the remainder of $V_{in} - V_{ref}$ is doubled. A chain of these stages gives the gray code equivalent of the input voltage in digitized form related to the magnitude of V_{ref}. Possessing high potential accuracy, the circuit using NE531 devices settles in 5μs.

TRIANGLE AND SQUARE WAVE GENERATOR

The circuit in Figure 2 will generate precision triangle and square waves. The output amplitude of the square wave is set by the output swing of the op amp A-1 and R1/R2 sets the triangle amplitude. The frequency of oscillation in either case is

$$f = \frac{1}{4RC} \cdot \frac{R2}{R1} \qquad (1)$$

The square wave will maintain 50% duty cycle even if the amplitude of the oscillation is not symmetrical.

The use of the NE531 in this circuit will allow good square waves to be generated to quite high frequencies. Since the amplifier A1 runs open loop, there is no need for compensation. The triangle-generating amplifier must be compensated.The NE5535device can be used as well, except for the lower frequency response.

CYCLIC A TO D CONVERTER

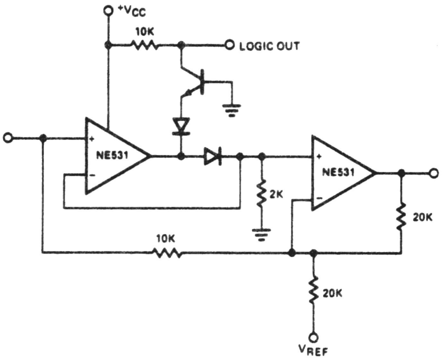


Figure 1a

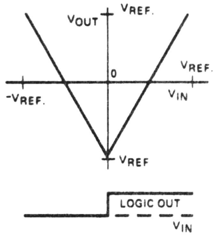


Figure 1b

TRIANGLE AND SQUARE
WAVE GENERATOR

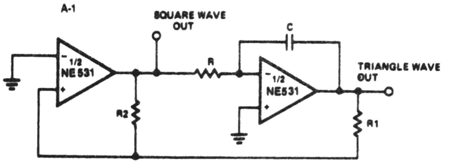


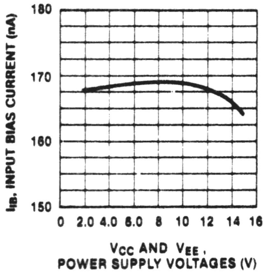
Figure 2

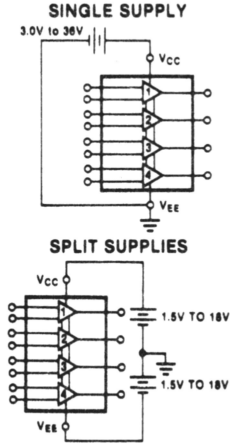
APPLICATIONS FOR THE MC3403 AN160

MC3403 DESCRIPTION

The MC3403 is a quad operational amplifier with true differential inputs. The device has electrical characteristics similar to the popular μA741. However, the MC3403 has several distinct advantages over standard operational amplifier types in single supply applications. The MC3403 can operate at supply voltages as low as 3.0V or as high as 36V. The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

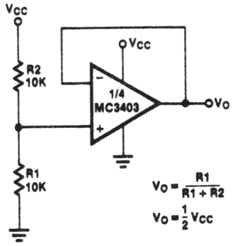
INPUT BIAS CURRENT vs SUPPLY VOLTAGE




SINGLE SUPPLY
3.0V to 36V
V_{CC}
1
2
3
4
V_{EE}
SPLIT SUPPLIES
V_{CC}
1.5V TO 18V
1.5V TO 18V
V_{EE}

APPLICATIONS

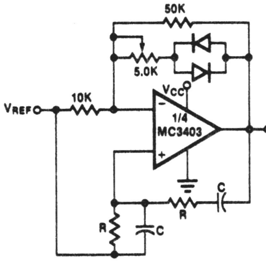
VOLTAGE REFERENCE


V_{CC}
R2 10K
V_{CC}
1/4 MC3403
V_O
R1 10K

$$V_O = \frac{R1}{R1 + R2}$$

$$V_O = \frac{1}{2} V_{CC}$$

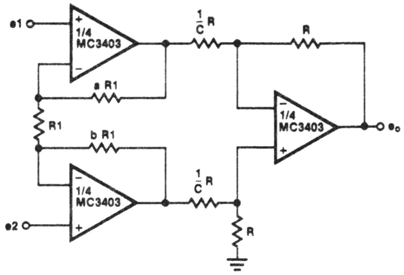
WEIN BRIDGE OSCILLATOR


50K
5.0K
V_{REF}
10K
V_{CC}
1/4 MC3403
V_O
C
R
R
C

$$f_o = \frac{1}{2\pi RC}$$

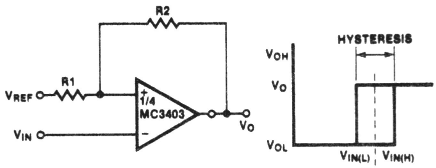
FOR $f_o = 1\text{kHz}$
$R = 16\text{k}\Omega$
$C = 0.01\mu F$

HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER


e1
1/4 MC3403
$\frac{1}{C}$ R
R
a R1
R1
b R1
1/4 MC3403
e_o
1/4 MC3403
e2
$\frac{1}{C}$ R
R

$$e_o = C(1 + a + b)(e2 - e1)$$

COMPARATOR WITH HYSTERESIS


R2
R1
V_{REF}
V_{IN}
1/4 MC3403
V_O
HYSTERESIS
V_{OH}
V_O
V_{OL}
$V_{IN(L)}$
$V_{IN(H)}$
V_{REF}

$$V_{IN(L)} = \frac{R1}{R1 + R2}(V_{OL} - V_{REF}) + V_{REF}$$

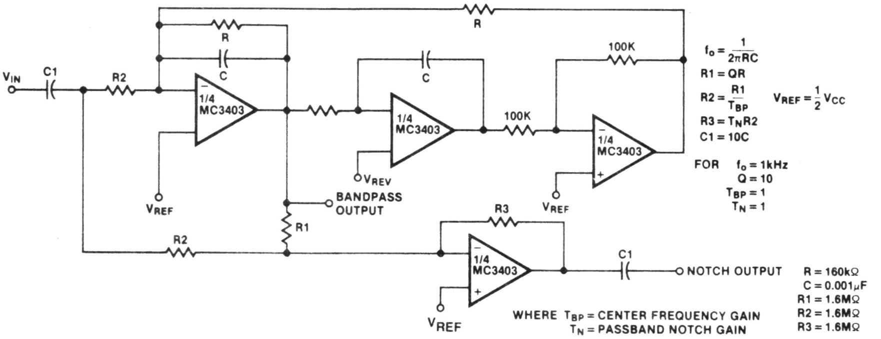
$$V_{IN(H)} = \frac{R1}{R1 + R2}(V_{OH} - V_{REF}) + V_{REF}$$

$$H = \frac{R1}{R1 + R2}(V_{OH} - V_{OL})$$

APPLICATIONS FOR THE MC3403

APPLICATIONS (Continued)

BI-QUAD FILTER


R
R
C
C
100K
V_{IN}
C1
R2
1/4 MC3403
1/4 MC3403
100K
1/4 MC3403
V_{REV}
V_{REF}
BANDPASS OUTPUT
R1
R3
V_{REF}
R2
1/4 MC3403
C1
NOTCH OUTPUT
V_{REF}

$f_o = \frac{1}{2\pi RC}$

$R1 = QR$

$R2 = \frac{R1}{T_{BP}}$ $V_{REF} = \frac{1}{2} V_{CC}$

$R3 = T_N R2$

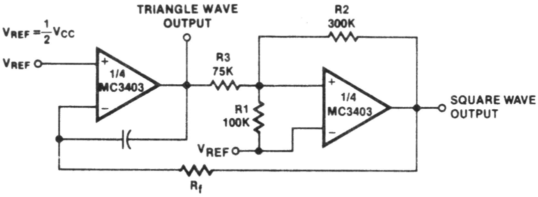
$C1 = 10C$

FOR $f_o = 1kHz$
$Q = 10$
$T_{BP} = 1$
$T_N = 1$

WHERE T_{BP} = CENTER FREQUENCY GAIN
T_N = PASSBAND NOTCH GAIN

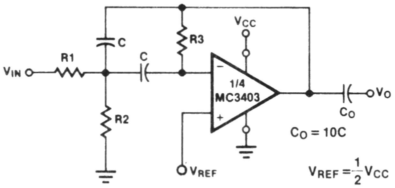
$R = 160k\Omega$
$C = 0.001\mu F$
$R1 = 1.6M\Omega$
$R2 = 1.6M\Omega$
$R3 = 1.6M\Omega$

FUNCTION GENERATOR


$V_{REF} = \frac{1}{2} V_{CC}$
V_{REF}
TRIANGLE WAVE OUTPUT
R2 300K
1/4 MC3403
R3 75K
R1 100K
1/4 MC3403
SQUARE WAVE OUTPUT
V_{REF}
R_f

$f = \frac{R1 + R_C}{4CR_f\, R1}$ IF $R3 = \frac{R2\, R1}{R2 + R1}$

MULTIPLE FEEDBACK BANDPASS FILTER


V_{CC}
C
R3
R1
C
V_{IN}
1/4 MC3403
V_O
C_O
R2
V_{REF}

$C_O = 10C$

$V_{REF} = \frac{1}{2} V_{CC}$

GIVEN f_o = CENTER FREQUENCY
$A(f_o)$ = GAIN AT CENTER FREQUENCY

CHOOSE VALUE f_o, C

THEN:

$R3 = \frac{Q}{\pi f_o C}$

$R1 = \frac{R3}{2\, A(f_o)}$

$R2 = \frac{R1\, R5}{4Q^2\, R1 - R5}$

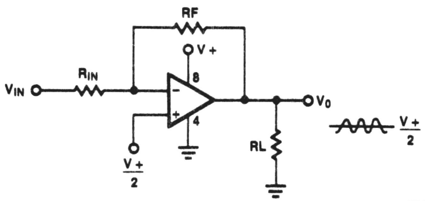
FOR LESS THAN 10% ERROR FROM OPERATIONAL AMPLIFIER
$\frac{Q_o\, f_o}{BW} < 0.1$ WHERE f_o AND BW ARE EXPRESSED IN Hz.

IF SOURCE IMPEDANCE VARIES, FILTER MAY BE PRECEDED WITH VOLTAGE FOLLOWER BUFFER TO STABILIZE FILTER PARAMETERS.

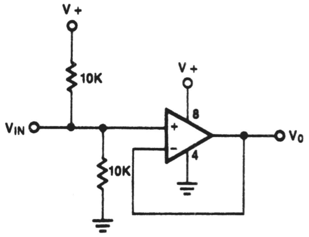
APPLICATIONS FOR THE MC3403 AN160

TYPICAL APPLICATIONS

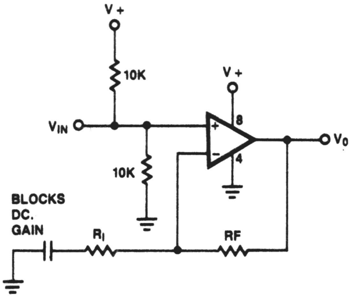
SINGLE SUPPLY INVERTING AMPLIFIER


RF
V+
8
RIN
VIN
−
+
4
VO
V+/2
RL
V+/2

INPUT BIASING VOLTAGE FOLLOWER


V+
10K
V+
8
VIN
+
−
4
VO
10K

NON-INVERTING AMPLIFIER


V+
10K
V+
8
VIN
+
−
4
VO
10K
BLOCKS
DC.
GAIN
RI
RF

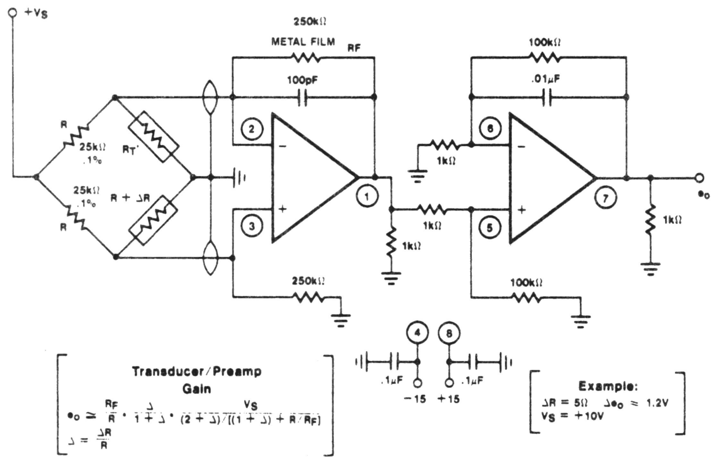
APPLICATIONS FOR THE NE5512/5514

AN144

DESCRIPTION

The 5512 series of high performance operational amplifier provides very good input characteristics. These amplifiers feature low input bias and voltage characteristics such as a 108 op amp with improved CMRR and a high differential input voltage limit achieved through the use of a bias cancellation and PNP input circuits with collector to emitter clamping. The output characteristics are like those of a 741 op amp with improved slew rate and drive capability yet have low supply quiescent current.

NE/SE5512 BRIDGE TRANSDUCER AMPLIFIER



Transducer/Preamp Gain

$$e_o \simeq \frac{R_F}{R} \cdot \frac{\Delta}{1+\Delta} \cdot \frac{V_S}{(2+\Delta)/[(1+\Delta)+R/R_F]}$$

$$\Delta = \frac{\Delta R}{R}$$

Example:

$\Delta R = 5\Omega$ $\Delta e_o \approx 1.2V$

$V_S = +10V$

*NOTE

Thermal compensation transducer (non-active)

Figure 1

BRIDGE TRANSDUCER AMPLIFIER

In applications involving strain gauges, accelerometers and thermal sensors a bridge transducer is often used. Frequently the sensor elements are high resistance units requiring equally high bridge resistance for good sensitivity. This type of circuit then demands an amplifier with high input impedance, low bias current and low drift. The circuit shown represents a possible solution to these general requirements (Figure 1).

For V_S = 10 volts, the common mode voltage is approximately +5 volts, well within the common mode limits of the NE5512.

The sensitivity of the input stage is approximately

$$\frac{RF \cdot Vs}{2R}$$

to a change in transducer resistance ΔR. This gives a gain factor of ≃50 for V_S = 10V and R = 25kΩ. The second stage gain is ×100 giving a total gain of ≃5000.

Noise is minimized by shielding the transducer leads and taking special care to determine a good signal ground. Common mode noise rejection is particularly important making matched differential impedance critical. The NE5512 typically provides 100dB of common mode rejection and will considerably reduce this undesirable effect.

The following are sensitivity figures for the transducer circuits.

	ΔR	ΔE_{out}
leg 1	10Ω	−2.6V
	5Ω	−1.3V
leg 2	10Ω	+2.4
	5Ω	+1.2

Temperature compensation of the bridge element is accomplished by using low drift metal film resistors and also by providing a complimentary non-active sensor element to thermally track the offset in the active element.

High frequency roll-off provides attenuation of unwanted noise above the pass band of the transducer. The shunt capacitors across both stage feedback resistors are for this purpose.

CURRENT TO VOLTAGE CONVERTER •

Taking advantage of the very low bias current and offset of the NE5512 is demonstrated in its adaptation to a current to voltage converter as shown below (Figure 2).

NE/SE5512 CURRENT TO VOLTAGE CONVERTER WITH 1% ACCURACY [SENSITIVITY: 1 VOLT PER MICROAMP]

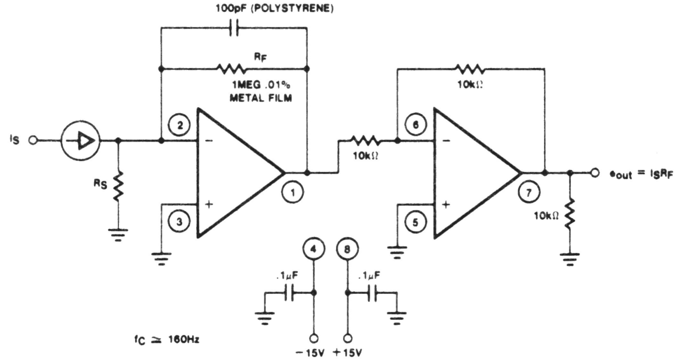


Figure 2

The lower limit of measuring accuracy is determined by I_B (inverting) which is typically 6nA. In order to attain a measurement accuracy of 1% the following inequality must hold,

$$I_B \lesssim (.01)\ I_{Smin}$$

Where I_B = input bias current, I_{Smin} = minimum measured current. For I_B = 6nA and I_{Smin} = 1µA,

$$6nA \lesssim (.01)\ 1\mu A = 10nA$$

and the inequality hold.

DC offset and current noise gain is determined by

$$\frac{R_F + R_S}{R_S}$$

which ≃ 1 for $R_S \gg R_F$.

The measured results for this circuit appear below (V_{CC} = ± 15 volts).

INPUT CURRENT	OUTPUT VOLTAGE
1μA	1.008 Volts
5μA	5.00 Volts
10.00μA	10.00 Volts

NE5512 OPERATIONAL DIFFERENTIATOR

By utilizing the very high input impedance characteristic of the NE5512, an excellent active differentiator can be realized. Using the circuit shown (Figure 3), good results were obtained as shown by the wave forms in Figures 4, 5 and 6. One of the primary problems with such circuits is the tendency towards instability and distortion either due to loading caused by input bias currents or amplifier non-linearity. In addition, gain increases with frequency requiring low input noise in the amplifier.

The relative stability is shown by the output signal wave forms mentioned above. Adding R_1 provides added compensation in the form of a zero near the amplifier unity gain frequency. Frequency range is 100Hz to 10kHz.

In order to obtain good differentiation, the network time constant, RC, must be small relative to the period of the highest frequency present at the input. Since the differentiator will attenuate the signal by a factor of ωRC which may be 100:1 in the operating region, the second amplifier stage is used to compensate for this loss. Various circuits are easily interfaced with the differentiator block due to the inherently low output impedance of the NE5512.

NE/SE5512 ACTIVE DIFFERENTIATOR WITH INVERTING ×10 BUFFER

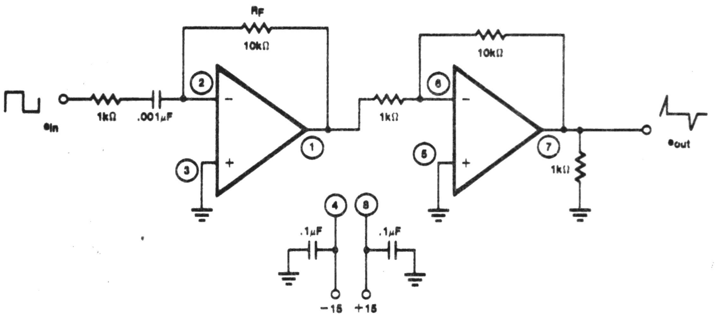


Figure 3

DIFFERENTIATOR WAVEFORMS

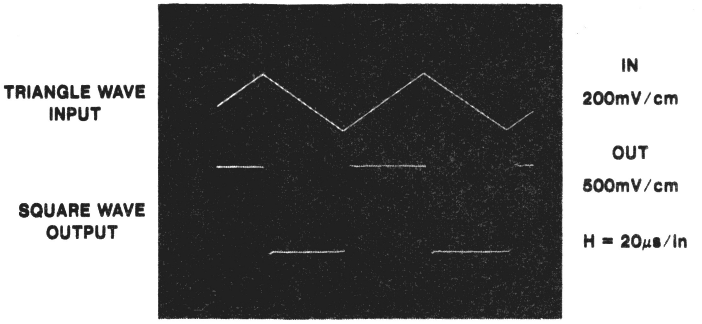


Figure 4

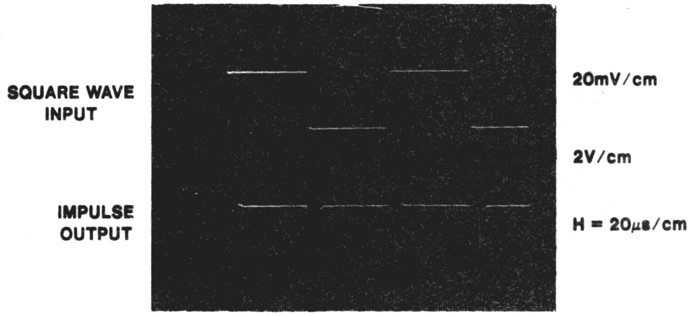


Figure 5

THE OPERATIONAL INTEGRATOR

The operational complement of the active differentiator is the active integrator. The NE5512 is easily adapted to this function as shown in the circuit below (Figure 7). to obtain satisfactory integration the time constant must fulfill the following requirement:

$$RC \geq 15T$$

Where T is the period of the input wave form. For the ideal integrator

$$e_{out} = \frac{1}{RC} \int e_{in}\, dt$$

The factor 1/RC represents an attenuation of the input signal. The low signal level is increased by using the second half of the NE5512 as a gain stage following the operational integration. The wave forms in Figures 8 and 9 show the input-output relationship for both a sine wave and a square wave function. A good integrator must exhibit a phase shift of ≥89° for sine wave input over the active frequency range. For a square wave the resultant output must be a linear ramp. The circuit shown fulfills this requirement (see Figure 7). No external compensation is required since the amplifier is unity gain stable.

DIFFERENTIATOR WAVEFORMS

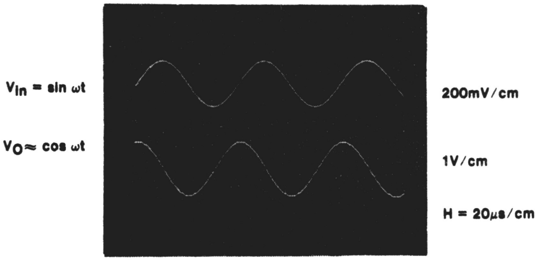


Figure 6

NE/SE5512 ACTIVE INTEGRATOR WITH INVERTING BUFFER

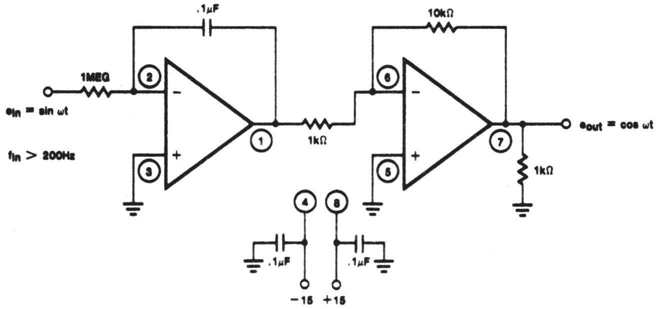


Figure 7

INTEGRATOR WAVEFORMS

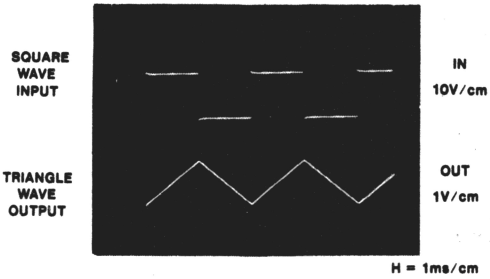


Figure 8

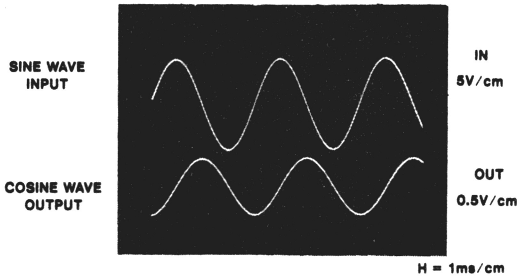


Figure 9

NE5514 DESCRIPTION

The SE/NE5514 family of Quad Operational Amplifiers sets new standards in Bipolar Quad Amplifier Performance. The amplifiers feature low input bias current and low offset voltages. Pin-out is identical to LM324/LM348 which facilitates direct product substitution for improved system performance. Output characteristics are similar to a μA741 with improved slew and drive capability.

FOUR QUADRANT PHOTO-CONDUCTIVE DETECTOR AMPLIFIER

When operating a photo diode in the photoconductive mode (reverse biased) very small currents in the micro ampere range must be sensed in the photo active operating region. Dark currents in the nano amperes are common. Generally, for this reason, J-FET input preamps are used to prevent interaction and accuracy degradation due to input bias currents.

The 5514 has sufficiently low input bias current (6na) to allow its use under these circuit constraints as shown in a possible design used to sense four quadrant motion of a light source. By proper summing of the signals form the X and Y axes, four quadrant output may be fed to an X-Y plotter, oscilloscope or computer for simulation. (See Figure 10.)

The wide input common mode voltage range of the device allows a +10 volt supply to be used to drive the signal bridge giving high sensitivity and improved signal to noise. Obviously, input balancing is critical to achieving common mode signal rejection in addition to adequate shielding of the sensor leads. The sensor head itself must be shielded and the shield grounded to signal common to avoid unwanted noise pick up from power line and other local noise sources. Amplifier response may be shaped to aid in noise reduction by more complex filter configurations. If possible the 5514 should be located in close proximity to the sensor head.

System balance may be done under dark field conditions if adequate photo detector tracking results. However, for high accuracy systems a bipolar balance adjust added to the non-inverting output stage is more desirable. With this latter method the signal bridge is balanced for a null output under uniform light field conditions using the bridge balance pot as shown. D.C. offset is then adjusted using the balance pot on the output amplifier under dark field conditions.

FOUR QUADRANT PHOTO DETECTOR

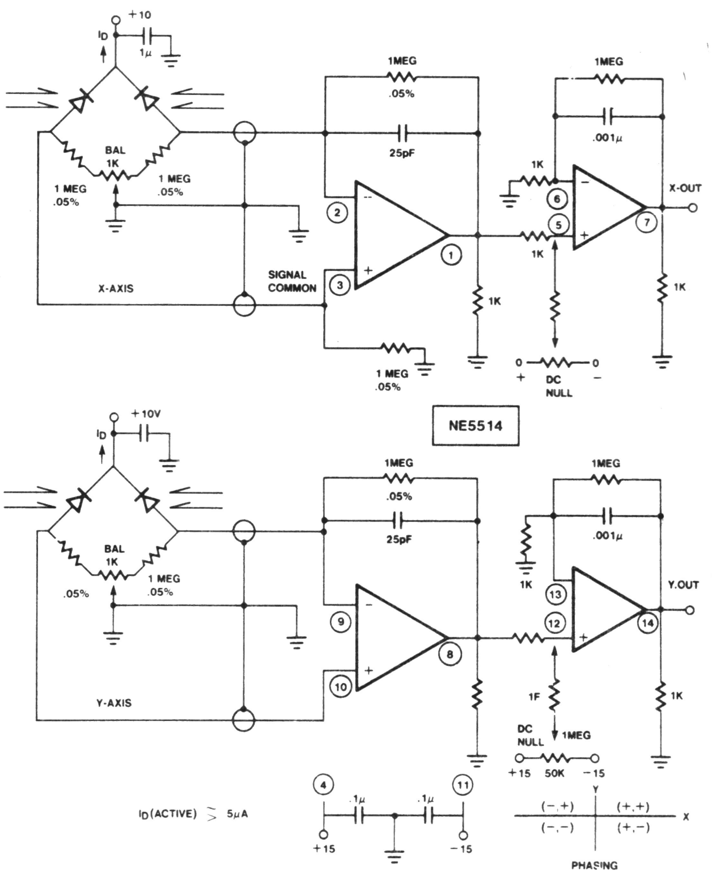


Figure 10

MULTI-TONE BANDPASS FILTER FOR PLL TONE DECODER

In the design of a multiple tone signaling system, particularly where signals are transmitted over long lines, noise and adjacent channel interference may be a significant barrier to reliable communications.

By the use of narrow band active pre-filters to attain selectivity and gain, the effective signal to noise ratio is greatly improved. The SE/NE5514 is easily adapted to such filter configurations due to its inherent stability. In addition its very high input, impedance drastically reduces loading o the passive networks and allows for increased "Q" and large value resistors.

The circuit in Figure 4 demonstrates multiple feedback filters operating at four of the standard signaling frequencies. More channels may be added to increase the capacity of the system.

Test results obtained from this filter configuration were as follows:

Wide band signal to noise	**63dB**
Gain (Mid band)	**30dB**
Q (effective)	**≈ 30**
Output	**OdBM** **(.775v_{rms})**

Note that the amplifiers are operated from a single +12 volt supply and are biased to half

V_{CC} by a simple resistive divider at point B which connects to all non-inverting inputs.

4-STATION 0–50° TEMPERATURE SENSOR

By using an NPN transistor as a temperature sensing element, the NE5514 forms the basis for a multi-station temperature sensor as shown in Figure 12. The principle used is fundamental to the current voltage relationship of a forward biased junction. The current flow across the base-emitter junction is determined by absolute temperature in the following way:

$$I_E = -(I_C + I_B)$$

and $I_E \infty I_S \exp(V_{BE}/V_T)$; $V_T = \frac{kt}{q}$

therefore, $V_{BE} \infty V_T \ln I_E/I_S$

Where I_E is the forward current and I_S is the saturation current inherent in the junction, I_E must be high enough such that the I_S variation with temperature is small relative to I_E ($I_E >> I_S$). I_S is typically .05 pA, therefore, setting I_E to 1 or 2 μA gives the desired condition.

Diode D_1 serves to substantially reduce error due to power supply variation by giving a fixed voltage reference. To calibrate the sensor adjust R_4 for "O" volts output from the NE5514 at 0°C. Adjust R_6 tracking resistor for a scale factor of 100 millivolts per °C output.

Only the transistor need be placed in the temperature controlled environment. Figure 13 shows the addition of an A/D converter and display to give a digital thermometer.

NE/SE5514
MFB BANDPASS FILTER
FOR
MULTI-CHANNEL TONE DECODER

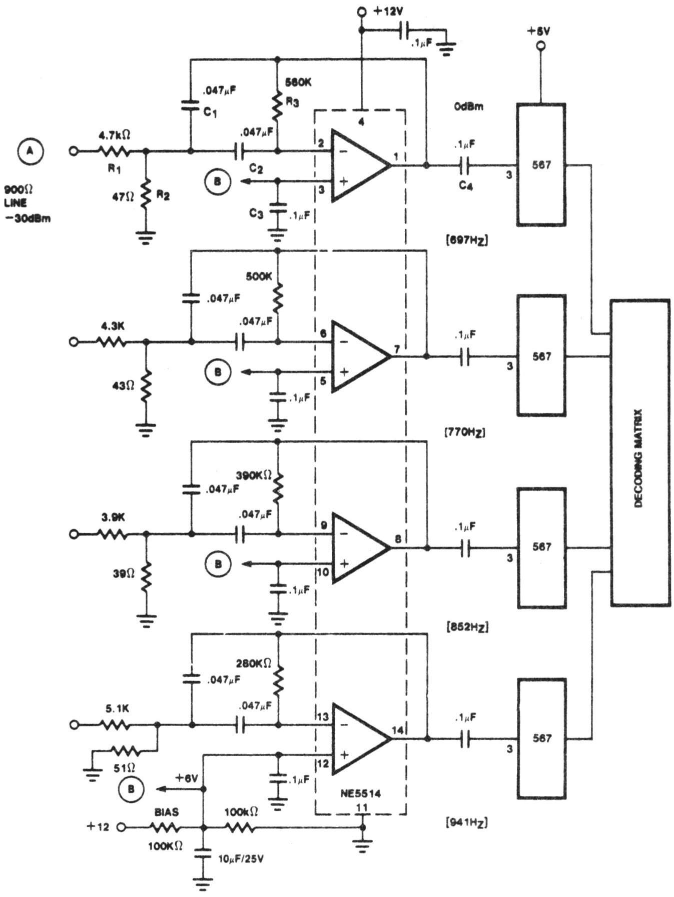

+12V
.1μF
+5V
.047μF
C1
560K
R3
0dBm
A
4.7kΩ
R1
.047μF
C2
B
47Ω
R2
900Ω LINE −30dBm
C3
.1μF
.1μF
C4
567
[697Hz]
500K
.047μF
4.3K
43Ω
[770Hz]
DECODING MATRIX
390KΩ
3.9K
39Ω
[852Hz]
280KΩ
5.1K
51Ω
+6V
BIAS
100kΩ
100KΩ
10μF/25V
+12
NE5514
[941Hz]
1
2
3
4
5
6
7
8
9
10
11
12
13
14

Figure 11

4-CHANNEL TEMPERATURE SENSOR
(0–50°C)

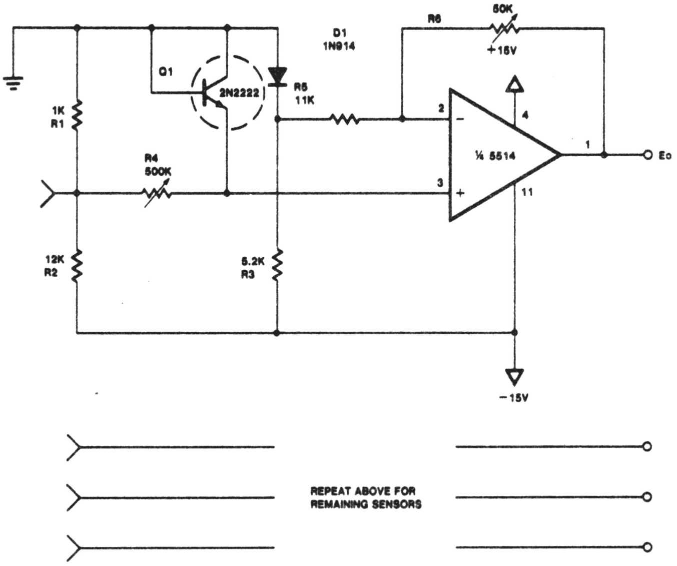

D1
1N914
R6
50K
+15V
Q1
2N2222
R5
11K
1K
R1
2
4
¼ 5514
1
Eo
R4
500K
3
11
12K
R2
5.2K
R3
−15V
REPEAT ABOVE FOR
REMAINING SENSORS

Figure 12

μP-CONTROLLED DIGITAL THERMOMETER

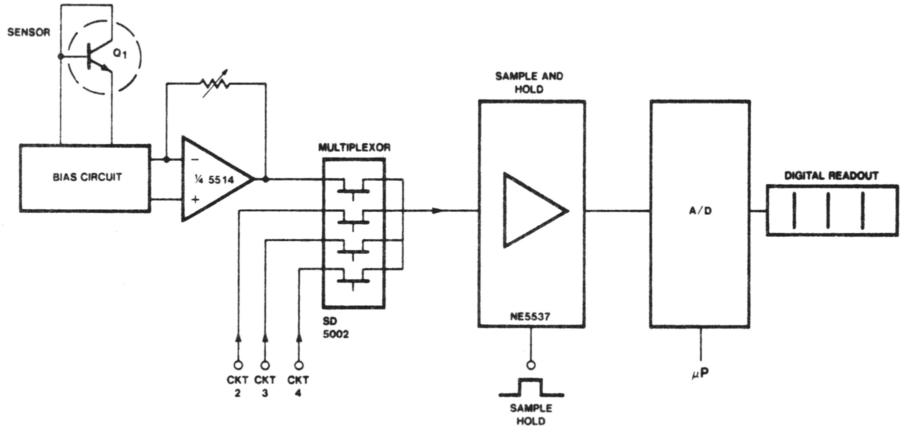

SENSOR
Q1
BIAS CIRCUIT
¼ 5514
MULTIPLEXOR
SD
5002
CKT 2
CKT 3
CKT 4
SAMPLE AND
HOLD
NE5537
SAMPLE
HOLD
A/D
μP
DIGITAL READOUT

Figure 13

NE5517/A TRANSCONDUCTANCE AMPLIFIER APPLICATIONS AN145

DESCRIPTION

The Signetics NE5517 is a truly versatile dual operational transconductance amplifier. In plain language, it is a voltage-to-current converter governed by the transconductance gm, which is equivalent to I_{out}/V_{in}. The gm is increased or decreased linearly by varying the amplifier bias current (I_{ABC}) through an external pin (see Figure 1). From the proper use of the I_{ABC} pin, many control circuits can be realized.

For more insight into the way the part operates, the transconductance can be thought of as gain and is governed by the following equation:

$$gm = \frac{I_{out}}{V_{in}} = \frac{I_{ABCq}}{2KT} \qquad (1)$$

where the transconductance is dependent on the constant KT/q (which is 26mv at 25°C), and I_{ABC} (which is controlled by the user).

To make the device more universal and adaptable for many functions, two impedance buffers for voltage output applications are also included with the amps so that the part can be used as a programmable operational amplifier.

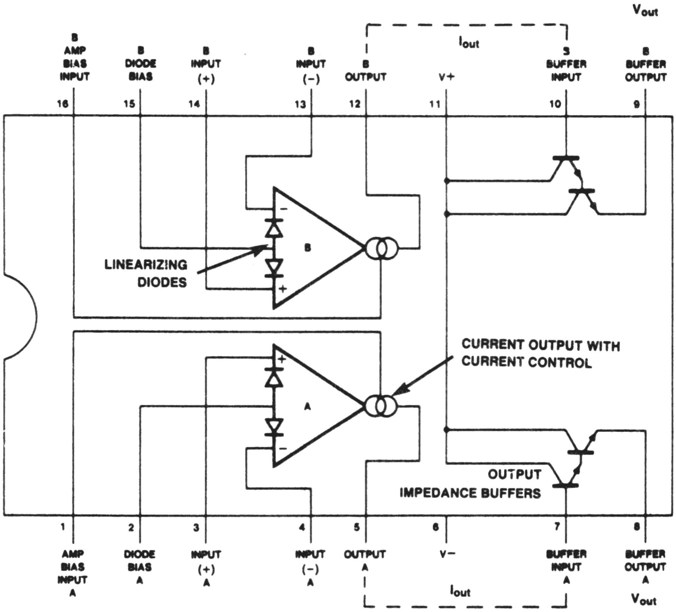
Linearizing diodes provide another useful option. These should be applied when large input voltages or wide temperature variations are encountered. To show the significance of the diodes, compare the difference between Equation 1 without diodes and Equation 2 with diodes:

$$\frac{I_{out}}{V_{in}} = \frac{2\ I_{ABC}}{R_{in}\ I_D} \text{ for } I_{in} \text{ greater than } \frac{i_D}{2} \qquad (2)$$

Here, it can be seen that the transconductance is not temperature dependent. R_{in} is the signal input resistance and I_{in} is the signal current. I_{in} must not exceed half the diode current (I_D, nominally 1mA). The diode current is set by a resistor tied to $+V_{CC}$. A graph showing the output distortion improvement versus differential imput voltage when using the diodes is shown in Figure 2.

An advantage that the NE5517 has over similar devices is a special biasing network between the amplifier and output impedance buffers. This network eliminates output offset current changes with a sudden change in the bias current (I_{ABC}). This is particularly important in audio applications where an audible offset would be produced.

PIN. NO.	SYMBOL	NAME AND FUNCTION
1	I_{ABCa}	Amplifier bias input A
2	D_a	Diode bias A
3	$+IN_a$	Non-inverting input A
4	$-IN_a$	Inverting input A
5	I_{oa}	Output A
6	V−	Negative supply
7	^{IN}Buffer (a)	Buffer input A
8	^{V_O}Buffer (a)	Buffer output A
9	^{V_O}Buffer (b)	Buffer output B
10	^{IN}Buffer (b)	Buffer input B
11	V+	Positive supply
12	I_{ob}	Output B
13	$-IN_b$	Inverting input B
14	$+IN_b$	Non-inverting input B
15	D_b	Diode bias B
16	I_{ABCb}	Amplifier bias input B



V_{out}
B AMP BIAS INPUT
B DIODE BIAS
B INPUT (+)
B INPUT (−)
B OUTPUT
V+
I_{out}
B BUFFER INPUT
B BUFFER OUTPUT
16
15
14
13
12
11
10
9
LINEARIZING DIODES
B
A
CURRENT OUTPUT WITH CURRENT CONTROL
OUTPUT IMPEDANCE BUFFERS
1
2
3
4
5
6
7
8
AMP BIAS INPUT A
DIODE BIAS A
INPUT (+) A
INPUT (−) A
OUTPUT A
V−
I_{out}
BUFFER INPUT A
BUFFER OUTPUT A
V_{out}

Figure 1 Pin Designation and Functional Diagram

APPLICATIONS

An application employing both amplifiers and buffers internal to the NE5517 is the adjustable triangle-square wave generator shown in Figure 3.

The center oscillating frequency is set by the capacitor C at the output of amplifier A. The output amplitude is set by the resistor R connected between the non-inverting inputs, amplifier B output, buffer B input and ground.

The oscillating frequency is varied by changing V_c, which in turn controls the amplifier bias current (I_{ABC1}). If a positive voltage is applied to V_c, the center frequency will increase linearly with increasing voltage. If a negative is applied, the center frequency will decrease linearly with increasing negative voltage. This makes a very good programable oscillator with variable amplitude.

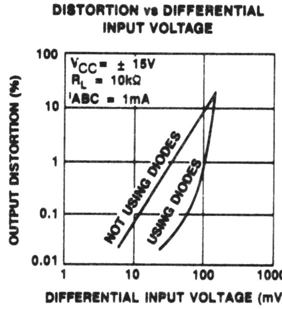


Figure 2 Output Distortion Versus Input Voltage Showing Benefit Of Diodes

By using a large value capacitor and negative control voltage, oscillations in the fractions of Hertz can be realized; a small capacitor and positive control voltage will give frequencies up to 500kHz. Graphs showing the linearity of control voltage versus frequency for different capacitor values are shown in Figure 4.

Pertinent calculations are:

$$f_c = \frac{I_{ABC1}}{4(C)\,(I_{ABC2})\,(R)} \qquad (3)$$

Where:
f_C = center frequency
I_{ABC1} = oscillator control current
I_{ABC2} = amplitude control current
R = amplitude control resistor
C = oscillator control capacitor

$$\text{Also: Amplitude} = (I_{ABC2})\,(R) \qquad (4)$$

Another very useful application is to use the NE5517 as a digitally programmable amplifier. The entire circuit is shown in Figure 5.

The circuit consists of a Signetics microprocessor compatible DAC, a transistor array, and the NE5517 configured as a voltage controlled amplifier. This arrangement can also be used with the VCO explained earlier to program its oscillating frequency.

The pertinent equations governing this application are as follows:

$$Av = \frac{V_{out}}{V_{in}} = \frac{BW\,(10)}{256} \times \frac{I_{DAC\,MAX} \times q \times R_L}{2 \times KT} \qquad (5)$$

Where:
BW (10) = binary word decimal
$I_{DAC\,MAX}$ = maximum DAC output current (1mA)
R_L = load resistance (30K)
q/KT = 38.5 at 25°C

Also:

$$I_{DAC\,MAX} = 2 \times \frac{V_{ref}}{R_{ref}} = 2 \times \frac{5K}{10K} = 1\text{mA} \qquad (6)$$

Where:
V_{ref} = supplied by DAC (5V)
R_{ref} = referenced resistor (10K ohms)

The $I_{DAC\,MAX}$ of 1mA is used to keep the transconductance within the linear range.

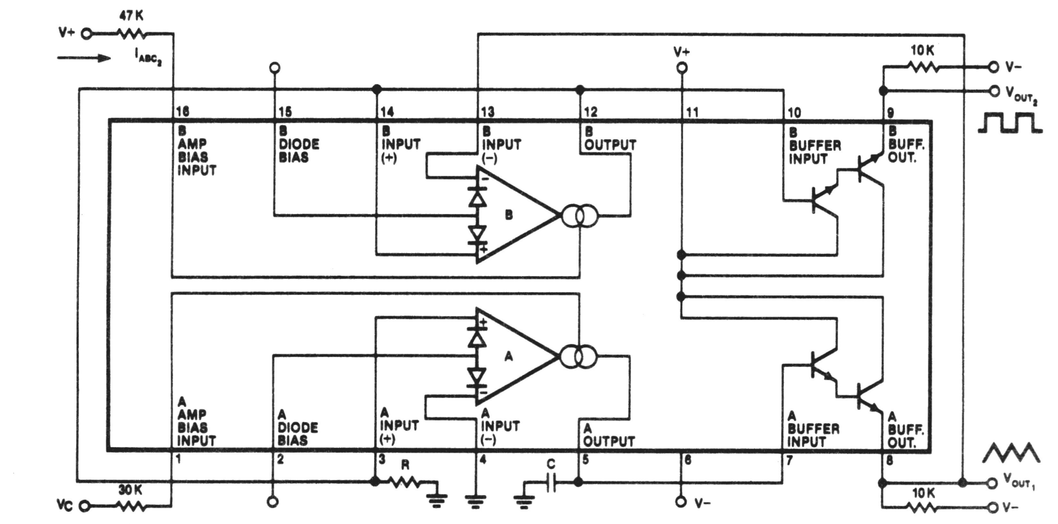
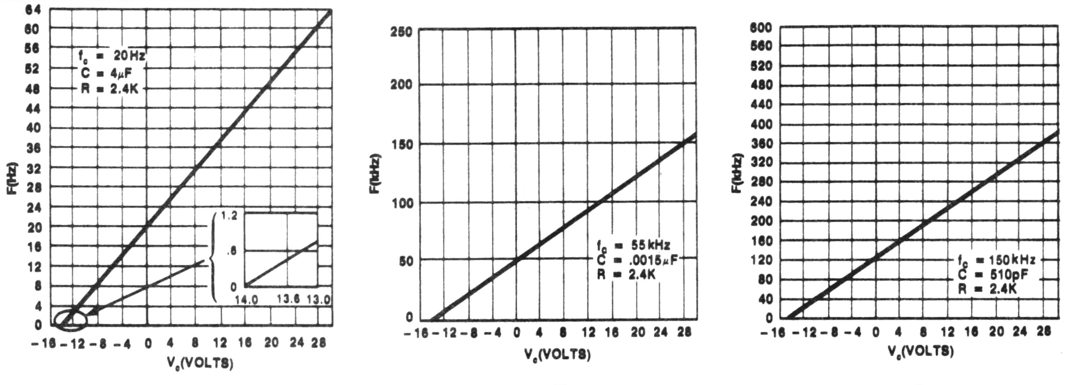


Figure 3 Triangle-Square Wave Generator



A B C

Note:
V_c Below −13.6V or above +30V will cause distortion.
Changing the C value will vary the frequency range.

Figure 4 Control Voltage (V_c) Versus Frequency Data

The current mirror matches the current flow into the DAC and supplies the same amount to the 5517 control pin. Using a current output DAC is much faster than using a voltage output device to control the part. (If speed is not important, this can be done and the current mirror can be replaced with a resistor.) Also, the input attenuation has not been calculated into the gain equation. Therefore, equation (5) pertains to the signal after the input divider.

Many other applications for the NE5517 exist; refer to the data sheet applications section in the Signetics Linear LSI data book for numerous ideas.

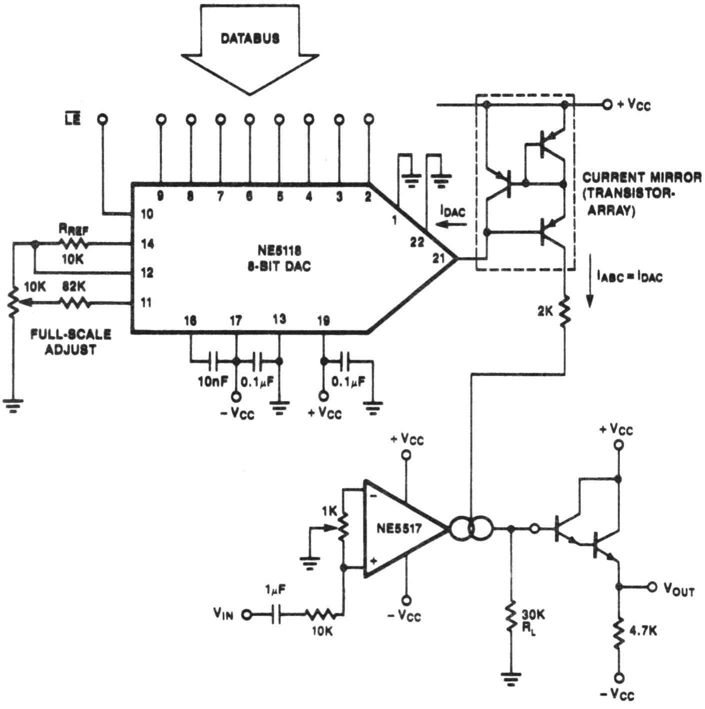

DATABUS
LE
9 8 7 6 5 4 3 2
10
14
12
11
1
22
21
16 17 13 19
NE5118
8-BIT DAC
R_{REF}
10K
10K
82K
FULL-SCALE
ADJUST
10nF
0.1μF
0.1μF
−Vcc
+Vcc
I_{DAC}
+Vcc
CURRENT MIRROR
(TRANSISTOR-
ARRAY)
$I_{ABC} = I_{DAC}$
2K
+Vcc
NE5517
1K
1μF
V_{IN}
10K
−Vcc
30K
R_L
+Vcc
V_{OUT}
4.7K
−Vcc

Figure 5 Digitally Programmable Amplifier

EXPLANATION OF NOISE

INTRODUCTION TO NOISE

Since fabrication techniques in the integrated circuit industry have improved so tremendously in the past few years, input offset voltages and bias currents are being minimized and noise parameters (whether measured at the output or referred to the input) have become a major source of concern. Reducing noise by improved process techniques and by use of peripheral component control will be the thrust of this application as a secondary effort, in understanding the noise components themselves.

An inspection of industry specifications show several methods of rating amplifier noise performance.

1. Output signal to noise ratio.
2. Output noise level (with specified loads and bandwidth).
3. Output noise level referenced to normal operating level.
4. Equivalent input noise (at a specified gain, source impedance and bandwidth).
5. Noise figure.

BASIC NOISE PROPERTIES

Noise, for purposes of this discussion, is defined as any signal appearing in an op amp's output that could not have been predicted by DC and AC input error analysis. Noise can be random or repetitive, internally or externally generated, current or voltage type, narrowband or wideband, high frequency or low frequency; whatever its nature, it can be minimized.

The first step in minimizing noise is source identification in terms of bandwidth and location in the frequency spectrum; some of the more common sources are shown in Figure 1. Some observations to be made from Figure 1 are that noise is present from DC to VHF from sources which may be identified in terms of bandwidth and frequency, noise source bandwidths overlap, making noise a composite quantity at any given frequency. Most externally caused noise is repetitive rather than random and can be found at a definite frequency. Noise effects from external sources must be reduced to insignificant levels to realize the full performance available from a low noise op amp.

EXTERNAL NOISE SOURCES

Since noise is a composite signal, the individual sources must be indentified to minimize their effects. For example, 60Hz power line pickup is a common interference noise appearing at an op amp's output as a 16ms sine wave. In this and most other situations, the basic tool for external noise source frequency characterization is the oscilloscope sweep rate setting. Recognizing the oscilloscope's potential in this area, there are available several preamplifiers with variable bandwidth and frequency which allow quick noise source frequency identification. Another basic identification tool is the simple low pass filter as shown in Figure 2 where the bandpass is calculated by:

$$1)\ f_0 = \frac{1}{2\pi RC} \qquad (1)$$

With such a filter, measurement bandpass can be changed form 10Hz to 100Hz (C = 4.7μF to 470pF), attenuating higher frequency components while passing frequencies of interest. Once identified, noise from an external source may be minimized by the methods outlined in Table 1, the external noise chart.

POWER SUPPLY RIPPLE

Power supply ripple at 120Hz is not usually thought of as noise, but it should be. In an actual op amp application, it is quite possible to have a 120Hz noise component that is equal in magnitude to all other noise sources combined, and, for this reason, it deserves a special discussion.

To be negligible, 120Hz ripple noise should be between 10nV and 100nV referred to the input of an op amp. Achieving these low levels requires consideration of three factors: the op amp's 120Hz power supply

NOISE FREQUENCY ANALYSIS RC LOW PASS FILTER

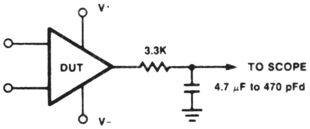


Figure 2

FREQUENCY SPECTRUM OF NOISE SOURCES AFFECTING OPERATIONAL AMPLIFIERS & LOW NOISE PREAMPLIFIERS

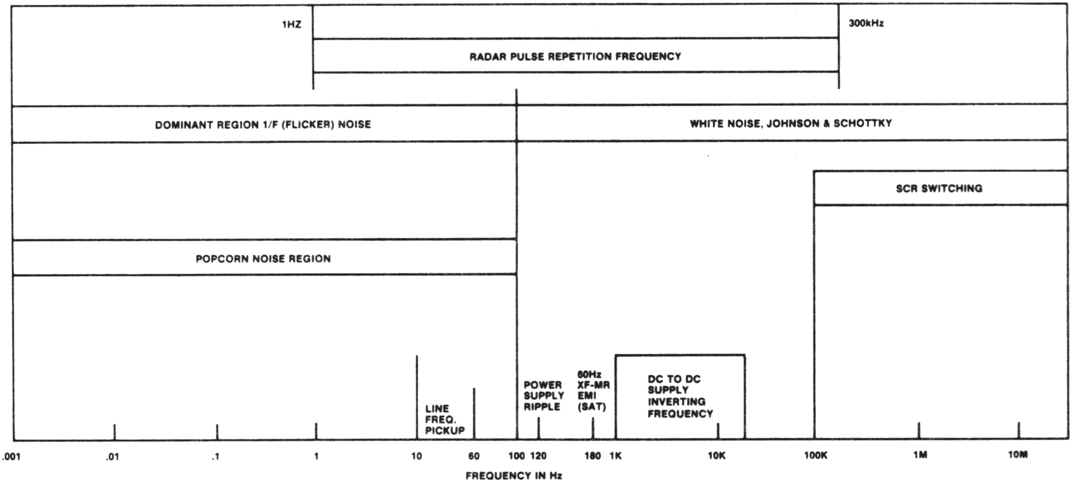


Figure 1

rejection ratio (PSRR), the regulator's ripple rejection ratio, and, finally, the regulator's input capacitor size.

PSRR at 120Hz for a given op amp may be found in the manufacturer's data sheet curves of PSRR versus frequency as shown in Figure 3. For the amplifier shown, 120Hz PSRR is about 74dB, and to attain a goal of 100nV referred to the input, ripple at the power terminals must be less than 5mV. Today's IC regulators provide about 60dB of ripple rejection; in this case the regulator input capacitor must be made large enough to limit input ripple to .5V.

Externally compensated low noise op amps can provide improved 120Hz PSRR in high close-loop gain configurations. The PSRR versus frequency curves of such an op amp are shown in Figure 5. When compensated for a closed loop gain of 1000, 120Hz PSRR is 115dB. PSRR is still excellent at much higher frequencies, allowing low ripple noise operation in exceptionally severe environment.

POWER SUPPLY DECOUPLING

Usually, 120Hz ripple is not the only power supply associated noise. Series regulator outputs typically contain at least 150μV of noise in the 100Hz to 10kHz range, switching types contain even more. Unpredictable amounts of induced noise can also be present on power leads from many sources. Since high frequency PSRR decreases at 20dB/decade, these higher freqency supply noise components must not be allowed to reach the op amp's power terminals. RC decoupling, as shown in Figure 6, will adequately filter most wideband noise. Some caution must be exercised with this type of decoupling, as load current changes will modulate the voltage as the op amp's supply pins.

POWER SUPPLY REGULATION

Any change in power supply voltage will have a resultant effect referred to an op amp's inputs. For the op amp of Figure 3, PSRR at DC is 110dB (3μV/V) which may be considered as a potential low frequency noise source. Power supplies for low noise op amp applications should, therefore, be both low in ripple and well-regulated. Inadequate supply regulation is often mistaken to be low frequency op amp noise.

When noise from external sources has been effectively minimized, further improvements in low noise performance are obtained by specifying the right op amp, and through careful selection and application of the peripheral components.

PSRR VS FREQUENCY

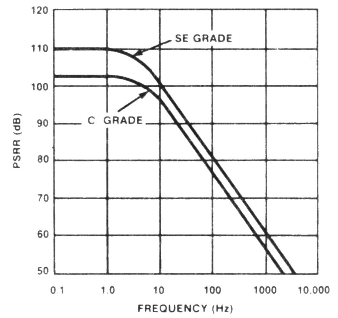


Figure 3

NOISE CHARACTERIZATION OF AMPLIFIER

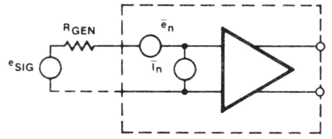


Figure 4

PSRR VS FREQUENCY (EXTERNALLY COMPENSATED DEVICE)

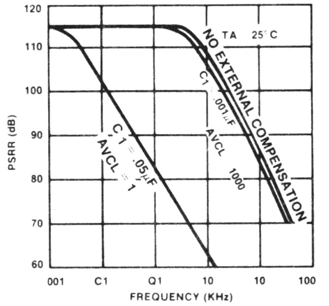


Figure 5

RC DECOUPLING

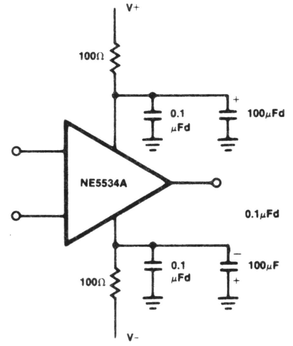


Figure 6

NOISE VOLTAGE AND CURRENT FOR AN OP AMP

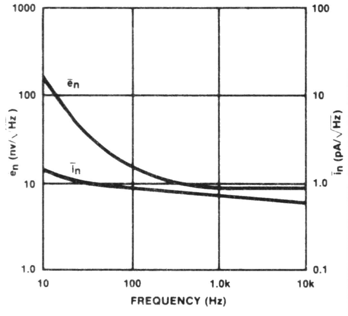


Figure 7

NOISE VOLTAGE, e_n, or more properly, EQUIVALENT SHORT-CIRCUIT INPUT RMS NOISE VOLTAGE is simply that noise voltage which would appear to originate at the input of a noiseless amplifier (referring to Figure 4) if the input terminals were shorted. It is expressed in nanovolts per root Hertz (nV/$\sqrt{Hz}$) at specified frequency, or in microvolts for a given frequency band. It is determined, or measured, by shorting the input terminals, measuring the output rms noise, dividing by amplifier gain, and referencing to the input. Hence the term, equivalent noise voltage. An output bandpass filter of known characteristic is used in measurements, and the measured value is divided by the square root of the bandwidth $\sqrt{B}$, if data is to be expressed per unit bandwidth or per root Hertz. The level of $\bar{e}_n$ is not constant over the frequency band; typically it increases at lower frequencies as shown in Figure 7. This increase is 1/f NOISE (flicker).

NOISE CURRENT, i_n, or more properly, EQUIVALENT OPEN-CIRCUIT RMS NOISE CURRENT is that noise which occurs apparently at the input of a noiseless amplifier due only to noise currents. It is expressed in picoamps per root Hertz (pA/$\sqrt{Hz}$) at a specified frequency or in nanoamps in a given frequency band. It is measured by shunting a capacitor or resistor across the input terminals such that the noise current will give rise to an additional noise voltage which is i_n x R_{in} (or X_{cin}). The output is measured, divided by amplifier gain, referenced to input, and that contribution known to be due to $\bar{e}_n$ and resistor noise is appropriately subtracted from the total measured noise. If a capacitor is used at the

EXTERNAL NOISE CHART			
Source	**Nature**	**Causes**	**Minimization Methods**
60Hz Power	Repetitive Interference	Powerlines physically close to op amp inputs. Poor CMRR at 60Hz.	Reorientation of power wiring. Shielded transformers.
120HzRipple	Repetitive	Inadequate ripple consideration. Poor RSRR at 120Hz	Thorough design to minimize ripple. RC decoupling at the op amp.
180Hz	Repetitive EMI	180Hz radiated from saturated 60Hz transformers.	Physical reorientation of components. Shielding. Battery power.
Radio stations	Standard AM broadcast through FM	Antenna action anyplace in system.	Shielding. Output filtering. Limited circuit bandwidth.
Relay & switch arcing	High frequency burst at switching rate.	Proximity to amplifier inputs, power lines, compensation terminals, or nulling terminals.	Filtering of HF components. Shielding. Avoidance of ground loops. Arc suppressors at switching source.
Printed circuit board contamination	Random low frequency	Dirty boards or sockets.	Thorough cleaning and humidity sealant.
Radar transmitters	High frequency gated at radar pulse repetition rate.	Radar transmitters from long range surface search to short range navigational especially near airports.	Shielding. Output filtering of frequencies >> PRR.
Mechanical vibration	Random < 100Hz	Loose connections, intermittent metallic contact in mobile equipment.	Attention to connectors and cable conditions. Shock mounting in severe environments.
Chopper frequency noise	Common mode input current at chopping frequency	Abnormally high noise chopper amplifier in system	Balanced source resistors. Use bipolar input op amps instead.

Table 1

input, there is only $\overline{e}_n$ and $\overline{i}_n X_{CIN}$. The $\overline{i}_n$ is measured with a bandpass filter and converted to pA/$\sqrt{Hz}$ if appropriate; typically it increases at lower frequencies for bipolar op amps and transistors, but it increases at higher frequencies for field-effect transistors and Bi-Fet/Bi MOS op amps.

NOISE FIGURE, NF, is the logarithm of the ratio of input signal-to-noise and output signal-to-noise.

$$NF = 10 \log \frac{(S/N)_{in}}{(S/N)_{out}} \qquad (2)$$

where: S and N are power or $(\text{voltage})^2$ levels

This is measured by determining the S/N at the input with no amplifier present, and then dividing by the measured S/N at the output with signal source present.

The values of R_{gen} and any X_{gen} as well as frequency must be known to properly express NF in meaningxul terms. This is because the amplifier $i_n \times Z_{gen}$ as well as R_{gen} itself produces input noise. The signal source contains some noise. However, e_{sig} is generally considered to be noise free and input noise is present as the THERMAL NOISE of the resistive component of the signal generator impedance $R_{gen.}$. This thermal noise is WHITE in nature as it contains constant NOISE POWER DENSITY per unit bandwidth. It is easily seen that the $\overline{e}_n^2$ has the units V²/Hz and that ($\overline{e}_n$) has the units V/$\sqrt{Hz}$

$$\overline{e}_R^2 = 4kTRB \qquad (3)$$

where: T is temperature in °K
R is resistor value in ohms
B is bandwidth in Hz
k is Boltzman's constant

OPERATIONAL AMPLIFIER INTERNAL NOISE

OP AMP NOISE SPECIFICATIONS

Most completely specified low noise op amp data sheets specify current and voltage noises in a 1Hz bandwidth and low frequency noise over a range of .1Hz to 10Hz. To minimize total noise, a knowledge of the derivation of these specifications is useful. In this section, the reader is provided with an explanation of basic op amp associated random noise mechanisms and introduced to a simplified method for calculating total input-referred noise in typical applications.

RANDOM NOISE CHARACTERISTICS

Op amp associated noise currents and voltages are random. They are aperiodic and uncorrelated to each other and have Gaussian amplitude distributions, the highest noise amplitudes having the lowest probability. Gaussian amplitude distribution allows random noises to be expressed as rms quantities; multiplying a Gaussian rms quantity by six results in a peak to peak value that will not be exceeded 99.73% of the time.

The two basic types of op amp associated noises are white noise and flicker noise (l/f). White noise contains equal amounts of power in each Hertz of bandwidth. Flicker noise is different in that it contains equal amounts of power in each decade of bandwidth. This is best illustrated by spectral noise density plots

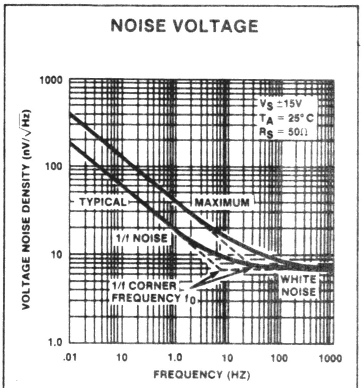


Figure 8

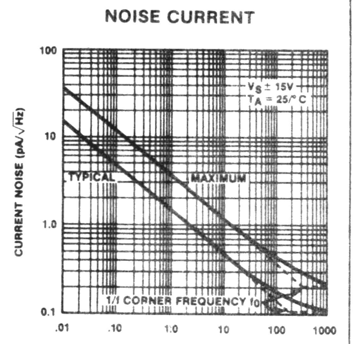


Figure 9

such as in Figure 8 and 9. Above a certain corner frequency, white noise dominates; below that frequency, flicker (l/f) noise is dominant. Low noise corner frequencies distinguish low noise op amps from general purpose devices.

SPECTRAL NOISE DENSITY

To utilize Figures 8 and 9, let us consider the definition of spectral noise density: the square root of the rate of change of mean-square noise voltage (or current) with frequency Eq. 4A.

$$e_n^2 = \frac{d}{dF}(E_n)^2 \tag{4A}$$

$$i_n^2 = \frac{d}{dF}(1_n)^2 \tag{4B}$$

$$E_n = \sqrt{\int_{f_L}^{f_H} e_n^2\, dF} \tag{5A}$$

$$I_n = \sqrt{\int_{f_L}^{f_H} i_n^2\, dF} \tag{5B}$$

where e_n, i_n = Spectral noise density
E_n, I_n = Total rms noise
f_H = Upper frequency limit
f_L = Lower frequency limit

Conversely, the rms noise value within a given frequency band is the square root of the definite integral of the spectral noise density over the frequency band (Equation 5B). This means that three things must be known to evaluate total voltage noise (E_n) or current noise (I_n): f_H, f_L, and a knowledge of noise behavior over frequency.

WHITE NOISE

White noise sources are defined to have a noise content that is equal in each Hertz of bandwidth, and Equation 5B may be rewritten for white noise sources as:

$$E_n(\omega) = e_n\sqrt{f_H - f_L} \qquad I_n(\omega) = i_n\sqrt{f_H - f_L} \tag{6}$$

It is therefore convenient to express spectral noise density in V/√Hz or A/√Hz where $f_H - f_L = 1$Hz. When $f_H \geq 10\,f_L$, the white noise expressions may be further reduced to:

$$E_n(\omega) = e_n\sqrt{f_H} \qquad I_n(\omega) = i_n\sqrt{f_H} \tag{7}$$

FLICKER NOISE & WHITE NOISE

Since flicker noise content is equal in each decade of bandwidth, total flicker noise may be calculated if noise in one decade is known. The .1Hz to 1Hz decade noise content (K) is widely used for this purpose because the white noise contribution below 10Hz is usually negligible.

$$E_n(f) \cong K\sqrt{\frac{1}{f}}\ ,\ I_n(f) \cong K\sqrt{\frac{1}{f}} \tag{8a and b}$$

When substituted in Equation (3), the expressions may be rewritten to:

$$E_n(f) = K\sqrt{\ln\left(\frac{f_H}{f_L}\right)},\ I_n(f) = K\sqrt{\ln\left(\frac{f_H}{f_L}\right)} \tag{9a and b}$$

When corner frequencies are known, simplified expressions for total voltage and current noise, (E_N and I_N), may be written:

$$E_N(f_H - f_L) = e_n\sqrt{f_{ce}\ln\left(\frac{f_H}{f_L}\right) + (f_H - f_L)} \tag{10}$$

$$I_N(f_H - f_L) = i_n\sqrt{f_{ci}\ln\left(\frac{f_H}{f_L}\right) + (f_H - f_L)} \tag{11}$$

where: e_n = White noise voltage in a 1Hz bandwidth
i_n = White noise current in a 1Hz bandwidth
f_{ce} = Voltage noise corner frequency
f_{ci} = Current noise corner frequency
f_H = Upper frequency limit
f_L = Lower frequency limit

The two most important internally generated noise minimization rules are: limit the circuit bandwidth and use operational amplifiers with low corner frequencies.

NOISE SUMMATION

In the spectral density discussions, the concepts of white noise and flicker noise were introduced. In Figure 10, the complete input-referred op amp noise model, internal white and flicker noise sources are combined into three equivalent input noise generators, E_n, I_{N1} and I_{N2}. The noise current generators produce noise voltage drops across their respective source resistors, R_{S1} and R_{S2}. The source resistors themselves generate thermal noise voltages, E_{t1} and E_{t2}. Total rms input referred voltage noise, over a given bandwidth, is the square root of the sum of the squares of the five noise voltage sources over that bandwidth.

$$E_{NT}(f_H - f_L) = \sqrt{E_N^2 + (I_{N1}\cdot R_{S1})^2 + (I_{N2}\cdot R_{S2})^2 + E_{t1}^2 + E_{t2}^2} \tag{12}$$

THERMAL NOISE

Thermal (Johnson) noise is a white noise voltage generated by random movement of thermally-charged carriers in a resistance; in op amp circuits this is the type of noise produced by the source resistances in series with each input. Its rms value over a given bandwidth is calculated by:

$$E_t = \sqrt{4kTR\,(f_H - f_L)} \tag{13}$$

Where: k = Boltzman's constant = 1.38 x 10^{-23} joules/°K
T = Absolute temperature, °Kelvin
R = Resistance in ohms
f_H = Upper frequency limit in Hertz
f_L = Lower frequency limit in Hertz

At room temperature Equation 13 simplifies to:

$$E_t = 1.28 \times 10^{-10}\sqrt{R(f_H - f_L)} \tag{14}$$

To minimize thermal noise (E_{t1} and E_{t2}) from R_{S1} and R_{S2}, large source resistors and excessive system bandwidth should be avoided.

Thermal noise is also generated inside the op amp, principally from r_{bb}, the base-spreading resistances in the input stage

OP AMP NOISE MODEL

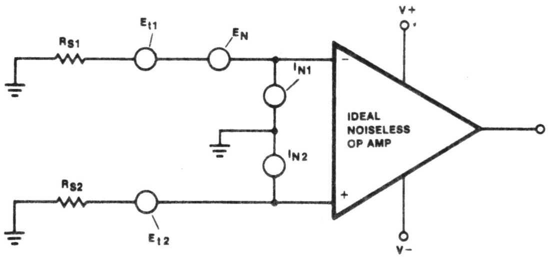


Figure 10

transistors. These noises are included in E_N, the total equivalent input voltage noise generator.

SHOT NOISE

Shot noise (Shottky noise) is a white noise current associated with the fact that current flow is actually a movement of discrete charged particles (electrons). In figure 10 I_{N1} and I_{N2}, above the 1/f frequency, are shot noise currents which are related to the amplifier's DC input bias currents:

$$I_{sh} = \sqrt{2qI_{BIAS}\,(f_H - f_L)} \qquad (15)$$

where: I_{sh} = RMS shot noise value in amps
q = Charge of an electron = 1.59×10^{-19}
I_{BIAS} = Bias current in amps
f_H = Upper frequency limit in Hertz
f_L = Lower frequency limit in Hertz

At room temperature Equation 15 simplifies to:

$$I_{sh} = 5.64 \times 10^{-10} \sqrt{I_{BIAS}\,(f_H - f_L)} \qquad (16)$$

Shot noise currents also flow in the input stage emitter dynamic resistances, (r_e), producing input noise voltages. These voltages, along with the r_{bb}, thermal noise, make up the white noise portion of E_N, the total equivalent input noise voltage generator.

FLICKER NOISE

In limited bandwidth applications, flicker (1/f) noise is the most critical noise source. An op amp designer minimizes flicker noise by keeping current noise components in the input and second stages from contributing to input voltages noise. Equation 17 illustrates this relationship:

$$\frac{i_n \text{ second stage}}{g_m \text{ first stage}} = e_n \text{ input} \qquad (17)$$

Another critical factor is corner frequency. For minimum noise the current and voltage noise corner frequencies must be low; this is crucial. As shown in Figure 11 low noise corner frequencies distinguish low noise op amps from ordinary industry standard 741 types.

POPCORN NOISE

Popcorn noise (burst noise) is a momentary change in input bias current usually occurring below 100Hz, and is caused by imperfect semiconductor surface conditions incurred during wafer processing. Minimization of this problem can be accomplished through careful surface treatment, general cleanliness, and a special three-step process known as "Triple Passivation".

Op amp manufacturers face a difficult decision in dealing with popcorn noise. Through careful low noise processing, it can be significantly reduced in almost all devices; alternatively, the processing may be relaxed, and finished devices must be individually tested for this parameter. Special noise testing takes valuable labor time, adds significant amounts to manufacturing cost, and ultimately increases the price a customer has to pay.

TOTAL NOISE CALCULATION

With data sheet curves and specifications, and a knowledge of source resistance values, total input-referred noise may be calculated for a given application. To illustrate the method, noise information from a data sheet is reproduced in Figure 12. The first step is to determine the current and voltage noise corner frequencies so that the E_N and I_N terms of Equation 12 may be calcuated using Equations 10 and 11.

CORNER FREQUENCY DETERMINATION

NOISE VOLTAGE COMPARISON

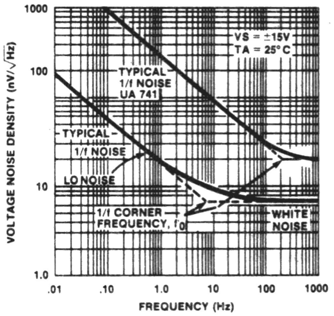


Figure 11

INPUT NOISE VOLTAGE VS FREQUENCY

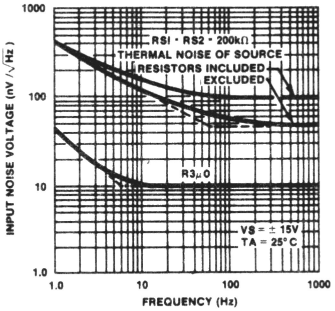


Figure 12

In the input shot noise versus frequency curves of Figure 12, it may be seen that voltage noise ($R_s = 0$) begins to rise at about 10Hz. Lines projected from the horizontal (white noise) portion and sloped (flicker noise) portion intersect at 6Hz, the voltage noise corner frequency (f_{ce}). In the center curve, excluding thermal noise multiplied by 200Ω is plotted as a voltage noise. Lines projected from the horizontal portion and sloped portions intersect at 60Hz, the current noise corner frequency (f_{ci}). Equations 10 and 11 also require e_n and i_n for calculation of E_N and I_N. To find e_n and i_n, use the data sheet specification a decade or more above the respective corner frequencies; in this case e_n is 9.6 nV/$\sqrt{Hz}$ (1000Hz), and i_n is 0.12 pA/$\sqrt{Hz}$ (1000Hz).

BANDWIDTH OF INTEREST

To be summed correctly, each of the five noise quantities must be expressed over the same bandwidth, (f_H - f_L). At this time, assume f_H to be the highest frequency component that must be amplified without distortion. Note that e_n, i_n, corner frequencies and bandwidth are independent of actual circuit component values. When doing noise calculations for a large number of circuits using the same op amp, these numbers only have to be calculated once.

TYPICAL APPLICATION EXAMPLE

Figure 13a shows a typical X10 gain stage with a 10kΩ source resistance. In Figure 13b, the circuit is redrawn to show five noise voltage sources. To evaluate total input-referred noise, the values of each of the five sources must be determined.

$e_n = 9.6\ \text{nV}/\sqrt{\text{Hz}}$
$I_n = .12\ \text{pA}/\sqrt{\text{Hz}}$
$f_{ce} = 6\text{Hz}$
$f_{ci} = 60\text{Hz}$

Using Equation 14: $E_t = \sqrt{4KTR\,(f_H - f_L)}$

$$E_{t1} = 1.28 \times 10^{10} \sqrt{(900\Omega)\,(100\text{Hz})} = 0.4\mu\text{V rms}$$

$$E_{t2} = 1.28 \times 10^{-10} \sqrt{(10\text{K}\Omega)\,(100\text{Hz})} = .128\mu\text{V rms}$$

Next, calculate I_N using Equation 11

$$I_N = i_n \sqrt{f_{ci}\ \ln\left(\frac{f_H}{f_L}\right) + (f_H - f_L)}$$

$$= .12\text{pA} \sqrt{60\ \ln\left(\frac{100\text{Hz}}{0.01\ \text{Hz}}\right) + (100 - 0.01)}$$

$$= 3.066\text{pA rms}$$

and:

$$I_{N1} \cdot R_{S1} \geqq 3.066\text{pA}\ (900\Omega) = .0027\mu\text{V rms}$$

$$I_{N2} \cdot R_{S2} = 3.066\text{pA}\ (10\text{k}\Omega) = .0306\mu\text{V rms}.$$

Finally, E_N from Equation 10

$$E_N = e_n \sqrt{f_{ce} \ln\left(\frac{f_H}{f_L}\right) + (f_H - f_L)}$$

$$= 9.6\text{nV} \sqrt{6\ \ln\left(\frac{100\text{Hz}}{0.01\text{Hz}}\right) + (100 - 0.01)}$$

$$= 0.120\mu\text{V rms}$$

Substituting in Equation 12

$$E_{NT}\,(f_H - f_L) = \sqrt{E_N^2 + I_{N1}^2 R_{S1}^2 + (I_{N2} R_{S2})^2 + E_{t1}^2 + E_{t2}^2}$$

$$= \sqrt{(.120\mu\text{V})^2 + (.0027\mu\text{V})^2 + (.0306\mu\text{V})^2 + (.04\mu\text{V})^2 + (.128\mu\text{V})^2}$$

$$= 0.183\mu\text{Vrms}$$

Using the factor of 6, total input-referred noise = 1.1μV peak to peak (0.01Hz to 100Hz).

741 CALCULATION EXAMPLE

The preceding calculation determined total noise in a given bandwidth using a low noise op amp. To place this level of performance into perspective, a calculation using the industry-standard 741 op amp in the circuit of Figure 13 is useful. Once again the starting point is corner frequency determination, using the data sheet curves:

$f_{ce} = 200\text{Hz}$; $f_{ci} = 2\text{kHz}$; $e_n = 20\text{nV}/\sqrt{\text{Hz}}$; $i_n = .5\text{pA}/\sqrt{\text{Hz}}$.

Using these corner frequencies and noise magnitudes, E_N and I_N are calculated to be 0.88μV rms and 68pA rms respectively. Multiplying this noise current by the source resistance gives terms 2 and 3 of Equation 12 as shown below.

$$E_{NT}\,(f_H - f_L) = \sqrt{E_N^2 + I_{N1}^2 R_{S1}^2 + I_{N2}^2 R_{S2}^2 + E_{+1}^2 + E_{t2}^2} \quad (12)$$

Substituting in Equation 12

$$= \sqrt{(0.88\mu\text{V})^2 + (.061\mu\text{V})^2 + (.68\mu\text{V})^2 + (0.4\mu\text{V})^2 + (.128\mu\text{V})^2}$$

$$= 1.12\mu\text{V rms}$$

Total input-referred noise = 6.7μV peak to peak (0.01Hz to 100Hz)

This is 5.9 times that of the low noise op amp example.

The calculation examples illustrate three rules for minimizing noise in operational amplifier applications:

RULE 1. Use an op amp with low corner frequencies.

RULE 2. Keep source resistances as low as possible.

RULE 3. Limit circuit bandwidth to signal bandwidth.

NOISE PERFORMANCE

This segment shall be concerned with determining the signal to noise characteristics and the noise figure of amplifiers.

The amplifier noise is composed of thermal noise generated in the base resistance shot noise caused by the arrival of discrete charges at diode junction and 1/f noise.

For simplification these noise sources can be combined and the amplifier modeled by a noise source and a noiseless amplifier as in Figure 14.

e_n = Amplifier's equivalent mean square noise voltage $/\sqrt{\text{Hz}}$
i_N = Amplifier's equivalent mean square noise current$/\sqrt{\text{Hz}}$

NOISE ANALYSIS CIRCUIT

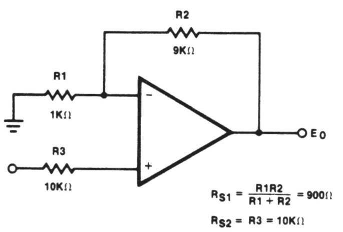

R2
9KΩ
R1
1KΩ
R3
10KΩ
-
+
EO
$R_{S1} = \frac{R1R2}{R1 + R2} = 900\Omega$
$R_{S2} = R3 = 10K\Omega$

Figure 13a

NOISE ANALYSIS EQUIVALENT CIRCUIT

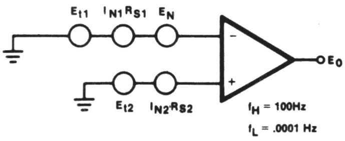


Figure 13b

The total output noise can now be computed by equation 8:

$$e_t = (e_n^2 + i_n^2 R_s^2 + 4KTR_s)^{1/2} B^{1/2}\ A \text{ rms volts} \quad (8)$$

*assuming R_S small compared to amplifier input.

If we now compare the total output noise to the output signal, A-Es, we find the output signal to noise ratio.

$$S/N = \frac{E_s}{(e_n^2 + i_n^2 R_s^2 + 4KTR_s)^{1/2} B^{1/2}} \quad (13)$$

The denominator of the S/N ratio is the total output noise divided by the midband gain or the equivalent input noise as shown on NE542 specification sheet.

$$E_{IN} = (e_n^2 + i_n^2 R_s^2 + 4KTR_s)^{1/2} B^{1/2} \text{ rms volts} \quad (14)$$

The S/N ratio may now be computed independent of the amplifier gain. However, the gain should be chosen to maintain linear operation of the amplifier. For example: If the input signal to the NE542 is 400μV rms from a source resistance of 680 ohm with a bandwidth of 100Hz to 10kHz, the S/N ratio becomes, in dB:

$$S/N = 20 \log \frac{400\ \mu\text{V}}{0.77\mu\text{V}}$$

$$= 54.3\text{dB}$$

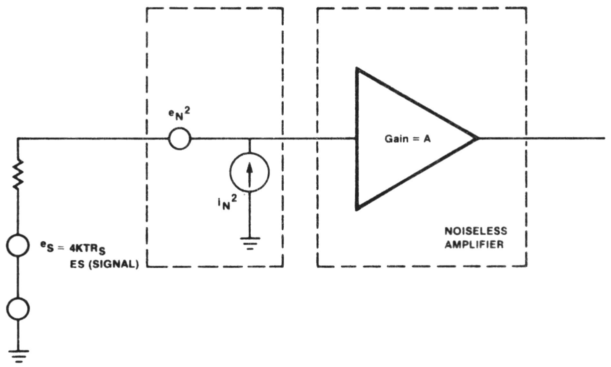


Figure 14

An amplifier gain of 68dB yields an output signal voltage of 1V rms.

For an input signal of 10mV rms, 40dB of gain, and 1V rms output, the NE542 gives a S/N ratio:

$$S/N = 20 \log \frac{10{,}000}{0.77} = 82.3\text{dB}$$

Another popular figure of merit for measuring the noise performance of an amplifier is noise figure. We first define noise factor (F) as

$$F = \frac{\text{Noise power input(Tot.)}}{\text{Thermal noise power}}$$

in terms of voltage this can be expressed as:

$$F = \frac{4KTR_s + (e_n{}^2 + i_n{}^2R_s{}^2)}{4KTR_s} = 5.34,\ R_S = 680\Omega \tag{15}$$

The noise figure is now defined as:

$$\text{N.F.} = 10 \log F \text{ (dB)}$$

or

$$\text{N.F.} = 10 \log \frac{4KTR_s + e_n{}^2 + i_n{}^2R_s{}^2}{4KTR_s} \text{(dB)} \tag{16}$$

A noiseless amplifier will, therefore, have a noise figure of "0" dB. Although the bandwidth has been eliminated from this calculation, it is still an influencing factor on the noise figure since the value of e_n and i_n will be dependent on the bandwidth of interest. This is especially true if l/f or high frequency noise is in this bandwidth.

From Figures 15 and 16 we can calculate the noise figure. For the NE542 the noise figure for 100 Hz to 10Hz, 3dB bandwidth (15.7 kHz equivalent noise bandwidth) and a source resistance of 5K ohms is:

$$\text{N.F.} = 10 \log \left(1 + \frac{e_n{}^2 + i_n{}^2R_s{}^2}{4KTRS}\right) \tag{17}$$

$$NF = 10 \log \left(1 + \frac{(7)^2 \times 10^{-18} + (.25)^2 \times 10^{-24} \times R_S{}^2}{75 \times 10^{-18}}\right)$$

$$4 \times 1.38 \times 15^{23} \times 300° K \times R_S$$

$$= 10 \log \times$$

$$= 7.27 @ R_S = 680\Omega$$
$$= 2.07 @ R_S = 5K\Omega$$
$$= 1.25 @ R_S = 10K\Omega$$

To this point, the discussion has been limited to flat band response and no mention of the effect of equalization networks has been made. In instances where the gain of the amplifier is changing significantly across the frequency band of interest, as is the case for NAB and RIAA equalization, the noise performance is significantly improved.

The following table lists the spectral voltage and current noise densities and the respective corner frequencies for several different operational amplifiers and low noise preamplifiers.

where I_N = total current noise over a specified bandwidth.
E_N = total voltage noise over a specified bandwidth.
E_{ti} = thermal (Johnson) noise of the source resistance.
$^*R_S$ = equivalent input source (or generator) resistance.

NOTE

If R_S is a complex function, Z_S, then this function must be calculated for the R_{SS} mean of each bandwidth considered. For example the input is a capacitor in parallel with a resistor, the input impedance is therefore:

$$Z_{in} = \frac{R}{1 + jwCR}$$

Therefore as the frequency varies the absolute value of Z_{in} will vary and will affect the $I_NR_S{}^*$, input noise value.

GENERAL EQUATIONS

Total Spectral Voltage Noise

$$E_N\,(f_H - f_L) = e_n \sqrt{f_{CE} \ln \left(\frac{f_H}{f_L}\right) + (f_H - f_L)} \tag{18}$$

Total Spectral Noise Current

$$I_n\,(f_H - f_L) = i_n \sqrt{f_{c1} \ln \left(\frac{f_H}{f_L}\right) + (f_H - f_L)} \tag{19}$$

Thermal

$$E_t = 4\ KTR\,(f_H - f_L) \tag{20}$$
$K = 1.38 \times 10^{-23}$ joules/° K
T = abs. temp in °K
k = ohms
$f_t = 1.28 \times 10^{-10} \sqrt{R(f_H - f_L)}$ at Room Temp.

Shot at Room

$$I_{SH} = 5.64 \times 10^{-10} \sqrt{I_{bias}\,(f_H - f_L)} \tag{21}$$

Total Noise*

$$\left|ENT\right|_{f_L}^{f_H} = \sqrt{E_n{}^2 + (I_N R_{S1})^2 + I_{N2} R_{S2}{}^2 + E_{t1}{}^2 + E_{t2}{}^2} \tag{22}$$

SPECTRAL VOLTAGE AND CURRENT NOISE DENSITIES

	μA741	5534	LF357	NE542	LM387
e_n (nv/√Hz)	40	4	12	7	9
i_n (pa/√Hz)	.25	.6	.01	.25	0.7
e_n fce (Hz)	200	90	50	800	850
i_n fci (Hz)	1.5k	200	1	700	2

TABLE 2

NOTES

1. The current spectral noise is omitted for the LF series since current noise levels in J-FET devices are insignificant.
2. The spectral current noise for the LM387 is relatively linear over the frequency spectrum of 100Hz to 10 kHz and is not specified below 100Hz.

EXPLANATION OF NOISE

INPUT NOISE CURRENT VS. FREQUENCY

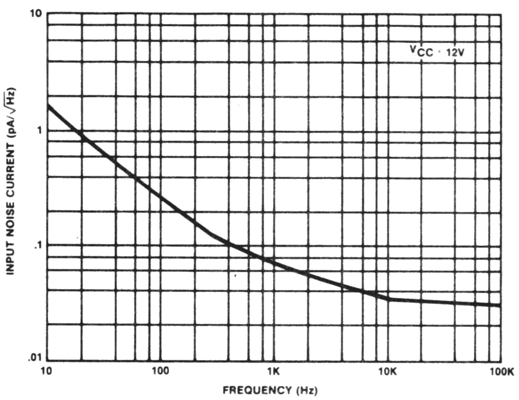


Figure 15

INPUT NOISE VOLTAGE VS. FREQUENCY

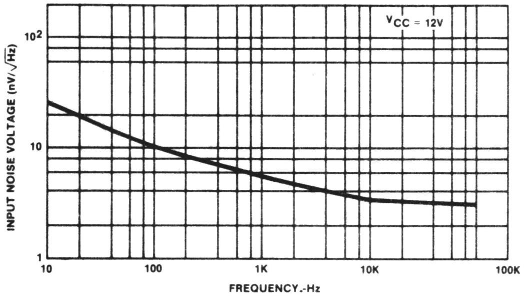


Figure 16

TOTAL NOISE CONFIGURATION

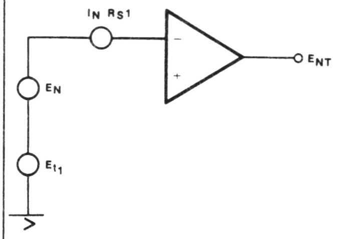


Figure 17

Example:

In order to determine the total noise of any device the following basic procedures can be used.

1. Determine the spectral voltage noise value $\bar{e}_n$ and the 3dB corner frequency. (If the value is not listed, but a curve given, the spectral noise value will be that value above the 3dB corner frequency on the flat portion of the curve.)
2. Determine the spectral current noise value $\bar{i}_n$ and the 3dB corner frequency. (The same note holds true as for the spectral voltage noise, except that the corner frequencies are generally not the same).
3. Determine the thermal noise of the input port source resistances by using the basic equal at room temperature of $E_T = 1.28 \times 10^{-10}\sqrt{R}/\sqrt{Hz}$
4. Using Equation 1, 2, and 4 and using Figure 1 as a basic block, we then can determine the total current and voltage noise at the input ports.
5. Employing Equation 5 we can then determine the total RSS voltage noise referred to the input of the amplifier.
6. If the closed loop gain of the system is known, then the total output noise is then
   $E_{Nout} = E_{Nin} \times A_{CL}$

Given: From Table 2, the NE5534 operating over the range of 10Hz to 1kHz and 1kHz to 10kHz, with $R_S = 10k\Omega$: determine total input noise over each bandwidth.

$$E_N\,(f_H - f_L) = e_n\sqrt{f_{ce}\,I_n\,\frac{f_H}{f_L} + (f_H - f_L)} \qquad (18)$$

$$I_N\,(f_H - f_L) = i_n\sqrt{f_{c1}\,I_n\,\frac{f_H}{f_L} + (f_H - f_L)} \qquad (19)$$

$$E_T = 1.28 \times 10^{-10}\sqrt{R(f_H - f_L)} \qquad (21)$$

$$\left|E_{NT}\right|_{f_L}^{f_H} = \sqrt{(E_N)^2 + (I_{n1}R_{s1})^2 + (E_t)^2} \qquad (22)$$

For the first band (10Hz to 1kHz)

$$E_N = 4 \times 10^{-9}\sqrt{90\ 1n\,(100) + (990)} = .15\mu V \text{ rms}$$

$$I_NR_S = .6 \times 10^{-12}\sqrt{200\ 1n\,(100) + (990) \times (10^4)} = .26\mu V \text{ rms}$$

$$E_T = 1.28 \times 10^{-8}\sqrt{990 =}\ 0.4\mu V \text{ rms}$$

$$E_{TH}\Big|_{10}^{1000} = \sqrt{(E_N)^2 + (I_NR_S)^2 + E_T{}^2 = 0.50\mu V \text{ rms}}$$

Using the factor of 6

$f_{noise\ p-p} = 3.00\mu V$ p-p will never be exceeded in 99.73% of all cases.

For the second band (1kHz to 10kHz)

$$^*E_N = 4 \times 10^{-9}\sqrt{9000} = .38\mu V \text{ rms}$$

$$^*I_NR_S = .6 \times 10^{-12}\sqrt{9000 \times (10^4)} = .58\mu V \text{ rms}$$

$$E_t = 1.28 \times 10^{-10}\sqrt{10^4\,(9000)} = 1.21\mu V \text{ rms}$$

NOTE
* For frequencies above 1kHz only white noise is a consideration.

$$\left|E_{TH}\right|_{1kHz}^{10kHz} = \sqrt{(.38)^2 + (.57)^2 + (1.21)^2}\,\mu V \text{ rms}$$

$$_{RSS}\left|E_{TH}\right|_{1kHz}^{10kHz} = \sqrt{1.39}\,\mu V \text{ rms}$$

$$E_{TH_{max}} = 8.34\mu V \text{ p-p}$$

CONCLUSION

The designer should look at the previous application note as a reasonable approach to determine system noise levels. The variations of parameters, such as resistance values, temperature, bandwidth are controllable by design procedure; however, the parametric variations of the monolithic op amps are controlled by the IC manufacturer. Signetics manufactures a wide variety of operational amplifiers designed to meet all contingencies.

NE5534 NOISE CHARACTERISTICS

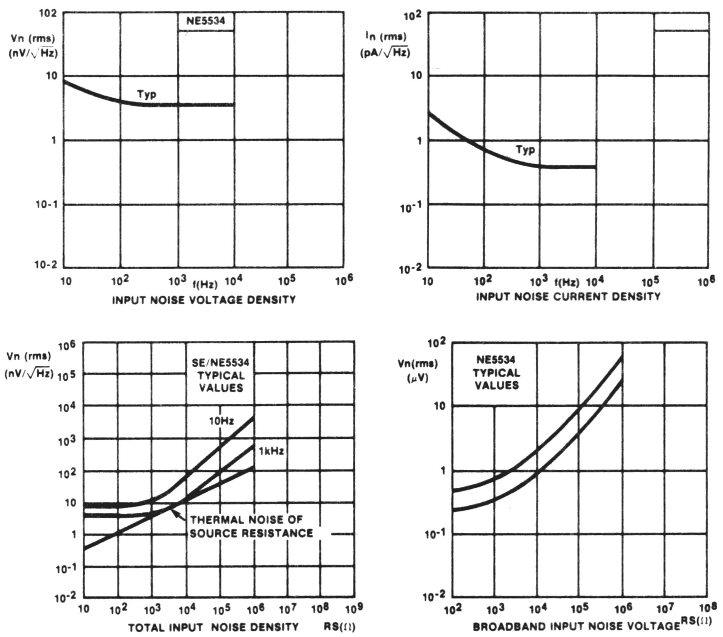


Figure 18

USING THE NE592/5592 VIDEO AMPLIFIER AN141

VIDEO AMPLIFIER PRODUCTS

NE/SE592 Video Amplifier

The 592 is a two stage differential output, wideband video amplifier with voltage gains as high as 400 and bandwidths up to 120MHz.

Three basic gain options are provided. Fixed gains of 400 and 100 result from shorting together gain select pins G_{1A} — G_{1B} and G_{2A}—G_{2B} respectively. As shown by Figure 1 the emitter circuits of the differential pair return thru independent current sources. This topology allows no gain in the input stage if all gain select pins are left open. Thus the third gain option of tying an external resistance across the gain select pins allows the user to select any desired gain from 0 to 400 volts per volt. The advantages of this configuration will be covered in greater detail under the filter application section.

Three factors should be pointed out at this time:

1. The gains specified are differential. Single ended gains are one half the stated value.
2. The circuit 3dB bandwidths are a function of and are inversely proportional to the gain settings.
3. The differential input impedance is an inverse function of the gain setting.

In applications where the signal source is a transformer or magnetic transducer the input bias current required by the 592 may be passed directly thru the source to ground. Where capacitive coupling is to be used, the base inputs must be returned to ground through a resistor to provide a dc path for the bias current.

Due to offset currents, the selection of the input bias resistors is a compromise. To reduce the loading on the source, the resistors should be large, but to minimize the output dc offset, they should be small — ideally 0 ohms. Their maximum value is set by the maximum allowable output offset and may be determined as follows:

1. Define the allowable output offset (assume 1.5V).
2. Subtract the maximum 592 output offset (from the data sheet). This gives the output offset allowed as a function of input offset currents (1.5V — 1.0V = 0.5V).
3. Divide by the circuit gain (assume 100). This refers the output offset to the input.
4. The maximum input resistor size is:

$$R_{MAX} = \frac{\text{Input Offset Voltage}}{\text{Max Input Offset Current}} \quad (1)$$

$$\frac{.005V}{5\mu A}$$

$$= 1.00k\Omega$$

Of paramount importance during the design of the NE592 device was bandwidth. In a monolithic device, this precludes the use of pnp transistors and standard level shifting techniques used in lower frequency devices. Thus without the aid of level shifting the output common mode voltage present on the NE592 is typically 2.9 volts. Most applications, therefore, require capacitive coupling to the load. An exception to the rule is a differential amplifier with an input common mode range greater than +2.9V as shown in Figure 2. In this circuit, the NE592 drives a NE511B transistor array connected as a differential cascode amplifier. This amplifier is capable of differential output voltages of 48V peak-to-peak with a 3dB bandwidth of approximately 10MHz (depending on the capacitive load). For optimum operation, R1 is set for a no signal level of + 18V. The emitter resistors, R_E, were selected to give the cascode amplifier a differential gain of 10. The gain of the composite amplifier is adjusted at the gain selected point of the NE592.

Filters

As mentioned earlier, the emitter circuit of the NE592 includes two current sources. Since the stage gain is calculated by dividing the collector load impedance by the emitter impedance, the high impedance contributed by the current sources causes the stage gain to be zero with all gain select pins open. As shown by the gain vs. frequency graph of Figure 3 the overall gain at low frequencies is a negative 48dB.

Higher frequencies cause higher gain due to distributed parasitic capacitive reactance. This reactance in the first stage emitter circuit causes increasing stage gain until at 10MHz the gain is 0dB or unity.

Referring to Figure 4, the impedance seen looking across the emitter structure includes small r_e of each transistor.

Any calculations of impedance networks across the emitters then must include this quantity. The collector current level is approximately 2mA causing the quantity of 2 r_e to be approximately 32 ohms. Overall device gain is thus given by

$$\frac{V_o(S)}{V_{IN}(S)} = \frac{1.4 \times 10^4}{Z_{(S)} + 32} \quad (2)$$

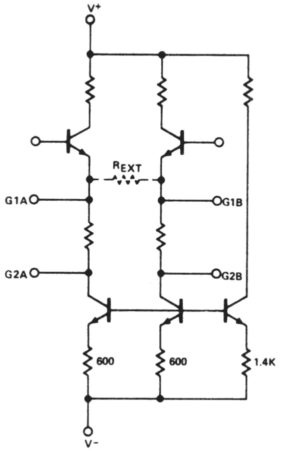
where $Z_{(S)}$ can be resistance or a reactive impedance. Table 2 summarizes the possible configurations to produce low, high, and bandpass filters. The emitter impedance is made to vary as a function of frequency by using capacitors or inductors to alter the frequency response. Included also in Table 2 is the gain calculation to determine the voltage gain as a function of frequency.

PARAMETER	NE/SE592	733
BANDWIDTH (MH$_Z$)	120	120
GAIN	0,100,400	10,100,400
R$_{IN}$ (K)	4-30	4-250
V$_{PP}$ (VOLTS)	4.0	4.0

Table 1 VIDEO AMPLIFIER COMPARISON FILE

USING THE NE592/5592 VIDEO AMPLIFIER

592 INPUT STRUCTURE



All resistor values are in ohms.

Figure 1

VOLTAGE GAIN AS A FUNCTION OF FREQUENCY (ALL GAIN SELECT PINS OPEN)

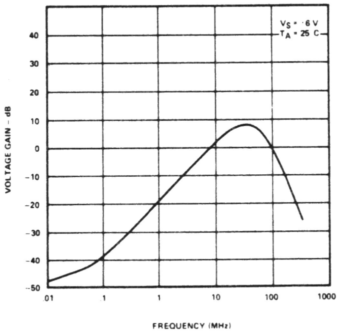
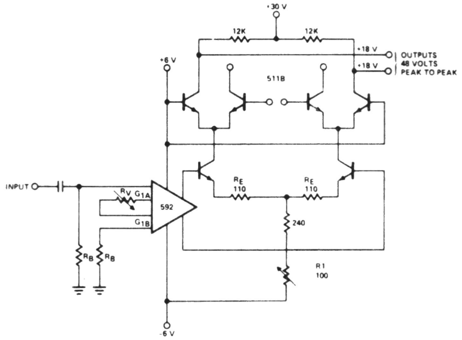


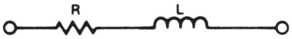
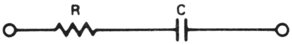
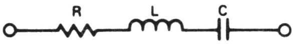
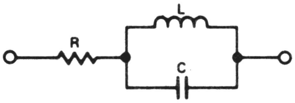
Figure 3

VIDEO AMPLIFIER WITH HIGH LEVEL DIFFERENTIAL OUTPUT



All resistor values are in ohms.

Figure 2

Z NETWORK	FILTER TYPE	$\frac{V_0(s)}{V_1(s)}$ TRANSFER FUNCTION
	LOW PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{1}{s + R/L}\right]$
	HIGH PASS	$\frac{1.4 \times 10^4}{R}\left[\frac{s}{s + 1/RC}\right]$
	BAND PASS	$\frac{1.4 \times 10^4}{L}\left[\frac{s}{s^2 + R/L\,s + 1/LC}\right]$
	BAND REJECT	$\frac{1.4 \times 10^4}{R}\left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC}\right]$

NOTE: In the networks above, the R value used is assumed to include 2 r_e, or approximately, 32 ohms.

Table 2 FILTER NETWORKS

Differentiation

With the addition of a capacitor across the gain select terminals the NE592 becomes a differentiator. The primary advantage of using the emitter circuit to accomplish differentiation is the retention of the high common mode noise rejection. Disc file playback systems rely heavily upon this common mode rejection for proper operation. Figure 5 shows a differential amplifier configuration with transfer function.

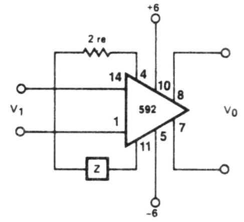
Disc file Decoding

In recovering data from disc or drum files, several steps must be taken to pre-condition the linear data. The NE592 video amplifier, coupled with the 8T20 bi-directional one-shot, provides all the signal conditioning necessary for phase encoded data.

When data is recorded on a disc, drum or tape system, the readback will be a Gaussian shaped pulse with the peak of the pulse corresponding to the actual recorded transition point. This readback signal is usually 500μV p-p to 3mV p-p for oxide coated disc files and 1 to 20mV p-p for nickel-cobalt disc files. In order to accurately reproduce the data stream originally written on the disc memory, the time of peak point of the Gaussian readback signal must be determined.

The classical approach to peak-time determination is to differentiate the input signal. Differentiation results in a voltage proportional to the slope of the input signal. The zero-crossing point of the differentiator, therefore, will occur when the input signal is

BASIC GAIN CONFIGURATION FOR NE592, N14


+6
2 re
14
4
10
8
592
V1
Vo
1
7
5
11
Z
-6

$$\frac{V_0(s)}{V_1(s)} = \frac{1.4 \times 10^4}{Z(s) + 2r_e}$$

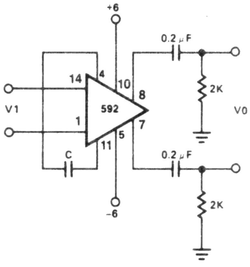
$$= \frac{1.4 \times 10^4}{Z(s) + 32}$$

Figure 4

at a peak. Using a zero-crossing detector and one-shot, therefore, results in pulses occurring at the input peak points.

A circuit which provides the preconditioning described above is shown in Figure 6. Readback data is applied directly to the input of the first NE592. This amplifier functions as a wideband ac coupled amplifier with a gain of 100. The NE592 is excellent for this use because of its high phase linearity, high gain and ability to directly couple the unit with the readback head. By direct coupling of readback head to amplifier, no matched terminating resistors are required and the excellent common mode rejection ratio of the amplifier is preserved. DC components are also rejected because the NE592 has no gain at dc due to the capacitance across the gain select terminals.

DIFFERENTIAL WITH HIGH COMMON MODE NOISE REJECTION


+6
0.2 μF
14
4
10
8
2K
V1
592
VO
1
7
5
11
C
0.2 μF
2K
-6

For frequency $F_1 << 1/2\ \pi(32)C$

$V_0 \cong 1.4 \times 10^4 C \frac{dvi}{dT}$

All resistor values are in ohms.

Figure 5

The output of the first stage amplifier is routed to a linear phase shift low pass filter. The filter is a single stage constant K filter, with a characteristic impedance of 200Ω. Calculations for the filter are as follows:

$L = 2R/\omega c$ Where R = characteristic impedance (ohms)

$C = 1/\omega c$ ωc = cutoff frequency (radians/sec)

The second NE592 is utilized as a low noise differentiator/amplifier stage. The NE592 is excellent in this application because it allows differentiation with excellent common mode noise rejection.

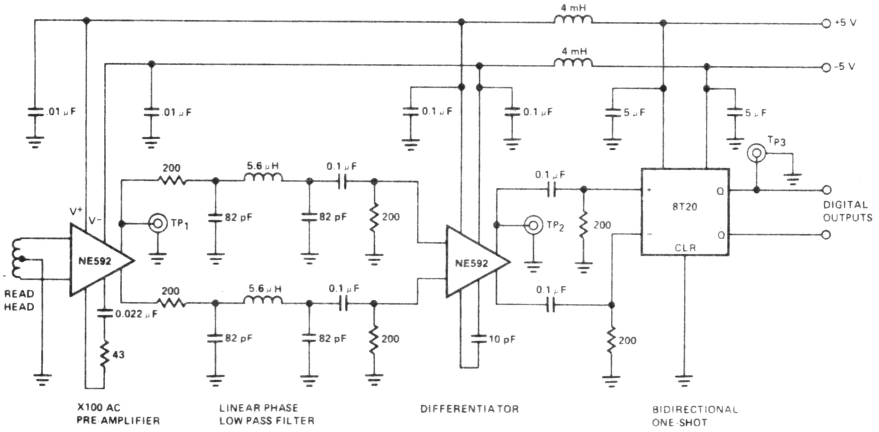
The output of the differentiator/amplifier is connected to the 8T20 bi-directional monostable unit to provide the proper pulses at the zero-crossing points of the differentiator.

The circuit in Figure 6 was tested with an input signal approximating that of a readback signal. The results are shown in Figure 8.

Automatic Gain Control

The NE592 can also be connected in conjunction with a MC1496 balanced modulator to form an excellent automatic gain control system.

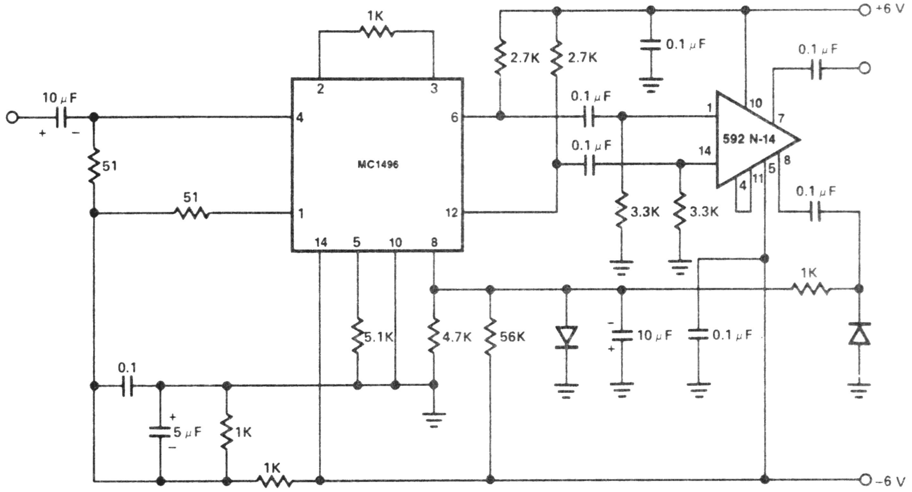
5MHz PHASE—ENCODED DATA READ CIRCUITRY


4 mH
+5 V
4 mH
-5 V
.01 μF
.01 μF
0.1 μF
0.1 μF
5 μF
5 μF
TP3
200
5.6 μH
0.1 μF
0.1 μF
V+
V-
TP1
82 pF
82 pF
200
TP2
200
8T20
Q
Q
CLR
DIGITAL OUTPUTS
NE592
NE592
READ HEAD
200
5.6 μH
0.1 μF
0.1 μF
0.022 μF
82 pF
82 pF
200
10 pF
200
43
X100 AC PRE AMPLIFIER
LINEAR PHASE LOW PASS FILTER
DIFFERENTIATOR
BIDIRECTIONAL ONE SHOT

All resistor values are in ohms

Figure 6

WIDE BAND AGC AMPLIFIER


1K
2.7K
2.7K
0.1 μF
+6 V
0.1 μF
10 μF
+
−
2
3
4
6
MC1496
0.1 μF
0.1 μF
1
10
7
592 N-14
14
8
5
11
4
51
51
1
12
14
5
10
8
3.3K
3.3K
0.1 μF
1K
5.1K
4.7K
56K
10 μF
0.1 μF
0.1
5 μF
1K
1K
−6 V

All resistor values are in ohms.

Figure 7

The signal is fed to the signal input of the MC1496 and RC coupled to the NE592. Unbalancing the carrier input of the MC1496 causes the signal to pass thru unattenuated. Rectifying and filtering one of the NE592 outputs produces a dc signal which is proportional to the ac signal amplitude. After filtering this control signal is applied to the MC1496 causing its gain to change.

TEST RESULTS OF DISC FILE DECODER CIRCUIT (FIGURE 5-108)

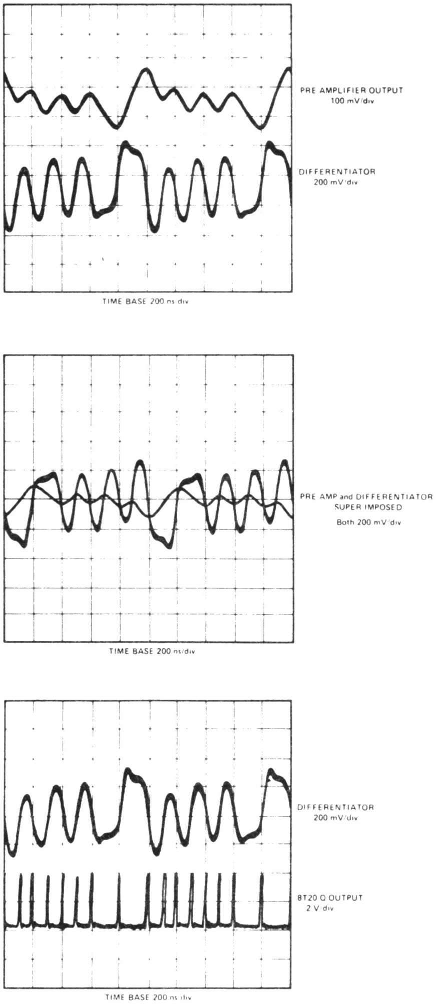


Figure 8

COMPENSATION TECHNIQUES FOR USE WITH THE SE/NE5539 AN140

NE5539 DESCRIPTION

The Signetics SE/NE5539 ultra-high frequency operational amplifier is one of the fastest monolithic amplifiers made today. With a unity gain bandwidth of 350MHz and a slew rate of 600V/μs, it is second to none. Therefore, it is understandable that to attain this speed, standard internal compensation would have to be left out of its design. As a consequence, the op amp is not unconditionally stable for all closed-loop gains and must be externally compensated for gains below 17dB. Properly done, compensation need not limit slew rate. The following will explain how to use the methods available with the SE/NE5539.

LEAD AND LAG-LEAD COMPENSATION

A useful method for compensating the device for closed-loop gains below seven is to use lag-lead and lead networks as shown in Figure 1. The lead network is primarily concerned with compensating for loss of phase margin caused by distributed board capacitance and input capacitance, while lag-lead is mainly for optimizing transient response. Lead compensation modifies the feedback network and adds a zero to the overall transfer function. This increases the phase, but does not greatly change the gain magnitude. This zero improves the phase margin.

To determine components, it can be shown that the optimal conditions for amplifier stability occur when:

$$(R1)(C_{dist}) = (R_F)(C_{lead}) \qquad (1)$$

However, when the stability criteria is obtained, it should be noted that the actual bandwidth of the closed-loop amplifier will be reduced. Based on using a double-sided copper-clad printed circuit board with a distributed capacitance of 3.5pF and a unity gain configuration, C_{lead} would be 3.5pF. Another way of stating the relationship between the distributed capacitance closed-loop gain and the lead compensation capacitor is:

$$C_{lead} = C_{dist}\frac{R1}{R_F} \qquad (2)$$

When bandwidth is of primary concern, the lead compensation will usually be adequate. For closed-loop gains less than seven, lag-lead compensation is necessary for stability.

If transient response is also a factor in design, a lag-lead compensation network may be necessary. (Reference Figure 1.) For practical applications, the following equations can be used to determine proper lag-lead components:

$$\frac{R_F}{R1 // R_{lag}} \geq 7 \qquad (4)$$

Therefore,

$$R_{lag} \leq \frac{R_F}{7 - R_F/R1} \qquad (5)$$

Using the above equation will insure a closed-loop gain of seven above the network break frequency. C_{lag} may now be approximated using:

$$W_{lag} \cong \frac{2\pi(GBW)}{10}\ \text{Rad/Sec} \qquad (6)$$

$$W_{lag} = \frac{\pi(GBW)}{5}\ \text{Rad/Sec} \qquad (7)$$

Where

$$W_{lag} = \frac{1}{(R_{lag})(C_{lag})} \qquad (8)$$

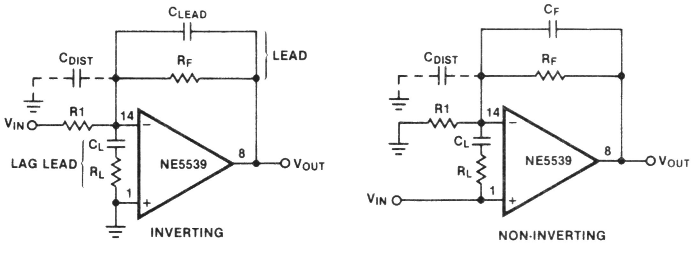
Therefore,

$$\frac{\pi(GBW)}{5} = \frac{1}{(R_{lag})(C_{lag})} \qquad (9)$$

And

$$C_{lag} = \frac{5}{\pi R_{lag}(GBW)} \qquad (10)$$

This method adds a pole and zero to the transfer function of the device, causing the actual open-loop gain and phase curve to be reshaped, thus creating a progressive improvement above the critical frequency where phase changes rapidly. (Near 70MHz; see Figures 2A and 2B.) But also, the lag-lead network can be adjusted to optimize gain peaking for transient responses. Therefore, rise time, overshoot, and settling time can be changed for various closed-loop gains. The result of using this technique is shown for a pulse amplifier in Figure 3.



$C_L = C_{LAG}$
$R_L = R_{LAG}$

Figure 1. Standard Lag-Lead Compensation

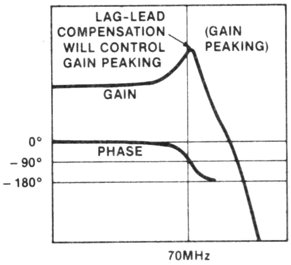


Figure 2A. Closed-Loop Inverting Gain of Seven Gain-Phase Response (Uncompensated)

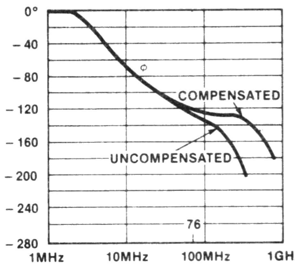


Figure 2B. Open-Loop Phase

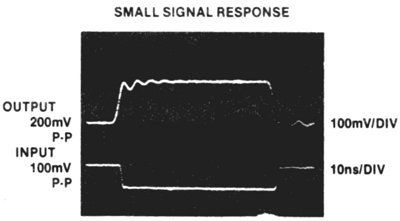


Figure 3. Compensated Pulse Response

USING PIN 12 COMPENSATION

An alternate method of external compensation is obtained by use of the SE/NE5539 frequency compensation pin. The circuits in Figure 4 show the correct way to use this pin. As can be seen, this method saves the use of one capacitor as compared to standard lag-lead and lead compensation as shown in Figure 1.

But, most important, both methods are equally effective; i.e., a good wideband amplifier below 17dB, with control over ringing and overshoot. For example, inverting and non-inverting amplifier circuits using pin 12 are shown in Figure 5. The corresponding pulse response for each circuit is shown in Figures 6 and 7 for the

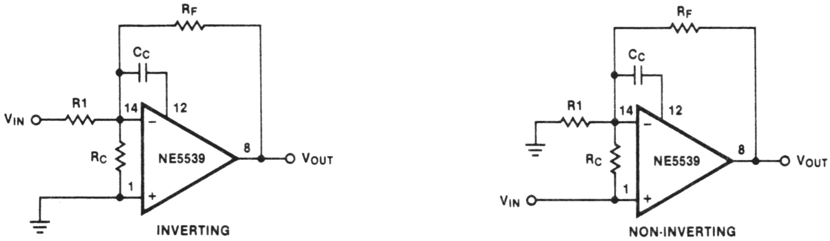

RF
CC
R1
VIN
14
12
RC
NE5539
8
VOUT
1
INVERTING
RF
CC
R1
14
12
RC
NE5539
8
VOUT
VIN
1
NON-INVERTING

Figure 4. Pin 12 Compensation

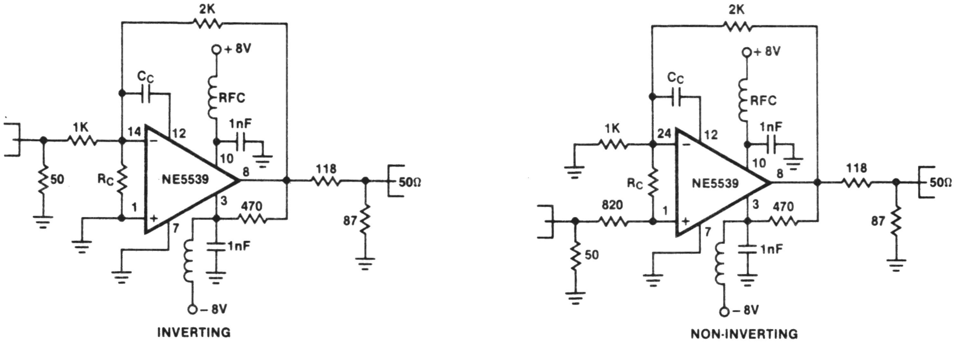
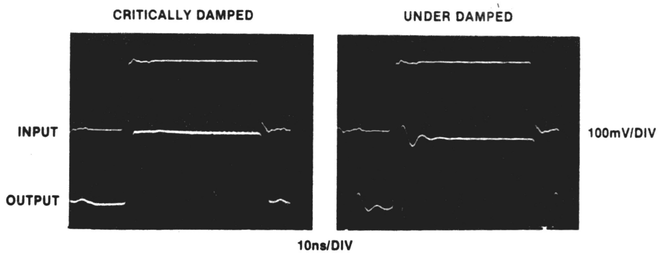

2K
+8V
CC
RFC
1nF
1K
14
12
10
50
RC
NE5539
8
118
50Ω
1
3
470
87
7
1nF
-8V
INVERTING
2K
+8V
CC
RFC
1nF
1K
24
12
10
RC
NE5539
8
118
50Ω
820
1
3
470
87
7
50
1nF
-8V
NON-INVERTING

Figure 5. Pulse Response Test Circuits



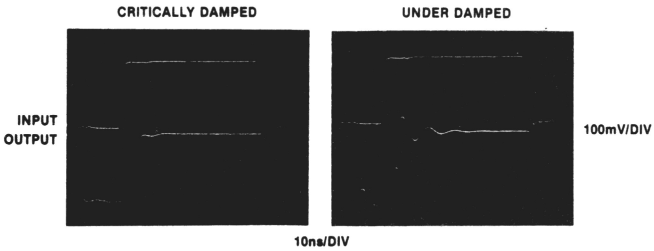
RISE TIME – 2.4ns
$R_C = 118\Omega$ — $C_C = 4.6pF$
PROPAGATION DELAY = 2.3ns

(a)

RISE TIME – 2.1ns
$R_C = 200$ — $C_C = 5.4pF$
PROPAGATION DELAY = 2.3ns

(b)

Figure 6. Small Signal Response — Non-Inverting



RISE TIME 5.3ns
$R_C = 226\Omega$ — $C_C = 2.3pF$
PROPAGATION DELAY = 5.1ns

(a)

RISE TIME – 3.3ns
$R_C = 460\Omega$ — $C_C = 2.0pF$
PROPAGATION DELAY = 4.5ns

(b)

Figure 7. Small Signal Response — Inverting

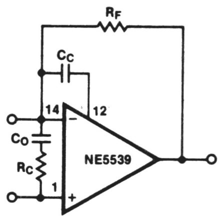


Figure 8. C_O Will Reduce Output Offset and Noise

network values recommended. As shown by the response photos, the overshoot and settling time can be controlled by adjusting R_C and C_C. In damping the overshoot, rise time is slightly decreased. Also, the non-inverting configuration (Figure 6) gives a very fast response time compared to the inverting mode.

If it is important to reduce output offset voltage and noise, an additional capacitor, C_O, can be added in series with the resistor (R_C) across the inputs. This should be a large value to block DC but not affect the benefits of the compensation components at high frequencies. A value of 0.01μF as shown in Figure 8 is sufficient.

INTERNAL CHARACTERISTICS OF THE SE/NE5539

In order to better understand the compensation procedure, a detailed discussion of the amplifier follows.

The complete amplifier schematic is shown in Figure 9. To clarify the effect of the compensation pin, the schematic is split into five main parts as shown in Figure 10.

Each segment in Figure 10 is defined as follows: starting from the non-inverting input, Section A_1 is the amplification from the input to the base of transistor Q_4. A_2 is from the base of Q_4 to the summation point at the collector of Q_3. Furthermore, A_3 represents the gain from the non-inverting input to the summation point via the common emitter side of Q_2 and Q_3. Finally, B_F is the feedback factor of the positive feedback loop from the collector of Q_3 to the base of Q_4.

From Figure 10, it can be seen that the total gain (A_T) is:

$$A_T = \frac{A_1A_2}{1-(B_FA_2)} + A_3(1 + B_FA_2)$$

Each term in this equation plays a role at different frequencies to determine the total transfer function of the device. Of particular importance is the pole in A_3 (near 340MHz) which causes a roll-off of 12dB/octave and loss of phase margin just before unity gain. This can be seen in the Bode plot in Figure 11A. To overcome this pole, a capacitor and resistor are connected as shown in Figures 12A and 12B. The compensation pin is connected to the emitter of Q_5, which is in an emitter-follower configuration. Therefore, a reactance connected to pin 12 acts essentially as if it were connected at the base of Q_5. Since the capacitor is connected here, it is now a component of B_F and a zero is added to the transfer function. The resistor across the input pins controls overall gain and causes A_T to cross 0dB at a lower frequency; the capacitor in the feedback loop controls phase shift and gain peaking.

To further explain, Bode plots of open-loop response using varying capacitor values and corresponding pulse responses are shown in Figures 13A through 13F. The changes in gain and phase can readily be seen, as is the effect on bandwidth.

COMPUTER ANALYSIS

The open-loop and pulse response plots were generated using an IBM 370 computer and SPICE, a general-purpose circuit

COMPENSATION TECHNIQUES FOR USE WITH THE SE/NE5539 AN140

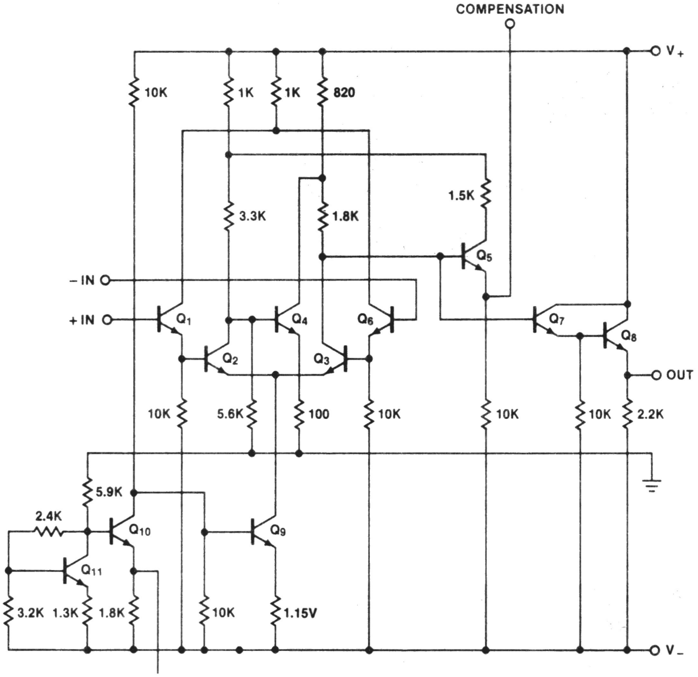

COMPENSATION
V+
10K
1K
1K
820
1.5K
3.3K
1.8K
Q5
−IN
+IN
Q1
Q4
Q6
Q7
Q8
Q2
Q3
OUT
10K
5.6K
100
10K
10K
10K
2.2K
5.9K
2.4K
Q10
Q9
Q11
3.2K
1.3K
1.8K
10K
1.15V
V−

Figure 9. Complete Schematic of SE/NE5539

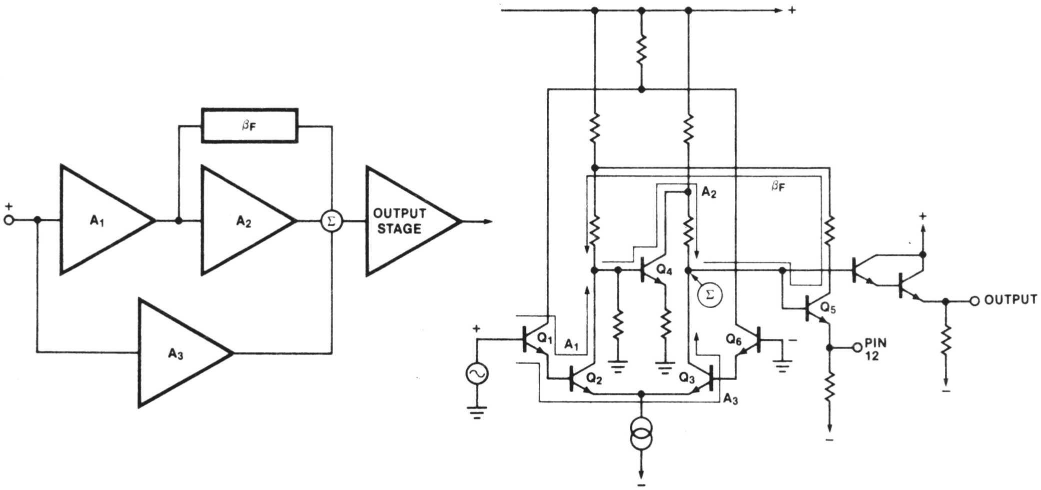

+
A1
βF
A2
Σ
OUTPUT STAGE
A3
+
A2
βF
Q4
Σ
+
Q5
OUTPUT
+
Q1
A1
Q6
PIN 12
Q2
Q3
A3
−
−
−

Figure 10. Internal Sections

COMPENSATION TECHNIQUES FOR USE WITH THE SE/NE5539 AN140

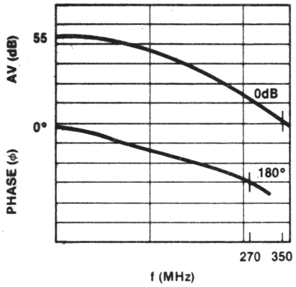


Figure 11A. Open-Loop Gain — No Compensation (Computer Simulation)

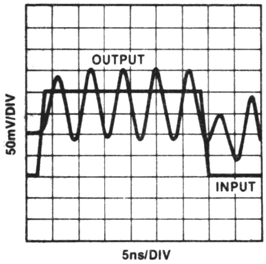


Figure 11B. Closed-Loop Non-Inverting Response — No Compensation (Computer Simulation — Oscillation is Evident)

simulation program. Each transistor in the part is mathematically modeled after actual device parameters, which were measured in the laboratory. Then these models are combined with the resistors and voltage sources through node numbers so that the computer knows where each is connected.

To indicate the accuracy of this system, the actual open-loop gain is compared to the computer plots in Figures 14 and 15. The real payoff for this system is that once a credible simulation is achieved, any outside circuit can be modeled around the op amp. This would be used to check for feasibility before breadboarding in the lab. The internal circuit can be treated like a black box and the outside circuit program altered to whatever application the user would like to examine.

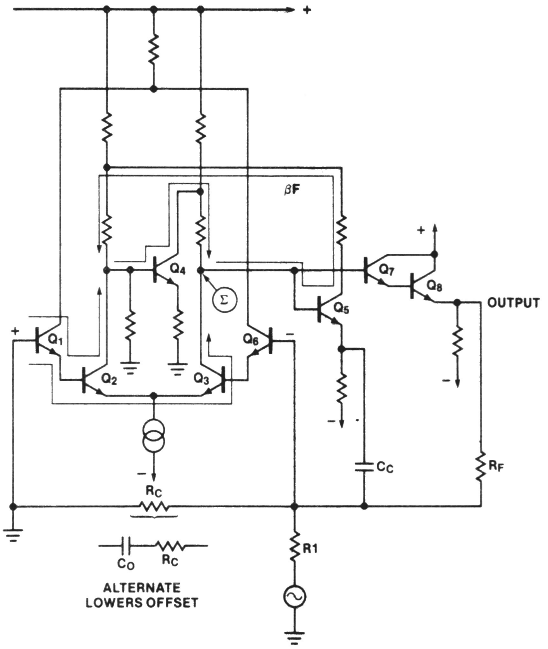

+
βF
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Σ
+
−
OUTPUT
Cc
RF
Rc
R1
Co
Rc
ALTERNATE
LOWERS OFFSET

Figure 12A. Pin 12 Compensation Showing Internal Connections — Inverting

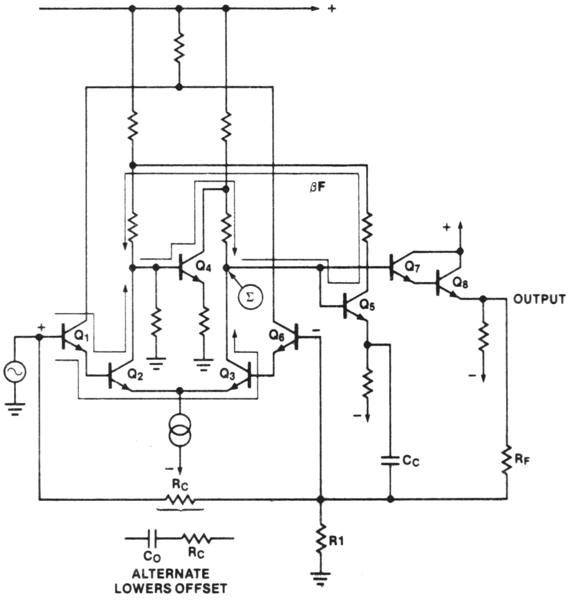

+
βF
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Σ
+
−
OUTPUT
Cc
RF
Rc
R1
Co
Rc
ALTERNATE
LOWERS OFFSET

Figure 12B. Pin 12 Compensation Showing Internal Connections — Non-Inverting

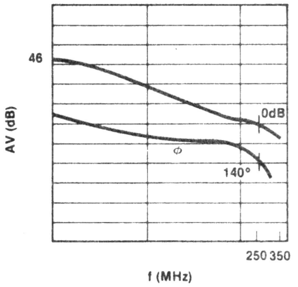


Figure 13A. Open-Loop Pin 12 Compensation — $R_C = 200\Omega$, $C_C = 1pF$, (Computer Simulation)

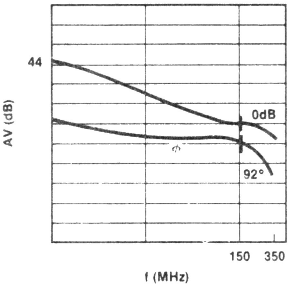


Figure 13C. Open-Loop Pin 12 Compensation — $R_C = 200\Omega$, $C_C = 2pF$, (Computer Simulation)

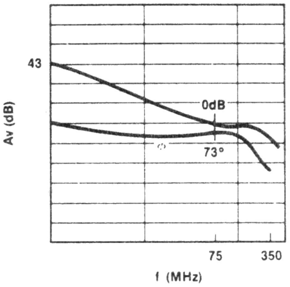


Figure 13E. Open-Loop Pin 12 Compensation — $R_C = 200\Omega$, $C_C = 3pF$, (Computer Simulation)

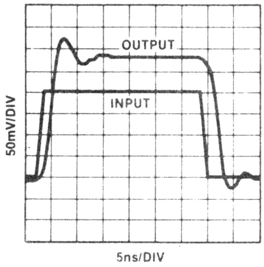


Figure 13B. Closed-Loop Non-Inverting Pulse Response — $R_C = 200\Omega$, $C_C = 1pF$, $Av = 3$ (Computer Simulation — Underdamped)

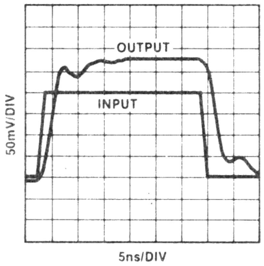


Figure 13D. Closed-Loop Non-Inverting Pulse Response — $R_C = 200\Omega$, $C_C = 2pF$, $Av = 3$ (Computer Simulation — Critically Damped)

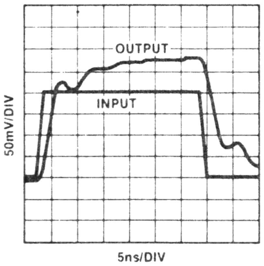


Figure 13F. Closed-Loop Non-Inverting Pulse Response — $R_C = 200\Omega$, $C_C = 3pF$, $A_V = 3$ (Computer Simulation — Overdamped)

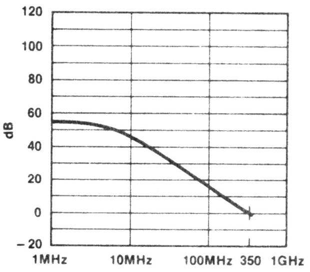


Figure 14. Actual Open-Loop Gain Measured in Lab

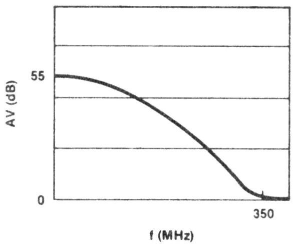


Figure 15. Computer-Generated Open-Loop Gain

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2. A. Vladimirescu, Kaihe Zhang, A. R. Newton, D. O. Peterson, A. Sanquiovanni-Vincentelli: "Spice Version 2G," University of California, Berkeley, California, August 10, 1981.
3. Signetics: *Analog Data Manual 1983*, Signetics Corporation, Sunnyvale, California 1983.

AN OVERVIEW OF SWITCHED MODE POWER SUPPLIES — AN120

Conceptually, three basic approaches exist for obtaining regulated DC voltage from an AC power source. These are:

- **Shunt regulation**
- **Series linear regulation**
- **Series switched mode regulation**

All required AC power line rectification

The series switched mode regulators will be referred to as switched mode power supplies or SMPS during the course of this article.

Briefly stated, if all three types of regulation can perform the same function, following are some of the key parameters to be addressed:

- From an economical point of view, cost of the system is paramount.
- From an operations point of view, weight of the system is critical.
- From a design criteria, system efficiency is the first order of business.

The series and shunt regulators operate on the same principle of sensing the DC output voltage, comparing to an internal reference level and varying a resistor (active device) to maintain the output levels within pre-specified limits.

Switched mode power supplies (SMPS) are basically DC to DC converters, operating at frequencies in the 20kHz and higher region. Basically the SMPS is a power source which utilizes the energy stored during one portion of its operating cycle to supply power during the remaining segment of its operating cycle.

Linear regulators, both shunt and series, suffer when required to supply large currents with resultant high dissipation across the regulating device. Efficiency suffers tremendously. (Efficiencies less than 40% are typical.)

Switched mode power supplies operate at much higher levels of efficiency (generally in the order of 75% to 80%) thereby reducing significantly the energy wasted in the regulated supply. The SMPS does, however, suffer significantly in the ripple regulation it is able to maintain as opposed to a much higher degree of regulation available in series (or shunt) linear regulators.

The linear regulators obtain improved regulation by virtue of the series pass elements always conducting, as opposed to SMPS devices having their active devices operative only during a portion of the overall operating period.

Some definitions and comparisons between linear regulators and switched mode power supplies are below for reference.

REGULATION

Line Regulation:

(Sometimes referred to as static regulation) refers to the changes in the output (as a percent of nominal or actual value) as the input AC is varied slowly from its rated minimum value to its rated maximum value (eg. from 105VAC$_{RMS}$ to 125VAC$_{RMS}$).

Load Regulation:

(Sometimes referred to as dynamic regulation) refers to changes in output (as a percent of nominal or actual value) when the load conditions are suddenly changed (eg. minimum load to full load.)

NOTE
The combination of static and dynamic regulation are cumulative; care should be taken when referring to the regulation characteristics of a power supply.

Thermal Regulation:

Referred to as changes due to ambient variations or thermal drift.

TRANSIENT RESPONSE

The ability of the regulator to respond to rapid changes in either line variations, load variations, or intermittent transiet input conditions. (This parameter is often referred to as "recovery time.")

AC PARAMETERS

Voltage Limiting:

The regulator's ability to "shut down" in the event that the internal control elements fail to function properly.

Current Limiting:

Often referred to as "fold-back" where the amplifier segment of the regulator folds back the output current of the device when safe operating limits are exceeded.

Thermal Shutdown:

The regulator's ability to shut itself down when the maximum die temperature is exceeded.

GENERAL PARAMETERS

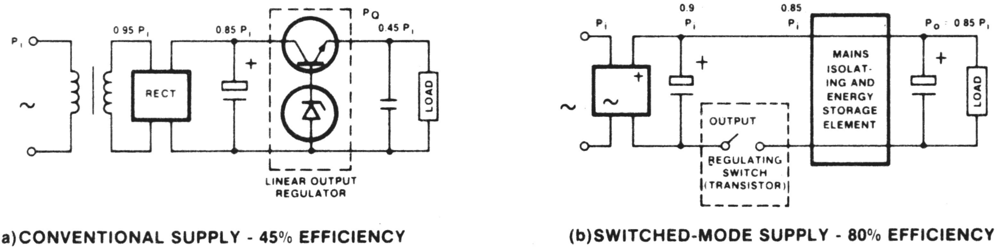
Power Dissipation:

The maximum power the regulator can tolerate and still maintain operation within the safe operating area of its active devices.

Efficiency:

The ratio (in percent) of the usable versus total power being dissipated in a regulated supply. (The losses can be ac as well as dc losses.)

LOSSES IN REGULATED POWER SUPPLIES



(a) CONVENTIONAL SUPPLY - 45% EFFICIENCY

(b) SWITCHED-MODE SUPPLY - 80% EFFICIENCY

Figure 1

AN OVERVIEW OF SWITCHED MODE POWER SUPPLIES

EMI/RFI:

Generation of radio frequency interference signals and magnetic field disturbance especially in SMPS devices. (Transformer and choke design are available which reduce both RFI & EMI to safe acceptance regions.)

The balance of this section will be dedicated to the discussion of the general operation of Switched Mode Power Supplies (SMPS) with emphasis on the Signetics NE5560 Control and Protection Module.

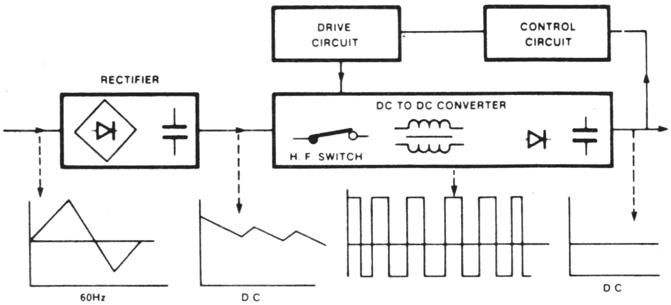
Switched-mode power supplies (SMPSs) have gained much popularity in recent years because of the benefits they offer. They are used now on a large scale in desk calculators, computers, as instrumentation supplies, etc., and it is confidently expected that the market for this type of supply will grow.

The advantages of SMPSs are low weight and small size, high efficiency, wide AC input voltage range, and low cost.

- Low weight and small size are possible because operation occurs at a frequency beyond the audible range; the inductive elements are small.
- High efficiency because, for output regulation, the power transistor is switched rapidly between saturation and cut-off and therefore has little dissipation; this eases heatsink requirements, which also contributes to weight and volume reduction. Conventional linear-regulator supplies may have efficiencies as low as 50%, or less, but efficiencies of 80% are readily achievable with SMPSs; see figure 1.
- Wide AC input voltage range because of the flexibility of varying the switching frequency in addition to the change in transistor duty cycle makes voltage adaptation unnecessary.
- Low overall cost, due to the reduced volume and dissipation, means that less material is required and smaller semiconductor devices suffice.

Switched-mode power supplies also have slight disadvantages in comparison with linear regulators, namely, somewhat greater circuit complexity, tendency to r.f.i. radiation, slower response to rapid load changes, and less ability to remove output ripple.

BLOCK DIAGRAM OF SWITCHED-MODE POWER SUPPLY



NOTE
Switching frequency is between 20kHz and 50kHz

Figure 2

HOW SWITCHED-MODE POWER SUPPLIES OPERATE

The switched-mode power supply is a modern version of its forerunner, the electromechanical vibrator used in the past to supply car radios. But the new concept is much more reliable because of the far greater lifetime of the transistor switch. Figure 2 shows the principle of the ac fed SMPS. In this system the ac voltage is rectified, smoothed, and supplied to the electronic chopper, which operates at a frequency above the audible range to prevent noise. The chopped dc voltage is applied to the primary of a transformer, and the secondary voltage is rectified and smoothed to give the required dc output. The transformer is necessary to isolate the output from the input. Output voltage is sensed by a control circuit, which adjusts the duty cycle of the switching transistor, via the drive circuit, to keep the output voltage constant irrespective of load and line voltage changes. Without the input rectifier, this system can be operated from a battery or other dc source.

Depending on the requirements of the application, the dc-to-dc converter can be one of the three basic types: flyback converter, forward converter, or push-pull (balanced) converter.

The Flyback Converter

Figure 3 shows the flyback converter circuit, and the waveforms of transistor voltage, V_{CE}, and choke current, i_L, reflected to the primary (choke double-wound for line isolation). Cycle time and transistor duty cycle are denoted T and δ, respectively. While Q1 conducts, energy is accumulated in the choke magnetic field (i_L rising and D_1 reversed biased), and it is discharged into the output capacitor and the load during the flyback period, that is, while Q1 is off (i_L falling and D_1 forward biased). During Q1 conduction, C_o continues delivering energy to the load so providing smoothing action. It will be noted that only one inductive element is needed, in distinction to the converter types discussed below, which require two. As the V_{CE} waveform shows, the peak collector voltage is twice the input voltage, V_i, for δ equal to 0.5.

The Forward Converter

A major advantage of the forward converter, particularly for low output voltage applications, is that the high-frequency output ripple is limited by the choke in series with the output. Figure 4 illustrates the circuit. During the transistor-on (or forward) period, energy is simultaneously stored in the choke L_O and passed via D_1 to the load. While Q1 is off, part of the energy accumulated in L_O is transferred to the load through free-wheeling diode D_2. Output capacitor C_O smoothes the ripple due to transistor switching. After transistor turn-off, the magnetic energy built up in the transformer core is returned to the dc input via the demagnetizing winding (closely coupled with the primary) and D_3, so limiting the peak collector voltage to twice the input voltage V_i.

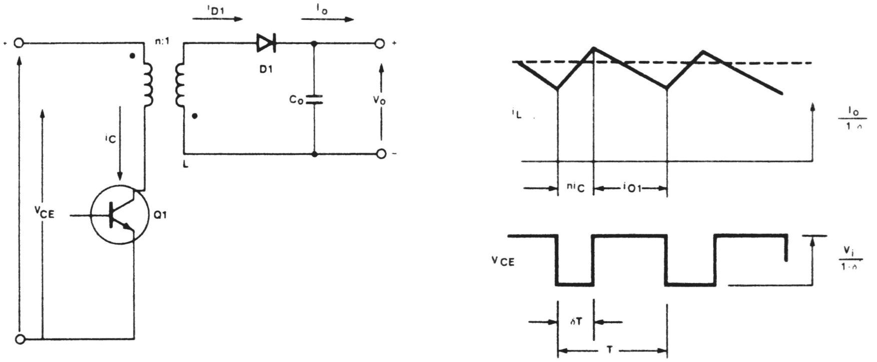
The Push-Pull Converter

This converter type, given in Figure 5, consists of two forward converters operating in push-pull. Diodes D_1 and D_2 rectify the rectangular secondary voltage generated by Q1 and Q2 being turned on during alternate half cycles. Push-pull operation doubles the frequency of the ripple current in output filter L_0C_0 and so reduces the output ripple voltage. The peak transistor voltage is $2V_i$.

MAKING THE BEST CONVERTER CHOICE

There exist several versions of the three fundamental circuits described earlier.

FLYBACK CONVERTER CIRCUIT DIAGRAM AND WAVEFORMS



NOTES
1. δ is the duty cycle of Q1; T is the cycle time
2. L is a double-wound choke

Figure 3

FORWARD CONVERTER CIRCUIT DIAGRAM

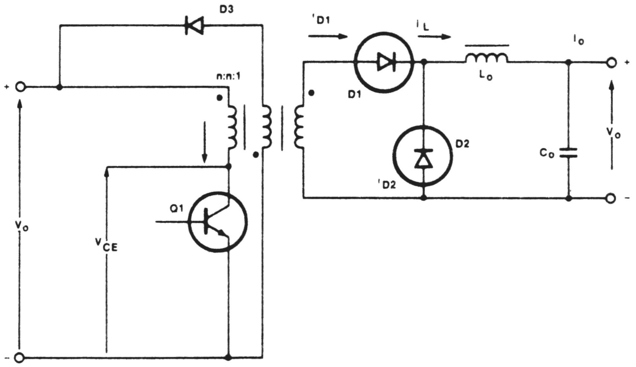


Figure 4

PUSH-PULL CONVERTER CIRCUIT DIAGRAM

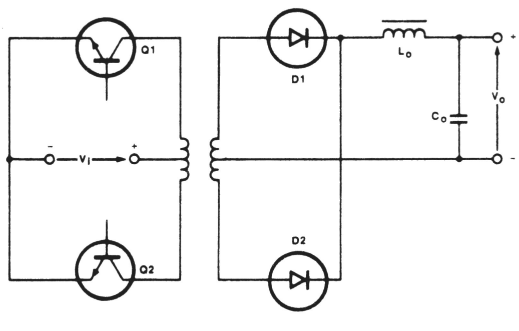


Figure 5

These are shown in Figure 6. Circuits IA, IIA and IIIA are the basic types. In the two-transistor circuits IB and IIB, transistors Q1 and Q2 conduct simultaneously and diodes D_4D_5 limit the peak collector voltage to the level of DC input voltage V_i. Similarly in the push-pull circuits IIIB and IIIC, the collector voltage does not exceed V_i, in circuit IIIB, Q1 and Q2 are turned on during alternate half cycles; in circuit IIIC, Q1 and Q4 are turned on in one half cycle and Q2 Q3 in the next.

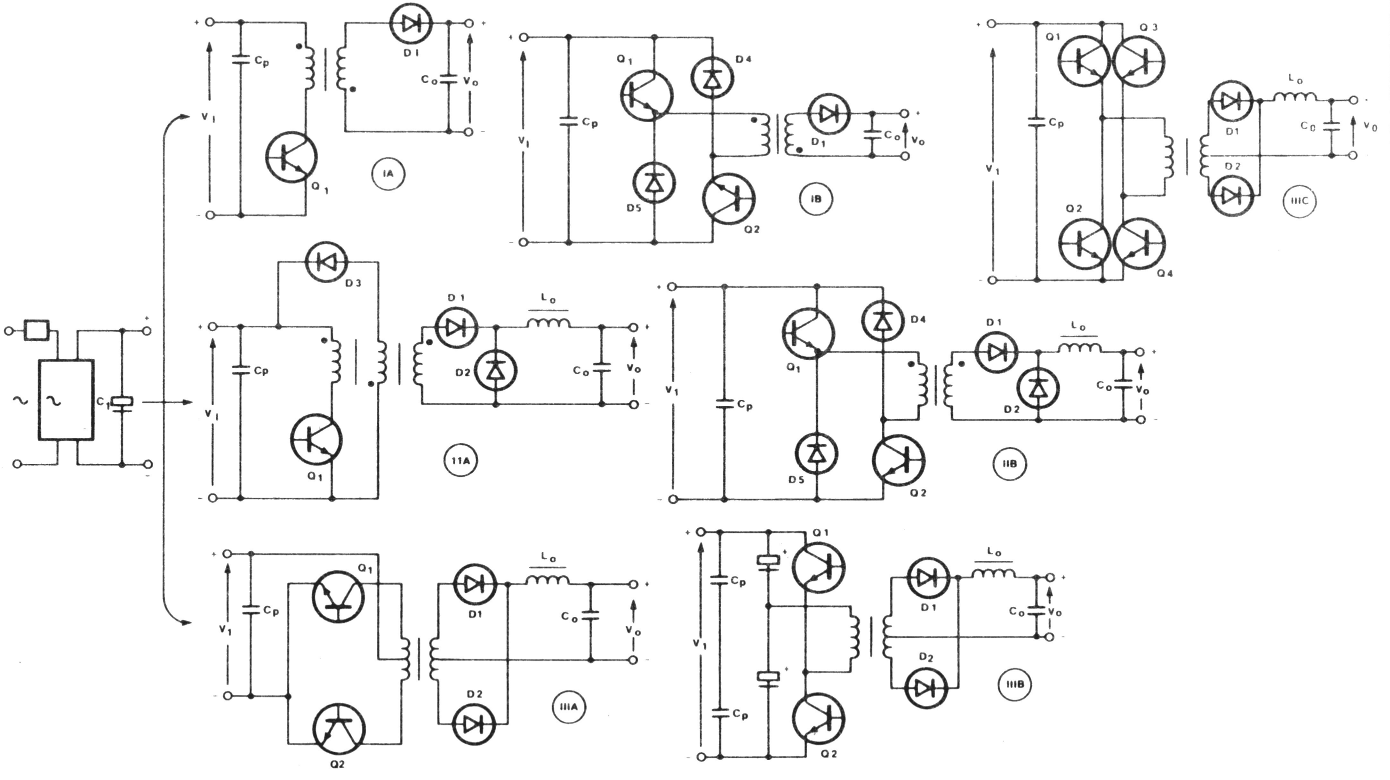
Converter choice depends on application and performance requirements. The flyback converter is the simplest and least expensive; it is recommended for multi-output supplies because each output requires only one diode and one capacitor. However, smoothing may be a problem where ripple requirements are severe. The push-pull type has the most complex base drive circuit but it produces the lowest output ripple with given values of L_O and C_O.

Figure 7 is a general guide for the choice of converter type, based on output voltage and power. In the case of the flyback converter, it becomes more and more difficult to keep the percentage output ripple below an acceptable level as the output power increases and the output voltage decreases; for reasons of circuit economy, however, the flyback converter is the best proposition if the output power does not exceed about 10W. For output powers higher than about 1kW, the push-pull converter is preferable.

THE CONTROL AND PROTECTION MODULE

In addition to providing adequate output voltage stabilization against line voltage

VARIOUS D.C.-TO-D.C. CONVERTER
TYPES WITH THEIR RECTIFIER SUPPLY



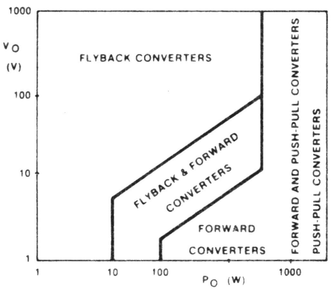
1A
1B
IIIC
11A
IIB
IIIA
IIIB
Q1
Q2
Q3
Q4
D1
D2
D3
D4
D5
Cp
Co
Lo
C1
V1
Vo
+
-
~

NOTES
1 = Flyback converter family with 1A single-transistor type and 1B two-transistor type
2 = Forward converter family with 2A single-transistor type and 2B two-transistor type
3 = Push-pull converter family with 3A conventional type, 3B single-ended type and 3C bridge type

Capacitor C_p is a high-frequency by-pass (20kHz to 50kHz switching frequency).

Figure 6

CONVERTER TYPE



NOTE
Converter choice as a function of SMPS output voltage V_O and output power P_O

Figure 7

SMPS CONTROL-LOOP

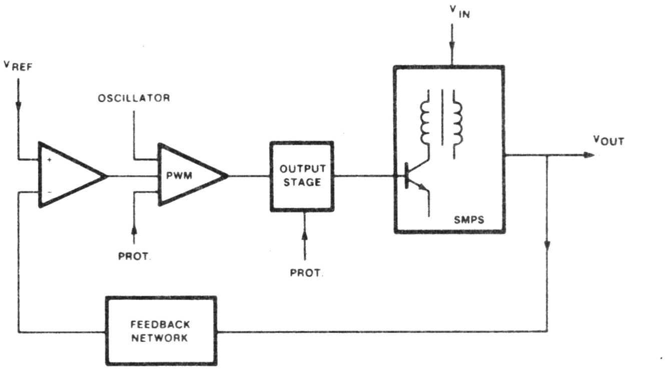


Figure 8

and load changes, the control module must give fast protection against overload, equipment malfunction, and the effects of switch-on immediately following switch-off. In addition the following features are desirable:

- Soft Start: that is, a gradual increase of the transistor duty cycle after switch-on causing a slow rise of the output voltage, which prevents an excessive inrush current due to a capacitive load or charging of the output capacitor.
- Synchronization: to prevent interference due to the difference in free-running frequencies (for example, in a system in which a low-power SMPS supplies the base drive circuit of the output switching transistor in a high-power SMPS).
- Remote switch-on and switch-off: essential for sequential switching of supply units in, for instance, a computer supply system.

The control and protection circuitry of a switched-mode power supply (SMPS) is a crucial and complicated part of the whole supply. Integration of this circuitry on a chip will therefore ease the design of an SMPS considerably.

SMPS CONTROL-LOOP

Figure 8 shows the principal control-loop of a regulated SMPS. The output voltage V_O is sensed and via a feedback network fed to the input of an error amplifier where it is compared with a reference voltage.

The output of this amplifier is connected to an input of the pulse-width modulator PWM.

The other input of this modulator is used for an oscillator signal, which can be a sawtooth or a triangle.

As a result, a rectangular waveform with the frequency of the oscillator is emerging at the output of the PWM.

The width of this pulse is dictated by the output voltage of the error amplifier. After passing through an output stage, the pulse can be used to drive the power transistor of the SMPS.

When the width of the pulse is varied, also the on-time of this transistor will vary and consequently the amount of energy taken from the input voltage V_I.

So, by controlling the duty cycle δ of the power transistor, one can stabilize the output of the SMPS against line and load variations. The duty cycle δ is defined as t_{ON}/T for the power transistor. Protections for overvoltage, overcurrent, etc. can be realized with additional inputs on the PWM or the output stage.

INTIAL TURN ON

It may be helpful to operate an SMPS open loop with reduced error amplifier gain. This provides an easy way to verify correct operation of control loop elements.

Dual Output ± 50V, 1 Amp, Forward Converter for Off-line Operation

A straightforward 100 watt off-line converter, with transformer isolation to load, is shown in Figure 1.

The NE5560 is operated at a switching frequency of 75kHz allowing minimum magnetics and component size. Line regulation is greatly improved also by making use of pin 16, the feed forward input. Typical transformer design recommended is: T_1: Primary 60T #24, Secondary 20T #26 on a Ferroxcube #2616 (3C8) pot core wound tightly coupled for minimum leakage inductance and having adequate primary inductance for low droop in the base drive waveform. Base drive to Q2 should approach 0.5A peak for fast turn-on response and minimum losses.

T2 provides 2.4 = 1 stepdown from primary to each secondary. A primary winding of 60 turns of #26 wire wound between the two secondaries with 25 turns each of #20 wire. The recommended core is a Ferroxcube-type 3622 pot core with a 25 mil gap to prevent saturation.

± 50V FEED FORWARD SWITCH MODE CONVERTER

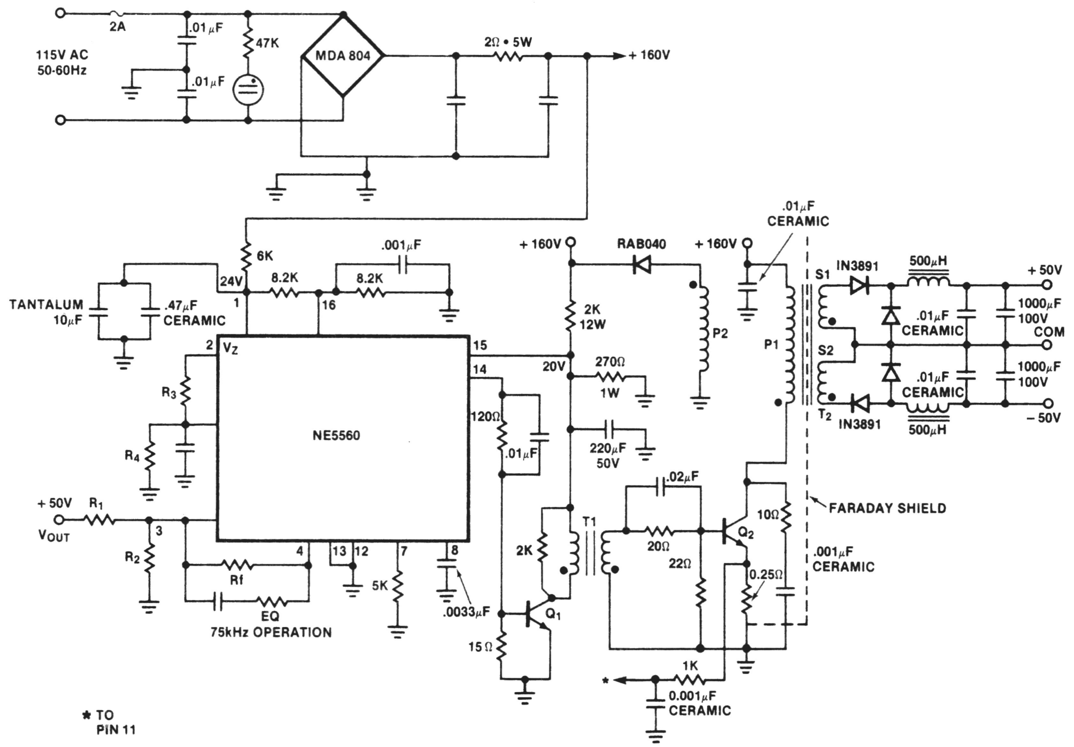

115V AC
50-60Hz
2A
.01μF
.01μF
47K
MDA 804
2Ω • 5W
+ 160V
6K
24V
.001μF
8.2K
8.2K
16
1
TANTALUM 10μF
.47μF CERAMIC
2
VZ
R3
R4
+ 50V
R1
VOUT
3
R2
Rf
EQ
75kHz OPERATION
4
13
12
7
8
5K
.0033μF
NE5560
15
14
120Ω
.01μF
15Ω
Q1
2K
+ 160V
2K 12W
20V
270Ω 1W
220μF 50V
RAB040
P2
+ 160V
.01μF CERAMIC
P1
T1
.02μF
20Ω
22Ω
Q2
10Ω
0.25Ω
1K
0.001μF CERAMIC
FARADAY SHIELD
.001μF CERAMIC
S1
S2
T2
IN3891
IN3891
500μH
500μH
.01μF CERAMIC
.01μF CERAMIC
1000μF 100V
1000μF 100V
+ 50V
COM
− 50V
* TO PIN 11

Figure 1

NE5560 PUSH-PULL REGULATOR APPLICATOR

APPLICATIONS

SE/NE5560 Push-Pull Regulator

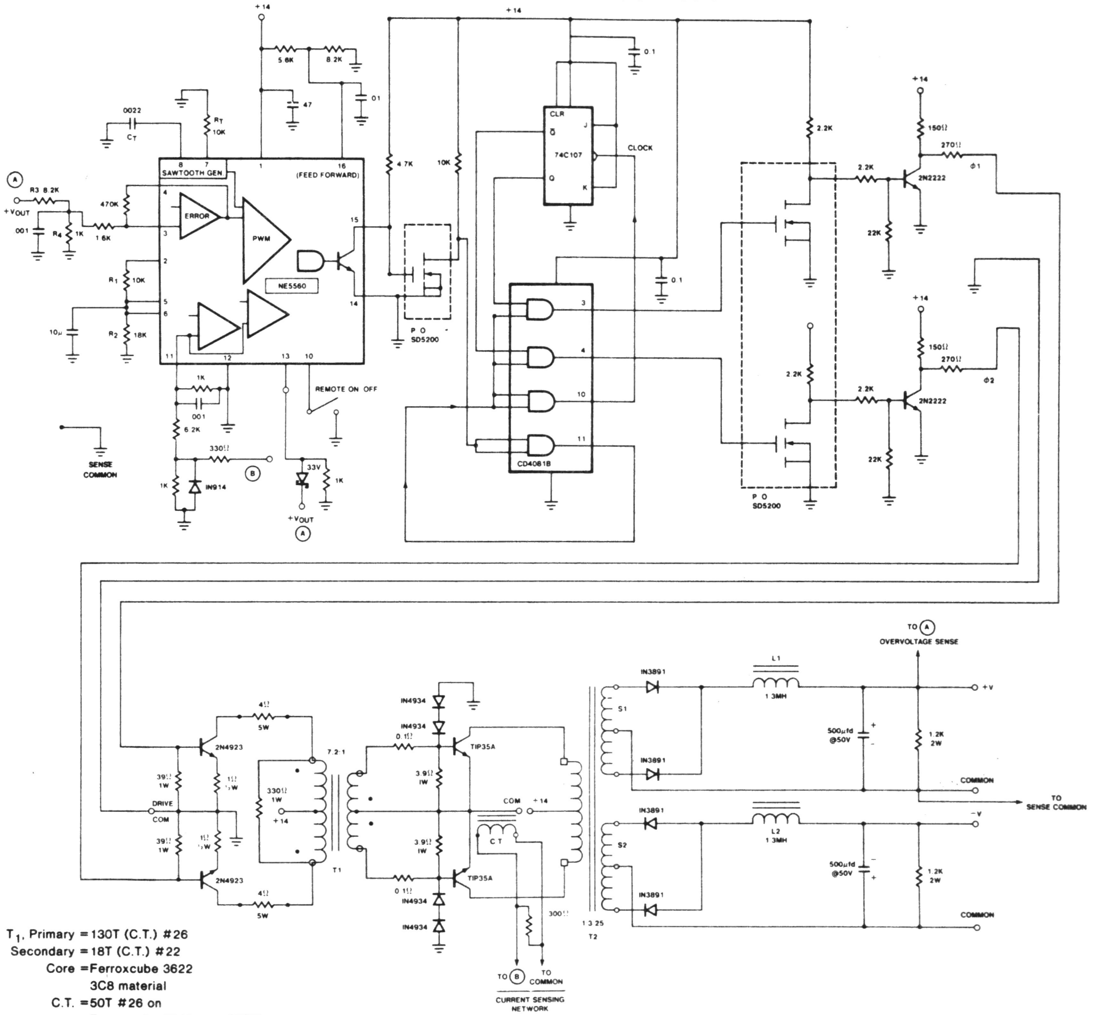
This application describes the use of the Signetics SE/NE5560 adapted to function as a push-pull switched mode regulator, as shown in Figures 1 and 2.

Input voltage range is +12 to +18V for a nominal output of +30 and −30V at a maximum load current of 1A with an average efficiency of 81%.

Features include feed forward input compensation, cycle-to-cycle drive current protection and other voltage sensing, line (to positive output) regulation <1% for an input range of +13 to +18V and load regulation to positive output of <3% for $\Delta I_L(+)$ of 0.1 to 1 Amp.

The main pulse width modulator operates to 48 kHz with power switching at 24 kHz.

SE/NE5560 PUSH-PULL SWITCH MODE REGULATED SUPPLY WITH CMOS DRIVE CONVERSION LOGIC



+14
5.6K
8.2K
.01
.47
.0022
C_T
R_T 10K
SAWTOOTH GEN
(FEED FORWARD)
ERROR
PWM
NE5560
R3 8.2K
+VOUT
470K
.001
R_4 1K
1.6K
R_1 10K
R_2 18K
10µ
1K
.001
6.2K
330Ω
IN914
REMOTE ON OFF
33V
SENSE COMMON
4.7K
10K
P O SD5200
CLR
74C107
CLOCK
CD4081B
0.1
2.2K
22K
2N2222
150Ω
270Ω
ϕ1
ϕ2
TO Ⓐ OVERVOLTAGE SENSE
IN3891
L1 1.3MH
L2 1.3MH
500µfd @50V
1.2K 2W
+V
−V
COMMON
TO SENSE COMMON
S1
S2
1:3.25
T2
IN4934
0.1Ω
3.9Ω 1W
TIP35A
COM
C T
300Ω
TO Ⓑ
TO COMMON
CURRENT SENSING NETWORK
2N4923
4Ω 5W
39Ω 1W
1Ω ½W
330Ω 1W
DRIVE
COM
7.2:1
T1

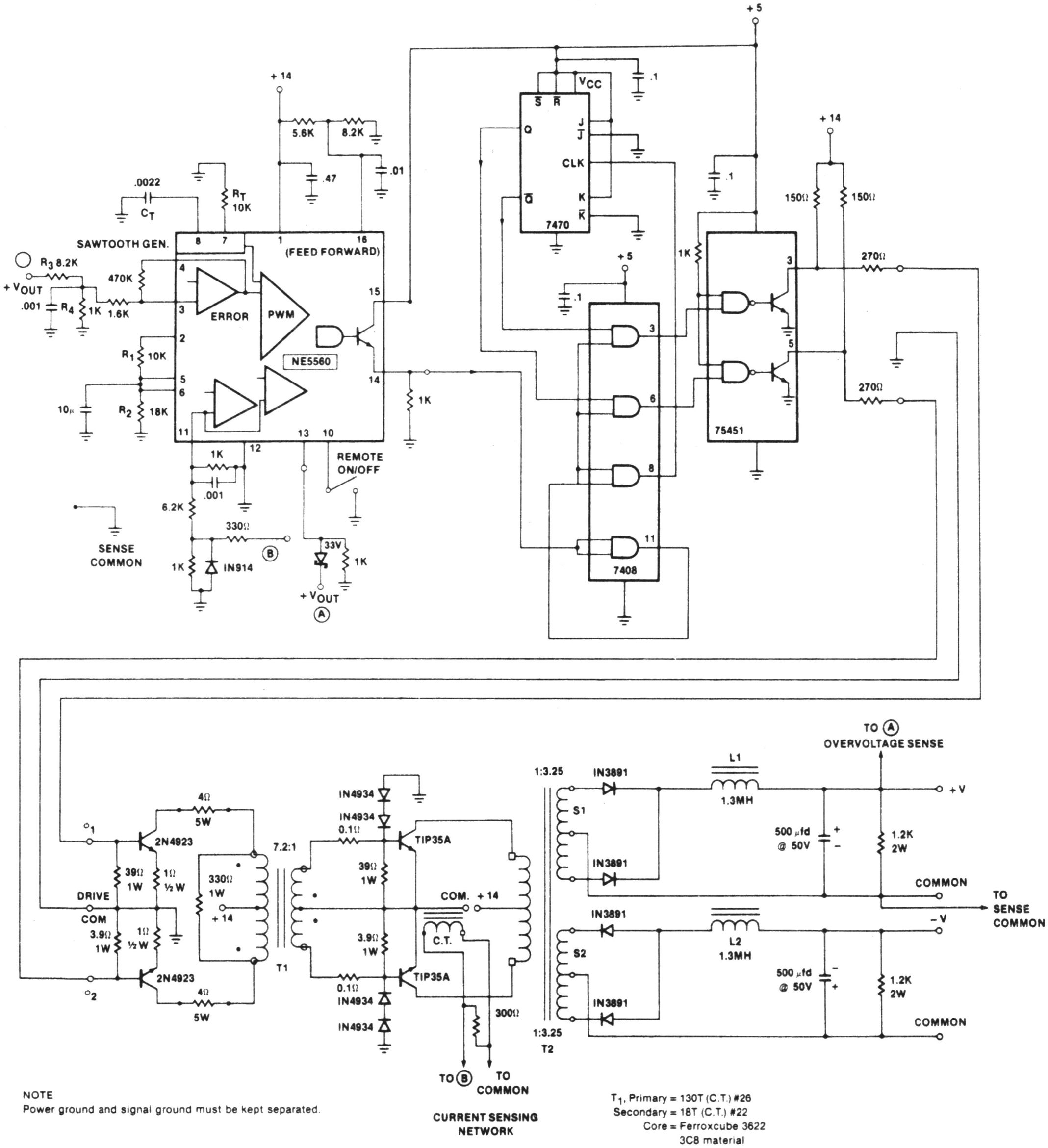
T_1, Primary = 130T (C.T.) #26
Secondary = 18T (C.T.) #22
Core = Ferroxcube 3622
3C8 material
C.T. = 50T #26 on
Ferroxcube 2616 core (3C8)
F2D bobbin
T_2, Primary = 16T (C.T.) #18 Secondaries (each) 52T (C.T.) #22,
Core = Ferroxcube 4229 3C8 material
L_1, L_2 120T #20 on single gapped EC35 Ferroxcube core. 3C8 material

NOTE
Power ground and signal ground must be kept separated.

Figure 1

NE5560 PUSH-PULL REGULATOR APPLICATOR

SE/NE5560 PUSH-PULL SWITCH MODE REGULATED SUPPLY WITH TTL DRIVE CONVERSION LOGIC


+5
+14
5.6K
8.2K
.47
.01
.0022
C_T
R_T 10K
SAWTOOTH GEN.
8
7
1
16
(FEED FORWARD)
R_3 8.2K
+V_{OUT}
.001
R_4 1K
470K
1.6K
4
3
2
ERROR
PWM
NE5560
15
14
R_1 10K
5
6
10µ
R_2 18K
11
13
10
12
1K
.001
REMOTE ON/OFF
6.2K
330Ω
Ⓑ
1K
IN914
33V
+V_{OUT}
Ⓐ
SENSE COMMON
V_{CC}
S̄
R̄
Q
Q̄
J
J̄
CLK
K
K̄
7470
.1
7408
3
6
8
11
75451
5
150Ω
270Ω
2N4923
4Ω 5W
39Ω 1W
1Ω ½W
3.9Ω 1W
330Ω 1W
DRIVE
COM
+14
7.2:1
T1
IN4934
0.1Ω
TIP35A
COM. +14
C.T.
300Ω
TO Ⓑ
TO COMMON
CURRENT SENSING NETWORK
1:3.25
S1
S2
T2
IN3891
L1
L2
1.3MH
500 µfd @ 50V
1.2K 2W
TO Ⓐ OVERVOLTAGE SENSE
+V
−V
COMMON
TO SENSE COMMON

NOTE
Power ground and signal ground must be kept separated.

T_1, Primary = 130T (C.T.) #26
Secondary = 18T (C.T.) #22
Core = Ferroxcube 3622
3C8 material
C.T. = 50T #26 on
Ferroxcube 2616 core (3C8)
F2D bobbin
T_2, Primary = 16T (CT.) #18 Secondaries (each) 52T (C.T.) #22.
Core = Ferroxcube 4229 3C8 material
L_1, L_2 = 120T #20 on single gapped EC35 Ferroxcube core, 3C8 material.

Figure 2

APPLICATIONS

5V, 0.5A Buck Regulator Operates from 15V

The converter design shows how simple it is to derive a TTL supply from a system supply of 15V (see Figure 1). The NE5561 drives a 2N4920 PNP transistor directly to provide switching current to the inductor. Overall line regulation is excellent and covers a range of 12V to 18V with minimal change (<10mV) in the output operating at full load.

As with all NE5561 circuits, the auxiliary slow start and δ_{max} circuit is required, as evidenced by Q1. The δ_{max} limit may be calculated by using the relationship.

$$\frac{R2}{R1 + R2}(8.2V) = V\delta_{(max)}$$

The maximum duty cycle is then determined from the pulse-width modulator transfer graph, and R1, R2 are defined from the desired conditions.

NE5561 Boost Converter with Output Variable (18V to 30V, 0.2A)

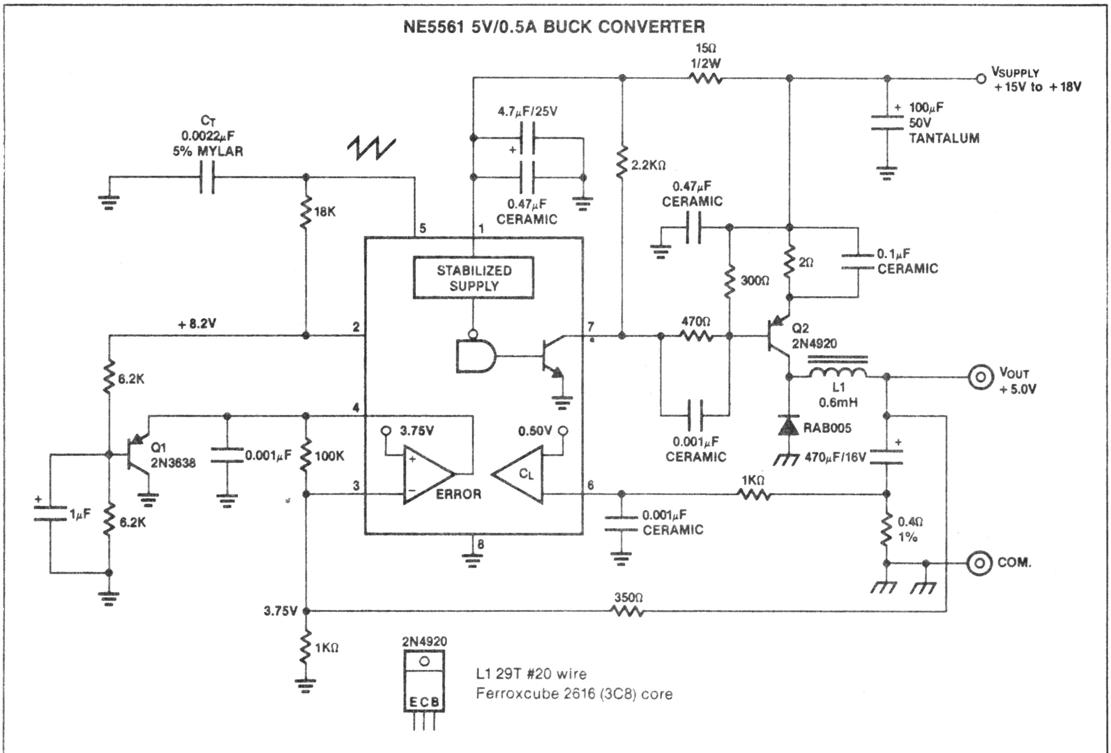
The circuit shown uses the NE5561 SMPS controller in a non-isolated boost converter operating from a 15V line. The addition of three transistors and one diode is necessary to complete the design (see Figure 3).

Operation is as follows. Q1 is a combination slow start and max duty cycle limit transistor. When power is first applied to the circuit, C7 in a discharged state begins to charge toward the divider voltage, V_δ. This $V_\delta + V_{BE}$ controls the voltage on pin 4, the error amp output, causing the duty cycle to be limited initially to δ_0, then to gradually approach its normal operating range, δ. The base divider is fed from V_Z, which is nominally 8.2V.

Output regulation starts at the error amplifier, with gain set by R2 (adj) and R5 combination. The error amp is stable for closed loop gain in excess of 40 dB (X100), for which the regulation will be approximately 1%. C4 is added to the output to insure stability at gain below 40 dB. C4 creates a dominant pole at approximately 1 kHz, descending at 6 dB per octave to unity near 1 MHz. Input to the error amplifier is referenced to 3.75V and must reach this reference level for the output of the NE5561 to be active. Output voltage is then the quantity 3.75V times the divider ratio from V_{OUT} to Pin 3 as set by R2.

If the ratio is, for instance, 10:1, the output will be ≃ 37V. If the ratio is 5:1, the output will be ≃ 18.5V, etc.

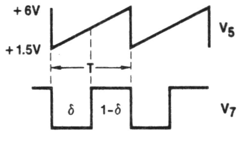
Output to Q2 base is a square wave of variable duty cycle as determined by load demand. The internal transistor is open collector and must have a pull-up resistance, in this application the base circuit of Q2. The duty cycle δ is a fraction between 0 and 1. The actual on-time is proportional then to $\delta \bullet T$, where T is the period of the free-running frequency of the sawtooth generator internal the NE5561. Frequency


NE5561 5V/0.5A BUCK CONVERTER
15Ω
1/2W
VSUPPLY
+15V to +18V
4.7μF/25V
+
100μF
50V
TANTALUM
CT
0.0022μF
5% MYLAR
2.2KΩ
0.47μF
CERAMIC
18K
0.47μF
CERAMIC
5
1
STABILIZED
SUPPLY
300Ω
2Ω
0.1μF
CERAMIC
+8.2V
2
7
470Ω
Q2
2N4920
6.2K
L1
0.6mH
VOUT
+5.0V
4
3.75V
0.50V
RAB005
Q1
2N3638
0.001μF
100K
0.001μF
CERAMIC
470μF/16V
+
ERROR
CL
1KΩ
3
6
1μF
6.2K
0.001μF
CERAMIC
0.4Ω
1%
8
COM.
3.75V
350Ω
1KΩ
2N4920
ECB

L1 29T #20 wire
Ferroxcube 2616 (3C8) core

Figure 1

is set by the RC combination, R7 • C5 with charging current supplied from V_Z (8.2V). The stabilizing effect of the internal zener supply gives a constant frequency. The sawtooth waveform is related to duty cycle as shown below.


+6V
+1.5V
V_5
T
δ
1-δ
V_7

(V_7 NOT TO SCALE)

Q3 is switched on during the saturated portion of the output waveform from pin 7 of the NE5561, termed δ, and is switched off during the remainder of the cycle (1-δ).

The sawtooth frequency is set at approximately 22 kHz in this example. The NE5561 is capable of operation to 100 kHz, however.

Pin 6 of the NE5561 operates an over-current protective feature which resets the output on pin 7 if the instantaneous pin 6 voltage exceeds 0.50V. In this case, R8 determines the peak current of Q3 emitter circuit prior to shutdown. The operation of the over-current circuit is on a pulse to pulse basis, returning to normal as soon as

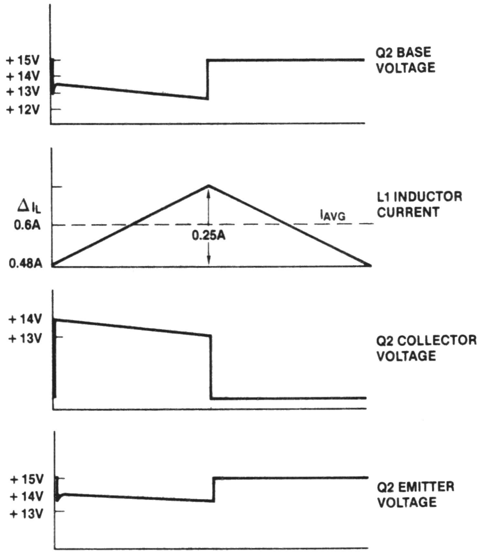
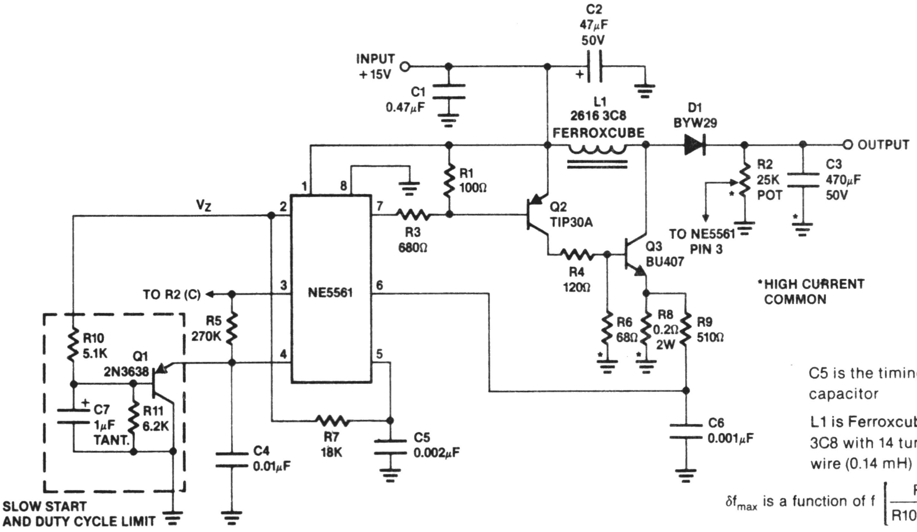


Figure 2

DC TO DC SMPS USING NE5561 VARIABLE 18V TO 30V OUT AT 0.2A


C2
47µF
50V
INPUT
+15V
C1
0.47µF
L1
2616 3C8
FERROXCUBE
D1
BYW29
OUTPUT
R2
25K
POT
C3
470µF
50V
R1
100Ω
Q2
TIP30A
TO NE5561 PIN 3
Q3
BU407
*HIGH CURRENT COMMON
V_Z
1
8
2
7
R3
680Ω
R4
120Ω
TO R2 (C)
3
NE5561
6
4
5
R5
270K
R10
5.1K
Q1
2N3638
C7
1µF
TANT.
R11
6.2K
C4
0.01µF
R7
18K
C5
0.002µF
R6
68Ω
R8
0.2Ω
2W
R9
510Ω
C6
0.001µF
SLOW START AND DUTY CYCLE LIMIT

C5 is the timing capacitor

L1 is Ferroxcube 2616 3C8 with 14 turns of #18 enameled wire (0.14 mH)

δf_{max} is a function of f $\left[\frac{R11}{R10 + R11}\ (V_Z) + V_{BE}\right]$

Figure 3

the pin 6 voltage falls below 0.50V. As is noted, a small degree of filtering is needed to eliminate short switching transient, allowing only the primary current waveform to be sensed.

Switching circuit operation proceeds as follows. Q3 turns on, causing magnetization current to begin increasing in L1, the switching inductor. After initial start up, C3 is charged to the output, thus with Q3 on, Diode D1 is reverse biased and does not conduct during the duty cycle, δ. C3, the output capacitor, sustains the full load current during this part of the cycle. When Q3 turns off, the magnetic field energy previously stored in L1 is discharged through D1 now forward biased. The output capacitor is incrementally charged, restoring its depleted voltage. The ripple voltage is a function of the size of C3 and its internal resistance. For minimum ripple, a low ESR (Equivalent Series Resistance) capacitor must be used, since previously mentioned peak load current flows in C3.

Single Transistor 100V, 250 mA Buck Converter

With a single 15V zener diode to limit package dissipation, the NE5561 controller may be operated directly from the rectified AC line. The following example shows the simplicity of such a converter which is capable of a nominal 100V output (see Figure 5). A base drive transformer is used to gain high voltage isolation between the NE5561 and the switching transistor, and to provide adequate base drive. A low power PNP transistor is used in an auxilliary slow start and duty cycle limiting circuit to prevent over-excitation (Q1).

Operation is as follows. Drive from the NE5561 output is fed to the primary of T1, base drive transformer, with a pulse-width modulated signal causing Q2 (BU407) to switch current to inductor, L1. As the current builds up, energy is stored in L1, coincident with the saturation period (δ) of the NE5561 output stage. During this period, current also flows through L1 to C_O and the load. When Q2 cuts off, the choke field collapses and D1 conducts as the load is sustained by the inductor-stored energy.

V_{OUT} is sampled by the divider R7 and R8, rising until the junction of the divider is forced to 3.75V. Load variations are thus translated to duty cycle variations to maintain constant voltage at the output. The measured efficiency at 0.5A load is in ex-

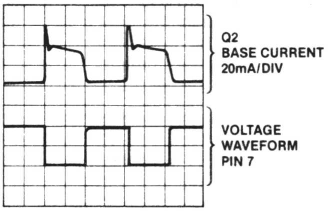


Figure 4

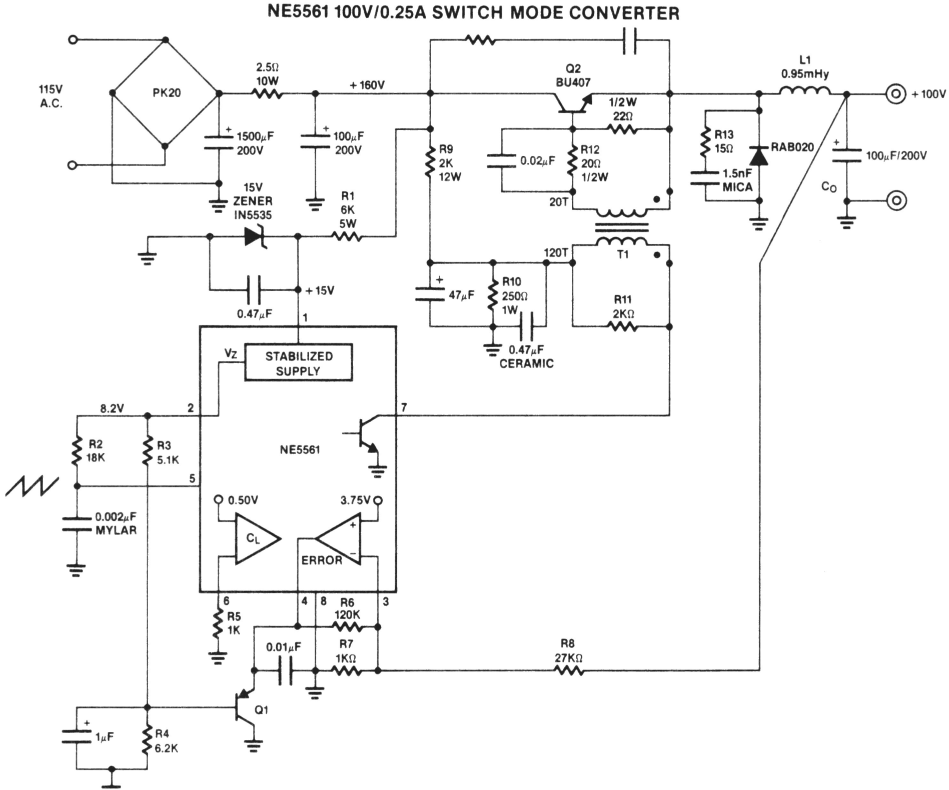

NE5561 100V/0.25A SWITCH MODE CONVERTER
115V
A.C.
PK20
2.5Ω
10W
+160V
1500μF
200V
100μF
200V
15V
ZENER
IN5535
R1
6K
5W
0.47μF
+15V
1
R9
2K
12W
0.02μF
Q2
BU407
1/2W
22Ω
R12
20Ω
1/2W
20T
120T
T1
47μF
R10
250Ω
1W
0.47μF
CERAMIC
R11
2KΩ
L1
0.95mHy
+100V
R13
15Ω
1.5nF
MICA
RAB020
100μF/200V
C_O
Vz
STABILIZED
SUPPLY
8.2V
2
7
R2
18K
R3
5.1K
NE5561
5
0.002μF
MYLAR
0.50V
3.75V
C_L
ERROR
6
4
8
3
R5
1K
R6
120K
0.01μF
R7
1KΩ
R8
27KΩ
Q1
1μF
R4
6.2K

Figure 5

cess of 72%. Line regulation is good from approximately 93V to 120V.

The base current waveform driving Q2 is shown in Figure 4. This indicates that the BU407 base current rises initially to 60 mA to obtain fast turn-on, then settles to about 40 mA for the remainder of the duty cycle, δ. Reverse biasing of the emitter-base junction occurs to enhance turn-off.

Snubber networks are necessary, as shown across Q2 and commutation diode, D1, to prevent component failure during fast switching. It is critical that these networks be placed physically adjacent to the respective components they protect, and that low inductance capacitors and resistors be used as snubbers (ceramic or dura mica caps and carbon resistors).

The base drive transformer is constructed using a Ferroxcube 2616-3C8 core, with primary of 120 turns of #26 wire, and 20 turns of #26 on secondary. The primary is wound in a simple solenoidal manner, first on the bobbin, followed by a layer of mylar tape to provide voltage isolation. Next, the secondary winding is added. Primary inductance measures 45 mH with a leakage inductance of 120 μH. It is important to have sufficient primary inductance to prevent excessive droop in base drive current. Also, leakage reactance must be kept reasonably low to minimize ringing.

DC Motor Drive with Fixed Speed Control

The circuit shown in Figure 7 incorporates a simple switch mode approach to DC motor control, which is efficient and free of the dissipation problems inherent in linear drives. The NE5561 provides pulse proportional drive and speed control based on DC tachometer feedback. A simple switching circuit consisting of one transistor (2N4920 PNP) and a commutation diode is used to deliver programmed pulse energy to the motor.

A frequency of approximately 20 kHz is used to eliminate audio noise present in some switching drives. The DC tach in this example delivers 2.7V/1000 RPM. Its output is such that negative feedback occurs when this voltage is applied to the error amplifier of the NE5561, pin 3, through a suitable divider. Note that the voltage to pin 3 must be 3.75V in order to obtain servo lock. Thus, the divider from the tach output must be appropriate to maintain the proper ratio for speed control to occur.

As shown in the waveform photo (Figure 6), duty cycle varies directly with load torque demand. No load current is ≈ 0.3A and full load is 0.6A. Current and voltage waveforms at 0.6A are shown in Figure 6. If desired, torque limiting may be set by feeding a derivative of motor return current back to pin 6 of the NE5561.

Operating range is 12V to 18V input for a tach output nominal variation of less than 20 mV, and approximately 4.35V for the divider values shown. The motor is a Globe 100A 565 rated at 12V DC.

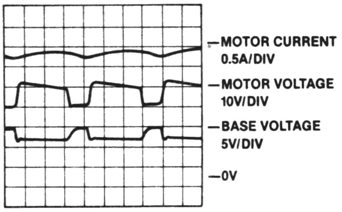


Figure 6

NE5561 PULSE-WIDTH MODULATED MOTOR DRIVE (CONSTANT SPEED)

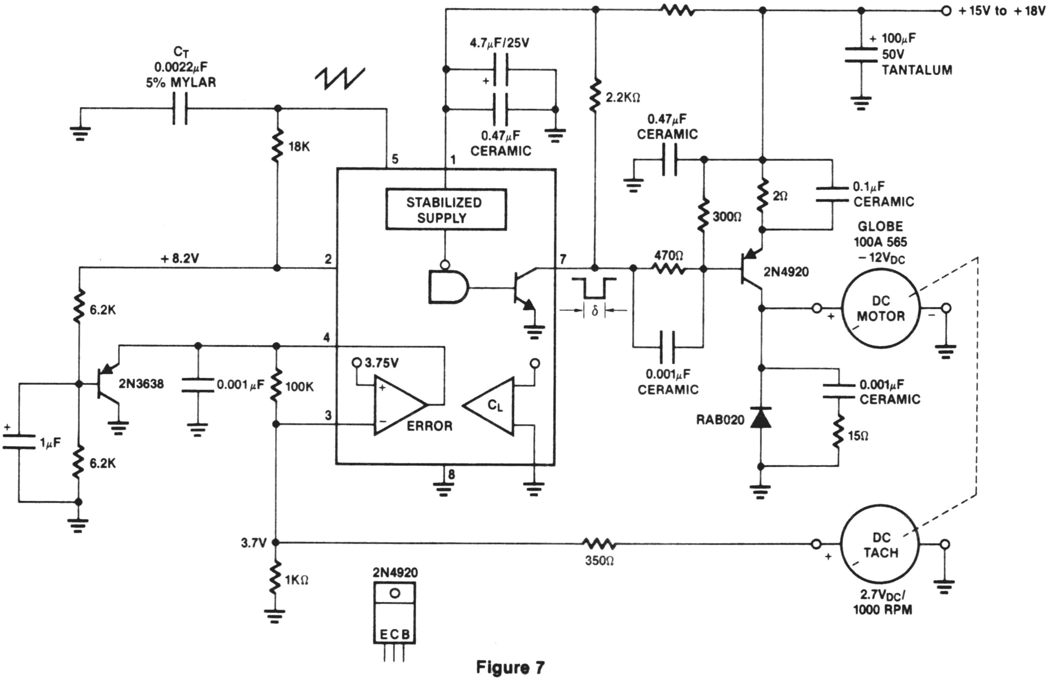
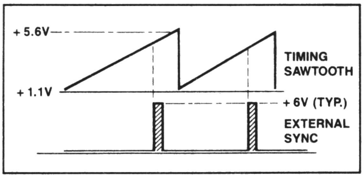

+15V to +18V
CT 0.0022μF 5% MYLAR
4.7μF/25V
+
0.47μF CERAMIC
2.2KΩ
+ 100μF 50V TANTALUM
0.47μF CERAMIC
18K
5
1
STABILIZED SUPPLY
0.1μF CERAMIC
2Ω
300Ω
GLOBE 100A 565 −12VDC
+8.2V
2
7
470Ω
2N4920
δ
DC MOTOR
+
−
6.2K
4
0.001μF CERAMIC
3.75V
2N3638
0.001μF
100K
CL
0.001μF CERAMIC
3
ERROR
RAB020
15Ω
1μF
6.2K
8
3.7V
350Ω
DC TACH
2.7VDC/ 1000 RPM
1KΩ
2N4920
ECB

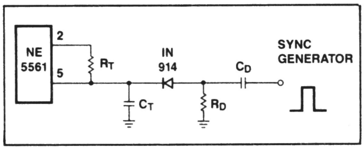
Figure 7

EXTERNAL SYNCHRONIZATION FOR THE NE5561 AN124

Synchronization of the 5561 can be accomplished by forcing the timing pin (Pin 5) above the 5.6 volt sawtooth limit comparator for a short time.



This can be accomplished with a simple diode-coupled narrow pulse source with fairly low source impedance:



A drawback to this approach is that when the 5.6 volt threshold is reached, a discharge transistor is turned on to quickly pull the timing capacitor to ground and will also attempt to pull the pulse generator to ground. This condition can be avoided by keeping the pulse width very narrow (0.1μs) or by placing a differentiator network between the pulse generator and the diode.

The differentiator will now produce a positive going spike with the positive edge of the sync pulse, resetting the sawtooth without passing too much current through the discharge transistor. The negative spike produced by the falling edge of the clock will be blocked by the diode and will have no effect on the sawtooth ramp. A narrow sync pulse is no longer necessary while a sharp *edged* pulse is. The value of C_D should be sufficient to ensure that a 10V pulse will drive the capacitor, C_T, high enough to trip the 5.6V comparator according to:

$$C_T \, \Delta V_{CT} = C_D \, (\Delta V_{CT} - V_D)$$

This relates the magnitude of the spike to the size of the pulse. Also assume $R_D C_D < 1\mu s$.

The free run frequency of the slaved 5561 should be slightly lower than the sync frequency for proper operation.

APPLICATIONS USING THE SG3524

APPLICATIONS

The capacitor-diode output circuit is used in Figure 1 as a polarity converter to generate a −5 volt supply from +15 volts. This circuit is useful for an output current of up to 20mA with no additional boost transistors required. Since the output transistors are current limited, no additional protection is necessary. Also, the lack of an inductor allows the circuit to be stabilized with only the output capacitor.

Another low-current supply is the flyback converter used in Figure 2 to generate ±15 volts at 20mA from a +5 volt regulated line. The reference generator in the SG3524 is unused with the input voltage providing the reference. Current limiting in a flyback converter is difficult and is accomplished here by sensing current in the primary line and resetting a soft-start circuit.

In the conventional single-ended regulator circuit shown in Figure 3, the two outputs of the SG3524 are connected in parallel for effective .0-90% duty-cycle modulation. The use of an output inductor requires an R-C phase compensation network for loop stability.

Push-pull outputs are used in this transformer-coupled DC-DC regulating converter shown in Figure 4. Note that the oscillator must be set at twice the desired output frequency as the SG3524's internal flip-flop divides the frequency by 2 as it switches the P.W.M. signal from one output to the other. Current limiting is done here in the primary so that the pulse width will be reduced should transformer saturation occur.

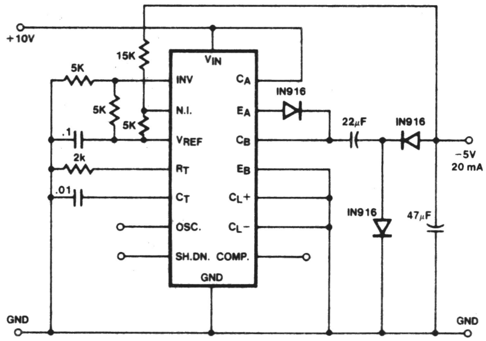

+10V
15K
5K
5K
5K
.1
2k
.01
VIN
INV
N.I.
VREF
RT
CT
OSC.
SH.DN.
COMP.
GND
CA
EA
CB
EB
CL+
CL−
IN916
22μF
IN916
−5V
20 mA
IN916
47μF
GND
GND

Figure 1

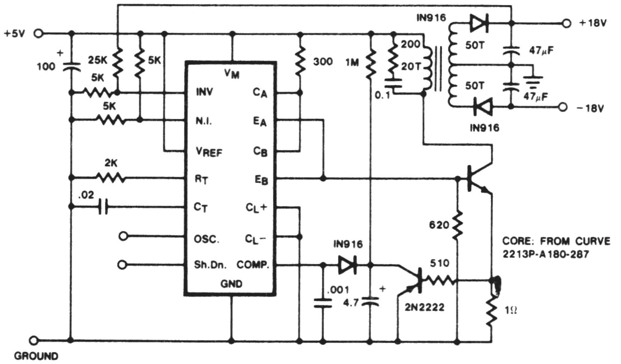

+5V
100
25K
5K
5K
5K
2K
.02
VM
INV
N.I.
VREF
RT
CT
OSC.
Sh.Dn.
COMP.
GND
CA
EA
CB
EB
CL+
CL−
300
1M
200
20T
0.1
IN916
50T
47μF
50T
47μF
+18V
−18V
IN916
620
CORE: FROM CURVE
2213P-A180-287
IN916
510
.001
4.7
2N2222
1Ω
GROUND

Figure 2

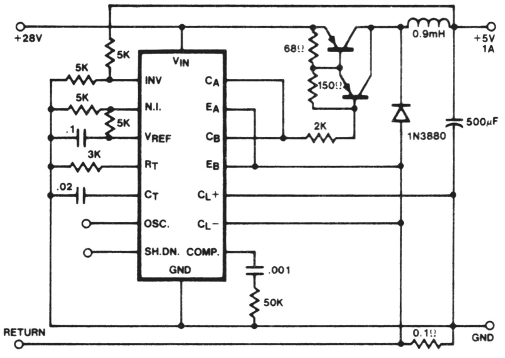

+28V
5K
5K
5K
5K
.1
3K
.02
VIN
INV
N.I.
VREF
RT
CT
OSC.
SH.DN.
COMP.
GND
CA
EA
CB
EB
CL+
CL−
68Ω
150Ω
2K
0.9mH
+5V
1A
1N3880
500μF
.001
50K
RETURN
0.1Ω
GND

Figure 3

SG3524 PUSH-PULL ±50V, 100 Watt Converter

A simple solution to off-line converter design for power audio amplifier circuits is shown in Figure 5. The SG3524 emitter outputs are used to drive directly a pair of VN3500A Power FETs in the primary side of the step down transformer at a 50kHz rate. (The main oscillator operates at 100kHz.) The transformer consists of 120T of #24 wire centertapped at 60T. This is sandwiched between two 50 turn center-tapped secondary windings of #20 wire. Diodes are fast recovery BYW30s; the output chokes, 500μH wound on EC35 (3C8) pair Ferroxcube cores, provide adequate filtering in conjunction with the 1000μF and .01μF ceramic capacitors across the output.

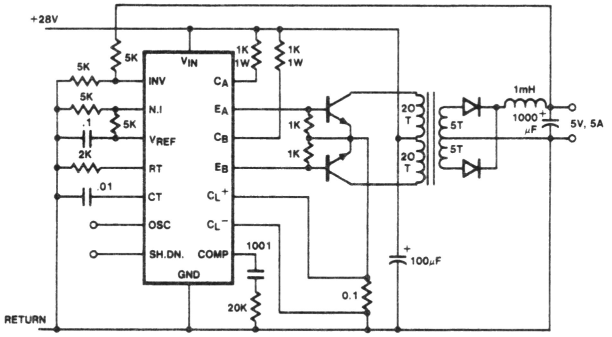

+28V
5K
5K
5K
.1
5K
2K
.01
VIN
INV
N.I
VREF
RT
CT
OSC
SH.DN.
GND
CA
EA
CB
EB
CL+
CL−
COMP
1K 1W
1K 1W
1K
1K
1001
20K
0.1
20 T
20 T
5T
5T
1mH
1000 μF
5V, 5A
100μF
RETURN

Figure 4

± 50 VOLT PUSH-PULL SWITCHED MODE CONVERTER

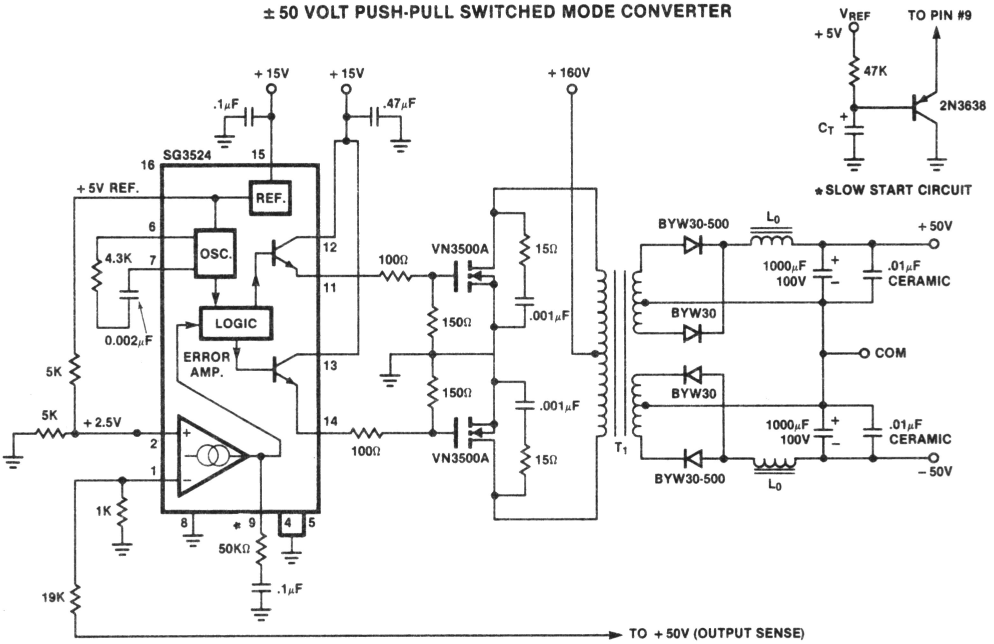

+15V
+15V
+160V
.1μF
.47μF
SG3524
16
15
+5V REF.
REF.
6
7
4.3K
OSC.
0.002μF
LOGIC
ERROR AMP.
12
11
13
14
2
1
8
* 9
4
5
50KΩ
.1μF
5K
5K
+2.5V
1K
19K
100Ω
100Ω
VN3500A
VN3500A
15Ω
15Ω
.001μF
.001μF
150Ω
150Ω
T1
BYW30-500
BYW30
BYW30
BYW30-500
L0
L0
1000μF 100V
1000μF 100V
.01μF CERAMIC
.01μF CERAMIC
+50V
COM
−50V
TO +50V (OUTPUT SENSE)
VREF
+5V
TO PIN #9
47K
CT
2N3638
* SLOW START CIRCUIT

Figure 5

APPLICATIONS

The encoder inputs have been designed to accept a wide variety of signal sources. This can range from simple systems using as an input the wiper of a control pot which is connected between V_R and ground to complex systems incorporating mixing, exponential processing and/or control polarity reversing. In all cases, it must be remembered that the control inputs to the encoder look like voltage followers, that is they draw only very small currents (>200nA). The voltage range for these inputs is +1.5V to +5V; however, internal clamps limit the linear control to approximately +1.5V to +3.5V. These clamps prevent interaction between channels if one input is open circuited or shorted to supply or ground.

An example was worked out previously which utilized mechanical fine trim of the inputs (where the control pot body is rotated a small amount). In some applications, it is desirable to implement this fine trim electrically with the use of an additional pot. Many methods exist to achieve this and two are shown below.

In Figure 1 the series resistors R_T and R_C are much larger than the control pots so as to minimize nonlinearity errors and the ratio of R_T to R_C control the relative sensitivity of the control and trim pots. This scheme allows the control pot to be centered at neutral so polarity reversing can be achieved by reversing V_R and ground on the pots.

The second approach, shown in Figure 2, is a simpler method for achieving electrical trim.

$$T_n = 4R_iC_{mux}\left(\frac{R_T + X_nR_C}{R_T + R_C} - Y\right)$$

$$CR = 4R_iC_{mux}\left(\frac{1}{1 + R_T/R_C}\right)$$

Interfacing the 5044 encoder to the modulator of an RF transistor can be done in several ways depending on the desired output power, freqency stability and oscillator leakage. The simplest method is to use the 5044 output to directly modulate the bias current of a crystal controlled oscillator. Figure 3 shows an example of such a connection.

In a high performance system, separate oscillator, modulator and RF output stages may be required. An example of such a circuit is shown in Figure 4. In some systems, it may be required to provide additional filtering between the encoder output (Pin 11) and the RF modulator to comply with FCC regulations.

In the previous section, a design example was given for a fixed frame encoder (T_F constant). In some applications, it may be desirable to make the frame time variable, allowing the synchronization pulse, which follows the last channel, to remain constant. The variable frame mode simplifies the synchronization pulse detector in the receiver since the pulse does not vary with the control inputs. However, the variable frame time may complicate

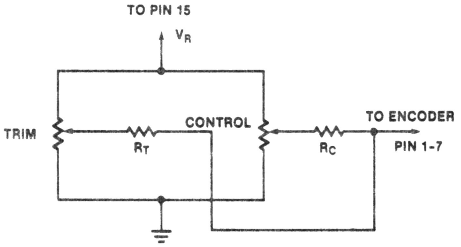


Figure 1

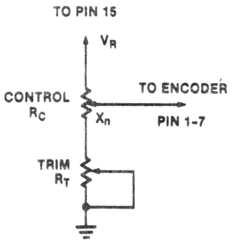


Figure 2

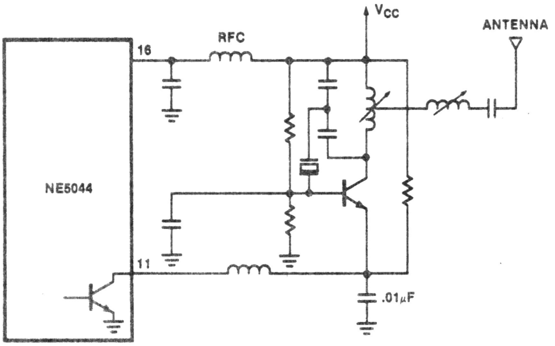


Figure 3. Modulated Oscillator Output Stage R.F. Transmitter

APPLICATIONS USING THE NE5044 ENCODER AN131

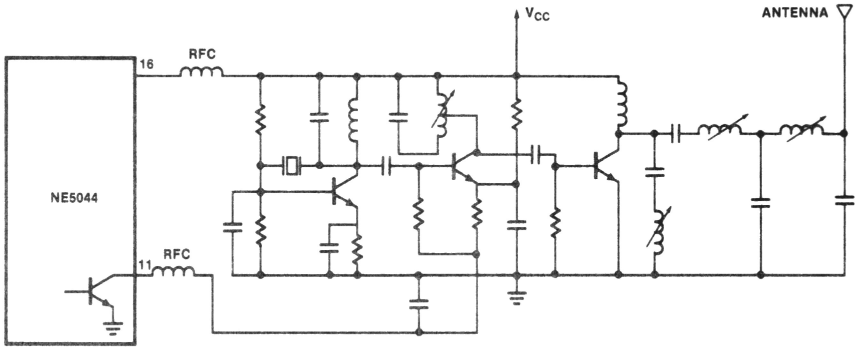


Figure 4. 5044 With High Performance RF Transmitter

the design of the pulse stretchers in the servos. The 5044 can be operated as a variable frame encoder by discharging the capacitor C_F each time the output goes high. After the last output pulse C_F is allowed to charge fully and the frame generator resets the encoder to channel 1. In this mode, the frame generator operates as a monostable multivibrator. Figure 5 shows the external connection. The sync pulse width (time between the falling edge of the last output pulse and the rising edge of the first pulse) is given by

$$T_S = .85\ R_FC_F + R_IC_{mux}.$$

So if a sync pulse of 6ms is desired and $C_F = .1\mu F$, then

$$R_F = \frac{.85 \times 6\text{ms} - .047\mu F \cdot 27k\Omega}{.1\mu F} \cong 39k$$

Some applications may require an RF bypass on each of the multiplexer inputs, depending on PC board layout and the wiring between the control pots and the board. If such is the case, a $.001\mu F$ capacitor is sufficient. Pin 12 may also require a bypass capacitor of $0.1\mu F$.

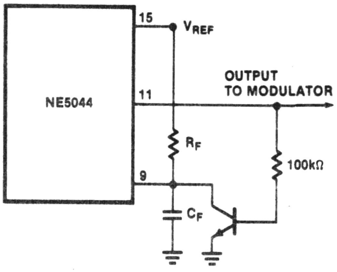


Figure 5. 5044 Variable Frame Encoder

DECODER APPLICATIONS

In most applications, the decoder input will be derived from the decoder of a radio receiver and will have the following characteristics:

1. Contain thermal noise at low levels
2. Will vary in level depending on R/F signal strength and may contain flutter

The thermal noise can be filtered with a simple RC circuit. This filter should have a cut-off frequency of about 3kHz which is approximately the bandwidth of the receiver IF amplifier. A lower cut-off frequency would limit the information rate and resolution of the system. Figure 1 shows the external connections for the decoder input amplifier in which the above-mentioned conditions are handled. Diodes D1 and D2 charge the 1μF coupling capacitor to the peak input voltage minus the fixed voltage at pin 12 and the diode drops. D2 also clamps the input signal reaching A1. The .2μF capacitor forms a filter which allows the amplitude of the input to vary over a wide range and at high rates (as a result of RF flutter in the receiver) without false triggering the decoder. When flutter occurs the baseline of the positive input pulses varies as shown in Figure 2. The .2μF charges up to the average baseline voltage but the 10k resistor does not allow it to be charged by the information pulses. Thus, so long as the pulse peaks exceed the baseline voltage by greater than the drop across diode D_2, the system will be unaffected by baseline flutter no matter what its rate is.

Positive feedback has also been incorporated in the connection of Figure 1 to provide 100mV of hysteresis on the threshold. When the input (pin 13) is low, the current generator is off and pin 11 is near ground. However, when pin 13 goes positive, the current generator turns on and approximately 150μA is sourced. This raises pin 11 by 150μA × 4.7kΩ = 0.7V. The threshold is now given by

$$V_{\text{threshold (on)}} = V_{12} - V_{13}$$

$$\simeq (V_{12} - V_{11}) \left(\frac{1}{1 + R_4/R_3}\right)$$

$$\simeq (3 - 0.7) \left(\frac{1}{1 + 330\text{k}/51\text{k}}\right)$$

$$= 0.3\text{V}$$

So the threshold has been reduced by 100mV or the amplifier will not turn off until the input drops below 0.3V. A low pass filter is also used in the circuit of Figure 1. The 5.6kΩ and .01μF form a 2.8kHz low pass filter to improve the noise rejection characteristics of the detector.

A particular application of the NE5045 may not require all the components shown in Figure 1, however this circuit demonstrates all the features of the decoder which may be utilized.

Figure 3 shows a decoder connected for negative input pulses without hysteresis or flutter rejection. In this case, V_{13} is set to 3V and V_{12} is set to 3V + $V_{\text{threshold}}$. If $V_{\text{threshold}} = 0.4\text{V}$

$$R_4 = \frac{V_R - V_{12}}{V_{\text{threshold}}/51\text{k}} = \frac{4.1 - 3.4}{0.4/51\text{k}}$$

$$= 89\text{k}\Omega \simeq 91\text{k}\Omega.$$

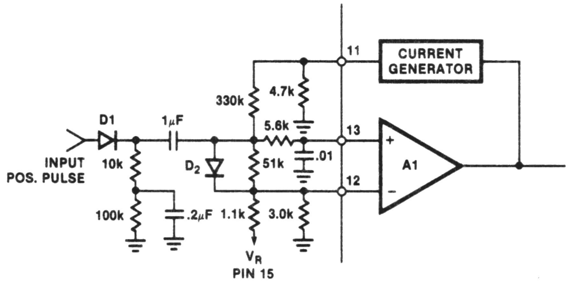


Figure 1. NE5045 Decoder Input Circuit With Flutter and Noise Filtering

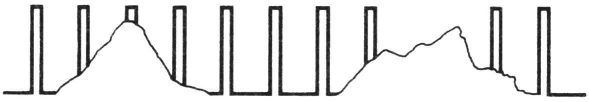


Figure 2. Input Signal With Fast Flutter

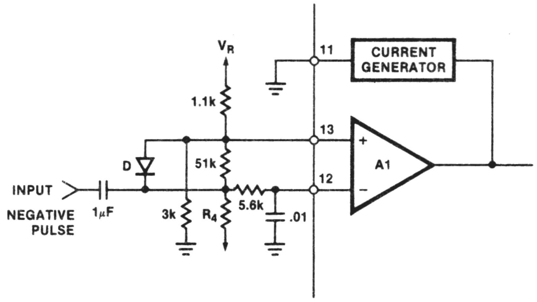

V_R
1.1k
11
CURRENT GENERATOR
13
+
A1
–
12
D
51k
INPUT
NEGATIVE PULSE
1μF
3k
R_4
5.6k
.01

Figure 3. NE5045 Decoder With Neg. Pulse Input

APPLICATIONS USING THE NE544 SERVO AMPLIFIER

APPLICATIONS

DESCRIPTION

The NE544 is a new servo amplifier design for digital proportional RC systems which incorporates the latest state-of-the-art in integrated circuit technology. The basic systems concept was developed in close cooperation with a number of leading manufacturers of radio control equipment.

The design philosophy behind the NE544 was to provide the RC servo systems designer with maximum flexibility in adapting the amplifier performance characteristic to his particular servo system and at the same time to keep the external components count low. To achieve this goal, all the basic servo amplifier functions, such as motor drive, deadband and minimum output pulse, are integrated into the IC, but can be modified over a wide range by using external transistors or padding resistors respectively. This makes it possible to use the IC for extremely low cost applications as well as for the most sophisticated RC servo systems. Additional features of the circuit are very low standby power drain (typically less than 6mA), an internal voltage regulator for improved power supply rejection and a highly accurate monostable multivibrator. This circuit may be used in 2 different charging modes: linear and exponential. In the linear charging mode, the internally generated charging current is programmable over a wide range with a resistor to ground. Usable currents range from below 10μA to above 1mA. In the exponential charging mode, the internal current source is simply bypassed with an external resistor from pin 1 to the regulator output.

The bidirectional power output stage can supply load currents up to 500mA (NE544N package only). Output drive pins for external PNP transistor provide the user with the option of increasing the motor drive by bypassing the internal compound PNP transistors.

The NE544 also provides external pins to adjust deadband and to vary the hysteresis of the Schmitt trigger. This gives the user maximum flexibility in adapting the servo amplifier to a large variety of servo motor and gear train combinations. A dynamic brake integrated into the output stage serves to suppress inductive noise spikes and helps to improve the dynamic performance.

IC PACKAGE

The NE544N has sufficient power dissipation to handle motors with a minimum of 8Ω impedance with the integrated power transistors.

OPERATION

The basic building blocks of the NE544 servo driver are shown in Figure 1.

A positive input signal applied to the input pin (4) sets the input flip-flop and starts the one shot time period. The directional logic compares the length of the input pulse to that of the internal one shot and stores the result of this comparison in a directional flip-flop. The exact difference in pulse width between input and internal one shot pulse, called the error pulse, is also fed to a pulse stretcher, deadband and trigger circuit. These circuits determine 3 important parameters:

1. *Deadband*—The minimum difference between input pulse and internally generated pulse to turn on the output
2. *Minimum output pulse*—The smallest output pulse that can be generated from the trigger circuit
3. *Pulse stretcher gain*—The relationship between error pulse and output pulse

Proper adjustment of these parameters can be achieved with external resistors and capacitors at pins 6, 7 and 8. The trigger circuit activates the gate for a precise length of time to provide drive to the bridge output circuitry in proportion to the length of the error pulse.

TYPICAL APPLICATION AS A LINEAR SERVO AMPLIFIER

Figure 2 shows a typical connection of the NE544 as a high performance servo amplifier for remote control servo applications using the 14-pin dual in-line package. The input pulse may be dc coupled if a reset is used in the receiver decoder. Output drive to the servo motor is applied through pins 9 and 13 with PNP transistors T_A and T_B optional for high performance applications. The wiper of potentiometer R P is mechanically coupled to the servo control surface providing positional feedback. The internal one shot in this application is operating in the linear charging code.

LINEAR ONE SHOT TIMING

In contrast to most conventional servo drivers which use exponential one shots, the NE544 uses a linear one shot. This makes it possible to design servo systems with very high positional accuracy and linear pulse width to position transfer fuctions. The timing of the linear one shot can best be explained with the help of Figure 3.

The timing cycle starts after the input pulse sets the input flip-flop and releases the reset transistor T_R. This allows current I_C to charge up capacitor C_T in a linear fashion. Current I is programmed by resistor R_T. The op amp serves as a linear voltage to current converter, with the current through R_T and C_T matched identically. The inverting input of the op amp is internally referenced to 1.8 volts so that the current I_R is given by this equation.

Equation 1

$$I_R = \frac{V_I}{R_T} = \frac{1.8V}{R_T}$$

BLOCK DIAGRAM OF NE544 SERVO AMPLIFIER

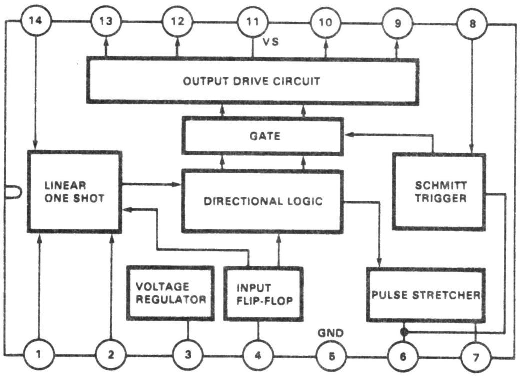


Figure 1

TYPICAL CONNECTION OF NE544AA FOR LINEAR ONE SHOT TIMING

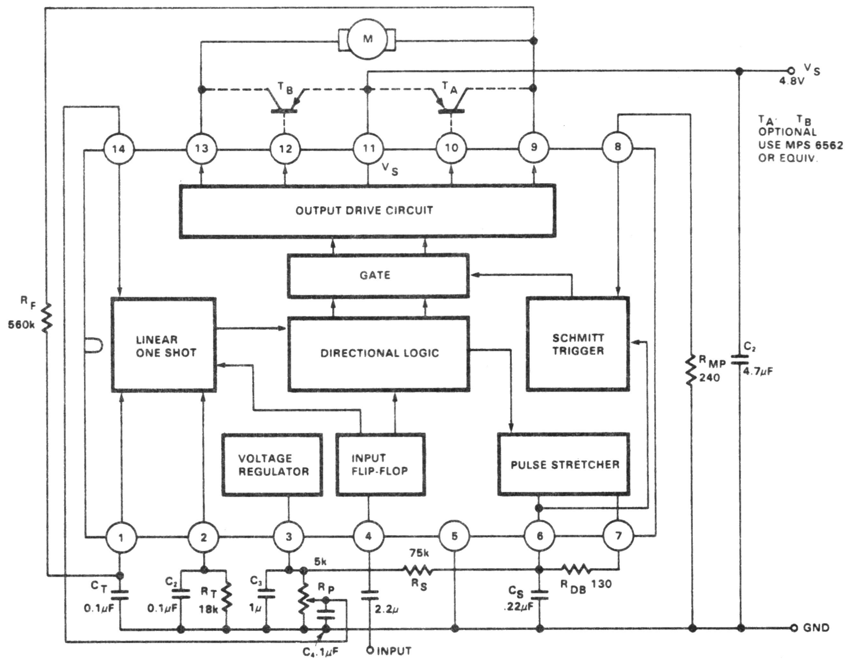

M
T B
T A
V S
4.8V
T A: T B
OPTIONAL
USE MPS 6562
OR EQUIV.
14
13
12
11
10
9
8
V S
OUTPUT DRIVE CIRCUIT
GATE
R F
560k
LINEAR
ONE SHOT
DIRECTIONAL LOGIC
SCHMITT
TRIGGER
R MP
240
C2
4.7µF
VOLTAGE
REGULATOR
INPUT
FLIP-FLOP
PULSE STRETCHER
1
2
3
4
5
6
7
5k
75k
R S
C T
0.1µF
C2
0.1µF
R T
18k
C3
1µ
R P
2.2µ
C S
.22µF
R DB 130
C4 .1µF
INPUT
GND

Figure 2

The timing period of the internal one shot is complete when the voltage ramp at pin 1 reaches the threshold set at pin 14. This time is given by this equation.

Equation 2

$$T = \frac{C_T V_{14}}{I_R}$$

If we substitute the typical values given in Figure 2 we obtain this equation.

Equation 3

$$T = \frac{(0.1 \times 10^{-6}F)\ (1.5V)}{0.1 \times 10^{-3}A} = 1.5 \times 10^{-3}\text{sec}$$

When the internal one shot has timed out, the input flip-flop is reset. The reset transistor T_R is clamped to ground as soon as the input pulse goes to zero. Figure 4 shows the relationship of the input pulse, the internal one shot pulse, the ramp at pin 1 and the error pulse for a condition where the input pulse is longer than the internal pulse.

In contrast to most conventional designs, the total value of the feedback pot R_P is no longer important, since it serves only as a voltage divider. A reasonable lower limit is 1.5kΩ to keep power consumption low and to prevent loading of the voltage regulator. In the typical application a 5K pot is used.

SIMPLIFIED CIRCUIT DIAGRAM OF LINEAR ONE SHOT

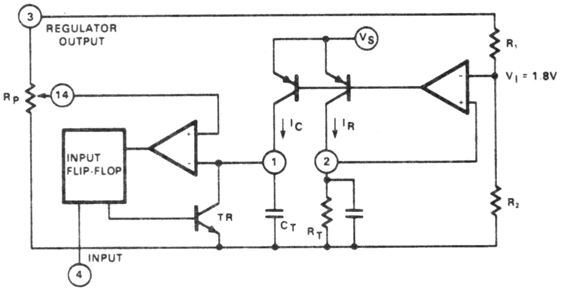
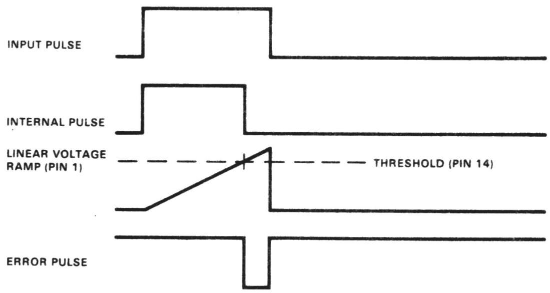

3
REGULATOR
OUTPUT
V S
R1
V1 = 1.8V
R P
14
I C
I R
INPUT
FLIP-FLOP
1
2
TR
C T
R T
R2
INPUT
4

Figure 3



TIMING DIAGRAM

Figure 4

ADJUSTMENT OF SERVO TRAVEL

The amount of angular rotation of the feedback pot R_P (or of the servo control surface) can be changed by simply changing the charging current. Figure 5 shows a plot of the servo travel as a function of input pulse width for 3 different values of current setting resistors R_T.

It should be noted that the center position of the wiper (1.5ms) will also shift when the amount of travel is changed. This shift may be compensated by mechanical wiper adjustment or by the addition of padding resistors as described in the next paragraph.

SERVO TRAVEL AS A FUNCTION OF INPUT PULSE FOR 3 DIFFERENT CHARGING CURRENTS

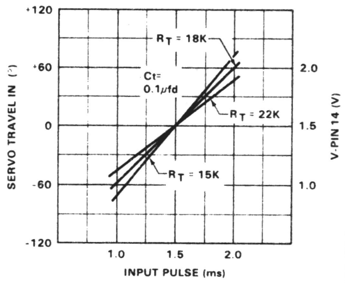


Figure 5

INCREASING SERVO TRAVEL TO MORE THAN 180°

Servo travel may be increased up to the maximum active area of the feedback pot by using padding resistors R_A and R_B as shown in Figure 6.

Figure 7 shows the values of resistors which are required to obtain a desired amount of servo travel.

INCREASED SERVO TRAVEL SCHEMATIC

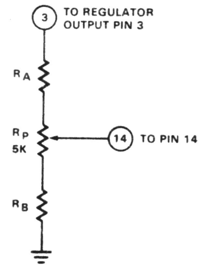


Figure 6

POT TRAVEL vs R_B

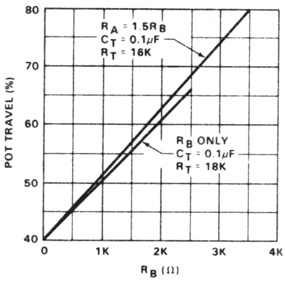


Figure 7

EXPONENTIAL TIMING OPTION

If an exponential timing characteristic is desired, the circuit shown in Figure 8 may be used.

The time constant of the one shot in this case is given by this equation.

Equation 4

$$T_E = R_{TE} C_T \ln \frac{V_3}{V_3 - V_{14}}$$

Substituting the values shown in Figure 8 where V_3 = 2.5V and V_{14} = 1.5V at the center position we obtain this equation.

Equation 5

$$T = (16k\Omega)\ (0.1\mu F)\ \ln \frac{2.5V}{2.5V - 1.5V} = 1.47ms$$

The center position and servo travel can be changed as described in the previous section for linear operation.

PULSE STRETCHER

The pulse stretcher and associated circuitry shown in Figure 9 determine important servo-parameters such as minimum output pulse, deadband and error pulse to output pulse conversion gain.

Initially transistor Q_S is off and capacitor C_S is charged to the regulator voltage. An error pulse from gate G turns on transistor Q_S and discharges capacitor C_S to ground through the parallel combination of R_{DB} and R_I. The deadband is determined by the time it takes for the voltage at pin 6 to reach the trigger threshold (V_1) as shown in Figure 10.

As soon as the Schmitt trigger threshold is reached, transistor Q_S is turned off and the capacitor is discharged through a constant current source I_S until the error pulse disappears.

After the error pulse disappears, capacitor C_S is charged up through resistor R_S. The output remains turned on until the upper threshold (V_2) of the Schmitt trigger is reached. The minimum output pulse is determined by the hysteresis in the Schmitt trigger. This hysteresis may be varied over a wide range by connecting an external resistor R_{MP} from pin 8 to ground or positive supply.

TYPICAL CONNECTION FOR EXPONENTIAL TIMING CHARACTERISTIC

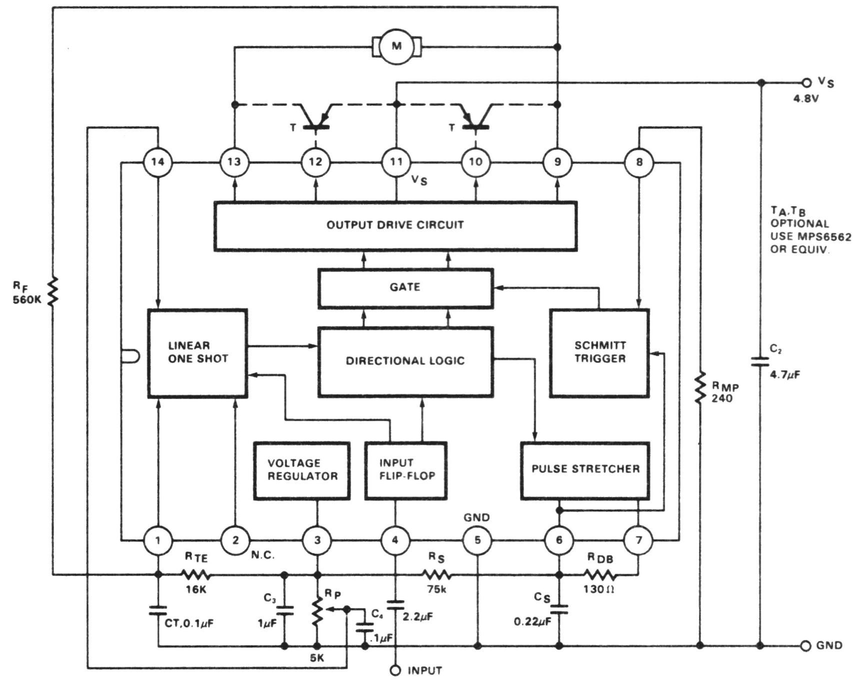

M
T
T
VS
4.8V
14
13
12
11
VS
10
9
8
OUTPUT DRIVE CIRCUIT
TA,TB
OPTIONAL
USE MPS6562
OR EQUIV.
GATE
RF
560K
LINEAR
ONE SHOT
DIRECTIONAL LOGIC
SCHMITT
TRIGGER
C2
4.7μF
RMP
240
VOLTAGE
REGULATOR
INPUT
FLIP-FLOP
PULSE STRETCHER
GND
1
2
3
4
5
6
7
N.C.
RTE
16K
RS
75k
RDB
130Ω
C3
1μF
RP
C4
.1μF
2.2μF
CS
0.22μF
CT,0.1μF
5K
INPUT
GND

Figure 8

TYPICAL CONNECTION OF PULSE STRETCHER CIRCUIT

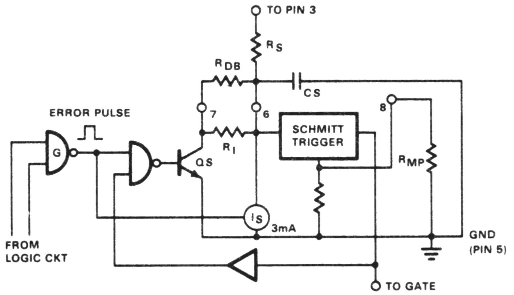

TO PIN 3
RS
RDB
CS
7
6
8
ERROR PULSE
G
R1
SCHMITT
TRIGGER
QS
RMP
IS
3mA
GND
(PIN 5)
FROM
LOGIC CKT
TO GATE

Figure 9

PULSE STRETCHER WAVE FORMS

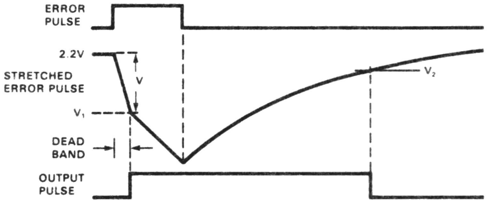


Figure 10

DEADBAND

Referring to Figure 10, the deadband can be calculated using these equations where T_{DB} is deadband in microseconds, C_S is the pulse stretching capacitor, I_T is the total discharge current, and ΔV is approximately .65 volts. The deadband is determined by the time it takes to discharge capacitor C_S from its initial voltage to the Schmitt trigger threshold.

Equations 6

$$T_{DB} \approx \frac{C_S \Delta V}{I_T}, \text{ and } I_T \approx I_S + \frac{2.2V\ (R_I\ \ R_{DB})}{R_I + R_{DB}}$$

The value of the internal deadband resistor R_I is approximately 150 Ω. I_T can be calculated with this equation.

Equation 7

$$I_T = 3mA + \frac{2.2V\ (150\ R_{DB})}{150 + R_{DB}}$$

For the typical values shown in Figure 2 we obtain this equation.

Equation 8

$$I_T = 3 + 27 = 30mA$$

The deadband can then be calculated using Equations 6 to obtain this equation.

Equation 9

$$T_{DB} = \frac{(.22 \times \mu F)\ .65V}{30mA} = 4.8\mu s$$

The total deadband then is twice this value, i.e., $T_{DB\ Total} = \pm T_{DB}$.

Figure 11 shows plots of total deadband versus R_{DB} for 3 different values of pulse stretching capacitor C_S. The value of the minimum pulse resistor R_{MP} is held constant at 240

DEADBAND vs RDB FOR 3 DIFFERENT PULSE STRETCHING CAPACITORS

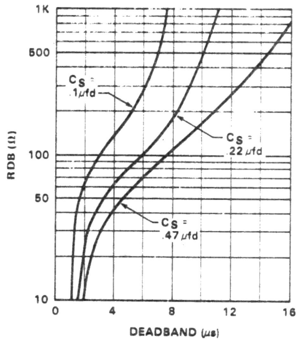


Figure 11

MINIMUM PULSE

The length of the minimum output pulse can be adjusted by changing the hysteresis of the Schmitt trigger. As can be seen from Figure 10, this will also affect the deadband. To aid in the selection of the right value of minimum pulse and deadband resistor, Table 1 may be consulted. This table gives typical values of deadband and minimum pulse for 5 combinations of R_{DB} and R_{MP} with C_S and R_S held constant at 0.22μF and 75k Ω respectively.

If a particular application requires different values, C_S and R_S can be changed accordingly. A capacitor with low series resistance should be used for C_S. If C_S is too resistive, the minimum pulse becomes equal to the error pulse causing the servo to buzz at the rest position.

RMP	RDB	DEAD-BAND (μs)	MINIMUM PULSE (ms)
		±7	5.0
360	130	±5	2.5
240	130	±5	2.0
160	82	±3.5	1.6
100	51	±2.3	2.0

Table 1 VALUES OF DEADBAND AND MINIMUM PULSE FOR CS = 0.22μF AND RS = 75k Ω

PULSE STRETCHER GAIN

For given values of R_{DB} and R_{MP}, the gain of the pulse stretcher can be adjusted with capacitor C_S and resistor R_S. The values chosen in the typical application turn the outputs fully on with an error pulse of approximately 200μs.

The charging resistor R_S can also be connected to the positive supply voltage instead of the voltage regulator output. This usually requires somewhat tighter tolerances on R_S and C_S, but allows operation over a wide range of supply voltage since pulse stretcher gain now varies inversely with supply voltage.

FEEDBACK RESISTORS FOR CLOSED LOOP DAMPING

The amount of feedback required for good closed loop damping depends on the motor and gear train used, the desired pulse stretcher gain and the deadband. In many applications, a single feedback resistor, R_F, from pin 9 to pin 1 is sufficient, since the dynamic brake provides some damping. If the mechanical gain is very high, an additional feedback resistor from pin 13 to pin 14 may be required.

A LOW-COST ANALOG/DIGITAL PROPORTIONAL CONTROL SYSTEM FOR PERSONAL COMPUTER AND ROBOTICS APPLICATIONS

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Signetics Corporation, Sunnyvale, California
Bob Blauschild
Linear Design, Inc., Los Altos, California

1. ABSTRACT

This paper describes an integrated circuit chip set* designed for low-cost transmission of analog and digital data. The system provides remote motion control capability and is designed for personal computer or microprocessor control applications. The control system is based on a multichannel serial bus concept and uses pulse position modulation (PPM) for information transfer. The input and output of the system interfaces directly with a personal computer.

2. OVERVIEW OF CONTROL SYSTEM DATA BUSES

With the rapid expansion of microprocessors and personal computers into virtually all areas of modern life, there is an increasing need for methods of communication between computers and remote devices. Communication is usually accomplished by parallel digital data transfer and digital/analog conversion. This method is used in the case of most stationary computer peripheral devices. For movable peripheral equipment, or when communication has to cover larger distances, various forms of serial data concepts are used. The choice of a particular serial data bus system depends on cost/performance tradeoffs and possible requirements for coding and protocol standardization. In a digital system a serial message unit typically consists of a byte of serial digital data plus additional bits for addressing, synchronization, and other management functions.

In consumer applications, where low cost is an important factor, mixed digital and analog encoding methods can offer significant advantages over other serial encoding methods. The digital proportional system[1,2] described here uses pulse position modulation for serial data transfer. In contrast to the pure digital systems, where one message block (or frame) contains one byte of data, the digital proportional system packs several bytes into one frame. This is possible because the information is encoded in the form of pulse position.

A comparison of various data transfer methods is shown in Table 1. The first three methods are purely digital and are mostly used for commercial serial bus systems and for computer networks. The fourth, a digital proportional method, is a special-purpose serial bus. It offers advantages in consumer applications due to combined analog and digital techniques. The concept also lends itself to either amplitude or frequency modulation for remote control.

Table 1. Comparison of Data Transfer Methods

TYPE	ENCODING	TYPICAL PERFORMANCE ACCURACY	TYPICAL PERFORMANCE SPEED	APPLICATION
Digital Bus	Parallel Data	8/16 bit	1 Mbaud	Computer Peripherals
Asynchronous or Synchronous Bus	Serial Data	8 bit	300-1200 baud	Data Communication Computer Peripherals Robotics Serial Ports (RS-232) Telephone Modems
Computer Network	Serial Data	8/16 bit	1 Mbaud	Computers Communication
Digital Proportional Bus	Serial PPM	8 bit	3500 baud	Consumer Home Control Robotics

3. DESCRIPTION OF THE ANALOG/DIGITAL PROPORTIONAL CONTROL SYSTEM

In a typical application, the system is interfaced to a personal computer through one of its peripheral 3-state I/O ports as shown in Figure 1. The 8-bit digital-to-pulse position encoder and the personal computer form the control center. In addition to the 8 data lines, 3 control lines are used to connect the computer to the pulse position encoder. The encoded information is transmitted via a standard radio control (RF) link. The signal is detected by a receiver in the remote control device or robot. The pulse position information is then decoded and processed with standard proportional circuit techniques[3].

The bus control program occupies 600 bytes of memory. The rest of the computer memory is available to the user for recording and playing back the stored programs. A floppy disk drive is used for permanent storage of information.

PULSE POSITION CODING AND SERVOMOTOR CONTROL

The circuit blocks required to perform the pulse position encoding function are shown in Figure 2. The encoder contains all the active circuits necessary to convert successive 8-bit words of digital information into accurate pulse position modulated signals, for up to 7 channels. Parallel data from the computer I/O bus is latched directly to an 8-bit DAC input. A bidirectional constant current generator alternately charges and discharges the CMUX capacitor.

The resulting voltage waveform is shown in the second trace of Figure 3. Two high-gain comparators compare the multiplex capacitor (CMUX) voltage to the DAC output voltage (VA) and to the range input voltage (Vrange). The counter control logic uses the two comparator output signals to increment the channel count and to reverse the current source polarity. Under computer control, the comparator analog input signal is taken from the DAC output; under manual control, this signal is taken from the multiplex switch analog output. The multiplex switch is controlled by the channel counter, and samples the analog voltages generated by the manual joystick inputs. The encoder output waveforms are shown in Figure 3. The top trace shows the frame pulse, which controls the encoder frame time and can be operated in either variable or fixed frame mode. The lower two traces show the channel pulses and the latch enable pulses, respectively. The latch enable pulse (DE) updates the DAC input data.

Two ICs are used to perform pulse decoding and servocontrol as shown in Figure 4. The serial PPM signal, after RF detection, is decoded into parallel pulses by the decoding IC. Each channel is now a pulse-width modulated signal. This IC contains two monostable multivibrators used for frame synchronization and for increased noise immunity. Each channel pulse is then sent to a servocontrol IC, which demodulates the pulse width information into position, speed, or other control parameters[3]. In this circuit a servoloop is used to compare the input pulse to an internally generated pulse that is proportional to the control parameter. Negative feedback is then used to drive the servomotor output to the desired position.

4. COMPUTER CONTROLLED ROBOTICS APPLICATION

The serial data transmission and proportional control system described in this paper can be used for various applications such as remote motion control, home control, alarm systems, and remote video games. A wide choice of transmission media can be used: hardwire, RF, current carrier, infrared, fiberoptics, and ultrasonic.

To take full advantage of the availability of multichannel analog data transmission, a robotics application was implemented. The system uses 7 channels. Each channel represents a robot control surface as listed below:

A1--Forward/Backward Motion
A2--Steering(Direction Control)
A3--Head Rotation
A4--Shoulder (Arm) Movement
A5--Elbow Movement
A6--Wrist Rotation
A7--Hand (Claw) Open/Closed

---

* Signetics NE5044 and NE5045 Encoder/Decoder, NE544 Servoamplifier, and NE5018 8-bit D/A Converter.

The robot can be exercised either manually or by computer. Individual channels may be recorded and played simultaneously. Reprogramming several channels while maintaining the rest unchanged becomes possible. The robot can be "taught" or its actions can be corrected. The final result may be stored on floppy disk for future playback. In the "Play" mode, the computer sends 8 bits per channel to a PPM encoder. In the "Learn" mode, manual inputs are converted into digital data and processed by the computer. Remote sensing capability can be added to the control system by adding a feedback transmission loop. Sensor feedback data is sent back to the computer and results in a full duplex system. Sensor information can then be processed and used to make decisions for execution by the forward path.

SUMMARY

A 7-channel robotics application was used to demonstrate the versatility of a serial bus concept that uses pulse position modulation. The consumer-oriented system interfaces directly with a personal computer and can be used in many control applications that require good performance at low cost.

ACKNOWLEDGEMENTS

The authors would like to express their appreciation to their colleagues at Signetics. In particular we thank Jock Ochiltree and Ed Ross for their support and encouragement throughout this project, and our former colleague Gary Kelson for his innovative design of the encoding and decoding concepts.

REFERENCES

1. J. Maloney, "Six Channel Digital Proportional System," R/C Modeler Magazine, October 1973.
2. F. M. Marks and W. Winter, "Radio Control for Model Builders," Hayden Book Co. Inc., 1972.
3. Hans H. Stellrecht and Robert W. Hamilton, "A Linear Servoamplifier for Remote Control Applications," IEEE Transactions on Consumer Electronics, February 1977.

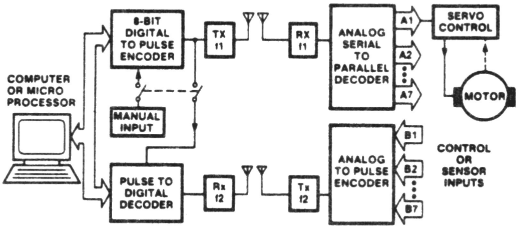

8-BIT DIGITAL TO PULSE ENCODER
TX f1
RX f1
ANALOG SERIAL TO PARALLEL DECODER
A1
A2
A7
SERVO CONTROL
MOTOR
COMPUTER OR MICRO PROCESSOR
MANUAL INPUT
PULSE TO DIGITAL DECODER
Rx f2
Tx f2
ANALOG TO PULSE ENCODER
B1
B2
B7
CONTROL OR SENSOR INPUTS

FIGURE 1. Block Diagram of the Analog/Digital Proportional Control System for Personal Computer Applications

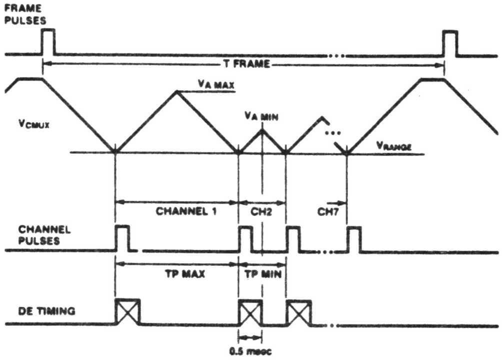

FRAME PULSES
T FRAME
$V_{A\,MAX}$
V_{CMUX}
$V_{A\,MIN}$
V_{RANGE}
CHANNEL 1
CH2
CH7
CHANNEL PULSES
TP MAX
TP MIN
DE TIMING
0.5 msec

FIGURE 3. Systems Timing Diagram

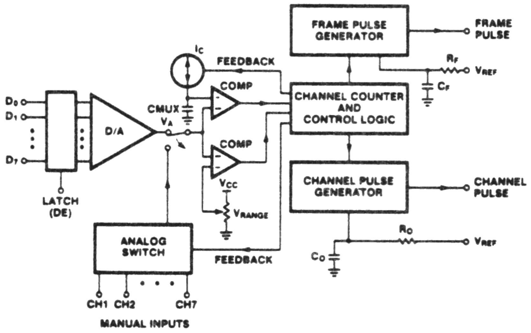

D_0
D_1
D_7
LATCH (DE)
D/A
CMUX
V_A
I_C
FEEDBACK
COMP
COMP
V_{CC}
V_{RANGE}
ANALOG SWITCH
CH1 CH2 CH7
MANUAL INPUTS
FEEDBACK
FRAME PULSE GENERATOR
FRAME PULSE
R_F
V_{REF}
C_F
CHANNEL COUNTER AND CONTROL LOGIC
CHANNEL PULSE GENERATOR
CHANNEL PULSE
R_O
V_{REF}
C_O

FIGURE 2. Block Diagram of the Digital to Pulse Position Encoder

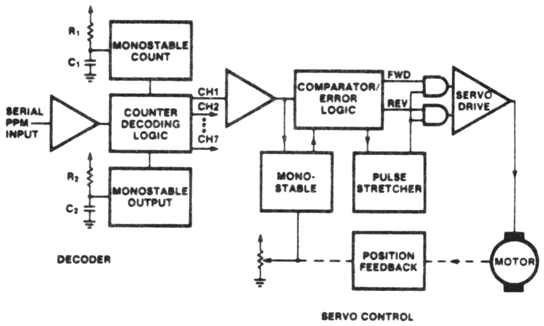

R_1
C_1
MONOSTABLE COUNT
SERIAL PPM INPUT
COUNTER DECODING LOGIC
CH1
CH2
CH7
R_2
C_2
MONOSTABLE OUTPUT
DECODER
COMPARATOR/ ERROR LOGIC
FWD
REV
SERVO DRIVE
MONO-STABLE
PULSE STRETCHER
POSITION FEEDBACK
MOTOR
SERVO CONTROL

FIGURE 4. Block Diagram of the Serial to Parallel Decoder and of the Servocontrol

Section 9
Package Outline
Index

INDEX

SECTION 9 — PACKAGE INFORMATION

Index 9-1
Package Outlines for product with prefixes: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN
D . . . . SO Plastic Dual-In-Line 9-3
E . . . . Metal Headers 9-5
F . . . . Hermetic Cerdip 9-7
H . . . . Metal Headers 9-8
I . . . . Hermetic Side Braze 9-11
N . . . . Plastic Dual-In-Line 9-11

PACKAGE OUTLINES

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, µA, ULN

INTRODUCTION

The following information applies to all packages unless otherwise specified on individual package outline drawings.

General

1. Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).
2. Lead spacing shall be measured within this zone.
   a. Shoulder and lead tip dimensions are to centerline of leads.
3. Tolerances non-cumulative.
4. Thermal resistance values are determined by utilizing the linear temperature dependence of the forward voltage drop across the substrate diode in a digital device to monitor the junction temperature rise during known power application across V_{CC} and ground. The values are based upon 120 mils square die for plastic packages and a 90 mils square die in the smallest available cavity for hermetic packages. All units were solder mounted to P.C. boards, with standard stand-off, for measurement.

PLASTIC ONLY

5. Lead material: Alloy 42 (Nickel/Iron Alloy) Olin 194 (Copper Alloy) or equivalents, solder dipped.
6. Body material: Plastic (Epoxy)
7. Round hole in top corner denotes lead No. 1.
8. Body dimensions do not include molding flash.
9. SO Packages-microminiature packages.
   a. Lead material: Alloy-42.
   b. Body material: Plastic (Epoxy).

HERMETIC ONLY

10. Lead material
    a. ASTM alloy F-15 (KOVAR) or equivalent—gold plated, tin plated, or solder dipped.
    b. ASTM alloy F-30 (Alloy 42) or equivalent—tin plated, gold plated or solder dipped.
    c. ASTM alloy F-15 (KOVAR) or equivalent—gold plated.
11. Body Material
    a. Eyelet, ASTM alloy F-15 or equivalent—gold or tin plated, glass body.
    b. Ceramic with glass seal at leads.
    c. BeO ceramic with glass seal at leads.
    d. Ceramic with ASTM alloy F-30 or equivalent.
12. Lid Material
    a. Nickel or tin plated nickel, weld seal.
    b. Ceramic, glass seal.
    c. ASTM alloy F-15 or equivalent, gold plated, alloy seal.
    d. BeO Ceramic with glass seal.
13. Signetics symbol, angle cut, or lead tab denotes Lead No. 1.
14. Recommended minimum offset before lead bend.
15. Maximum glass climb .010 inches.
16. Maximum glass climb or lid skew is .010 inches.
17. Typical four places.
18. Dimension also applies to seating plane.

PACKAGE OUTLINES

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

PLASTIC PACKAGES

	PACKAGE CODE	Θ_{ja}/Θ_{jc}(°C/W)	DESCRIPTION
Standard Dual-in-Line Packages			
8-Pin	N	99/50	
14-Pin	N	86/48	TO-116/MO-001
16-Pin	N	83/42	MO-001
18-Pin	N	63/29	
20-Pin	N	61/24	
22-Pin	N	51/23	
24-Pin	N	52/23	MO-015
28-Pin	N	52/23	MO-015
Metal Headers			
4-Pin	E	100/20	TO-46 Header
4-Pin	E	150/25	TO-72 Header
8-Pin	H	150/25	TO-5 Header
10-Pin	H	150/25	TO 5/TO-100 Header, Short Can
10-Pin	H	150/25	TO-5/TO-100 Header, Tall Can
Cerdip Family			
8-Pin	FE	110/30	Dual-in-Line Ceramic
14-Pin	F	110/30	Dual-in-Line Ceramic
16-Pin	F	100/30	Dual-in-Line Ceramic
18-Pin	F	93/27	Dual-in-Line Ceramic
20-Pin	F	90/25	Dual-in-Line Ceramic
22-Pin	F	75/27	Dual-in-Line Ceramic
24-Pin	F	60/26	Dual-in-Line Ceramic
28-Pin	F	57/27	Dual-in-Line Ceramic
Laminated Ceramic, Side Brazed Lead			
16-Pin	I	90/25	Dip Laminate

SO Package Thermal Data

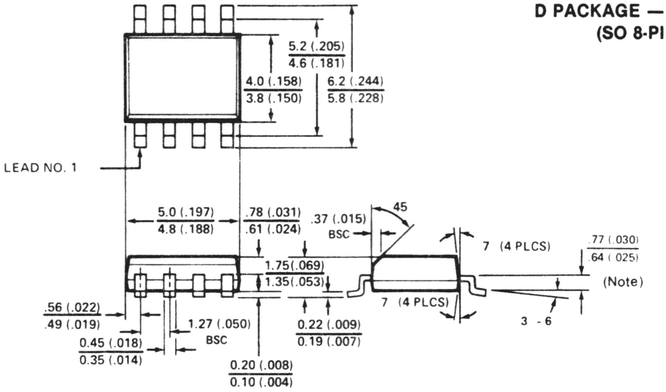
Package Type	Package Mounting Technique*	Max. Allowable Power Diss. (mW) at 25°C	Max. Allowable Power Diss. (mW) at 70°C	Thermal Resistance (θ_{JA}°C/Watt)	
				Average	Maximum
SO-14	PCB	658	421	190	225
	Ceramic	962	615	130	165
	Ceramic w/H.S.	1471	941	85	110
SO-16	PCB	862	551	145	170
	Ceramic	1250	800	100	125
	Ceramic w/H.S.	1923	1231	65	85
SO-16L	PCB	1250	800	100	140
	Ceramic	1743	1143	70	100
	Ceramic w/H.S.	2500	1600	50	65
SO-20	PCB	1471	941	85	115
	Ceramic	2273	1454	55	85
	Ceramic w/H.S.	3572	2286	35	55
SO-24	PCB	1563	1000	80	110
	Ceramic	2000	1600	50	80
	Ceramic w/H.S.	4167	2667	30	50

PCB = Printed circuit board
Ceramic = Ceramic substrate
Ceramic w/H.S. = Ceramic substrate with heat sink and/or thermal compound
*Air gap is 0.006 inches unless thermal compound is used

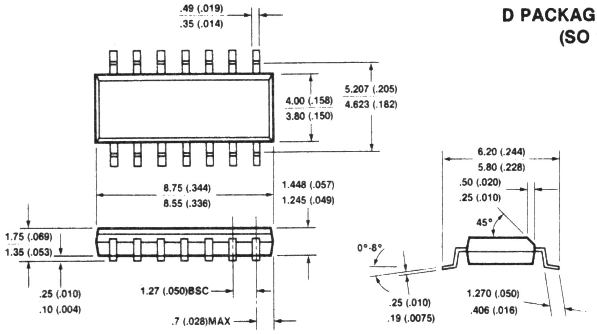
PACKAGE OUTLINES

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

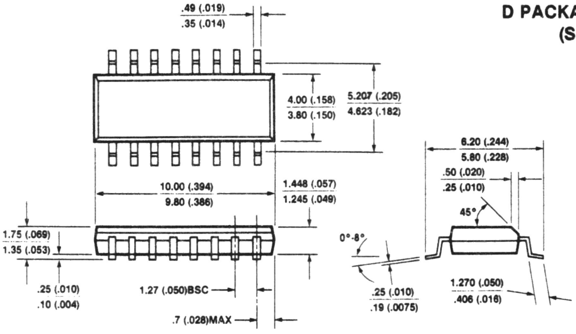
D PACKAGE — PLASTIC (SO 8-PIN)


5.2 (.205)
4.6 (.181)
4.0 (.158)
3.8 (.150)
6.2 (.244)
5.8 (.228)
LEAD NO. 1
5.0 (.197)
4.8 (.188)
.78 (.031)
.61 (.024)
.37 (.015)
BSC
45
7 (4 PLCS)
.77 (.030)
.64 (.025)
(Note)
1.75 (.069)
1.35 (.053)
7 (4 PLCS)
3 - 6
.56 (.022)
.49 (.019)
1.27 (.050)
BSC
0.45 (.018)
0.35 (.014)
0.22 (.009)
0.19 (.007)
0.20 (.008)
0.10 (.004)

D PACKAGE — PLASTIC (SO 14-PIN)


.49 (.019)
.35 (.014)
4.00 (.158)
3.80 (.150)
5.207 (.205)
4.623 (.182)
6.20 (.244)
5.80 (.228)
8.75 (.344)
8.55 (.336)
1.448 (.057)
1.245 (.049)
.50 (.020)
.25 (.010)
45°
1.75 (.069)
1.35 (.053)
0°-8°
.25 (.010)
.10 (.004)
1.27 (.050)BSC
.25 (.010)
.19 (.0075)
1.270 (.050)
.406 (.016)
.7 (.028)MAX

D PACKAGE — PLASTIC (SO 16-PIN)

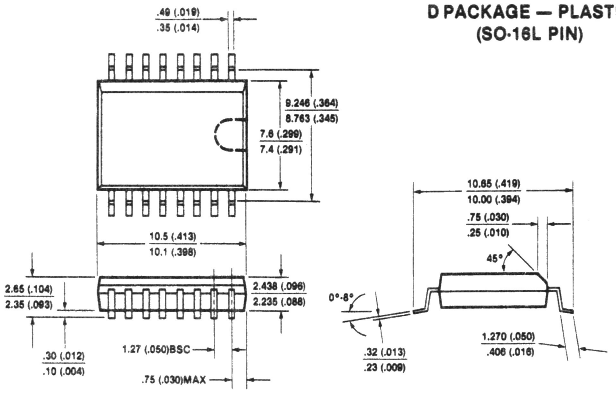

.49 (.019)
.35 (.014)
4.00 (.158)
3.80 (.150)
5.207 (.205)
4.623 (.182)
6.20 (.244)
5.80 (.228)
10.00 (.394)
9.80 (.386)
1.448 (.057)
1.245 (.049)
.50 (.020)
.25 (.010)
45°
1.75 (.069)
1.35 (.053)
0°-8°
.25 (.010)
.10 (.004)
1.27 (.050)BSC
.25 (.010)
.19 (.0075)
1.270 (.050)
.406 (.016)
.7 (.028)MAX

Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

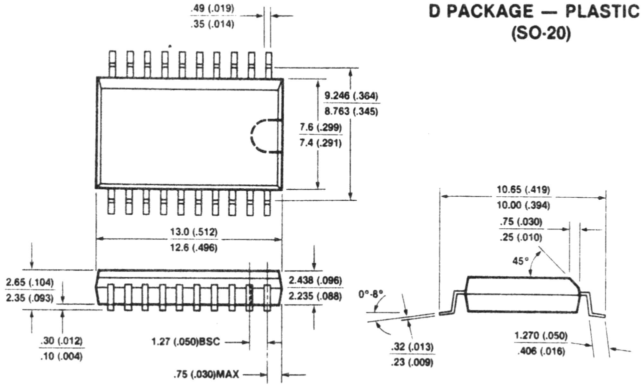
PACKAGE OUTLINES

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

D PACKAGE — PLASTIC
(SO-16L PIN)


.49 (.019)
.35 (.014)
9.246 (.364)
8.763 (.345)
7.6 (.299)
7.4 (.291)
10.5 (.413)
10.1 (.398)
2.65 (.104)
2.35 (.093)
2.438 (.096)
2.235 (.088)
.30 (.012)
.10 (.004)
1.27 (.050)BSC
.75 (.030)MAX
0°-8°
.32 (.013)
.23 (.009)
10.65 (.419)
10.00 (.394)
.75 (.030)
.25 (.010)
45°
1.270 (.050)
.406 (.016)

D PACKAGE — PLASTIC
(SO-20)

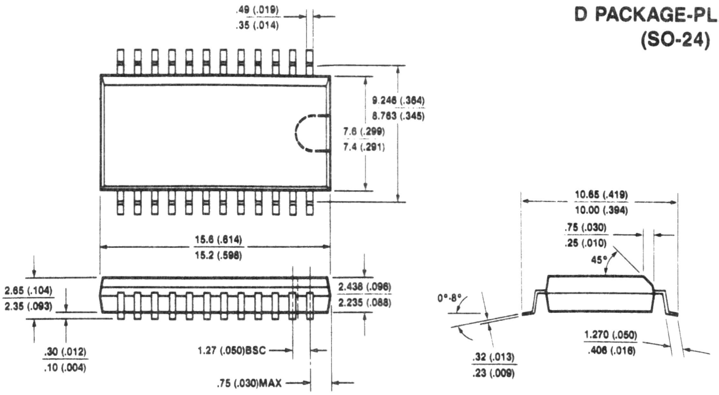

.49 (.019)
.35 (.014)
9.246 (.364)
8.763 (.345)
7.6 (.299)
7.4 (.291)
13.0 (.512)
12.6 (.496)
2.65 (.104)
2.35 (.093)
2.438 (.096)
2.235 (.088)
.30 (.012)
.10 (.004)
1.27 (.050)BSC
.75 (.030)MAX
0°-8°
.32 (.013)
.23 (.009)
10.65 (.419)
10.00 (.394)
.75 (.030)
.25 (.010)
45°
1.270 (.050)
.406 (.016)

Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

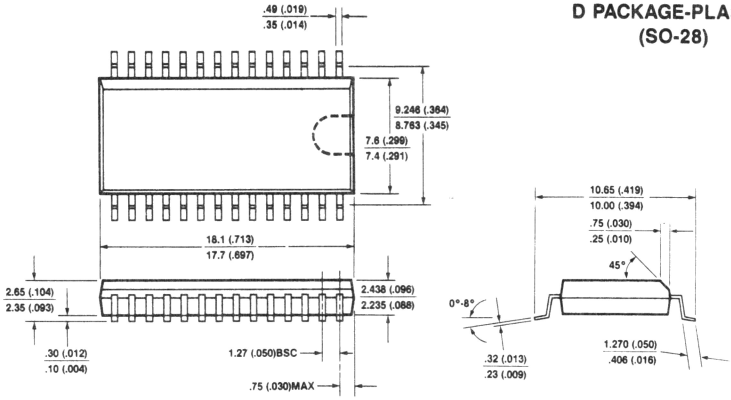
PACKAGE OUTLINES

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

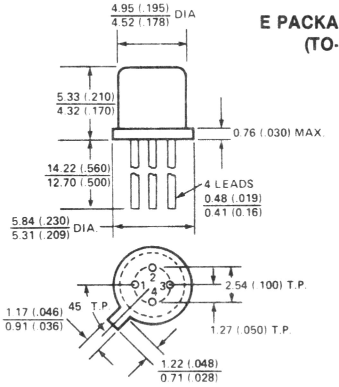
D PACKAGE-PLASTIC (SO-24)


.49 (.019)
.35 (.014)
9.246 (.364)
8.763 (.345)
7.6 (.299)
7.4 (.291)
15.6 (.614)
15.2 (.598)
2.65 (.104)
2.35 (.093)
2.438 (.096)
2.235 (.088)
.30 (.012)
.10 (.004)
1.27 (.050)BSC
.75 (.030)MAX
10.65 (.419)
10.00 (.394)
.75 (.030)
.25 (.010)
45°
0°-8°
1.270 (.050)
.406 (.016)
.32 (.013)
.23 (.009)

D PACKAGE-PLASTIC (SO-28)


.49 (.019)
.35 (.014)
9.246 (.364)
8.763 (.345)
7.6 (.299)
7.4 (.291)
18.1 (.713)
17.7 (.697)
2.65 (.104)
2.35 (.093)
2.438 (.096)
2.235 (.088)
.30 (.012)
.10 (.004)
1.27 (.050)BSC
.75 (.030)MAX
10.65 (.419)
10.00 (.394)
.75 (.030)
.25 (.010)
45°
0°-8°
1.270 (.050)
.406 (.016)
.32 (.013)
.23 (.009)

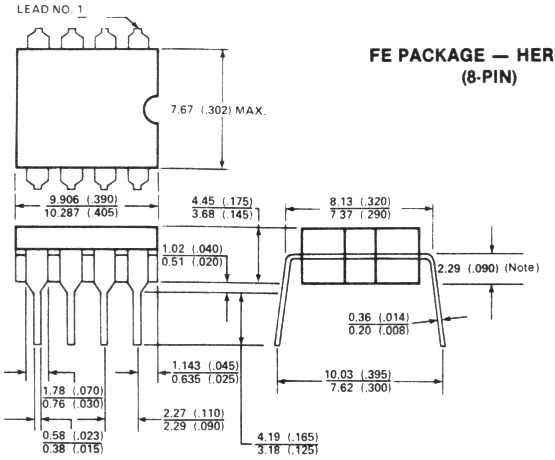
E PACKAGE — HERMETIC (TO-72 HEADER)


4.95 (.195)
4.52 (.178)
DIA
5.33 (.210)
4.32 (.170)
0.76 (.030) MAX.
14.22 (.560)
12.70 (.500)
4 LEADS
0.48 (.019)
0.41 (0.16)
5.84 (.230)
5.31 (.209)
DIA.
1
2
3
4
2.54 (.100) T.P.
1.27 (.050) T.P.
45 T.P.
1.17 (.046)
0.91 (.036)
1.22 (.048)
0.71 (.028)

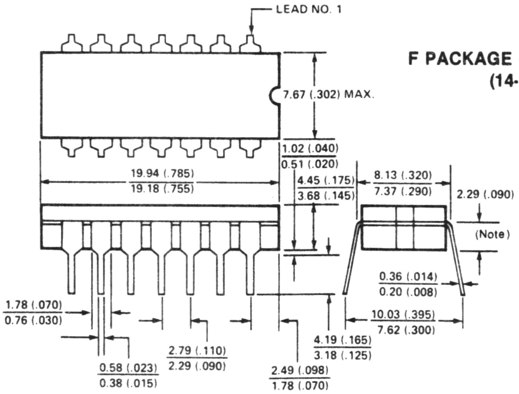
Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

PACKAGE OUTLINES

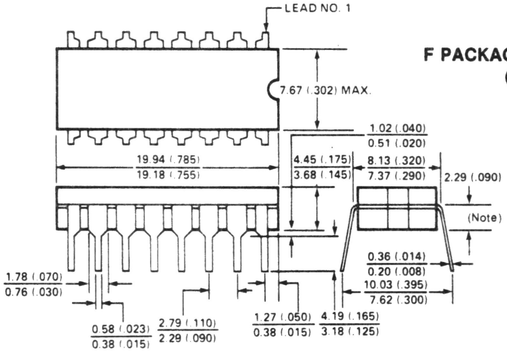
FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN


LEAD NO. 1
7.67 (.302) MAX.
9.906 (.390)
10.287 (.405)
4.45 (.175)
3.68 (.145)
8.13 (.320)
7.37 (.290)
1.02 (.040)
0.51 (.020)
2.29 (.090) (Note)
0.36 (.014)
0.20 (.008)
1.143 (.045)
0.635 (.025)
10.03 (.395)
7.62 (.300)
1.78 (.070)
0.76 (.030)
2.27 (.110)
2.29 (.090)
0.58 (.023)
0.38 (.015)
4.19 (.165)
3.18 (.125)

FE PACKAGE — HERMETIC
(8-PIN)


LEAD NO. 1
7.67 (.302) MAX.
1.02 (.040)
0.51 (.020)
19.94 (.785)
19.18 (.755)
4.45 (.175)
3.68 (.145)
8.13 (.320)
7.37 (.290)
2.29 (.090)
(Note)
0.36 (.014)
0.20 (.008)
10.03 (.395)
7.62 (.300)
1.78 (.070)
0.76 (.030)
4.19 (.165)
3.18 (.125)
2.79 (.110)
2.29 (.090)
0.58 (.023)
0.38 (.015)
2.49 (.098)
1.78 (.070)

F PACKAGE — HERMETIC
(14-PIN)


LEAD NO. 1
7.67 (.302) MAX.
1.02 (.040)
0.51 (.020)
19.94 (.785)
19.18 (.755)
4.45 (.175)
3.68 (.145)
8.13 (.320)
7.37 (.290)
2.29 (.090)
(Note)
0.36 (.014)
0.20 (.008)
10.03 (.395)
7.62 (.300)
1.78 (.070)
0.76 (.030)
1.27 (.050)
0.38 (.015)
4.19 (.165)
3.18 (.125)
0.58 (.023)
0.38 (.015)
2.79 (.110)
2.29 (.090)

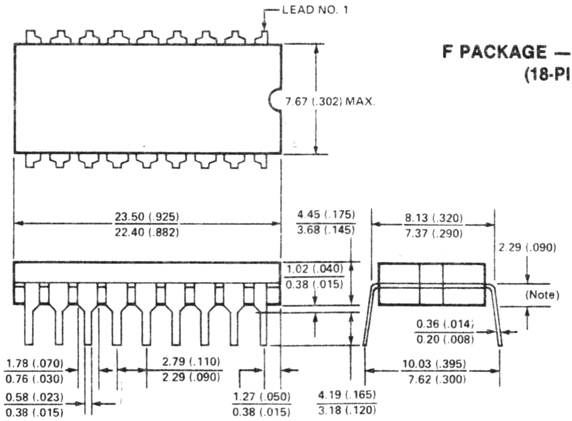
F PACKAGE — HERMETIC
(16-PIN)

Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

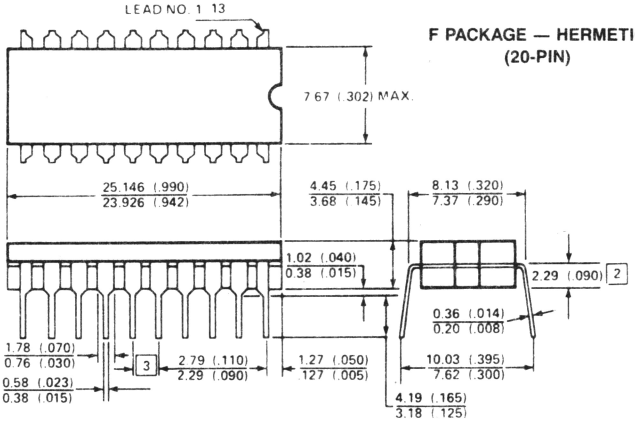
PACKAGE OUTLINES

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

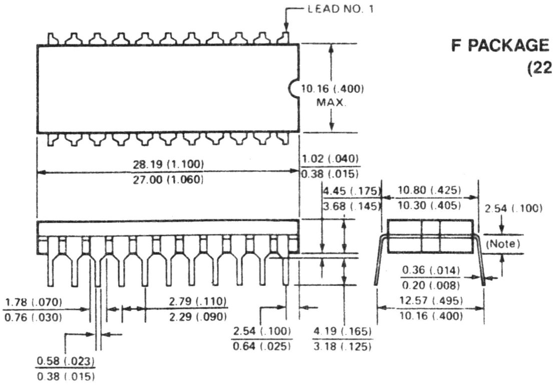
F PACKAGE — HERMETIC
(18-PIN)


LEAD NO. 1
7.67 (.302) MAX.
23.50 (.925)
22.40 (.882)
4.45 (.175)
3.68 (.145)
8.13 (.320)
7.37 (.290)
2.29 (.090)
(Note)
1.02 (.040)
0.38 (.015)
0.36 (.014)
0.20 (.008)
10.03 (.395)
7.62 (.300)
1.78 (.070)
0.76 (.030)
2.79 (.110)
2.29 (.090)
0.58 (.023)
0.38 (.015)
1.27 (.050)
0.38 (.015)
4.19 (.165)
3.18 (.120)

F PACKAGE — HERMETIC
(20-PIN)


LEAD NO. 1 13
7.67 (.302) MAX.
25.146 (.990)
23.926 (.942)
4.45 (.175)
3.68 (.145)
8.13 (.320)
7.37 (.290)
1.02 (.040)
0.38 (.015)
2.29 (.090) 2
0.36 (.014)
0.20 (.008)
1.78 (.070)
0.76 (.030)
3
2.79 (.110)
2.29 (.090)
1.27 (.050)
.127 (.005)
10.03 (.395)
7.62 (.300)
0.58 (.023)
0.38 (.015)
4.19 (.165)
3.18 (.125)

F PACKAGE — HERMETIC
(22-PIN)

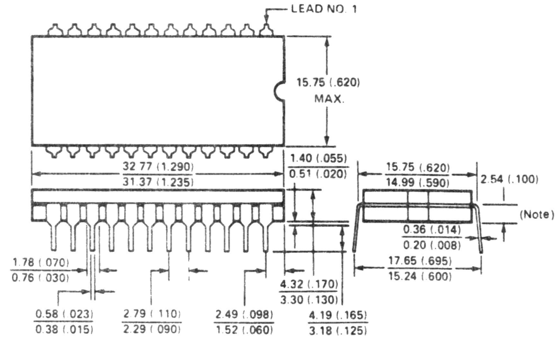

LEAD NO. 1
10.16 (.400)
MAX.
28.19 (1.100)
27.00 (1.060)
1.02 (.040)
0.38 (.015)
4.45 (.175)
3.68 (.145)
10.80 (.425)
10.30 (.405)
2.54 (.100)
(Note)
0.36 (.014)
0.20 (.008)
12.57 (.495)
10.16 (.400)
1.78 (.070)
0.76 (.030)
2.79 (.110)
2.29 (.090)
2.54 (.100)
0.64 (.025)
4.19 (.165)
3.18 (.125)
0.58 (.023)
0.38 (.015)

Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

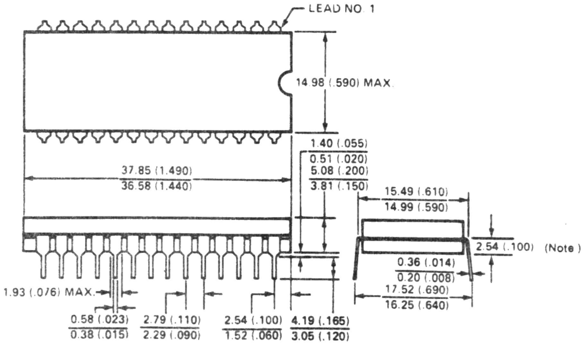
PACKAGE OUTLINES

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

F PACKAGE — HERMETIC
(24-PIN)


LEAD NO. 1
15.75 (.620) MAX.
32.77 (1.290)
31.37 (1.235)
1.40 (.055)
0.51 (.020)
15.75 (.620)
14.99 (.590)
2.54 (.100)
(Note)
0.36 (.014)
0.20 (.008)
17.65 (.695)
15.24 (.600)
1.78 (.070)
0.76 (.030)
4.32 (.170)
3.30 (.130)
0.58 (.023)
0.38 (.015)
2.79 (.110)
2.29 (.090)
2.49 (.098)
1.52 (.060)
4.19 (.165)
3.18 (.125)

F PACKAGE — HERMETIC
(28-PIN)

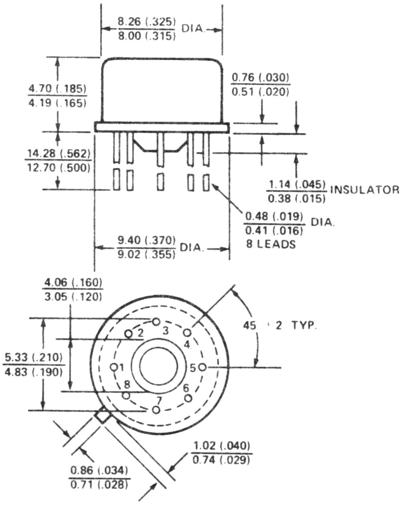

LEAD NO. 1
14.98 (.590) MAX.
1.40 (.055)
0.51 (.020)
5.08 (.200)
3.81 (.150)
37.85 (1.490)
36.58 (1.440)
15.49 (.610)
14.99 (.590)
2.54 (.100) (Note)
0.36 (.014)
0.20 (.008)
17.52 (.690)
16.25 (.640)
1.93 (.076) MAX.
0.58 (.023)
0.38 (.015)
2.79 (.110)
2.29 (.090)
2.54 (.100)
1.52 (.060)
4.19 (.165)
3.05 (.120)

Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

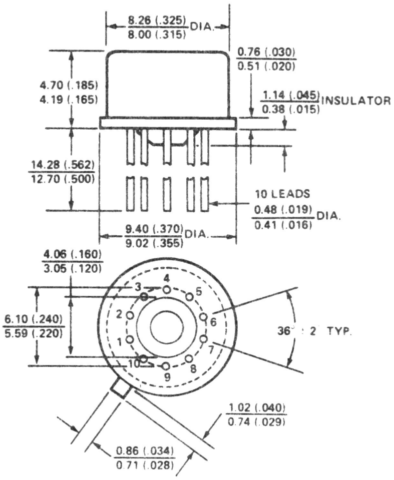
PACKAGE OUTLINES

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

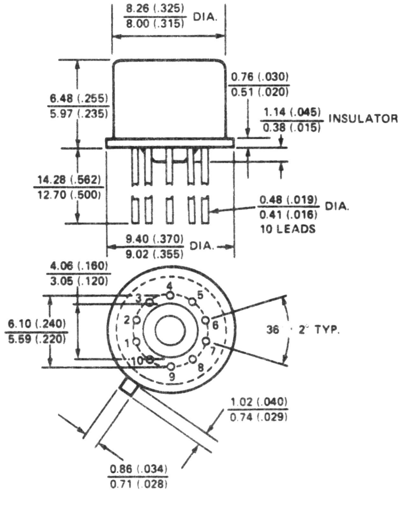
H PACKAGE — HERMETIC
8-PIN
(TO-5 HEADER)


8.26 (.325) / 8.00 (.315) DIA.
4.70 (.185) / 4.19 (.165)
0.76 (.030) / 0.51 (.020)
14.28 (.562) / 12.70 (.500)
1.14 (.045) / 0.38 (.015) INSULATOR
0.48 (.019) / 0.41 (.016) DIA. 8 LEADS
9.40 (.370) / 9.02 (.355) DIA.
4.06 (.160) / 3.05 (.120)
45° ± 2° TYP.
5.33 (.210) / 4.83 (.190)
1
2
3
4
5
6
7
8
1.02 (.040) / 0.74 (.029)
0.86 (.034) / 0.71 (.028)

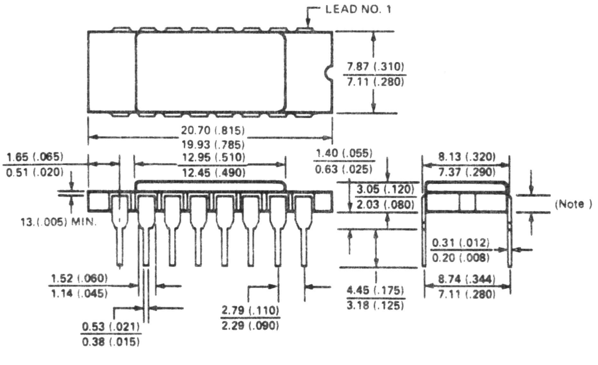
H PACKAGE — HERMETIC
10-PIN
(TO-5/100 HEADER SHORT CAN)


8.26 (.325) / 8.00 (.315) DIA.
0.76 (.030) / 0.51 (.020)
4.70 (.185) / 4.19 (.165)
1.14 (.045) / 0.38 (.015) INSULATOR
14.28 (.562) / 12.70 (.500)
10 LEADS
0.48 (.019) / 0.41 (.016) DIA.
9.40 (.370) / 9.02 (.355) DIA.
4.06 (.160) / 3.05 (.120)
6.10 (.240) / 5.59 (.220)
36° ± 2° TYP.
1
2
3
4
5
6
7
8
9
10
1.02 (.040) / 0.74 (.029)
0.86 (.034) / 0.71 (.028)

H PACKAGE HERMETIC
10-PIN
(TO-5/100 HEADER TALL CAN)


8.26 (.325) / 8.00 (.315) DIA.
0.76 (.030) / 0.51 (.020)
6.48 (.255) / 5.97 (.235)
1.14 (.045) / 0.38 (.015) INSULATOR
14.28 (.562) / 12.70 (.500)
0.48 (.019) / 0.41 (.016) DIA. 10 LEADS
9.40 (.370) / 9.02 (.355) DIA.
4.06 (.160) / 3.05 (.120)
6.10 (.240) / 5.59 (.220)
36° ± 2° TYP.
1
2
3
4
5
6
7
8
9
10
1.02 (.040) / 0.74 (.029)
0.86 (.034) / 0.71 (.028)

I PACKAGE — HERMETIC
(16-PIN)

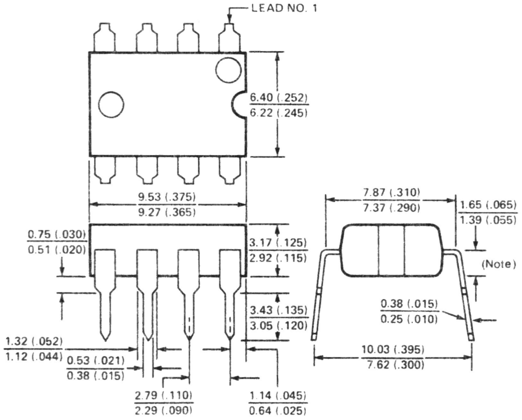

LEAD NO. 1
7.87 (.310) / 7.11 (.280)
20.70 (.815) / 19.93 (.785)
12.95 (.510) / 12.45 (.490)
1.65 (.065) / 0.51 (.020)
1.40 (.055) / 0.63 (.025)
8.13 (.320) / 7.37 (.290)
3.05 (.120) / 2.03 (.080)
(Note)
.13 (.005) MIN.
0.31 (.012) / 0.20 (.008)
1.52 (.060) / 1.14 (.045)
4.45 (.175) / 3.18 (.125)
8.74 (.344) / 7.11 (.280)
2.79 (.110) / 2.29 (.090)
0.53 (.021) / 0.38 (.015)

Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

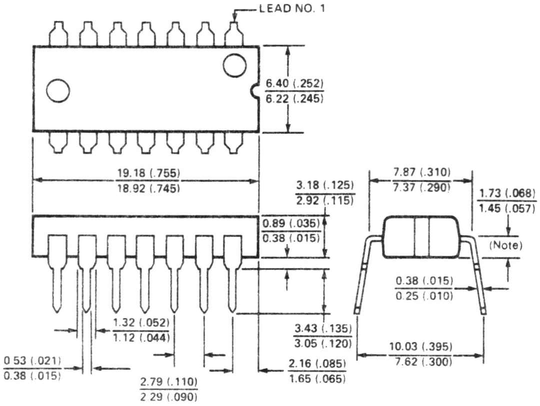
PACKAGE OUTLINES

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

N PACKAGE — PLASTIC
(8-PIN)


LEAD NO. 1
6.40 (.252)
6.22 (.245)
9.53 (.375)
9.27 (.365)
0.75 (.030)
0.51 (.020)
3.17 (.125)
2.92 (.115)
3.43 (.135)
3.05 (.120)
1.32 (.052)
1.12 (.044)
0.53 (.021)
0.38 (.015)
2.79 (.110)
2.29 (.090)
1.14 (.045)
0.64 (.025)
7.87 (.310)
7.37 (.290)
1.65 (.065)
1.39 (.055)
(Note)
0.38 (.015)
0.25 (.010)
10.03 (.395)
7.62 (.300)

N PACKAGE — PLASTIC
(14-PIN)

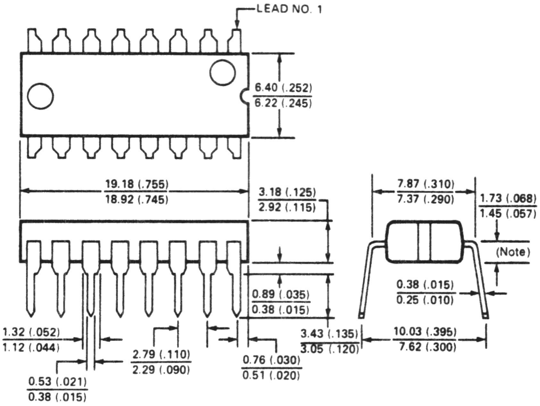

LEAD NO. 1
6.40 (.252)
6.22 (.245)
19.18 (.755)
18.92 (.745)
3.18 (.125)
2.92 (.115)
0.89 (.035)
0.38 (.015)
7.87 (.310)
7.37 (.290)
1.73 (.068)
1.45 (.057)
(Note)
0.38 (.015)
0.25 (.010)
1.32 (.052)
1.12 (.044)
3.43 (.135)
3.05 (.120)
10.03 (.395)
7.62 (.300)
0.53 (.021)
0.38 (.015)
2.16 (.085)
1.65 (.065)
2.79 (.110)
2.29 (.090)

Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

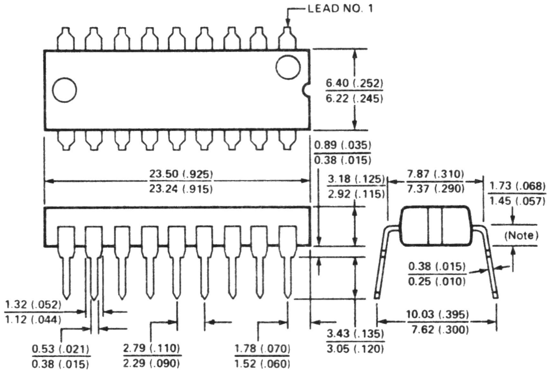
PACKAGE OUTLINES

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

N PACKAGE — PLASTIC (16-PIN)


LEAD NO. 1
6.40 (.252)
6.22 (.245)
19.18 (.755)
18.92 (.745)
3.18 (.125)
2.92 (.115)
7.87 (.310)
7.37 (.290)
1.73 (.068)
1.45 (.057)
(Note)
0.89 (.035)
0.38 (.015)
0.38 (.015)
0.25 (.010)
1.32 (.052)
1.12 (.044)
3.43 (.135)
3.05 (.120)
10.03 (.395)
7.62 (.300)
2.79 (.110)
2.29 (.090)
0.76 (.030)
0.51 (.020)
0.53 (.021)
0.38 (.015)

N PACKAGE — PLASTIC (18-PIN)

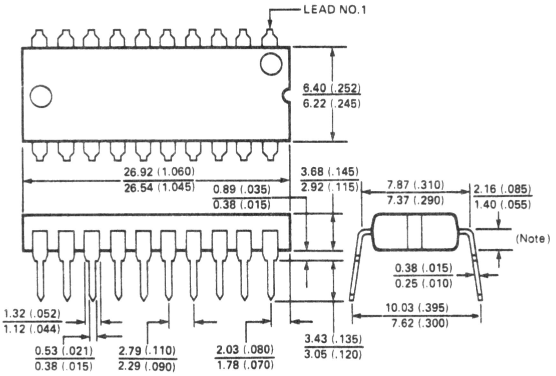

LEAD NO. 1
6.40 (.252)
6.22 (.245)
0.89 (.035)
0.38 (.015)
23.50 (.925)
23.24 (.915)
3.18 (.125)
2.92 (.115)
7.87 (.310)
7.37 (.290)
1.73 (.068)
1.45 (.057)
(Note)
0.38 (.015)
0.25 (.010)
1.32 (.052)
1.12 (.044)
10.03 (.395)
7.62 (.300)
3.43 (.135)
3.05 (.120)
0.53 (.021)
0.38 (.015)
2.79 (.110)
2.29 (.090)
1.78 (.070)
1.52 (.060)

Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

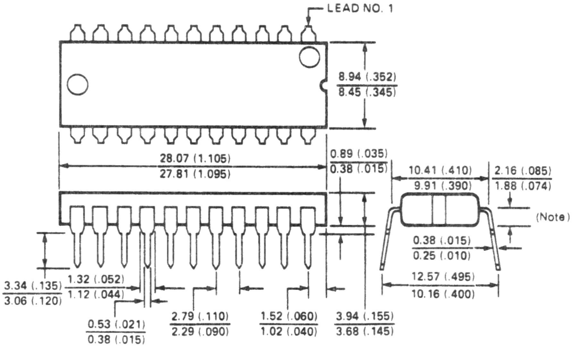
PACKAGE OUTLINES

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

N PACKAGE — PLASTIC (20-PIN)


LEAD NO.1
6.40 (.252)
6.22 (.245)
26.92 (1.060)
26.54 (1.045)
0.89 (.035)
0.38 (.015)
3.68 (.145)
2.92 (.115)
7.87 (.310)
7.37 (.290)
2.16 (.085)
1.40 (.055)
(Note)
0.38 (.015)
0.25 (.010)
10.03 (.395)
7.62 (.300)
1.32 (.052)
1.12 (.044)
0.53 (.021)
0.38 (.015)
2.79 (.110)
2.29 (.090)
2.03 (.080)
1.78 (.070)
3.43 (.135)
3.05 (.120)

N PACKAGE — PLASTIC (22-PIN)

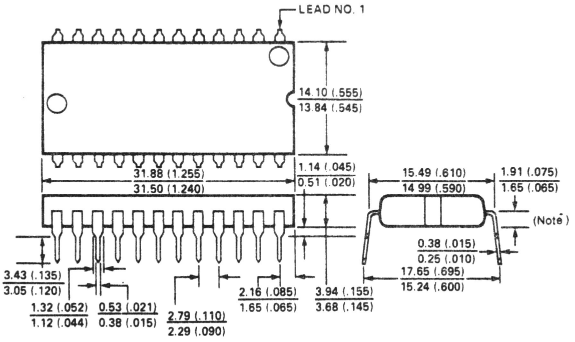

LEAD NO. 1
8.94 (.352)
8.45 (.345)
28.07 (1.105)
27.81 (1.095)
0.89 (.035)
0.38 (.015)
10.41 (.410)
9.91 (.390)
2.16 (.085)
1.88 (.074)
(Note)
0.38 (.015)
0.25 (.010)
12.57 (.495)
10.16 (.400)
3.34 (.135)
3.06 (.120)
1.32 (.052)
1.12 (.044)
0.53 (.021)
0.38 (.015)
2.79 (.110)
2.29 (.090)
1.52 (.060)
1.02 (.040)
3.94 (.155)
3.68 (.145)

Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

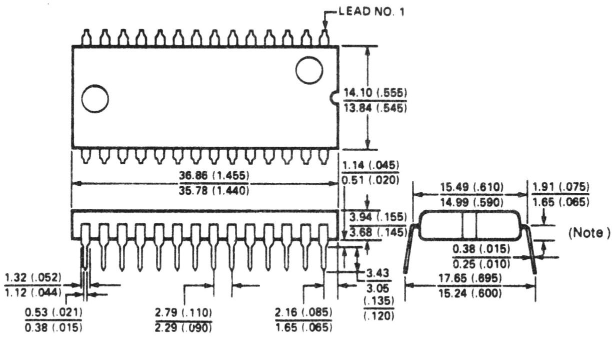
PACKAGE OUTLINES

FOR PREFIXES: ADC, AM, CA, DAC, LF, LM, MC, NE, SA, SE, SG, μA, ULN

N PACKAGE — PLASTIC
(24-PIN)


LEAD NO. 1
14.10 (.555)
13.84 (.545)
1.14 (.045)
0.51 (.020)
31.88 (1.255)
31.50 (1.240)
15.49 (.610)
14.99 (.590)
1.91 (.075)
1.65 (.065)
(Note)
0.38 (.015)
0.25 (.010)
17.65 (.695)
15.24 (.600)
3.43 (.135)
3.05 (.120)
1.32 (.052)
1.12 (.044)
0.53 (.021)
0.38 (.015)
2.79 (.110)
2.29 (.090)
2.16 (.085)
1.65 (.065)
3.94 (.155)
3.68 (.145)

N PACKAGE — PLASTIC
(28-PIN)


LEAD NO. 1
14.10 (.555)
13.84 (.545)
1.14 (.045)
0.51 (.020)
36.86 (1.455)
35.78 (1.440)
15.49 (.610)
14.99 (.590)
1.91 (.075)
1.65 (.065)
3.94 (.155)
3.68 (.145)
(Note)
0.38 (.015)
0.25 (.010)
17.65 (.695)
15.24 (.600)
3.43
3.05
(.135)
(.120)
1.32 (.052)
1.12 (.044)
0.53 (.021)
0.38 (.015)
2.79 (.110)
2.29 (.090)
2.16 (.085)
1.65 (.065)

9

Note:
Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).

Section 10

FORTHCOMING NEW PRODUCTS BY PRODUCT GROUP

Amplifiers	
LT1012	Low noise op amp with internal compensation: 0.5μV p-p noise (0.1Hz-10Hz)
LT1037	Precision op amp: high speed 11V/μs; low noise: 0.13μV p-p
NE5230	Low voltage (1.8V) op amp: 8 pin 741 pin out with internal compensation
—	40 watt amplifier with 0.01% THD
Communications	
NE568	150MHz phase locked loop
Interface/Data Conversion	
DAC800	12-Bit, 2.5μs multiplying D/A with internal reference; V or I output
NE5030	10-Bit, 1.5μs μP compatible A/D with three-state outputs, internal reference, 5V operation
NE5170	Octal line drivers RS232C/RS423A
NE5180	Octal line receivers RS232C/RS423A/RS422
NE5181	Octal line receivers RS232C/RS423A/RS422 without filter
NE5521	Improved NE5520 LVDT for −55°C to +125°C operation
Power Conversion and Control	
NE5562	20 pin, 5560-type SMPS for driving power FET's
SG1526B	SMPS controller with full features and dual FET drive (Sprague ULN8126 second source)

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MC 1408-8	4-50
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